EE 452 – Power Electronics Design
Experiment 1 Pre-lab Assignment: Part C

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Introduction

The purpose of this assignment is to prepare you to conduct Experiment 1C. Please make sure you have read and understand the experimental procedure *before* attending your designated lab section.

This assignment will be due at the *beginning* of your lab section. Like your homework, you will submit the prelab assignments through Canvas. For each problem, please provide written analysis where appropriate, show your work, and clearly label all plots, if any.

Parts

Experiment 1 will be done on the PCB using the following parts. In the electronic version of this document, you may click on the hyperlink embedded in the “Part number” column to bring up the data sheet for a given part. In addition to the components below, this experiment will also require resistors and capacitors of your choosing.

Description	Manufacturer	Part number
Power MOSFET	Infineon Technologies	IRFB4615PbF
Power MOSFET	Texas Instruments	CSD19535KCS
Half-bridge Gate driver	Infineon Technologies	IRS2184PBF
PWM Controller	Texas Instruments	UC3525AN

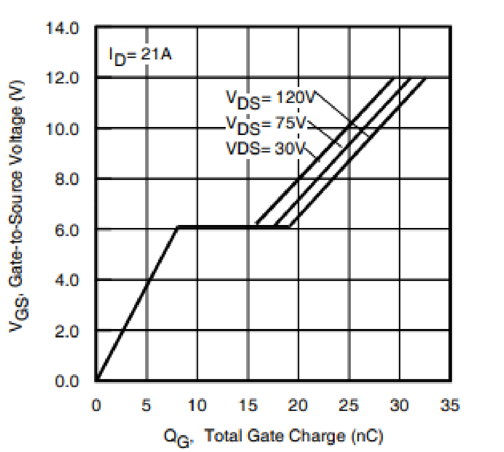
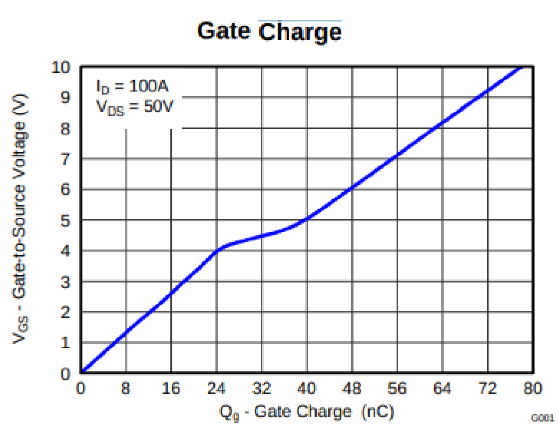


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage



Prelab tasks

Component familiarization. Using the applicable data sheets, determine the following **(10 pts)**:

- The drain-to-source resistance of both power MOSFETs in the on state.

Power MOSFET	Drain-to-Source Resistance
IRFB4615PbF	32 mΩ
CSD19535KCS	3.4 mΩ

- The threshold gate-to-source voltage of the power MOSFETs.

Power MOSFET	Gate-to-Source Voltage
IRFB4615PbF	3 V
CSD19535KCS	2.7 V

- The rated drain current of the MOSFETs.

Power MOSFET	Drain Current (@25C)
IRFB4615PbF	35 A
CSD19535KCS	150 A

- The gate charge of both power MOSFETs

Power MOSFET	Total Gate Charge (@ V_{GS} = 10V)
IRFB4615PbF	26 nC
CSD19535KCS	78 nC

- The rise and fall times of both power MOSFETS

Power MOSFET	Rise Time	Fall Time
IRFB4615PbF	35 ns	20 ns
CSD19535KCS	15 ns	5 ns

- The minimum logic high input voltage of the gate driver.
  V_{IH} = 2.5V

IRFB4615PbF

International
IOR Rectifier

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.19	—	V/°C	Reference to 25°C, I_D = 5mA①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	32	39	mΩ	V_{GS} = 10V, I_D = 21A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	V_{DS} = V_{GS}, I_D = 100μA

CSD19535KCS

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 μA	100			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 80 V			1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.2	2.7	3.4	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 6 V, I_D = 100 A		3.4	4.4	mΩ
		V_{GS} = 10 V, I_D = 100 A		3.1	3.6	mΩ
g_{fs}	Transconductance	V_{DS} = 10 V, I_D = 100 A		274		S

Internationa
IOR Rectifier

IRS2184/IRS21844(S)PbF

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, DT= V_{SS} and T_A = 25 °C unless otherwise specified. The V_{IL}, $V_{IH,}$ and I_{IN} parameters are referenced to V_{SS} /COM and are applicable to the respective input leads: IN and $\overline{SD}$. The V_O, $I_{O,}$ and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HO & logic "0" for LO	2.5	—	—	V	V_{CC} = 10 V to 20 V
V_{IL}	Logic "0" input voltage for HO & logic "1" for LO	—	—	0.8		
$V_{SD,TH+}$	$\overline{SD}$ input positive going threshold	2.5	—	—		
$V_{SD,TH-}$	$\overline{SD}$ input negative going threshold	—	—	0.8		

Possible PWM frequency (5 pts) Using data from q1, compute the maximum possible switching frequency for both MOSFETS.

[skip]

GRAD STUDENTS REQUIRED: Bootstrap circuit design. (10pts) Study the UCC27712 gate driver datasheet. This datasheet has better guidance than the IRS 2184.

Compute the following for each MOSFET with a 5% boot capacitor ripple voltage.

- Bootstrap capacitance
- Bootstrap resistance (assuming a boostrap diode peak current of 3A)
- Consider: why do we need a bootstrap capacitance? (just for learning)

5% ripple voltage of 12V = 0.6V

Bootstrap capacitance used in circuit will be at least twice as large as calculated values as mentioned in datasheet.

$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{BOOT}}$

$R_{BOOT} = \frac{V_{DD} - V_{DBOOT}}{I_{DBOOT}}$

Power MOSFET	Boot Capacitance	Boot Resistance
IRFB4615PbF	$26nC/0.6 = 43.3nC$	$(12 - 0.6)/3 = 3.8\Omega$
CSD19535KCS	$78nC/0.6 = 130nC$	$(12 - 0.6)/3 = 3.8\Omega$

UCC27712

8.2.2.2 Selecting Bootstrap Capacitor (C_{BOOT})

The bootstrap capacitor should be sized to have more than enough energy to drive the gate of FET Q1 high, and maintain a stable gate drive voltage for the power transistor.

The total charge needed per switching cycle can be estimated with:

$$Q_{Total} = Q_G + \frac{I_{QBS}}{f_{SW}} = 68\,nC + \frac{65\,\mu A}{f_{SW}} = 68.65\,nC \tag{1}$$

This design example targets a boot capacitor ripple voltage of 0.5 V. Therefore, the absolute minimum C_{BOOT} requirement is:

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{BOOT}} = \frac{68.65\,nC}{0.5\,V} \approx 137\,nF \tag{2}$$

In practice, the value of C_{BOOT} needs to be greater than the calculated value. This allows for capacitance shift from DC bias and temperature, and also skipped cycles that occur during load transients. For this design example 2x 220-nF capacitors were chosen for the bootstrap capacitor.

$$C_{BOOT} = 440\,nF \tag{3}$$

8.2.2.4 Selecting Bootstrap Resistor (R_{BOOT})

Resistor R_{BOOT} is selected to limit the current in D_{BOOT} and limit the ramp up slew rate of voltage of HB-HS to avoid the phenomenon shown in Figure 45. It is recommended when using the UCC27712 that R_{BOOT} is between 2 Ω and 20 Ω. For this design we selected an R_{BOOT} current limiting resistor of 2.2 Ω. The bootstrap diode current ($I_{DBOOT(pk)}$) was limited to roughly 5.0 A.

$$I_{DBOOT(pk)} = \frac{V_{DD} - V_{DBOOT}}{R_{BOOT}} = \frac{12\,V - 1\,V}{2.2\,\Omega} = 5.0\,A \tag{5}$$

The power dissipation capability of the bootstrap resistor is important. The bootstrap resistor must be able to withstand the short period of high power dissipation during the initial charging sequence of the boot-strap capacitor. This energy is equivalent to 1/2 × CBOOT × V^2. This energy is dissipated during the charging time of the bootstrap capacitor (~3 × R_{BOOT} × C_{BOOT}). Special attention must be paid to use a bigger size R_{BOOT} when a bigger value of C_{BOOT} is chosen.

TI Bootstrap Circuitry

3.1 Bootstrap Capacitor

From a design perspective, this is the most important component because it provides a low impedance path to source the high peak currents to charge the high-side switch. As a general rule of thumb, this bootstrap capacitor should be sized to have enough energy to drive the gate of the high-side MOSFET without being depleted by more than 10%. This bootstrap cap should be at least 10 times greater than the gate capacitance of the high-side FET. The reason for that is to allow for capacitance shift from DC bias and temperature, and also skipped cycles that occur during load transients. The gate capacitance can be determined using Equation 1:

$$C_g = \frac{Q_g}{V_{Q_{1g}}}$$

where Q_g: gate charge (MOSFET's datasheet)

$$V_{Q_{1g}} = V_{DD} - V_{BootDiode}$$

where $V_{BootDiode}$: forward voltage drop across the boot diode. (1)

Once the gate charge determined, the minimum value for the bootstrap capacitor can be estimated using Equation 2:

$$C_{boot} \geq 10 \times C_g \tag{2}$$