EE 452 – Power Electronics Design
Experiment 2A Procedure

Department of Electrical & Computer Engineering
University of Washington

Introduction

The main objective of this experiment is to learn how voltage/current sensing, and protection are achieved in power electronics. **This experiment will require hand soldering of your sensing and protection circuit and will continue to build on the experiment 1 circuitry.**

Parts

This experiment will be done using the following parts. In the electronic version of this document, you may click on the hyperlink embedded in the "Part number" column to bring up the data sheet for a given part. In addition to the components below, this experiment will also require resistors, a potentiometer, and capacitors of your choosing.

Description	Manufacturer	Part number
Analog comparator	TI	LMC6482
Current sensor	Texas Instruments	ACS711KLCTR-12AB-T
3.3V Regulator	Murata	OKI-78SR-3.3/1.5-W36H-C

Overview of experiment

Below is an overview of what each key component in this circuit:

1. ACS711KLCTR-12AB-T current sensor: The device **(8 pin surface mount IC)** consists of a linear Hall sensor circuit with a copper conduction path located near the surface of the die. Applied current flowing through this copper conduction path generates a magnetic field which is sensed by the integrated Hall IC and converted into a proportional voltage. The output of the device has a positive slope proportional to the current flow from IP+ to IP− (pins 1 and 2, to pins 3 and 4). Pins 5 and 6 are supply voltage (3.3 and 5V logic) and sensor output, which varies from bias voltage to 0V and 3.3V. Pins 7 and 8 are fault out and ground. Awlays double check your pinouts with the datasheet.

2. LMC6482 dual analog comparator: This IC contains two comparators within one package. This a Dual Rail-to-Rail Input comparator. This is 3.3V supply compatible,

and we can use negative rail voltages as well. But we will use it as a single supply op-amp in this experiment.It has two comparators in it, and we will use only one of them for over voltage condition. There is no explicit necessity for the over current control as all of you have access to a regulated power supply.

3. The 3.3V regulator is similar to the 12V regulator used for your input power to the PWM and Gate Driver ICs. Its nominal Vin is 12V but it can handle 7-36V. The output voltage is 3.3V.

First you will supplement the circuit from Experiment 1-B/C with the sensing and load circuitry. The lab concludes by constructing the comparator circuit which controls the driver shutdown pin $\bar{SD}$.

Task 1: Building load and sensing circuitry

Keeping in mind, the layout discussion from the lab class, layout your power stage. The full schematic is given in the lab lecture notes. **You are to not connect the gate driver outputs to your switch gate terminals. You do not need to connect all of these components, you just need to lay them out.** You will short your DC power supply to the load so you can control the load voltage for testing purposes. This will be removed in later labs.

Make sure that your current sensor is properly soldered onto the breakout board, to get your through hole configuration. Use your multimeter to check for continuity between the surface-mounted pins and the through-hole pins, as well as short circuits between adjacent pins. **Make sure that the current sensor is in series with your load.**

Next design the voltage sensing divider circuit formed by R_1 and R_2 to measure your load voltage for overvoltage protection purposes. Keep in mind that for this experiment the output voltage level of your circuit is only going to be a maximum of 30V. But the circuit is to be designed for the power converter be operated at 48V, with a maximum voltage of 55V. **At any point, the input to the comparator (both inverting and non-inverting) cannot exceed 3.3V. Select the resistor values such that the midpoint of the divider never exceeds 3.3 V (even during the condition where the duty D is maximum.** Your divider is needed to ensure that the protection comparator in Task 2 isn't damaged. Size the divider such that the sensed voltage is 3.3V when the output voltage is 60V.

The output of your comparator will be a 3.3V logic level (HI-3.3V, LO-0V), and this can directly fed to your gate driver shutdown pin.

In your report, you should include:

- Design calculations for voltage sensing divide for the load voltage measurement. Clearly show how 60 V upper limit was translated into the parameters for your divider. (**10 pts**)
- A schematic showing the details of your load and sensing circuitry. All parts and values should be clearly labeled. (**10 pts**)

Task 2: Build Protection Logic

For this task, you will need a potentiometer. Connect the comparator positive supply pin to the output of 3.3V regulator and the negative supply pin to GND. Connect the sensed voltage from your divider circuit to an inverting input of one comparator. In addition, add a potentiometer and resistor divider circuit where the adjustable midpoint of the potentiometer is connected to the noninverting comparator input, and the divider circuit is across 3.3V to GND (similar to the voltage divider for pin 2 of the PWM IC). This divider circuit can also be placed across the 5.1 V voltage rail from the UC3525AN `VREF` pin or 12/24V supply. Just be sure you are not drawing more current than the supplying pin can provide.

In essence, this divider circuit will allow you to adjust the overvoltage threshold where the protection kicks in. Carefully analyze your voltage sensing circuits, then design the two divider circuits so that the power stage voltage limit is adjustable between 0 V and 60 V across the full potentiometer range.
Note: depending on how you design your divider circuits, you may not need a resistor for the noninverting input divider.

Check out the following link for a tutorial on how to use op-amps as comparators.

- Texas Instruments, Tutorial on Comparator Circuits

Turn on the power supply and your full circuit. Adjust the voltage threshold potentiometer and verify that it can indeed enforce a voltage limit. Convince yourself that the protection circuit is fully functional.

Finally, replace the pull-up resistor for the gate driver $\bar{SD}$ with the output of the overvoltage protection comparator. This should make it so that when the sensed voltage is higher than the threshold, this pin should be low and effectively shut down the gate driver.

In your report, you should include:

- **Capture 1**: The measured load current using the current sensor circuit and the measured output voltage of the voltage divider circuit. **(20 pts)**

  Calculate the expected output voltage of the current sensor and show your computations. Based on the expected current through the load, compare the expected and measured output voltages and comment on any differences. See the datasheet for sensitivity and details on voltage output. **(10 pts)**

- **Capture 2/3**: Capture the output voltage of the comparator and the reference voltage input in two instances one when the reference is greater than input and the other when it is lesser than input. Each capture should show the reference voltage, the input voltage, and the comparator output voltage.**(20 pts)**

- **Capture 4**: Capture the low-side gate driver output and show how it is being driven low when protection is active. Show functional protection at one threshold value (15-24V) by varying the potentiometer connected to your non-inverting input to show that it works over an adjustable range.**(20 pts)**

- **Optional for EE452** Take current sensor output voltage measurements for both 0A and a different current. You should see a noticeable increase in voltage between the two. What is the range of possible voltage outputs from the current sensor? Is the 0A measurement in the middle? If not, what is the datasheet parameter that gives the value you found?(**10pts**)

Notes on circuit construction and debugging

Supply voltage decoupling. In all circuits, especially those that produce pulsating waveform, decoupling capacitors are essential to ensure that the dc supply voltage is undisturbed by large current transitions and spikes, and to prevent propagation of noise through the power distribution circuitry. Without decoupling capacitors, current spikes and transitions can cause large voltage transients and oscillations on the power supply wires, because of the inductance of the wiring. Such voltage "spikes" and "ringing" can disrupt operation of all devices connected to the power supply.

It is necessary to ensure that adequate capacitors are included in your circuitry for power supply decoupling. Here are some suggestions:

- Between the positive supply and ground terminals of the controller circuit board, connect an electrolytic capacitor of at least 10 µF (in the case of a power converter circuit board, a considerably larger capacitance may be required). This capacitor filters low-frequency variations in the power supply. Note that this electrolytic capacitor is polarized; connecting it to a power source with the wrong polarity will cause the capacitor to fail.

- For all integrated circuits on the controller board, a ceramic capacitor of at least 0.1 µF should be connected between each power supply pin and ground pin, as close as possible to the IC. This capacitor filters high-frequency variations in the power supply. Gate driver circuitry often requires additional high-frequency decoupling capacitance, perhaps 1 µF or more.

Constructing and debugging test circuits. Do not forget to power down the circuit before you make any additions or changes to the circuit. This is especially important in later experiments that drive the converter power stage. Turn on the power only after you have checked that your are correct. In particular, always check the polarity of the power supply connections to the ICs.

If your circuit does not work, it is suggested that you troubleshoot it in a systematic manner. Use the oscilloscope to view the voltage waveforms at every pin of the first IC, beginning with its input. Are they as you expect? If not, then you have localized the problem. When the operation of the first IC is correct, then repeat the process for the next IC (and so on).