EE 452 – Power Electronics Design
Experiment 1 Procedure: Part B,C

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Introduction

The main objective of this experiment is to understand analog pulse width modulation and gate driver circuits in power converters. To achieve this aim, you will assemble a circuit on a prototype board using a PWM integrated circuit (IC), gate-drive IC, some resistors and capacitors. Soldering will be necessary and it is important that you not damage your parts since you will use them in the coming experiments. Each group must construct a prototype board with the needed circuitry, and all members must participate in soldering/circuit construction.

Parts

This experiment will be done on a breadboard using the following parts. In the electronic version of this document, you may click on the hyperlink embedded in the "Part number" column to bring up the data sheet for a given part. In addition to the components below, this experiment will also require resistors, a potentiometer, and capacitors of your choosing.

Description	Manufacturer	Part number
12V Regulator	Murata	OKI-78SR-12
Half-bridge Gate driver	Infineon Technologies	IRS2184PBF
PWM Controller	Texas Instruments	UC3525AN

Overview of experiment

Below is an overview of what each key component does:

1. UC3525AN PWM controller: This device is responsible for producing the switch logic signals that eventually control the two MOSFETs in your boost converter circuit. You will build circuitry that connects to the pins of the UC3525AN. These circuits will select the switching frequency and allow you to vary the duty ratio between some upper and lower limit using a potentiometer. The logic outputs of the UC3525AN will be fed to a downstream gate driver IC.
2. IRS2184PBF half-bridge gate driver: This IC is designed to receive logic signals and translate those into corresponding output signals that drive the gates of two power

MOSFETs. The two MOSFETs it drives are connected in series across a dc voltage. This configuration is called a *half-bridge* circuit. The half-bridge gate driver has special circuitry that enables control of both the high-side and low-side switches. The output side of the gate driver is designed to carry significant current to rapidly charge and discharge the gate capacitance. This ensures quick on/off switching transitions.

3. 12V Regulator: Steps down voltage from 24V to 12V.

First you should build the PWM controller and its supporting circuitry. Secondly interface the PWM IC to the gate driver and debug the circuit until you verify that the gate driver outputs look correct. The sections below give some guidance on each task.

Task 1B: Pulse width modulation

Before beginning, you should have studied the UC3525AN datasheet to get familiar with its operating principles. Section 7 of the datasheet is particularly important and contains key information. Also review the lecture material on the UC3525AN. Your task is to design circuitry around the pins to achieve a 50 kHz switching frequency and a potentiometer that adjusts the duty between 0% some upper limit that doesn't exceed 80%. The Keysight bench power supply features two independently adjustable sets of outputs. Configure one of the supply outputs to produce 12 V and connect this across the power supply and ground return pins on the UC3525AN IC. Leave the power supply turned off until you are ready to test the circuit. Later, you will use a 24V input, and will use the Murata 12V regulator to step down the voltage from 24V to 12V.

First consider the switching frequency objective. Use the equation on the bottom of page 5 to select the values of C_T, R_T, and R_D that provide the needed switching frequency. See section 6.3 for guidelines on typical ranges of C_T, R_T, and R_D. These components are each connected between their respective pins and ground pin, and interact with an internal oscillator circuit whose periodic sawtooth (ramp) waveform will have the same frequency as the switching frequency. The output of the oscillator can be observed on pin 4. Measure the output of this pin to ensure that the sawtooth waveform has a frequency that matches the desired switching frequency. Be sure to add diodes on the A and B outputs to OR the signals together.

Next it is necessary to build the voltage divider that adjusts the duty ratio. Using a potentiometer and one or more other resistors, create a voltage divider across the 12 V supply rail. The voltage created by the divider is then connected to the noninverting input of the error amplifier op-amp (pin 2). Note that the error amplifier is typically used for analog control where error amplification is needed. Since we are doing an open-loop design with no closed-loop control action, the functionality of this amplifier will be bypassed. We will achieve this by configuring the internal op-amp as a buffer (i.e., follower circuit). This is done by short circuiting pins 9 (op-amp output) and 1 (inverting input) together.

In your report, you should include:

- A complete and labeled circuit diagram of the PWM IC along with labeled component names and values. **(8pts)**
- Computation of switching frequency along with R_d included **(2pts)**

- Capture the below listed waveforms for a desired duty $d \in [0.25, 0.75]$. They should be time-aligned and labelled with important values.
  Capture 1 (20pts):
  - Noninverting input pin (PWM Reference Voltage)
  - Oscillator output pin voltage

  Capture 2 (20pts):
  - PWM A Output
  - PWM B Output

  Capture 3 (10pts):
  - PWM 'OR' output

Be sure to include the deadtime measurement using cursors on Capture 2.

Before proceeding to Task 2, verify operation of your PWM circuit with the TA.

Note: EE452 to use a constant R_D of 33Ω
Note: **(Optional for EE452)** EE532 students to use a range of $R_D(33 - 100\Omega)$ and record **Capture 3** for different R_D values (2 values other than 33Ω and be sure to include deadtime measurement.

Task 1C: Half-bridge gate driver

First, interface the gate driver supply pin V_{cc} and ground pin COM to the 12 V supply voltage. Leave the power supply turned off until you are ready to test the circuit. The half-bridge gate driver functions by receiving the logic signal from the PWM IC and adding a *deadtime* between the two output signals that connect to each MOSFET. Deadtime refers to the very brief period in time where both MOSFETs in a half-bridge are commanded to turn off (low gate-to-source voltages on both MOSFETs). This is used to account for the fact that real devices have a turn-on and turn-off delay, and hence, the absence of deadtime will result in a brief overlap where both devices are on and the half-bridge acts as a short circuit. To prevent this catastrophic condition, deadtime is added in the turn-on/off transitions for the two MOSFETs.

Configure the input logic pin of your gate driver so that it can receive a signal from either a signal generator or the PWM controller from Task 1. Here, the signal generator is useful for debugging due to its ideal behavior. Once debugging is complete, you can leave the logic input pin connected to the PWM controller. Next, it is necessary to build the bootstrap circuitry that supplies charge to the top-side driver circuit. Refer to the document linked below to understand the operating principles of the bootstrap circuit and how it is designed:

- Texas Instruments, Application Report on Bootstrap Circuitry
- See example design in Section 8 of UCC27712 datasheet. Even though we aren't using this IC, the design principles are identical to our setup.

Compute the minimum bootstrap capacitance, C_{BOOT}, such that the high-side voltage changes no more than 5% of 12 V at a switching frequency of 50 kHz (use equation (1)

in UCC27712 datasheet example linked above). Obtain a capacitor larger than this value and assemble the output-side circuitry of the driver. **(Optional but preferred)** For debugging, first give a logic signal from a function generator at the driver input side. Once that is working, connect the logic input pin to the output of the PWM IC from Task 1. In your report, you should include:

- A complete and labeled circuit diagram of the driver IC along with labeled component names and values.**(5pts)**
- A detailed computation of your boot resistance, capacitance, and gate on/off resistance values. **(10pts)**

Capture 1 and 2 (20pts):

- Capture the input and output LO signal of the driver.
- Capture the input and output HI signal of the driver.

Capture 3 (10pts):

- Include a zoomed in capture of an on/off transient and use the scope cursors to show the inbuilt deadtime of the gate driver IC.

(Optional for EE452 Students) Capture 4:

- Voltage waveform across your bootstrap capacitance. This is a floating voltage, so you cannot measure it directly with one normal oscilloscope probe. **(Hint: use the arithmetic feature of the oscilloscope)**

Once you verify that the signals on the output side are correct, obtain approval from the TA before doing Task 3.

Notes on circuit construction and debugging

Supply voltage decoupling. In all circuits, especially those that produce pulsating waveform, decoupling capacitors are essential to ensure that the dc supply voltage is undisturbed by large current transitions and spikes, and to prevent propagation of noise through the power distribution circuitry. Without decoupling capacitors, current spikes and transitions can cause large voltage transients and oscillations on the power supply wires, because of the inductance of the wiring. Such voltage "spikes" and "ringing" can disrupt operation of all devices connected to the power supply.

It is necessary to ensure that adequate capacitors are included in your circuitry for power supply decoupling. Here are some suggestions:

- Between the positive supply and ground terminals of the controller circuit board, connect an electrolytic capacitor of at least 10 µF (in the case of a power converter circuit board, a considerably larger capacitance may be required). This capacitor filters low-frequency variations in the power supply. Note that this electrolytic capacitor is polarized; connecting it to a power source with the wrong polarity will cause the capacitor to fail.
- For all integrated circuits on the controller board, a ceramic capacitor of at least 0.1 µF should be connected between each power supply pin and ground pin, as close as

possible to the IC. This capacitor filters high-frequency variations in the power supply. Gate driver circuitry often requires additional high-frequency decoupling capacitance, perhaps 1 µF or more.

Constructing and debugging test circuits. Do not forget to power down the circuit before you make any additions or changes to the circuit. This is especially important in later experiments that drive the converter power stage. Turn on the power only after you have checked that your are correct. In particular, always check the polarity of the power supply connections to the ICs.

If your circuit does not work, it is suggested that you troubleshoot it in a systematic manner. Use the oscilloscope to view the voltage waveforms at every pin of the first IC, beginning with its input. Are they as you expect? If not, then you have localized the problem. When the operation of the first IC is correct, then repeat the process for the next IC (and so on).