

## Lab 1B: PWM Lecture Notes

Thursday, October 14, 2021 6:45 AM

### Lab Topics:

#### - PWM

- What is it?
- purpose
- deadtime
- 3525A

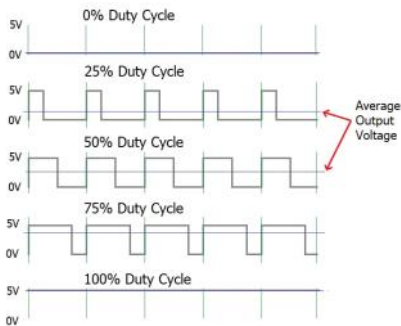
#### - Ckt layout considerations

- avoid large loops
- avoid needlessly long wires
- use top and bottom of board
- notice critical (high switch) loops, keep small.

#### - Hands-on demos (in class)

- wire stripping
- soldering
- desoldering

### PWM:

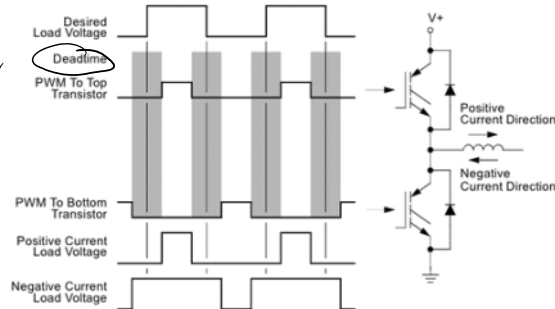


- often used to control switches in switching devices

- switch pairs are switched complementary to each other. (below)

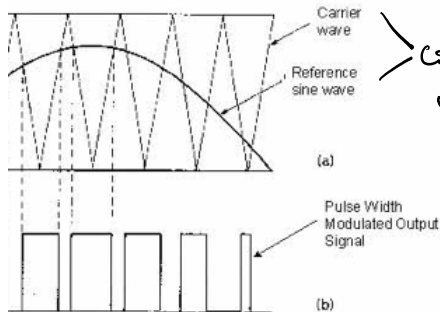
<https://circuitdigest.com/tutorial/what-is-pwm-pulse-width-modulation>

- real switches take time to switch. Deadtime avoids both switches being closed simultaneously.



[https://granitedevices.com/wiki/Dead-time\\_distortion](https://granitedevices.com/wiki/Dead-time_distortion)

PWM usually achieved by:

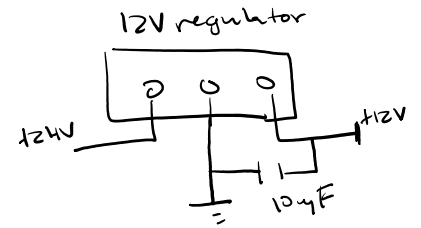
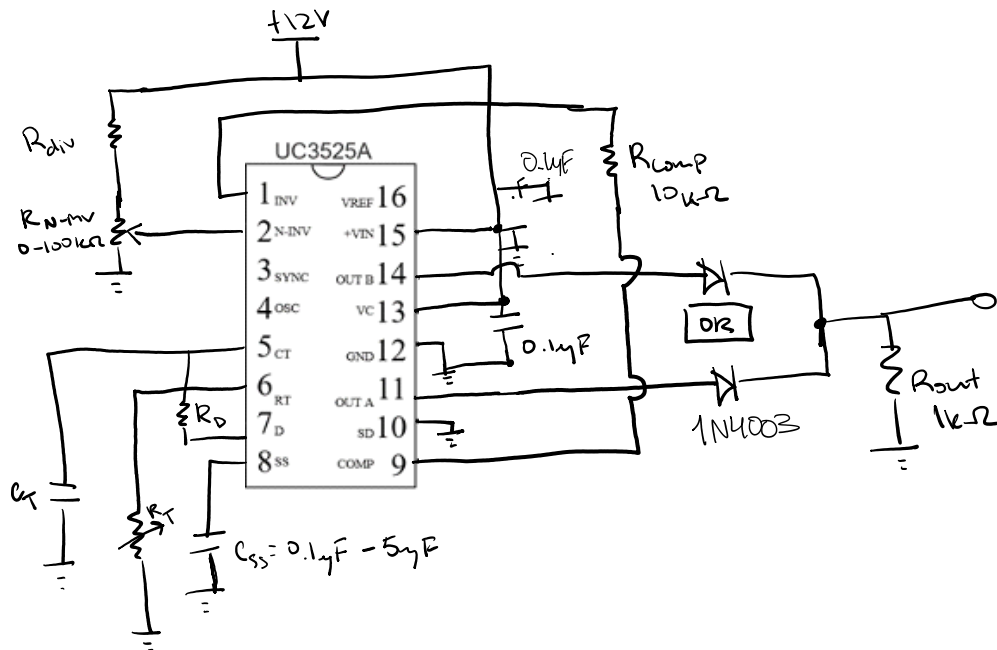


comparator yields logic hi/lo

- For 3525A: oscillator waveform is the carrier, and n-inu input is reference

# UC3525A

- common PWM controller
- we are using to control gate driver (will go over next lab section)



Calculations:

$$f = \frac{1}{C_T(0.7 R_T + 3 R_D)}$$

undergrads:  $R_D \approx 33\Omega$

grads:  $R_D = 0 - 100\Omega$  (recommended)

or  
 $0 - 500\Omega$  (datasheet recommended)

TBt: deadtime here does not matter much  
since gate driver adds own deadtime

Why **OR** outputs?

- gate driver needs only 1 input
- increased  $f_{sw}$  ( $f_{os} f_{sw}$ )
- increased duty cycle range

Capacitors:

- bypass caps filter high frequency noise  
(more on this in capstone class)

Divider:

