Lecture # 10, 10/22/2021

Last time:

- Finished Ch 3
- Started Ch 4

} HW 3 posted

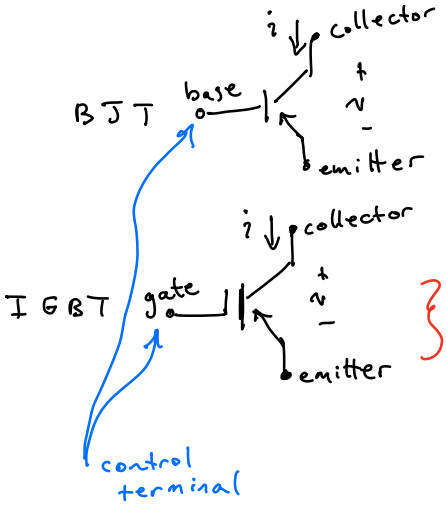
Today:

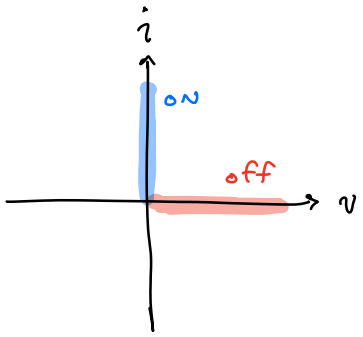
- Tiny bit of Ch 4, devices
- Lab discussion

- Devices continued

not really used in power electronics

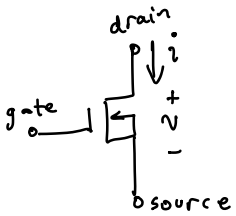
- The Insulated Gate Bipolar Trans (IGBT) & BJT



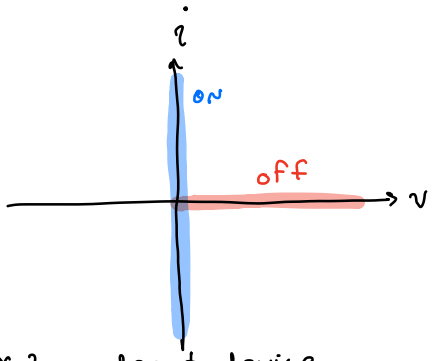


* Usually for "high power"
* single quadrant applications

- The MOSFET



n-channel



* 2 quadrant device
* usually for "low power" applications

PWM Controller
UC3525

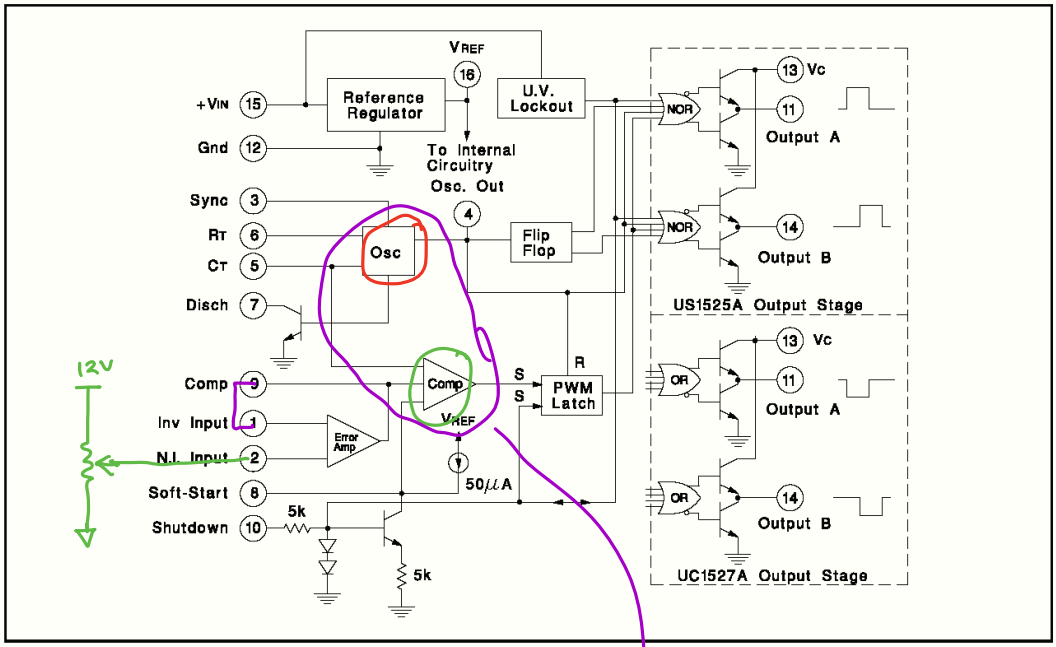
The UC3525 PWM Control IC

PWM carrier waveform

Key functions:

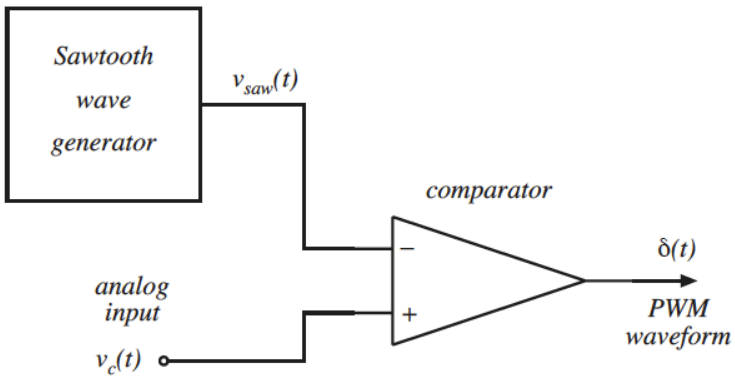
- Oscillator (sawtooth wave generator)
- PWM comparator and latch
- Error amplifier
- 5.1 V reference
- Pulse-steering logic
- Output drivers
- Shutdown and softstart circuitry

BLOCK DIAGRAM

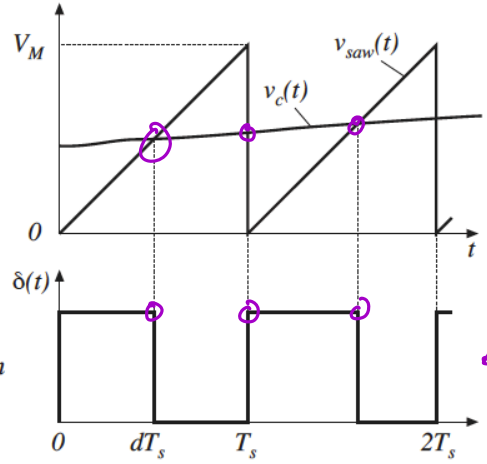


How a pulse-width modulator works

closer look



what adjusts duty ratio



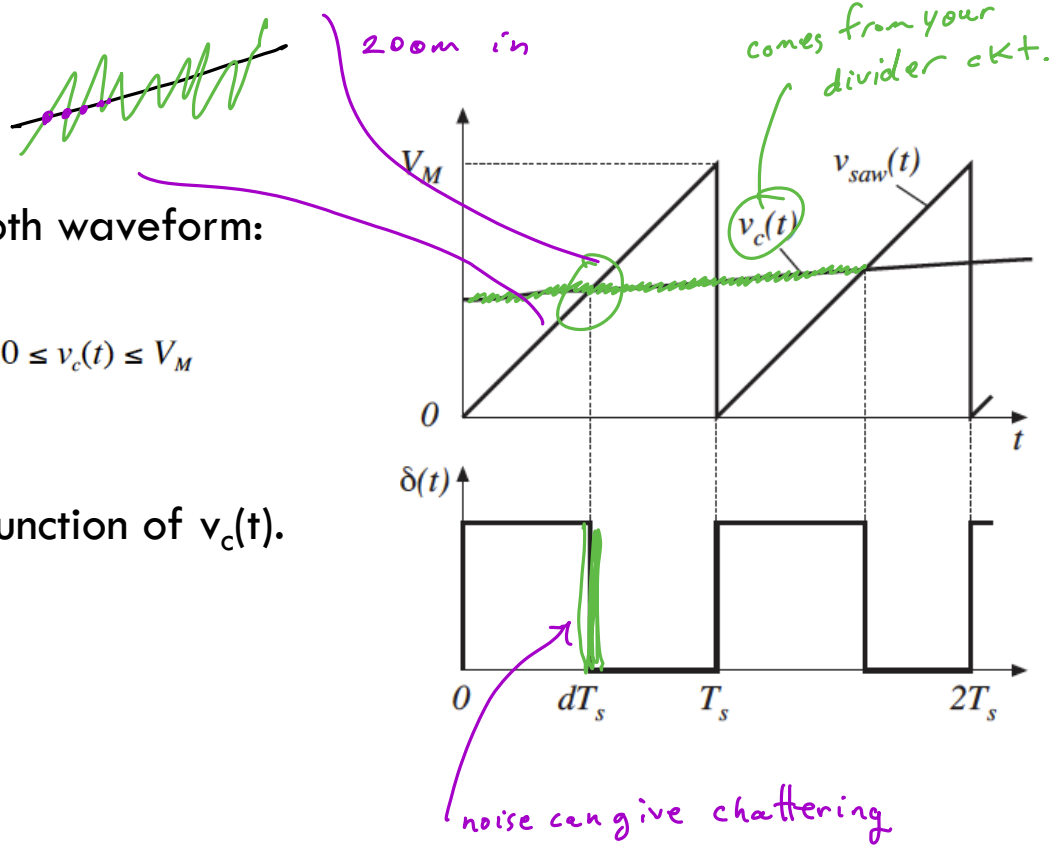
← comparator output

How a pulse-width modulator works

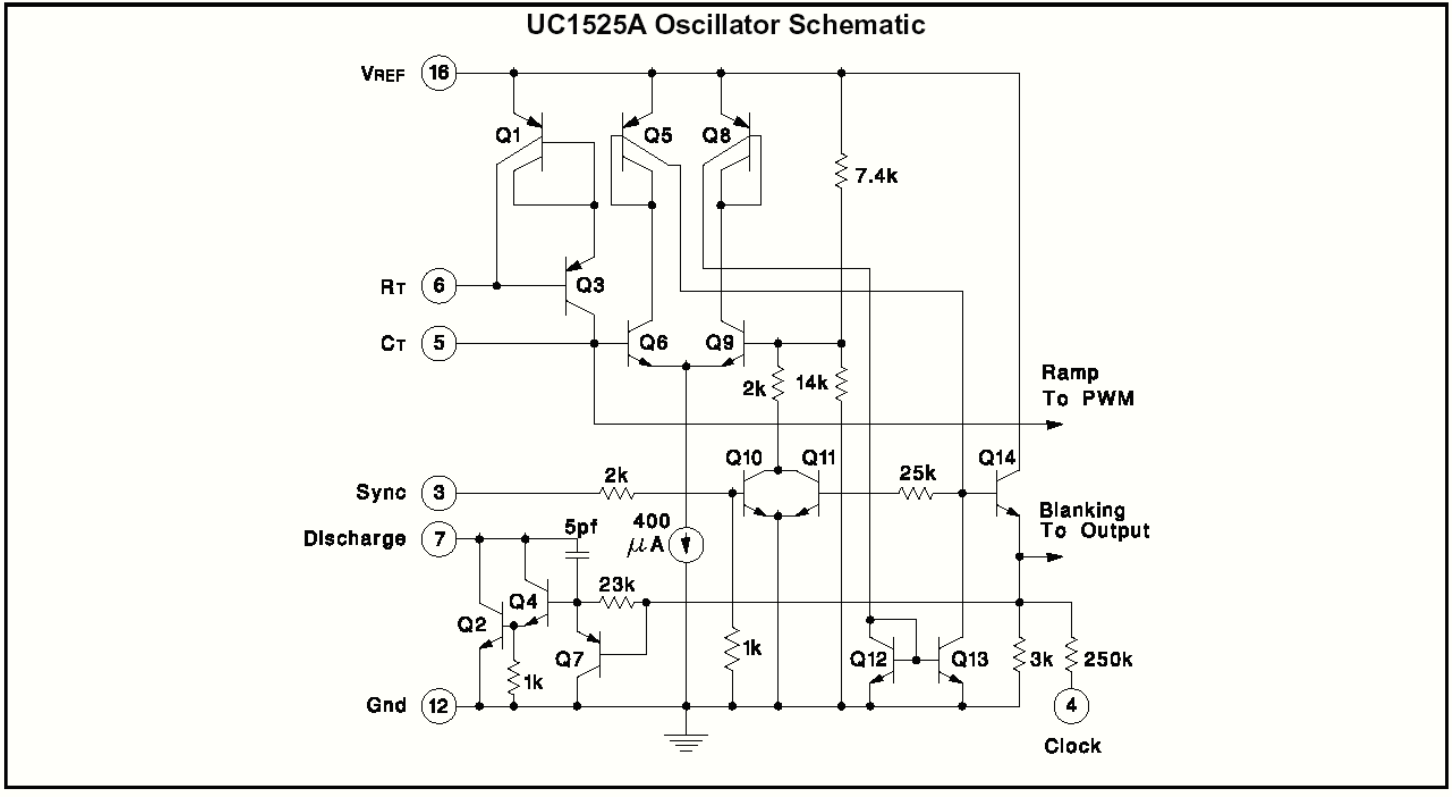
For a linear sawtooth waveform:

$$d(t) = \frac{v_c(t)}{V_M} \qquad for\ 0 \le v_c(t) \le V_M$$

So d(t) is a linear function of $v_c(t)$.

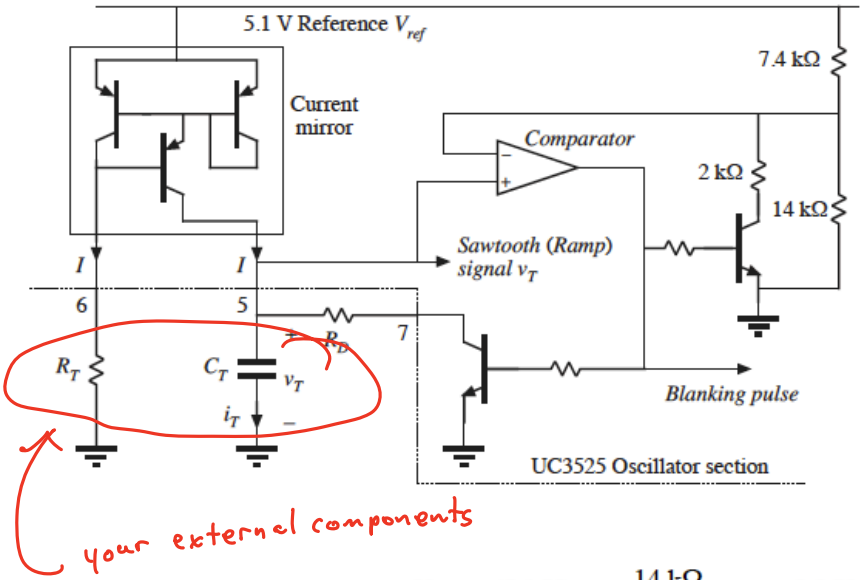


Sawtooth (ramp) oscillator

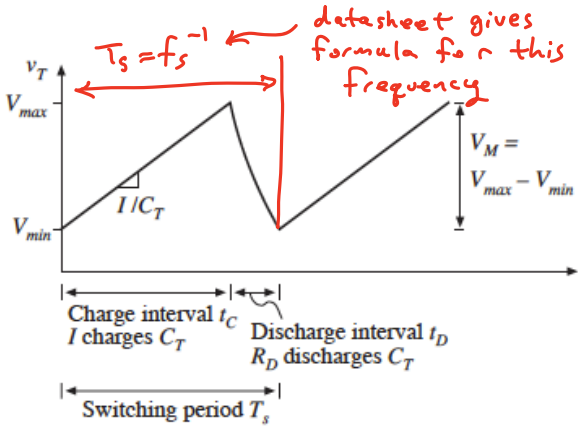


Simplified diagram of oscillator

Need a way to adjust $T_s = f_s^{-1}$



$$i_T = C_T \frac{dv_T}{dt} \qquad \text{hence} \qquad \frac{dv_T}{dt} = \frac{i_T}{C_T}$$



$$I = \frac{(5.1\text{ V}) - 2(0.7\text{ V})}{R_T}$$

$$V_{max} = (5.1\text{ V})\frac{14\text{ k}\Omega}{14\text{ k}\Omega + 7.4\text{ k}\Omega} = 3.3\text{ V}$$

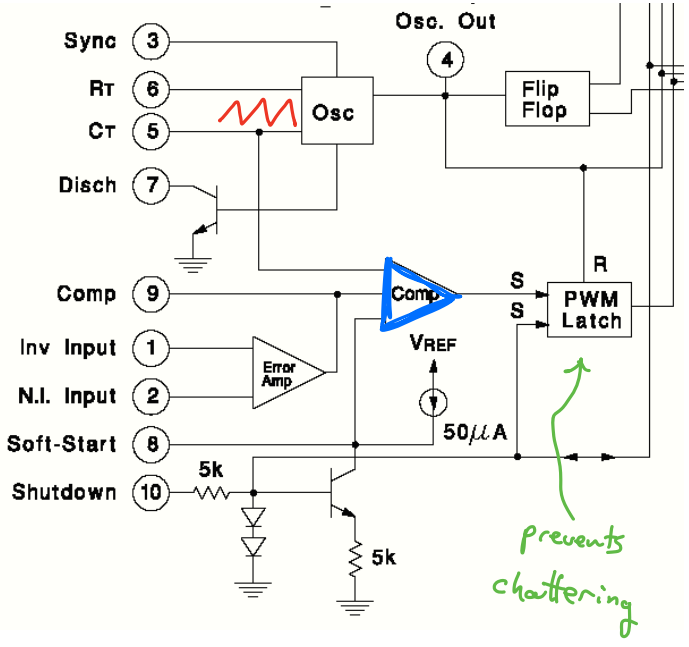
$$V_{min} = (5.1\text{ V})\frac{(2\text{ k}\Omega \parallel 14\text{ k}\Omega)}{(2\text{ k}\Omega \parallel 14\text{ k}\Omega) + 7.4\text{ k}\Omega} = 1.0\text{ V}$$

Blanking pulse causes driver outputs to be low, so that $dT_s \le t_c$

Increasing R_D reduces maximum allowed duty cycle D_{max}

PWM comparator and latch

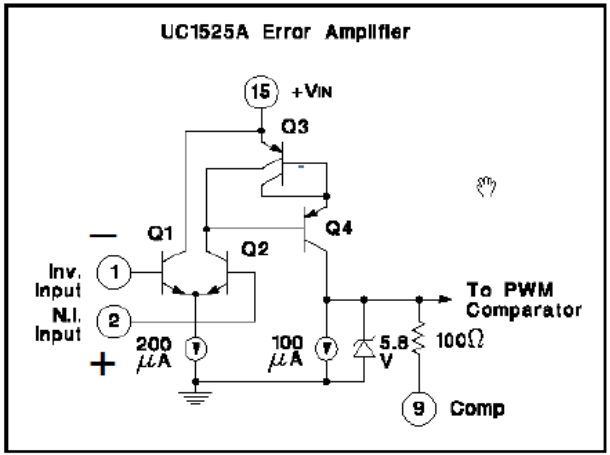
- PWM comparator "Comp"
- PWM latch is reset by oscillator during blanking interval, which starts the DTs interval
- PWM latch is set by PWM comparator, which ends the DTs interval
- The PWM latch prevents noise in the analog input from causing multiple switching during a switching period



* latch acts on first edge, & ignores other spurious transitions.

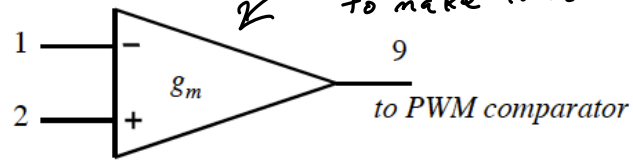
Error amplifier

can be used to make analog PI controller

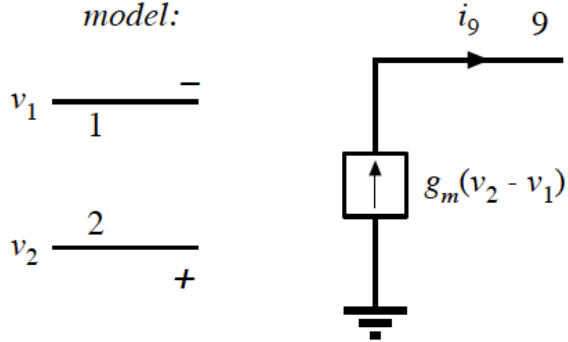


Transconductance amplifier

can add external feedback to make into a PI

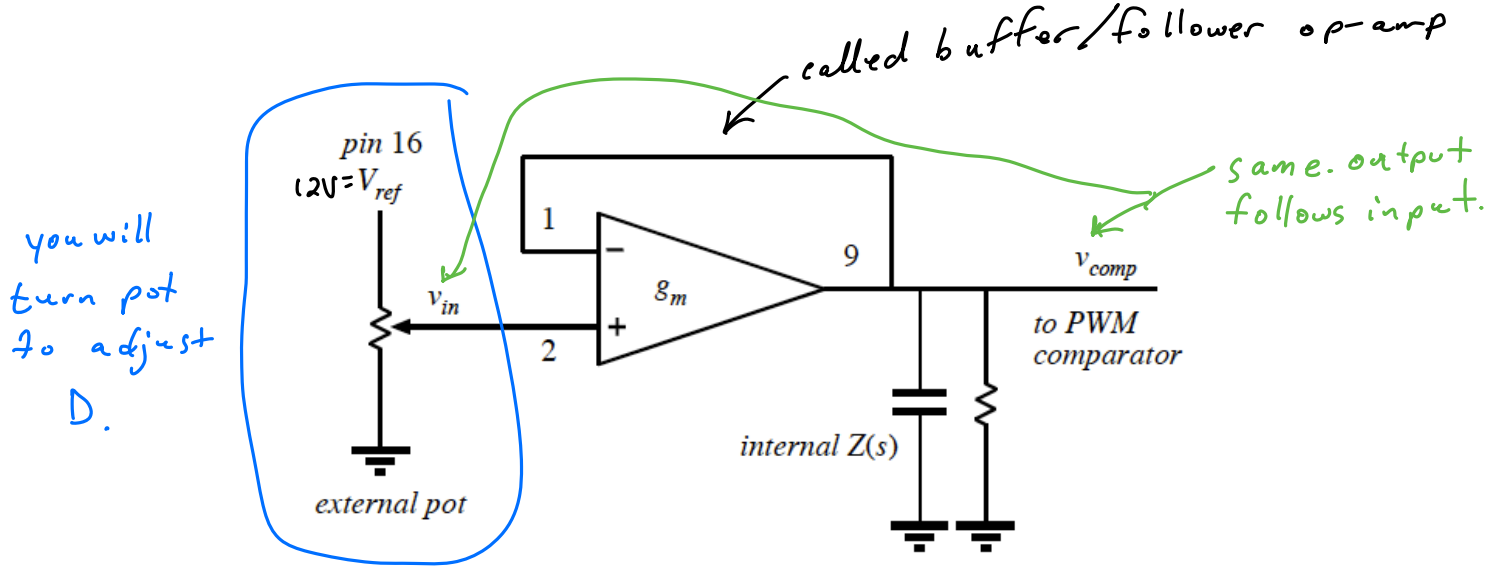


model:



* Don't need this since we are doing open loop.

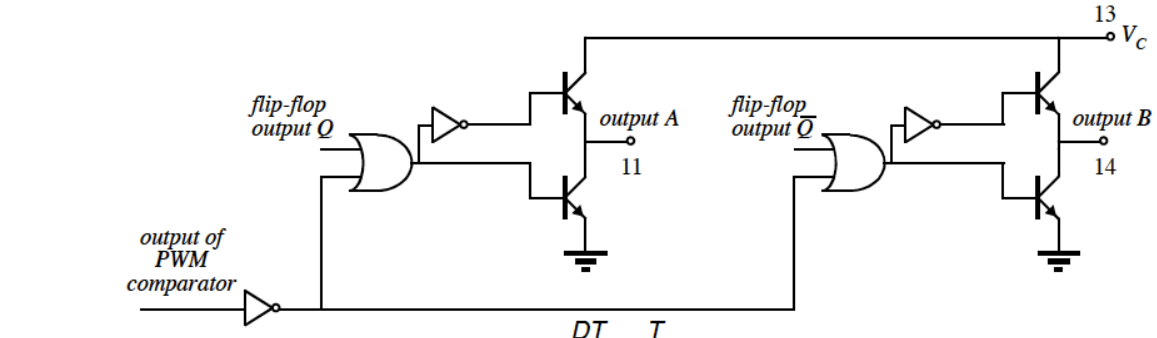
Bypass buffer & add divider ckt for adjustable D



The error amplifier is connected as a unity-gain stage: $v_{comp} = v_{in}$

The duty cycle D can be adjusted by the external pot.

Outputs of the UC3525A

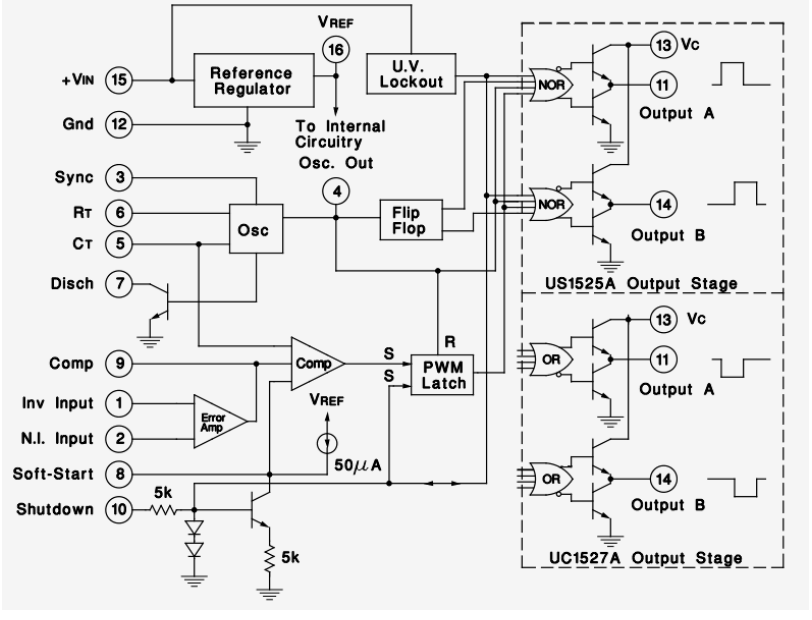


Outputs A and B can be OR-ed to restore the PWM pulses at the oscillator frequency.

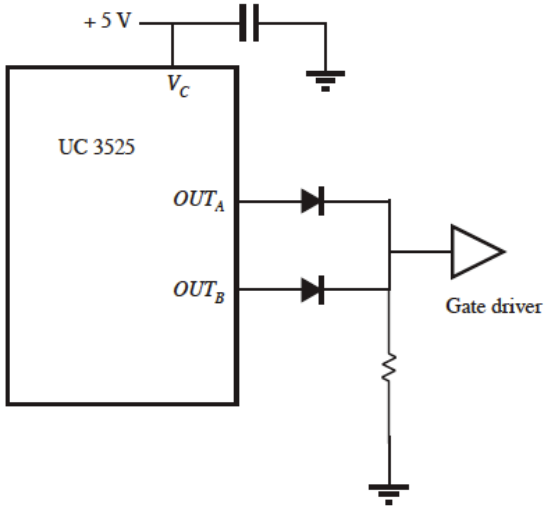
Soft start and shutdown

The shutdown pin (10) turns off the chip outputs. Ground this pin to ensure that the outputs are not shut down.

A capacitor can be connected to the soft start pin (8). The voltage on this pin limits the maximum duty cycle. At turn on, the capacitor will start at 0V, and then will charge from the 50 µA current source. This overrides the feedback loop and starts the converter gently.



OR-ing the outputs



A cheap way to OR the outputs of the UC3525

The + 5 V *can be obtained from the* 5 V *reference of the* UC3525

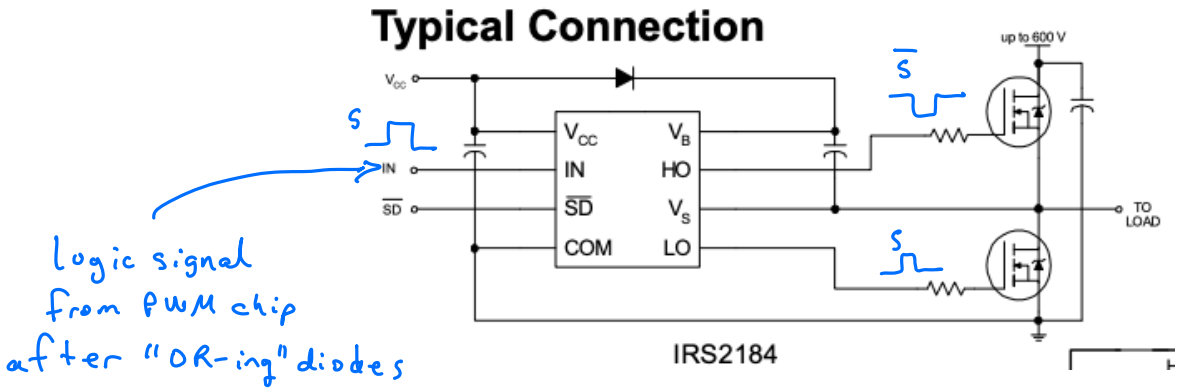
Bypass the + 5 V *so that the switching EMI of this circuit does not disrupt the internal control circuitry of the* UC3525*, which also uses the* + 5 V.

More* UC3525 *tips:

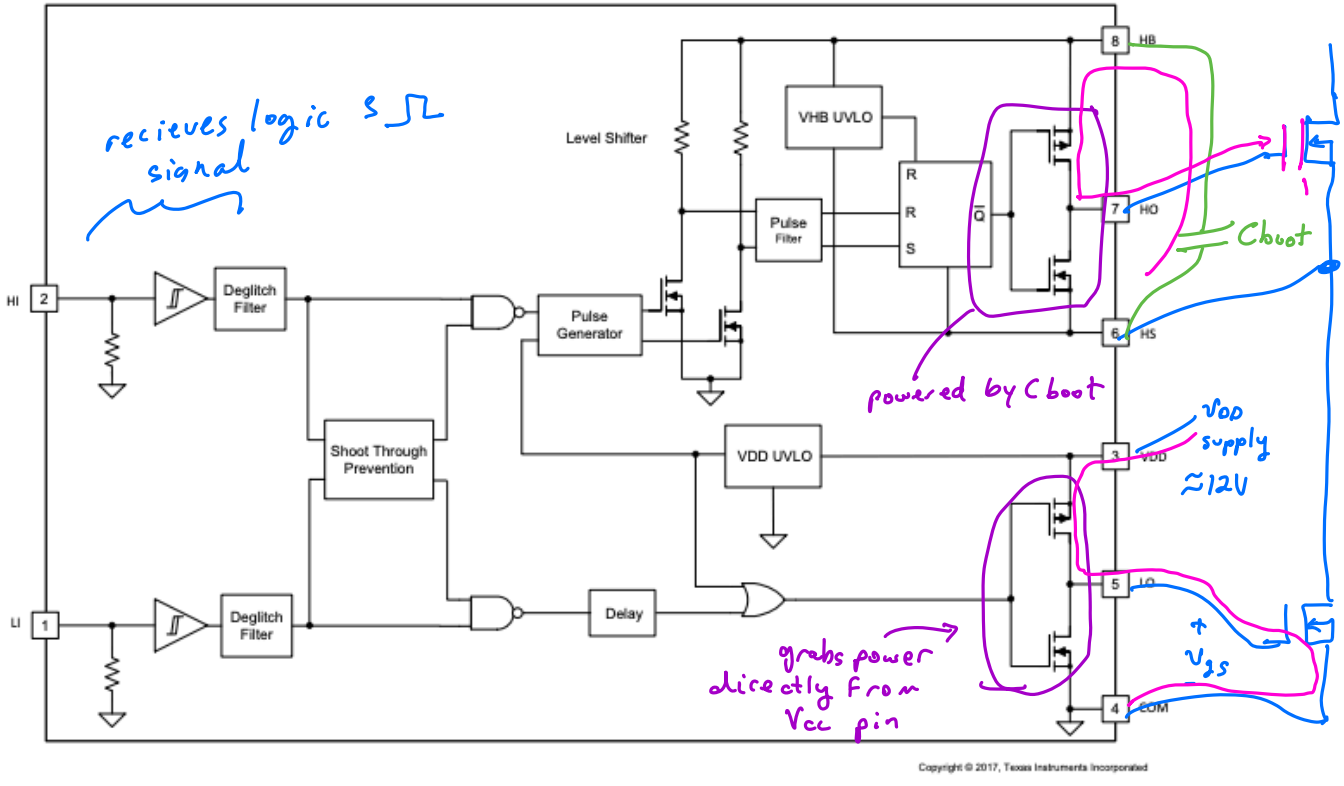
- *You will need to ground the SHUTDOWN pin. Otherwise the* UC3525 *will shut down.*
- R_T *must be greater than* 2 kΩ*; otherwise the* UC3525 *oscillator will not work*
- R_D *is usually a few hundred Ohms;* R_D *must be substantially smaller than* R_T.

Gate Driver
IRS2184

The IRS2184 driver



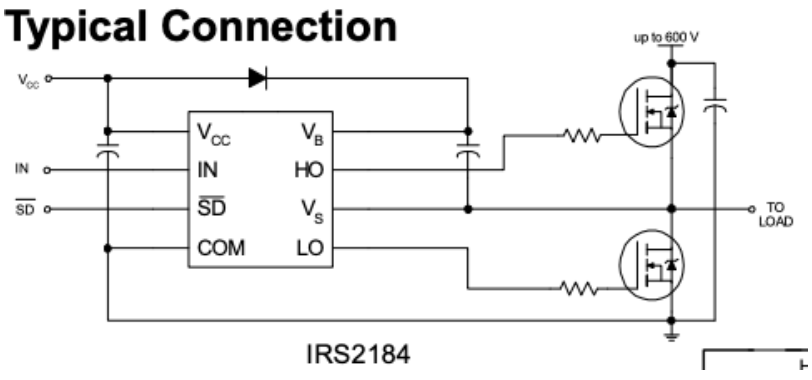
Internal structure of typical driver



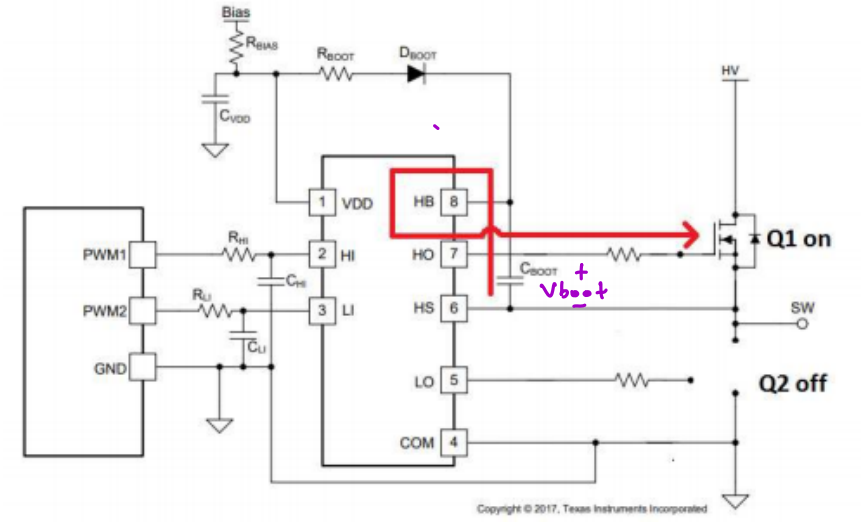
Example circuit… not our exact IC

Driver logic inputs

- Vcc power supply primarily used to power output
- IN pin accepts 3.3 V and 5 V logic
- IN pin connected to PWM IC output

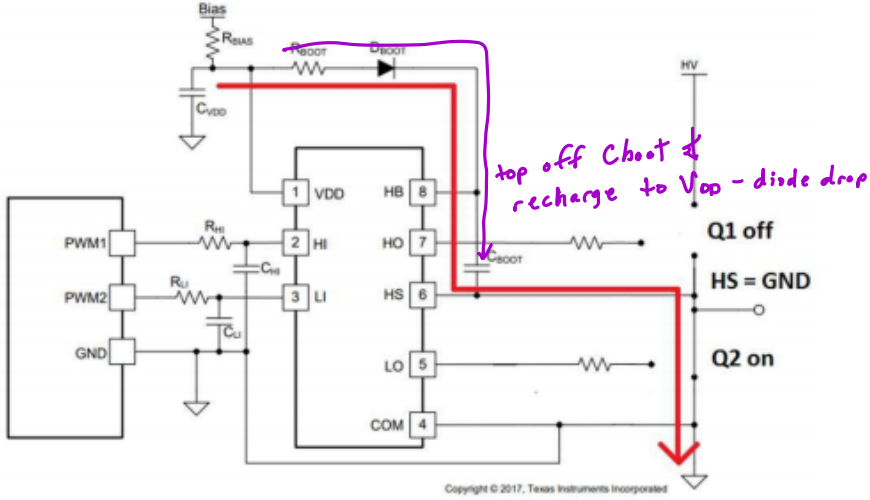


Boostrap circuit to power high-side output



discharging

Vboot will start dropping



charging