EE 473/538 Linear IC Design

HW2 February 11, 2022

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12.1. Derive an expression for I_{out} in Fig. 12.42.

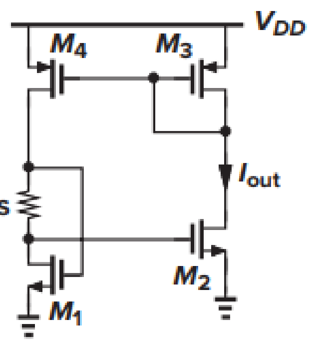

Figure 12.42

1. Given $M_3 = M_4$, then $I_{ref} = I_{out}$

Proof: Current Mirror

$$I_{ref} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W_4}{L_4}\right)(V_{gs} - V_{th_4})^2 \qquad I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W_3}{L_3}\right)(V_{gs} - V_{th_3})^2$$

M_3 and M_4 are same device $\rightarrow$ $V_{th_4} = V_{th_3}$

KCL $\quad I_{out} - I_{ref} = 0$

$$I_{out} = \frac{(W_3/L_3)}{(W_4/L_4)} I_{ref} = I_{ref}$$

Also, $M_1 = M_2$

KVL $\quad (I_{ref} R_S - V_{gs_1}) + V_{gs_2} = 0 \quad | \quad I_{D_1} = I_{ref} \ ; \ I_{D_2} = I_{out}$

$$I_{ref} R_S - \left(\sqrt{\frac{2 I_{ref}}{\mu_n C_{ox}\left(\frac{W_1}{L_1}\right)}} + \cancel{V_{th_1}}\right) + \left(\sqrt{\frac{2 I_{out}}{\mu_n C_{ox}\left(\frac{W_2}{L_2}\right)}} + \cancel{V_{th_2}}\right)$$

Known: $I_{ref} = I_{out}$, $V_{th_1} = V_{th_2}$

$$I_{out} R_S = \sqrt{\frac{2 I_{out}}{\mu_n C_{ox}\left(\frac{W_1}{L_1}\right)}} - \sqrt{\frac{2 I_{out}}{\mu_n C_{ox}\left(\frac{W_2}{L_2}\right)}} = \left(\sqrt{\frac{2 I_{out}}{\mu_n C_{ox}}}\right)\left(\frac{1}{\sqrt{\left(\frac{W_1}{L_1}\right)}} - \frac{1}{\sqrt{\left(\frac{W_2}{L_2}\right)}}\right)$$

$$I_{out}^2 R_S^2 = \left(\frac{2 I_{out}}{\mu_n C_{ox}}\right)\left(\sqrt{\frac{L_1}{W_1}} - \sqrt{\frac{L_2}{W_2}}\right)^2$$

$$I_{out} = \left(\frac{2}{\mu_n C_{ox} R_S^2}\right)\left(\sqrt{\frac{L_1}{W_1}} - \sqrt{\frac{L_2}{W_2}}\right)^2$$

12.2. Explain how the start-up circuit shown in Fig. 12.43 operates. Derive a relationship that guarantees that $V_X < V_{TH}$ after the circuit turns on.

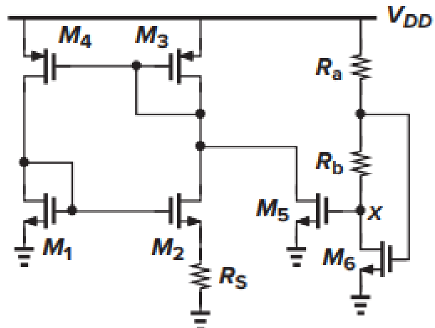

Figure 12.43

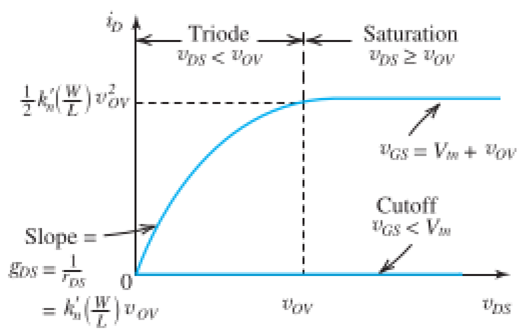

Figure: Sedra Smith Microelectronic Circuits

Define V_y at the point between R_a and R_b.

Initially, all channels are closed because $V_{DS} = V_{GS} < V_{th}$ and no current runs through R_a and R_b.

V_{DS} increases such that $V_x = V_y = V_{GS} = V_{th}$.

The channel is no longer pinched and allows current.

Both M_5 and M_6 turn on and the drain current through M_5 turns on the remaining circuit.

Now the channel is induced and V_{DS} keeps increasing, allowing more drain current through M_6.

The voltages at V_y and V_x are defined as

$$V_y = V_{DD}-I_{D6}R_a \text{ and } V_x = V_{DD}-I_{D6}\left(R_a + R_b\right) = V_y-I_{D6}R_b.$$

As I_{D6} continues to grow, V_y decreases and also V_x decreases.

It is guaranteed that $V_x < V_{th}$ when

$$V_{DD}-I_{D6}\left(R_a + R_b\right) < V_{th} \text{ where}$$

$$I_{D6} = \mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{gs} - V_{th}\right)^2 \Big|_{V_{gs}=V_{DD}-I_{D6}R_a}$$

12.5. In the circuit of Fig. 12.15, assume that Q_2 and Q_4 have a finite current gain β. Calculate the error in the output voltage.

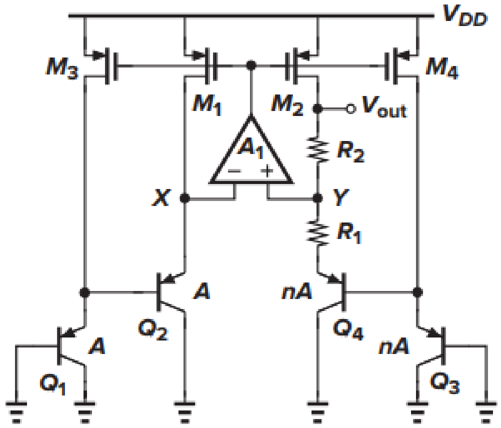

Figure 12.15 Reference generator incorporating two series base-emitter voltages.

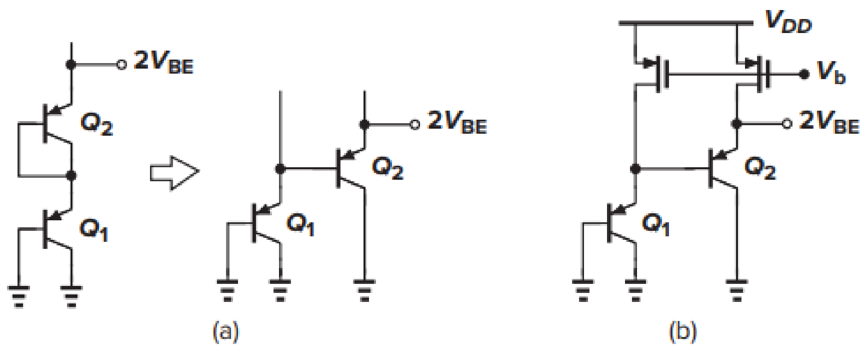

Figure 12.14 (a) Conversion of series diodes to a topology with grounded collectors; (b) circuit of part (a) biased by PMOS current sources.

5. $I_C = I_S e^{-V_{BE}/V_T}$ $\qquad V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$

$$I_E = \alpha I_C = \frac{\beta+1}{\beta} I_C$$

$$\Delta V_{BE} = 2V_T \ln\left(\frac{I_0}{I_S}\right) - 2V_T \ln\left(\frac{I_0}{nI_S}\right)$$

Assume all devices are same size

$$\Delta V_{BE} = 2V_T \ln n$$

$$I_{C4} = \frac{\Delta V_{BE}}{R_1} \rightarrow I_{E4} = \left(\frac{\beta+1}{\beta}\right)\frac{\Delta V_{BE}}{R_1}$$

$$V_{out} = V_{BE4} + V_{BE3} + (R_2+R_1) I_{E4}$$

$$V_{out} = 2V_{BE} + (R_2+R_1)\frac{2V_T \ln n}{R_1}\left(\frac{\beta+1}{\beta}\right)$$

$$V_{out} = 2V_{BE} + (R_2+R_1)\frac{2V_T \ln n}{R_1}\left(1+\frac{1}{\beta}\right)$$

(V_{out} without error has no $\frac{1}{\beta}$ term)

$$V_{out,\,error} = (R_2+R_1)\frac{2V_T \ln n}{R_1}\left(\frac{1}{\beta}\right)$$

$$\boxed{= \left(1+\frac{R_2}{R_1}\right)\left(\frac{1}{\beta}\right)\frac{2V_T \ln n}{1}}$$