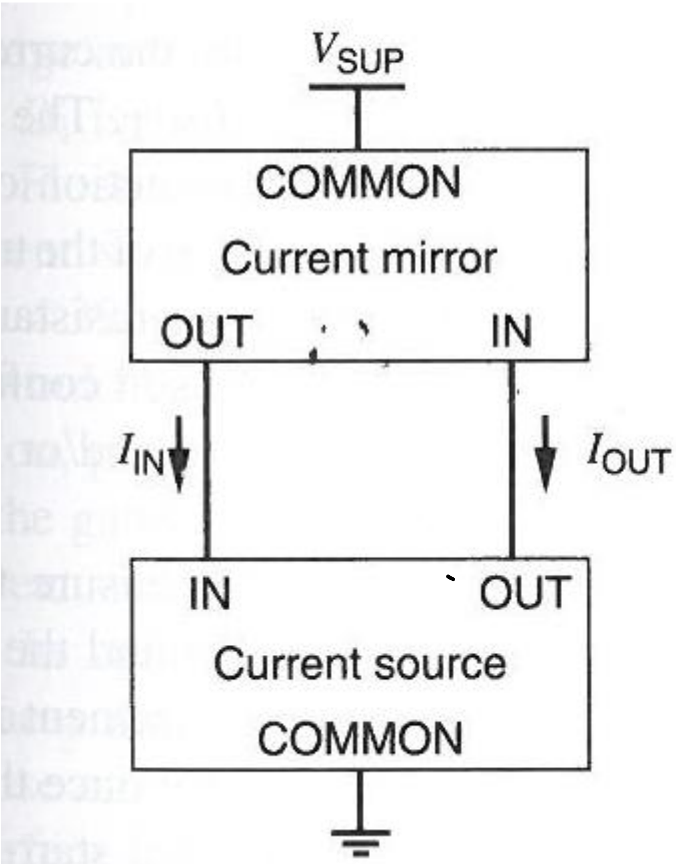
Lecture #9, Jan 26th, 2022

- Read Chapter 12.
- No Class this Friday
- Class will be in person next week with virtual option.
- Today: Continue Reference Voltage Design.
  - Current References
  - Process Voltage and Temperature Dependence.
  - Constant Voltage (Temp)
  - Proportional to Absolute Temperature (PTAT)
  - Constant Gm (Temp).

Self-Biased/Referenced Circuits

"Bootstrapped" Biasing



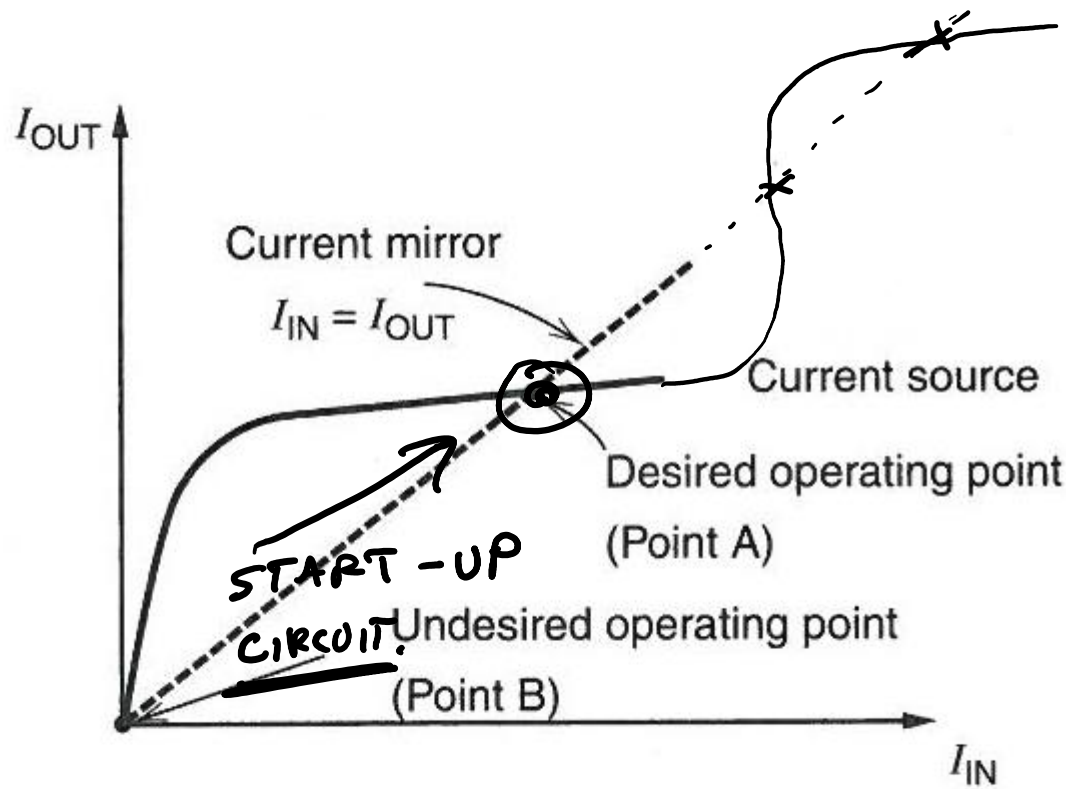
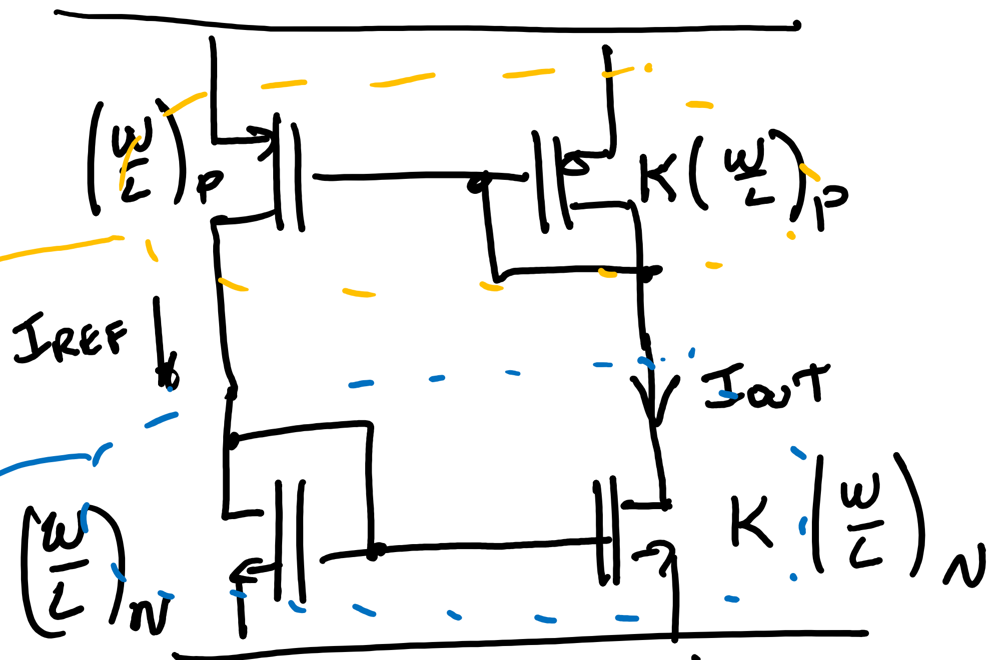


FIG. 12.2



$$I_{out} = \frac{K\,\cancel{(W/L)_n}}{\cancel{(W/L)_n}}\, I_{REF}$$

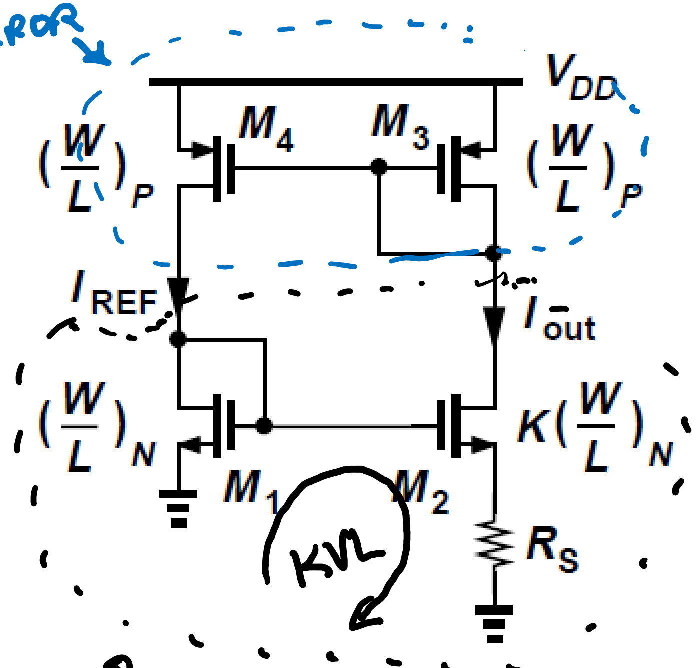
$$I_{out} = K \cdot I_{REF}$$

NO INFORMATION ABOUT I_{REF}

$$I_{REF} = \frac{(W/L)_P}{(W/L)_P\,K} \cdot I_{out}$$

Intuition Behind ΔV_{GS} Circuit

CURRENT MIRROR



CORE CURRENT SOURCE

ASSUME

- $\mu_{n1} C_{ox} = \mu_{n2} C_{ox}$
- SQ. LAW DEVICES
- IGNORE $\lambda = 0. \Rightarrow r_o = \frac{1}{\lambda I_D}$
- ALL XSISTORS IN SAT.

$$I_{D1,2} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_{1,2}\left(V_{GS1,2} - V_{tn}\right)^2$$

- FURTHER ASSUME $V_{tn1} = V_{tn2}$

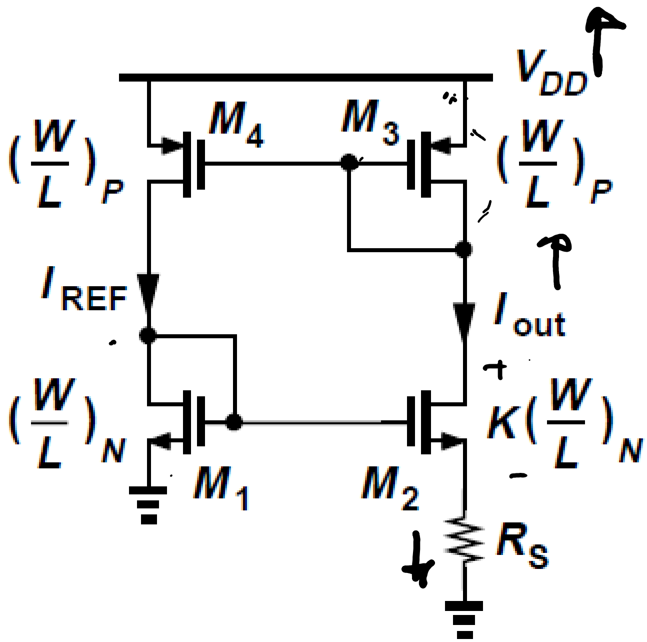
KVL

$$V_{GS1} - V_{GS2} - I_{OUT} \cdot R = 0$$

$$V_{GS} = \sqrt{\frac{2 I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)}} + V_{th}$$

$$\sqrt{\frac{2 REF}{\mu_n C_{ox}\left(\frac{W}{L}\right)}} + V_{tn} - \sqrt{\frac{2 \cdot I_{OUT}}{\mu_n C_{ox} K\left(\frac{W}{L}\right)}} - V_{tn} - I_{out} \cdot R = 0$$

Intuition Behind ΔV_{GS} Circuit



$$I_{out} = \frac{2}{\mu_n C_{ox} \left(\frac{W}{L}\right)} \cdot \frac{1}{R^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

$\mu_n(T)$ $R(T)$

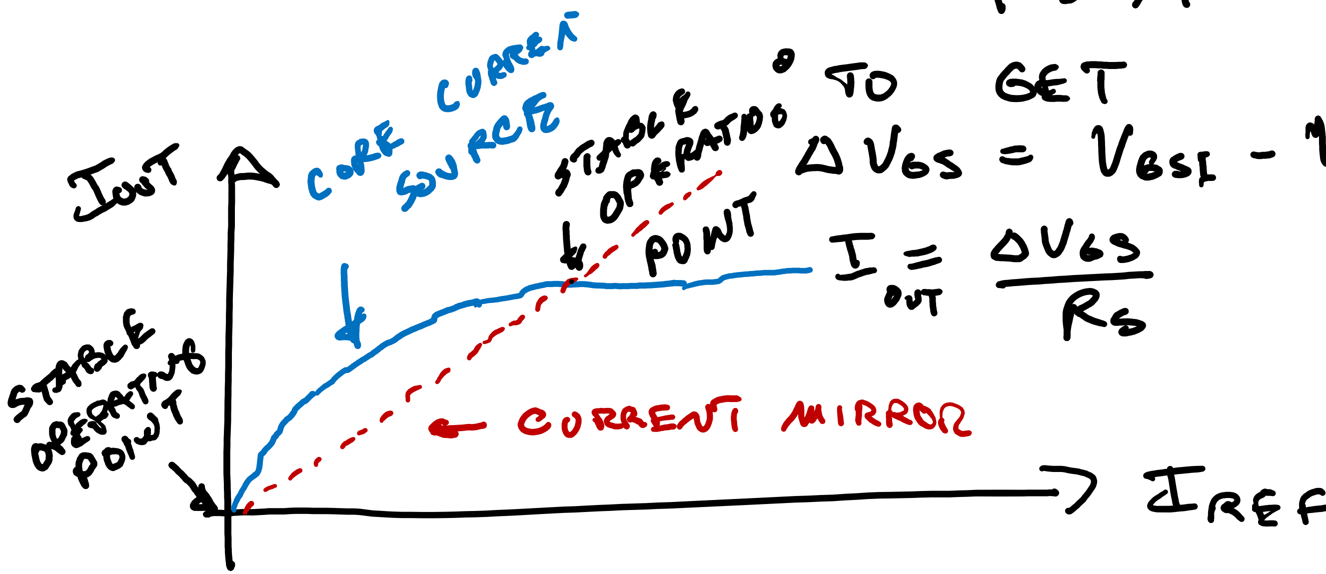
- M2 MUST WIDER (W), THAN M1.

$$\left(\frac{W}{L}\right)_1 < \left(\frac{W}{L}\right)_2$$

- TO GET

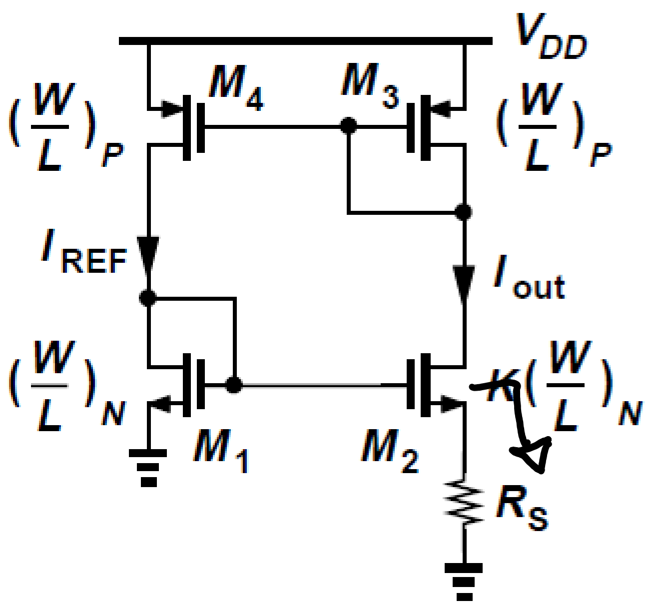
$$\Delta V_{GS} = V_{GS1} - V_{GS2}$$

$$I_{OUT} = \frac{\Delta V_{GS}}{R_S}$$



Supply-Independent Biasing

- **To uniquely define the currents, we add another constraint to the circuit as in Fig. (a)**
- **Resistor R_S decreases the current of M_2 while the PMOS devices need $I_{out} = I_{REF}$ due to identical dimensions and thresholds**



(a)

EFFECTS OF FINITE λ

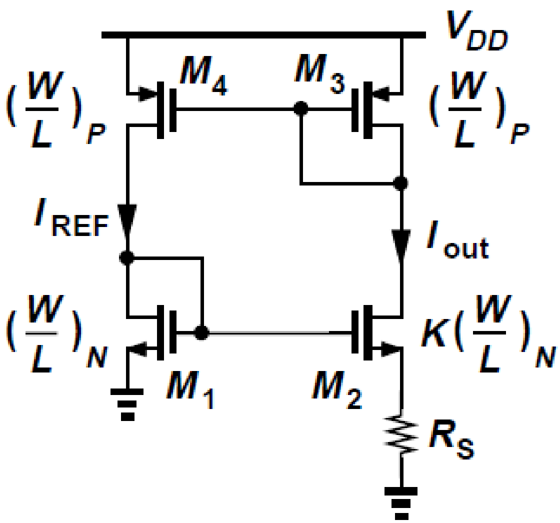
$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{th})^2(1+\lambda V_{DS})$$

$I_{OUT} \neq I_{IN}$ DUE TO FINITE r_O.

BODY EFFECT

- M_2 V_{tn} IS SLIGHTLY DIFFERENT THAN M_1.

ΔV_{GS} over R Bias Circuit



(a)

- **We can write,** $V_{GS1} = V_{GS2} + I_{D2}R_S$**, or,**

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}} + V_{TH1} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox}K(W/L)_N}} + V_{TH2} + I_{out}R_S$$

- **Neglecting body effect,**

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}}\left(1 - \frac{1}{\sqrt{K}}\right) = I_{out}R_S$$

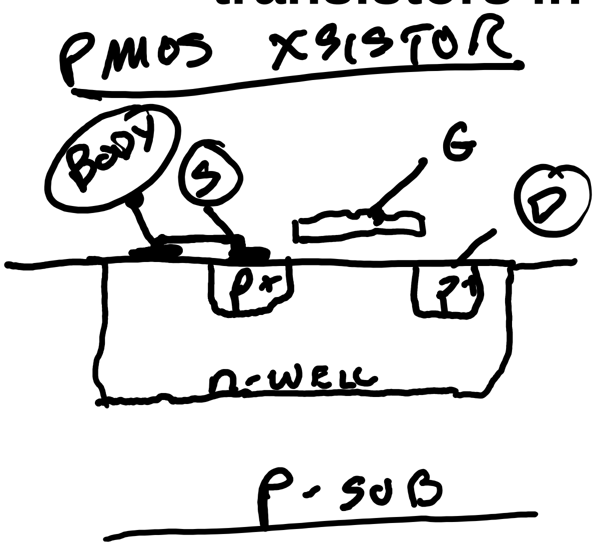
- **Hence,**

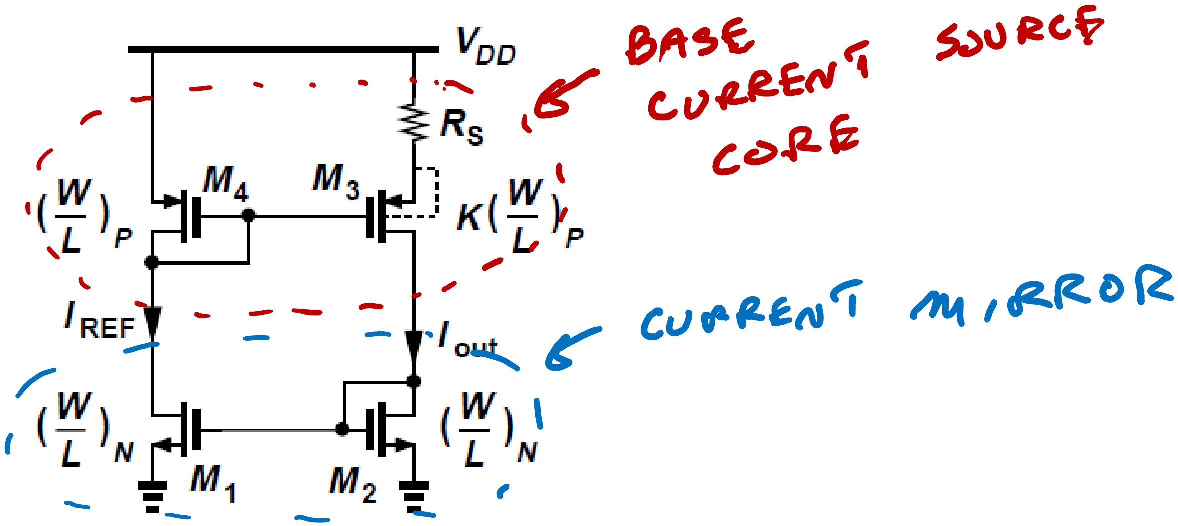
$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N} \cdot \frac{1}{R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

- **As expected, the current is independent of the supply voltage (but still a function of process and temperature)**

Removing Body Effect

- **The assumption $V_{TH1} = V_{TH2}$ introduces some error in the foregoing calculations because sources of M_1 and M_2 are at different voltages**
- **Simple remedy is to place the resistor at the source of M_3 while eliminating body effect by tying the source and bulk of each PMOS**
- **Relatively long channel lengths are used for all transistors in the circuit**

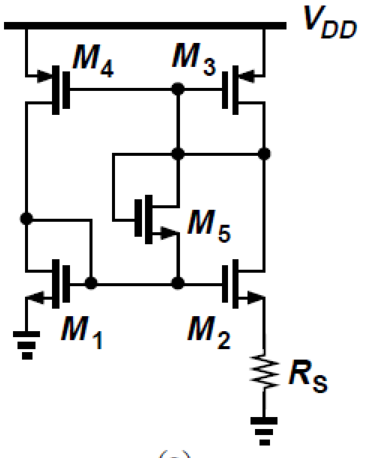




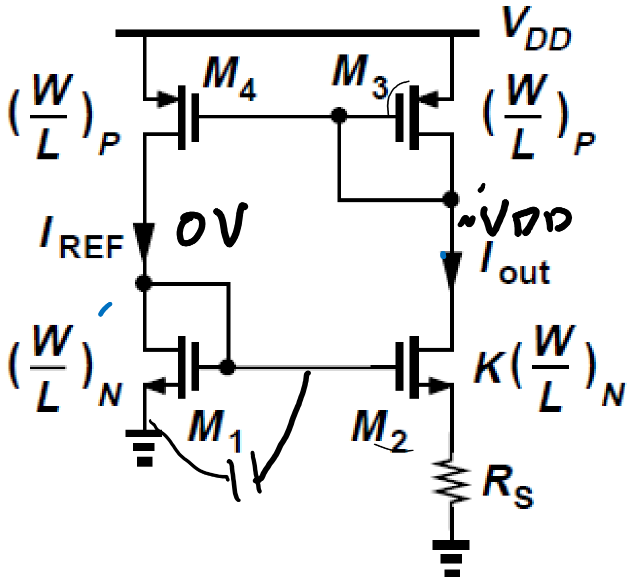
(b)

Start-Up Circuitry

- **Start-up problem can be solved by adding a mechanism to drive the circuit out of degenerate bias point when supply is turned on**
- **In Fig. (a), diode-connected device M_5 provides a current path from V_{DD} through M_3 and M_1 to ground upon start-up**
- **M_3 and M_1, and hence M_2 and M_4, cannot remain off**
- **This technique is practical only if $V_{TH1} + V_{TH5} + |V_{TH3}| < V_{DD}$ and $V_{GS1} + V_{TH5} + |V_{GS3}| > V_{DD}$ to ensure M_5 remains off after start-up**

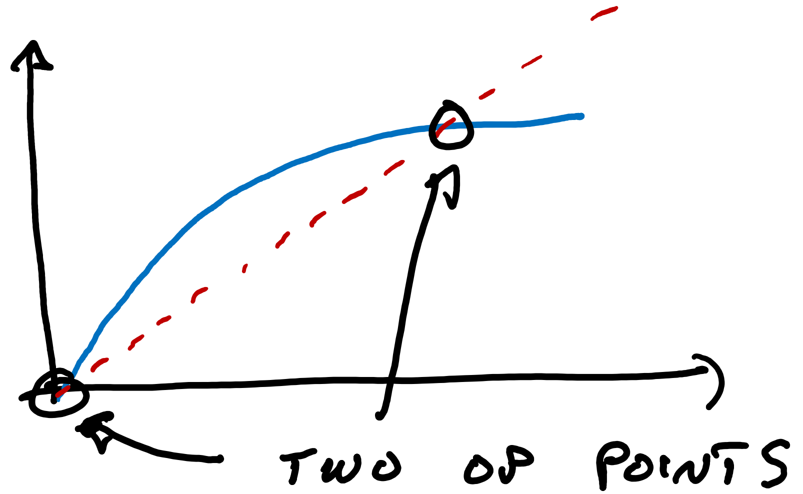


(a)



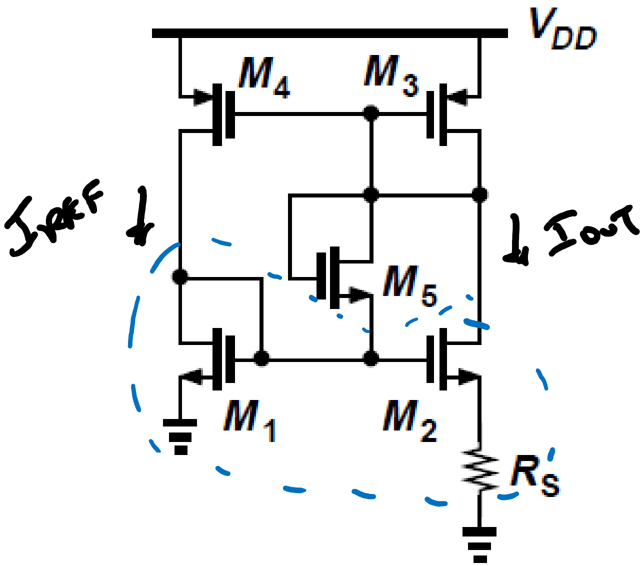
VDD
M4
M3
(W/L)P
(W/L)P
IREF
0V
~VDD
Iout
(W/L)N
K(W/L)N
M1
M2
RS

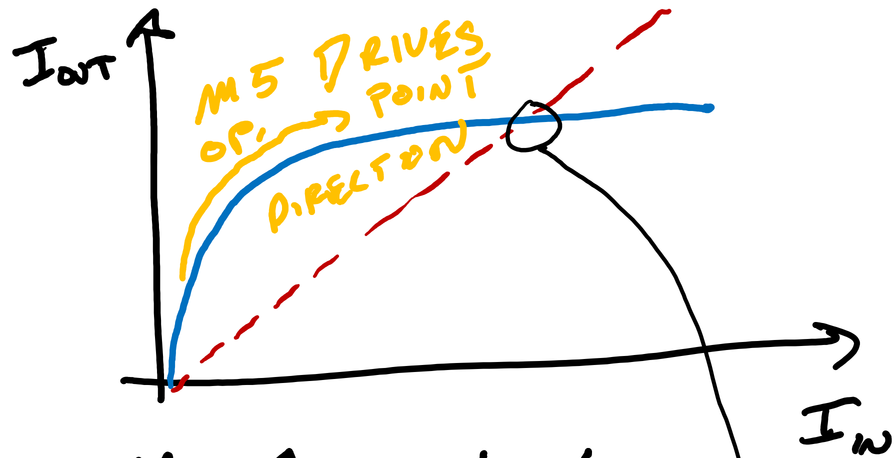
(a)



TWO OP POINTS.

Start-Up Circuitry





- IF V_{DD} ↑ 0 – 1.5V

→ $I_{OUT} = 0$

→ V_{G4} & $V_{G3} = V_{DD}$

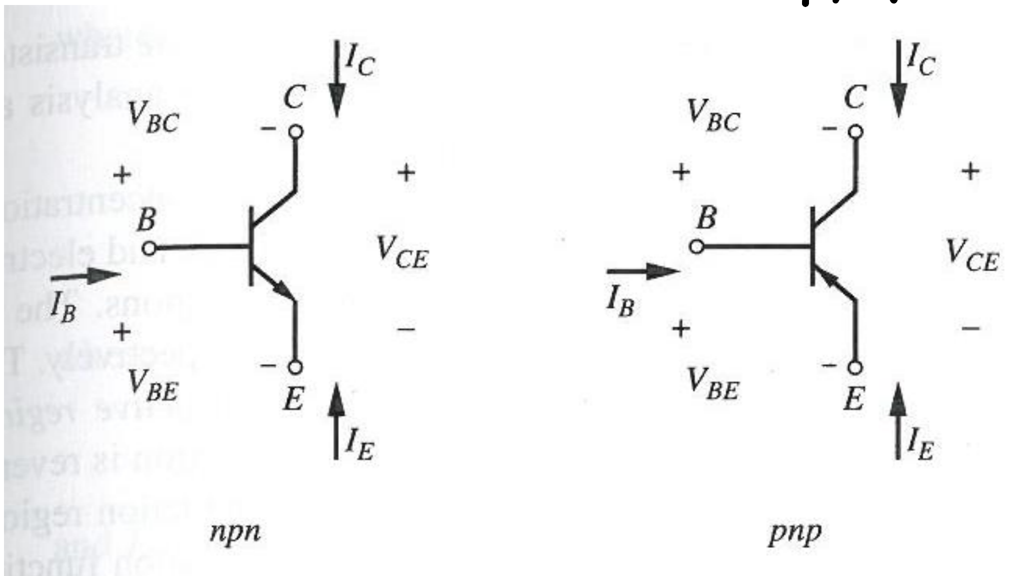
→ V_{G1} & $V_{G2} = 0V$

- AFTER C-SOURCE REACHES SS I_{OUT},

$$(|V_{GS3,4}| - V_{G1,2}) < V_{th5}$$

Bipolar Primer

NPN　　　　　　　　PNP



$I_C = -(I_E + I_b)$　　　　$I_C = -(I_E + I_B)$

LARGE SIGNAL DC CURRENT

$$I_C = \frac{q\,A\,D_n\,n_{po}}{W_B} \exp\left(\frac{V_{BE}}{V_T}\right)$$

$$I_S = \frac{q\,A\,D_n\,n_{po}}{W_B}$$

MINORITY CARRIERS IN BASE

$V_T = KT/q$

V_T @ ROOM TEMP $\approx 25\,mV$

BiPolar Device Layout