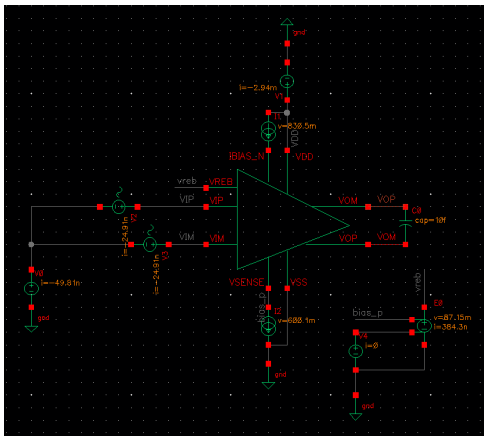
EE473/538 Cadence Lab4
Due Thursday, Feb. 17th, 2022
Kevin Egedy

Lab 4 discusses the design of a single-stage, fully differential op-amp. The input signal is common mode 600mV and AC signal 10uV. The opamp output sits on top of 673.7mV with approximately 150uV AC signal.



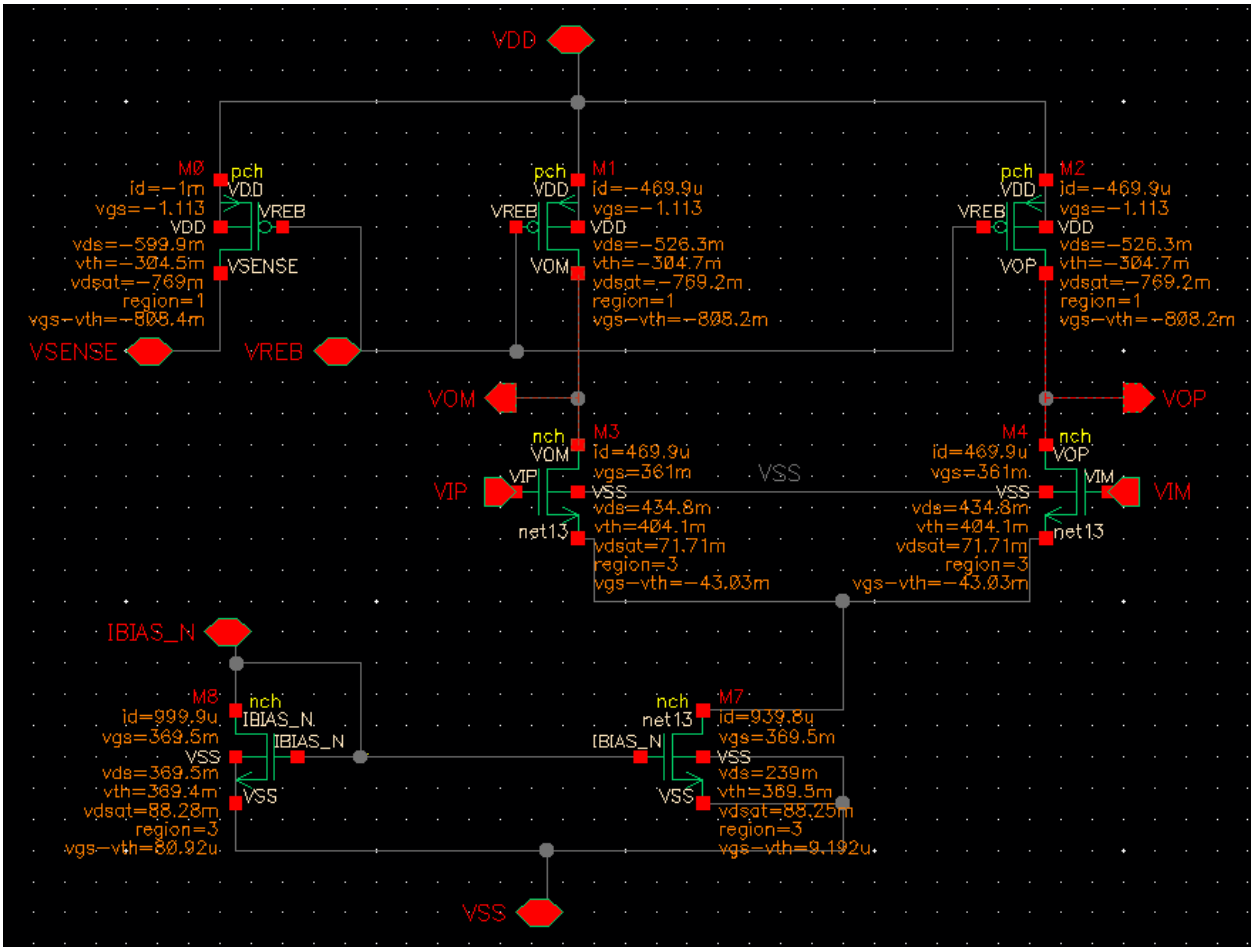
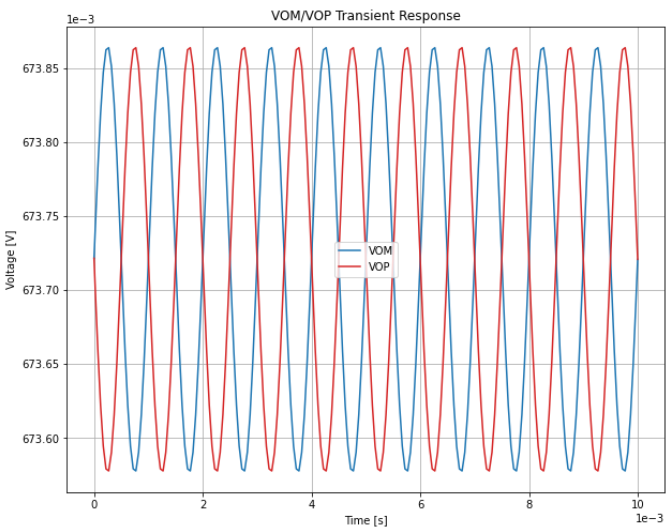
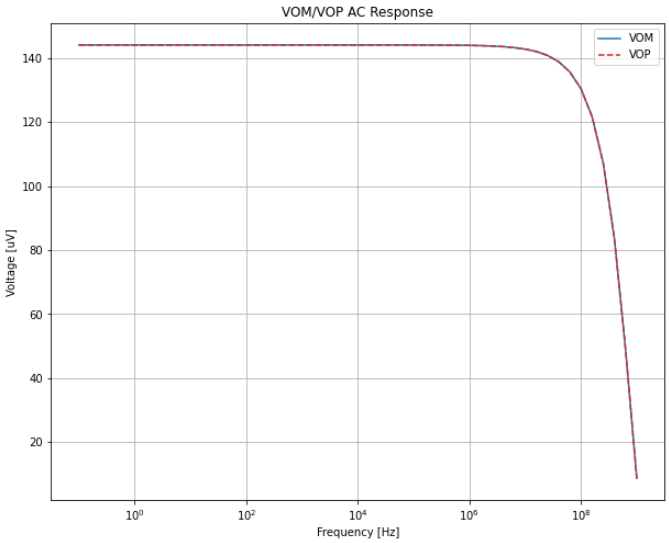


Figure: Amplifier Internal Circuit. PMOS in Triode, NMOS in Saturation

Regions
0 Cutoff
1 Triode
2 Saturation
3 Subthreshold
4 Breakdown

Device	W	L	Device	$\|id\|$	$\|vds\|$	$\|vgs - vth\|$
M0	2u	500n	M0	1m	599.9m	808.4m
M1	2u	500n	M1	469.9u	526.3m	808.2m
M2	2u	500n	M2	469.9u	526.3m	808.2m
M3	8u	200n	M3	469.9u	434.8m	43.03m
M4	8u	200n	M4	469.9u	434.8m	43.03m
M7	8u	200n	M7	939.8u	239m	9.192u
M8	8u	200n	M8	999.9u	369.5m	80.92u





Given 10uV AC signal, the amplifier small signal gain is approximately 15 V/V from the frequency response. The expected output signal now has an amplitude of 150uV and is evident on the transient response. Note, the amplifier has a small amount of common mode gain because it is no longer sitting at the 600mV input. The AC signal is riding on top of 673.7mV such that the common mode gain is (673.7mV)/(600mV) = 1.12 V/V. The output waveform is from [673.57mv, 673.87mV].