Bandgap References

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***Abstract*—Overview of the design decisions and challenges for a 1.25V reference using 65nm TSMC PDK technology.**

I. Introduction

The need for temperature-independent references are essential for modern applications and rapidly changing environments. This article discusses the negative and positive temperature coefficients (TC) of a bipolar device and how to cancel their effects to create a stable reference.

A. Negative-TC Voltage (CTAT)

For a bipolar device, the forward voltage of a *pn*-junction diode exhibits a negative TC.

$$I_C = I_s \exp(V_{BE}/V_T) \text{ where } V_T = \frac{kT}{q}$$

$$I_S = bT^{4+m} \exp(-\frac{Eg}{kT})$$

$$V_{BE} = V_T \ ln\left(\frac{I_C}{I_S}\right)$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ ln\frac{I_C}{I_S} - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T}$$

$$\frac{V_T}{I_S}\frac{\partial I_S}{\partial T} = (4+m)\frac{V_T}{T} + \frac{E_g}{kT^2}V_T$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T} \ ln\frac{I_C}{I_S} - (4+m)\frac{V_T}{T} + \frac{E_g}{kT^2}V_T$$

$$= \frac{V_{BE} - (4+m)V_T - E_g/q}{T}$$

Thus, at $T = 300K$ and $V_{BE} \approx 750$mV, the change in TC voltage with respect to temperature is $\partial V_{BE}/\partial T \approx -1.5$mV.

B. Postive-TC Voltage (PTAT)

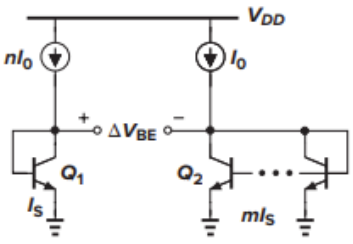

Fig. 1. PTAT Circuit

Figure 1 shows two bipolar transistors operating with ideal current sources. The difference between their base-emitter voltages is directly proportional to absolute temperature. The circuit emphasizes design choices by scaling bias current *n* and number of devices *m*.

$$\begin{aligned}\Delta V_{BE} &= V_{BE1} - V_{BE2} \\ &= V_T \ ln(\frac{nI_0}{I_S}) - V_T \ ln(\frac{I_0}{mI_S}) \\ &= V_T \ ln(nm) \\ &= \frac{kT}{q} \ ln(nm) \\ \frac{\partial}{\partial T}\Delta V_{BE} &= \frac{\partial}{\partial T}\frac{kT}{q} \ ln(nm) \\ &= \frac{k}{q} \ ln(nm)\end{aligned}$$

The positive temperature coefficient is proportional to $\frac{k}{q}$ such that $\frac{\partial}{\partial T}\Delta V_{BE} = \alpha \ 0.087$ mV/C.

C. Bandgap Reference

Now a temperature independent reference can be obtained by combining the negative and positive coefficients mentioned previously. The reference is defined as

$$V_{REF} = \alpha_1 V_{BE} + \alpha_2 V_T ln(nm)$$

For simplicity, α_1 is chosen to be 1. Then V_{REF} is

$$V_{REF} = V_{BE} + \alpha_2 V_T ln(m)$$

$*m$ is the number of devices, denoted as n in figure 2

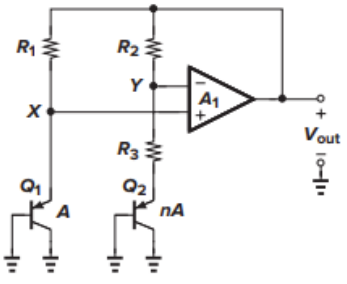

Fig. 2. Practical Bandgap Implementation

Multiple closed-loop topologies exist to implement necessary α_2. Given sufficiently large gain, V_{out} of figure 2 is

$$V_{out} = V_{BE} + \frac{V_T\ ln(n)}{R_3}(R_2 + R_3)$$
$$= V_{BE} + V_T\ ln(n)\left(1 + \frac{R_2}{R_3}\right)$$
$$\alpha_2 = 1 + \frac{R_2}{R_3}$$

There are multiple solutions for α_2 and n to cancel out the negative TC voltage. In this solution, n is chosen to be 4 such that the ratio of R_2 to R_3 is not large. The temperature coefficients are set equal to each other and $\frac{\partial}{\partial T}V_{BE}$ is assumed to be 1.5 mV.

$$\alpha_2\ ln(n)\ \frac{\partial}{\partial T}\Delta V_{BE} = -\frac{\partial}{\partial T}V_{BE}$$
$$\alpha_2\ ln(4)\ 0.087mV = 1.5mV$$
$$\alpha_2 = \frac{-1.5/0.087}{ln(4)}$$
$$\alpha_2 \approx 12.4$$

Note, this is just an approximation for α_2. The actual $\frac{\partial}{\partial T}V_{BE}$ needs to be measured to appropriately scale the PTAT voltage.

D. CTAT & PTAT Measurements

The circuit from figure 2 is implemented with an additional startup circuit to force the DC operating point out of zero current state. Initially, all resistors are set to the same value $(R_1 = R_2 = R_3 = 1K)$ because I'm only interested in measuring $\frac{\partial}{\partial T}V_{BE}$. Also, the size of the resistors determines how much current flows through the circuit since $I_0 = \frac{V_T\ ln(n)}{R_3}$. Resistors are chosen with magnitudes of 1 KΩ in order to force a current of μAs through R_3.

The CTAT voltage is simulated from -40 to 120 Celcius and the change with respect to temperature is measured at -1.57mV at 40 degrees Celcius.

Now α_2 is scaled to this measurement.

$$\alpha_2 = \frac{-1.56/0.087}{ln(4)}$$
$$\alpha_2 \approx 13$$
$$\frac{R_2}{R_3} \approx 12$$

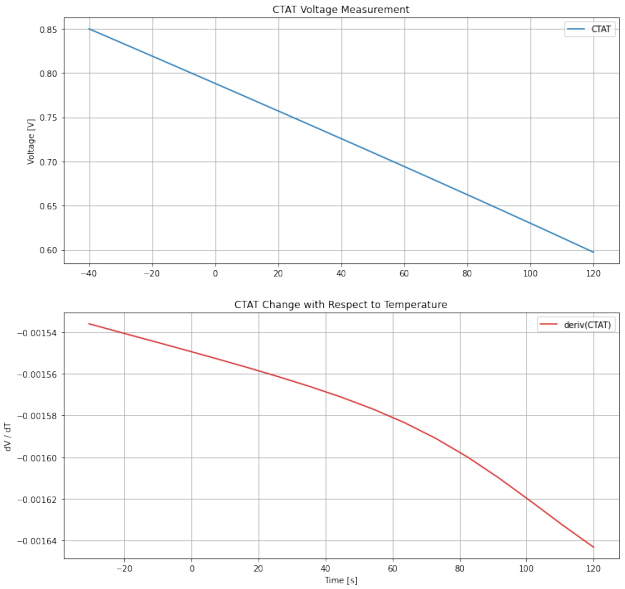

Fig. 3. CTAT Voltage and CTAT Change with Temperature

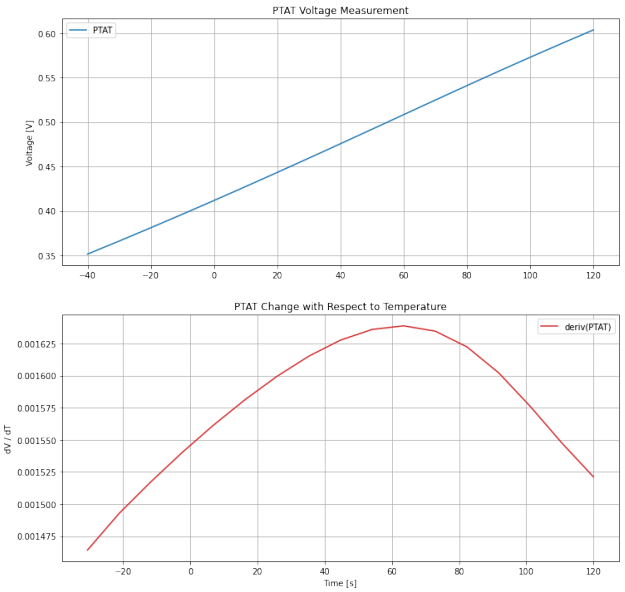

Fig. 4. PTAT Voltage and PTAT Change with Temperature

E. Design Mismatch

The amplifier for this design is a voltage controlled voltage source with open loop gain 500V/V. The amplification is not very large and results in some error from the expected value $1 + \frac{R_2}{R_3}$. In addition, the PTAT coefficient does not follow a linear relationship and results in a slightly mismatched cancellation. Thus, the actual resistor combination is chosen such that

$$\frac{R_2}{R_3} \approx 9.$$

F. Voltage Reference

The median voltage reference from -40 to 120C is 1.202V and ΔV_{out} is 0.0034V. The measured results agree well with the expected calculations. The expected output voltage is defined as

$$V_{out} = V_{BE} + V_T \; ln(n)\left(1 + \frac{R_2}{R_3}\right)$$

$$= 0.85 + (26mV) \; ln(4)\left(1 + \frac{11.329K}{1.292K}\right)$$

$$= 1.202V$$

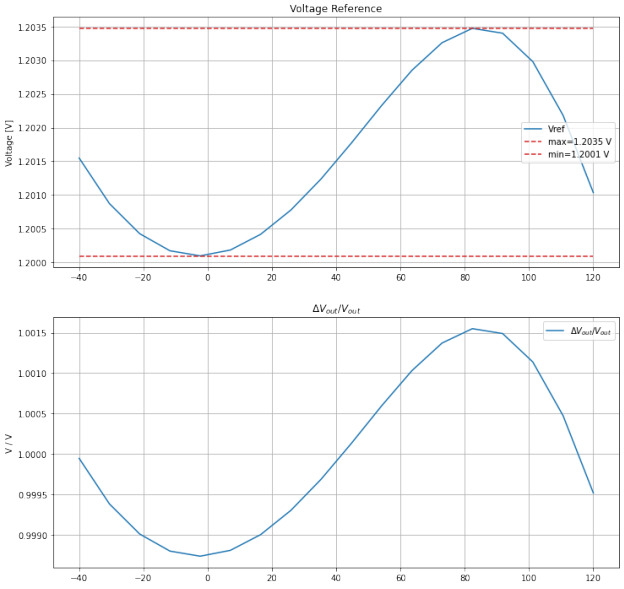

Fig. 5. Voltage Reference

G. Device Sizes

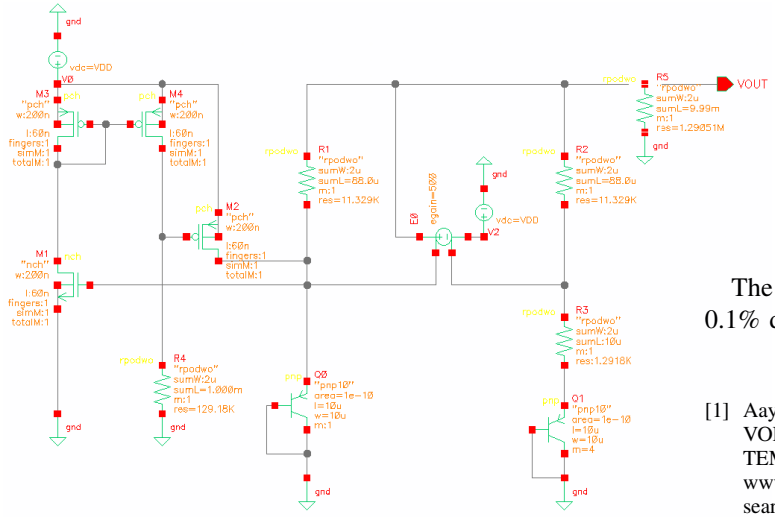

Fig. 6. Bandgap Schematic and Device Size

Device	Name	W	L
Q0	pnp10	10u	10u
Q1	pnp10	10u	10u
M1	nch	200n	60n
M2	pch	200n	60n
M3	pch	200n	60n
M4	pch	200n	60n
R1	rpodwo	2u	88u
R2	rpodwo	2u	88u
R3	rpodwo	2u	10u
R4	rpodwo	2u	1m
R5	rpodwo	2u	9.99m

H. DC Operating Point

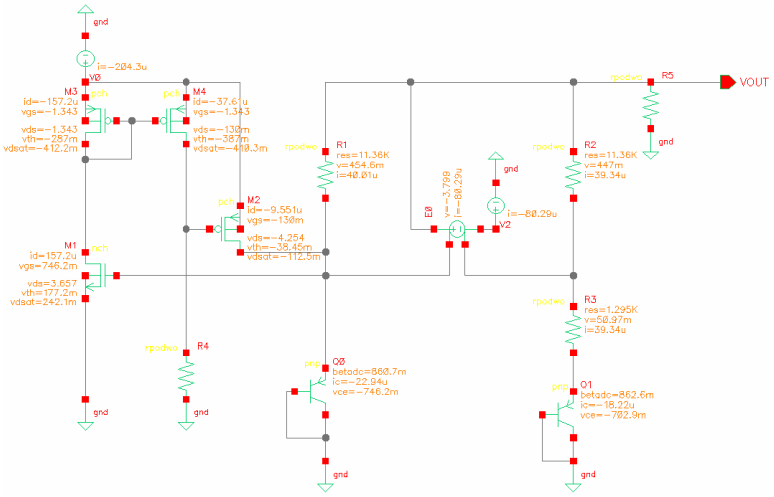

Fig. 7. Bandgap DC Operating Point

Device	Voltage	Current
Q0	vce= 746.2mV	ic= 22.92uA
Q1	vce= 702.9mV	ic= 18.22uA
M1	vds= 3.657 V	id= 157.2uA
M2	vds= 4.254 V	id= 9.551uA
M3	vds= 3.657 V	id= 157.2uA
M4	vds= 3.657 V	id= 157.2uA
R1	v= 454.6mV	i= 40.10uA
R2	v= 447mV	i= 39.34uA
R3	v= 50.97mV	i= 39.34uA

II. Conclusion

The proposed solution achieves a 1.202V reference with 0.1% deviation.

References

[1] Aayushi Vijh and Dr. S.R.P. Sinha. “DESIGN OF A CMOS BANDGAP VOLTAGE REFERENCE CIRCUIT WITH HIGH PSRR AND LOW TEMPERATURE COEFFICIENT USING 180nm TECHNOLOGY.” www.jetir.org, Journal of Emerging Technologies and Innovative Research, Nov. 2018, https://www.jetir.org/papers/JETIR1811038.pdf