EE473/538 Cadence Lab3
Due Monday, Feb. 7th, 2022
Kevin Egedy

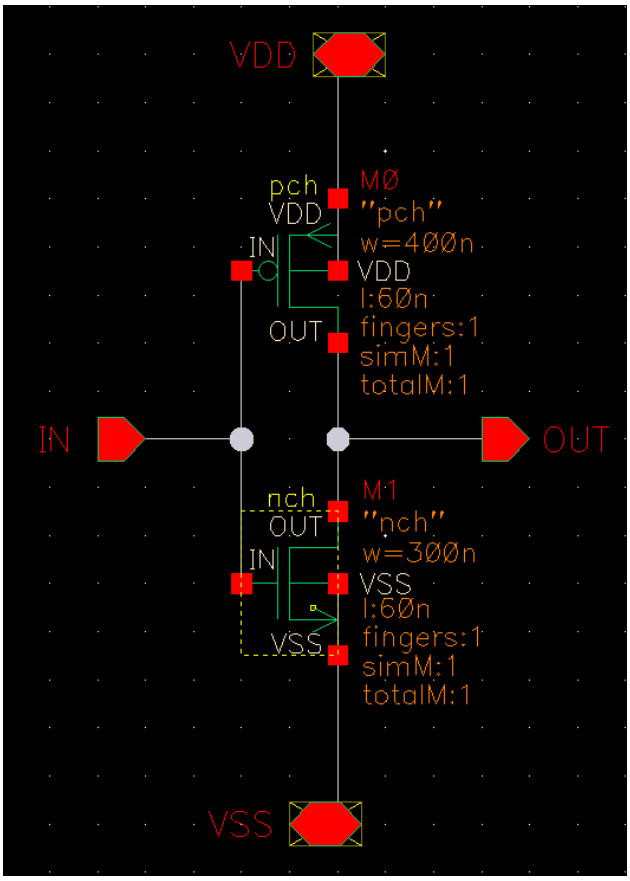

Figure1: Inverter Schematic

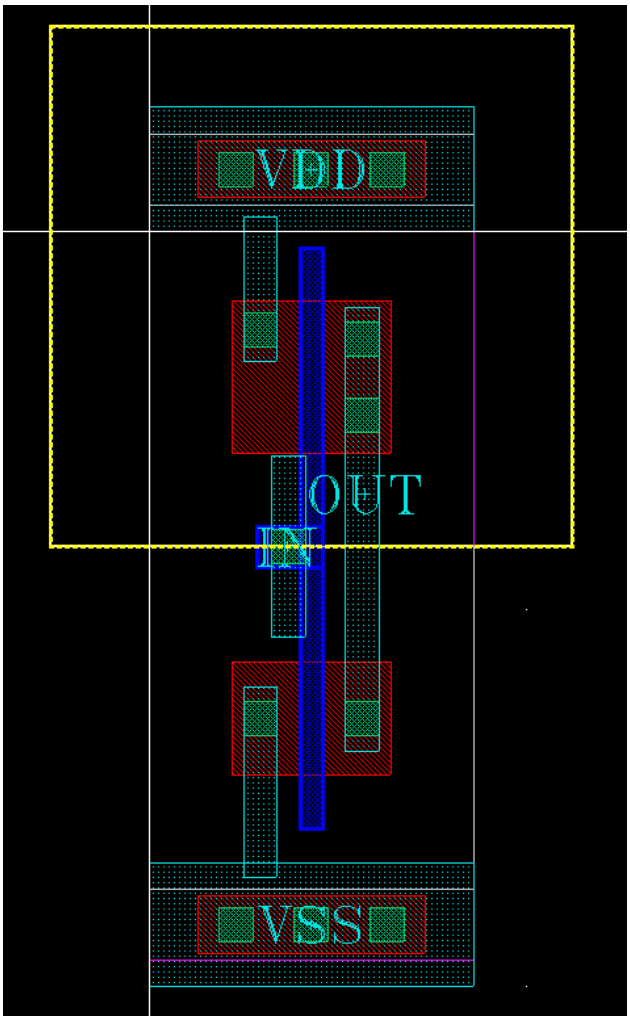

Figure2: Inverter Layout

Summary

Lab 3 emphasizes real world layout vs schematic simulations. In figure7, the layout waveform OUT_EX is slightly more damped, i.e. has a slower response, than the OUT waveform. The layout response takes ~50ps (0.05ns) longer to reach the steady state value than the schematic response. Other noticeable differences are seen in the input currents. The layout waveform VEX_PLUS is more damped and its peak current doesn't obtain the same values compared to the schematic. The layout current is several μA smaller at peak draw than VSCHEM_PLUS.

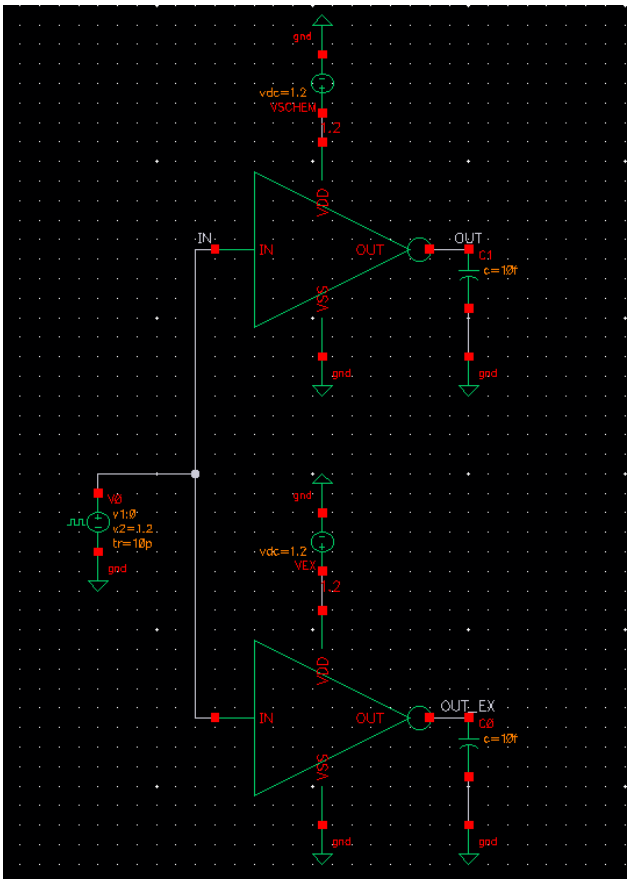

Figure3: Testbench Schematic

Check / Cell	Results
Check OD.DN.1L	1
Check DOD.R.1	1
Check PO.DN.1L	1
Check PO.R.8	2
Check DPO.R.1	1
Check M9.DN.1L	1
Check CSR.R.1.NWi	1
Check CSR.R.1.PPi	2
Check CSR.R.1.NPi	2
Check CSR.R.1.COi	12
Check CSR.R.1.M1i	4
Check CSR.R.1.M1_real	4
Check CSR.R.1.ODi	4
Check CSR.R.1.POi	1
Check DM1.R.1	1
Check DM2.R.1	1
Check DM3.R.1	1
Check DM4.R.1	1
Check DM5.R.1	1
Check DM6.R.1	1
Check DM7.R.1	1
Check DM8.R.1	1
Check DM9.R.1	1
Check ESD.WARN.1	1
Check DENSITY_PRINT_FILES	0

Figure4: DCR Clean Report

Fixed: PO.EX.1 & CO.EN3_CO.EN.4

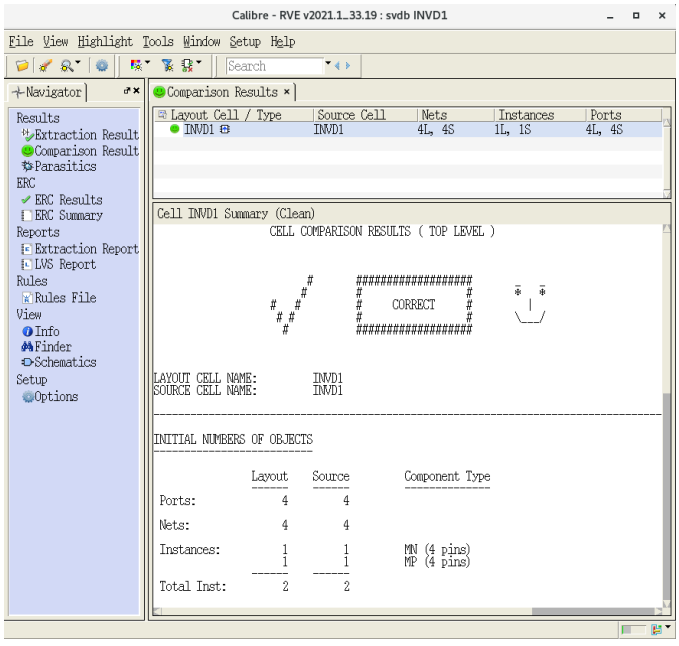

Figure5: LVS Clean Report

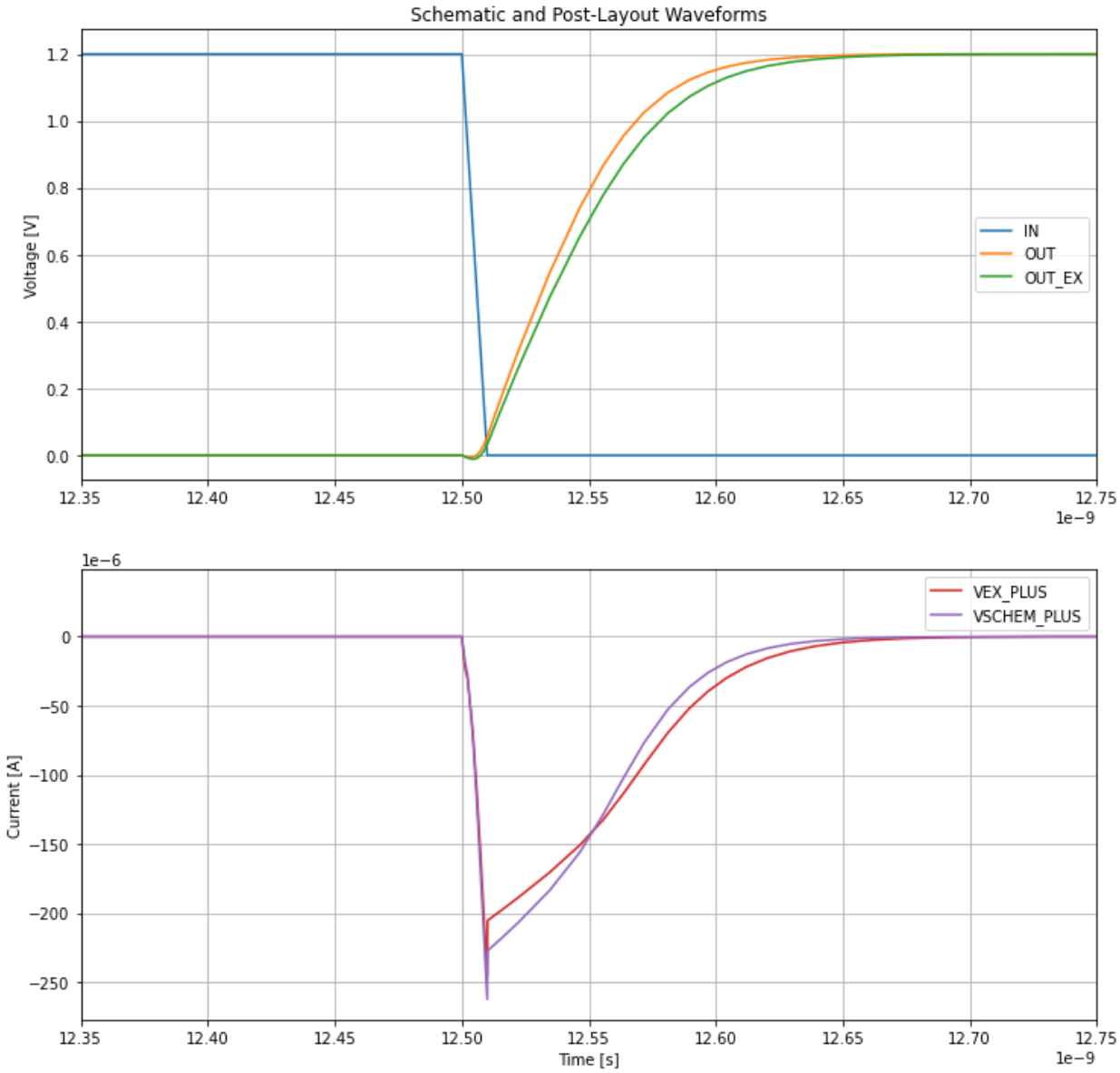

Figure6: Schematic and Layout Waveforms