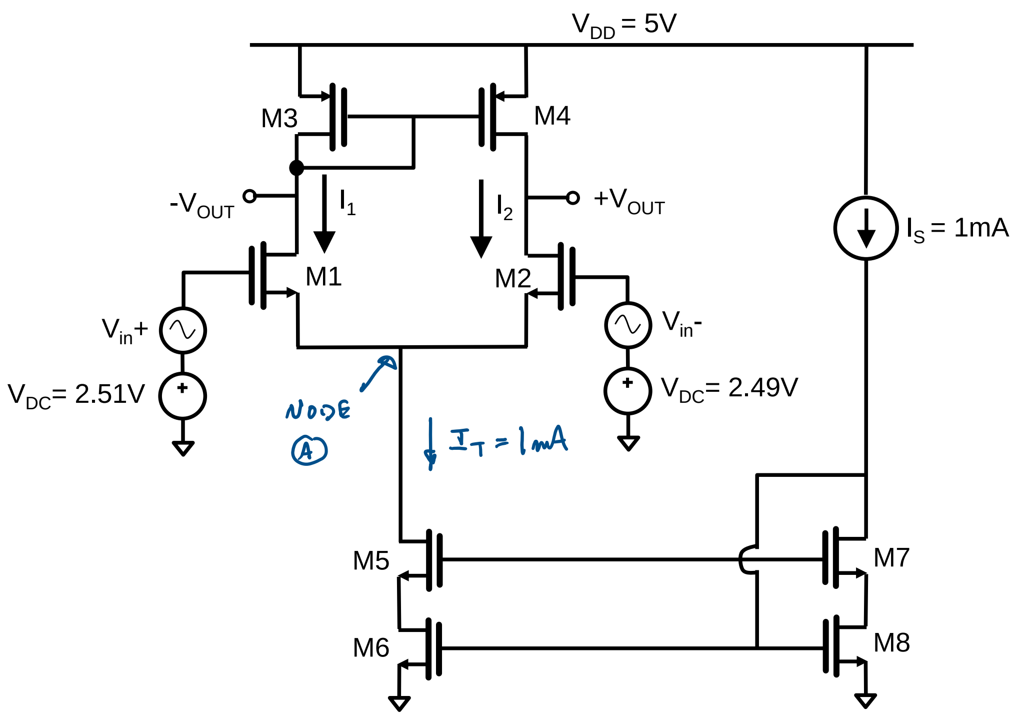
Name: SOLUTIONS

50 points total

EE 473 Quiz 3 Winter 2022

1) a) For the below amplifier, assume all devices are in the saturation region. Find the DC current I_1 and I_2. (10 points) Assume all devices in the saturation region and all device sizes are $\frac{10\mu}{1\mu}$. **Note:** there is a DC offset at the opamp input. Use the following parameters for the entire quiz, $\mu_n C_{ox} = 2mA/V^2$, $\mu_p C_{ox} = 1mA/V^2$, $V_{TH(NMOS)} = 0.7V$ and $V_{TH(PMOS)} = 0.8V$, $\lambda_n = 0.1$, and $\lambda_p = 0.1$. Ignore the body effect ($\gamma = 0$).



KCL @ NODE A

$I_T = I_1 + I_2$ (1)

FIND THE NOMINAL V_{GS} w/ NO INPUT OFFSET.

$I_{D1} = 0.5mA \quad I_{D2} = 0.5mA$.

$I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2$

$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)}} + V_{th} = 0.924V$

w/ THE INPUT OFFSET

$V_{GS1} = 0.924 + 0.01V$

$V_{GS2} = 0.925 - 0.01V$

$$I_{D1} = \frac{2\,mA/V^2}{2}\left(\frac{10}{1}\right)(0.934 - 0.7)^2$$

$V_{GS} + 0.01V$

$$= 0.55\,mA$$

$$I_{D2} = \frac{2\,mA/V^2}{2}\left(\frac{10}{1}\right)(0.914 - 0.7)^2$$

$V_{GS} - 0.1V$

$$= 0.45\,mA$$

$$\boxed{\begin{array}{c} I_{D1} = 0.55\,mA \\ \hline I_{D2} = 0.45\,mA \end{array}}$$

NEEDED FOR PART B)

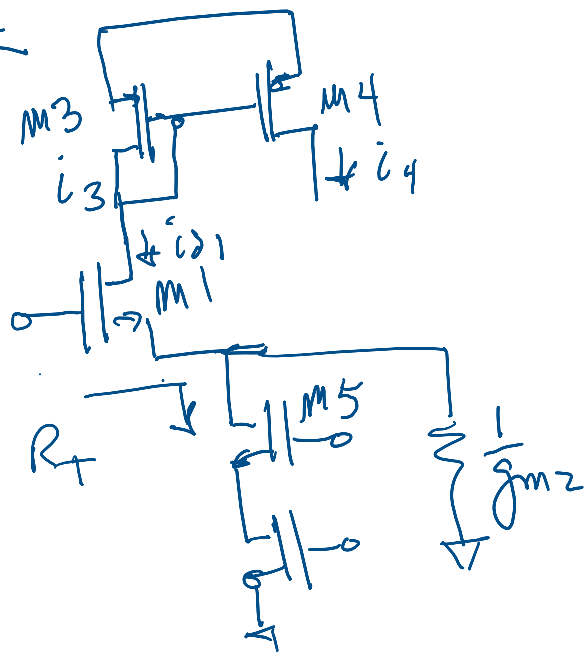
$$g_{m1} = \frac{2 I_{D1}}{(V_{GS_1} - V_{th})} = \frac{2 \cdot 0.55\,mA}{(0.934 - 0.7)} = 4.7\,mA$$

$$g_{m2} = \frac{2 I_2}{(V_{GS_2} - V_{tn})} = \frac{2 \cdot 0.45\,mA}{(0.914 - 0.7)} = 4.2\,\frac{mA}{V}$$

b) Find the AC small-signal gain of the op amp in part a) (25 points)

TWO UNEQUAL PATHS

PATH 1



$i_3 = i_4 = i_{d1}$

ASSUME

$$i_{d1} = \frac{g_{m1}\, v_{in}}{1 + g_{m1}\frac{1}{g_{m2}}}$$

$\frac{1}{g_{m2}} \ll R_T$

$$G_{m1} = \frac{g_{m1}}{1+2}$$

$g_{m1} \approx g_{m2}$

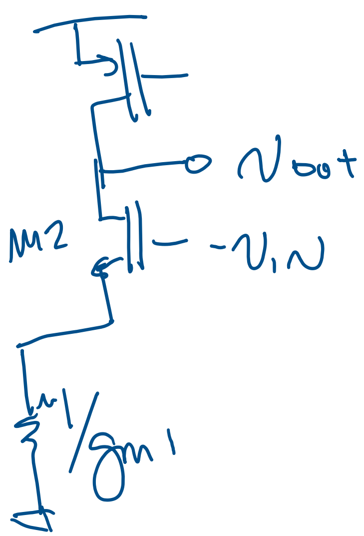
$$A_{v1} = +G_{m1} \cdot (r_{o2} \| r_{o4})$$

$$= \frac{4.7\,\text{mA/V}}{2} \cdot \left(\frac{1}{(\lambda \cdot I_{D2})\cdot 2}\right)$$

$I_{D2} = 0.45\,\text{mA}$

$$\approx 26.1\ \text{V/V}$$

PATH 2



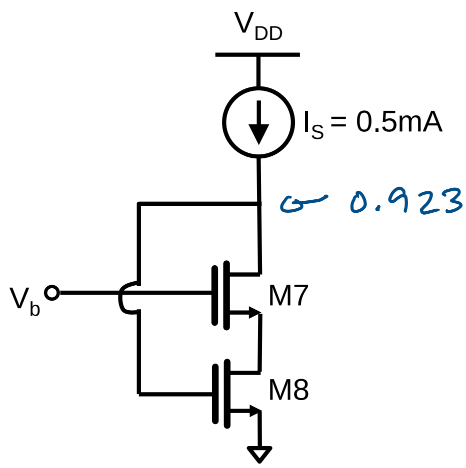
$$A_v = -\left(-\frac{g_{m2}}{2} \cdot r_{o2} \| r_{o4}\right)$$

$$= \frac{4.2\,\text{mA}}{2}\left(\frac{1}{(0.1)(0.45\,\text{mA})\cdot 2}\right)$$

$$= +23\ \text{V/V}$$

$$\boxed{A = A_{v1} + A_{v2} \approx 49.4\ \text{V/V} \approx 50\ \text{V/V}}$$

2) Find the range of acceptable values for the bias voltage, V_b in the below circuit. Assume all device sizes are $\frac{10\mu}{1\mu}$. (15 points)



FIRST FIND V_{GS8}

$$V_{GS8} = \sqrt{\frac{2 \cdot 0.5mA}{2mA/V \cdot \left(\frac{10}{1}\right)}} + V_{tn}$$

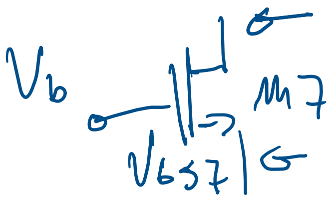
$$= 0.923\ V$$

$$(V_{GS8} - V_{tn}) = V_{GS7} - V_{tn} = 0.223V$$

$$V_{DSAT7} = V_{DSAT8} = 0.223V$$

- V_b IS LIMITED ON THE HIGH END BY PUSHING M7 INTO TRIODE

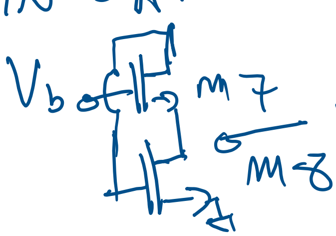
M7 IS ON THE EDGE OF TRIODE WHEN



$$0.923 - V_{DSAT} = 0.7V$$

$$V_{b(HIGH)} = 0.7 + V_{GS7} = 0.7 + 0.923V$$
$$= 1.623V$$

- V_b IS LIMITED ON THE LOW END BY KEEPING M8 IN SATURATION.



$$V_{DSAT8} = 0.223V$$

$$V_{b(LOW)} = V_{DSAT8} + V_{GS7}$$
$$= 0.223 + 0.923V$$
$$= 1.123V$$

$$1.123V \leq V_b \leq 1.623V$$