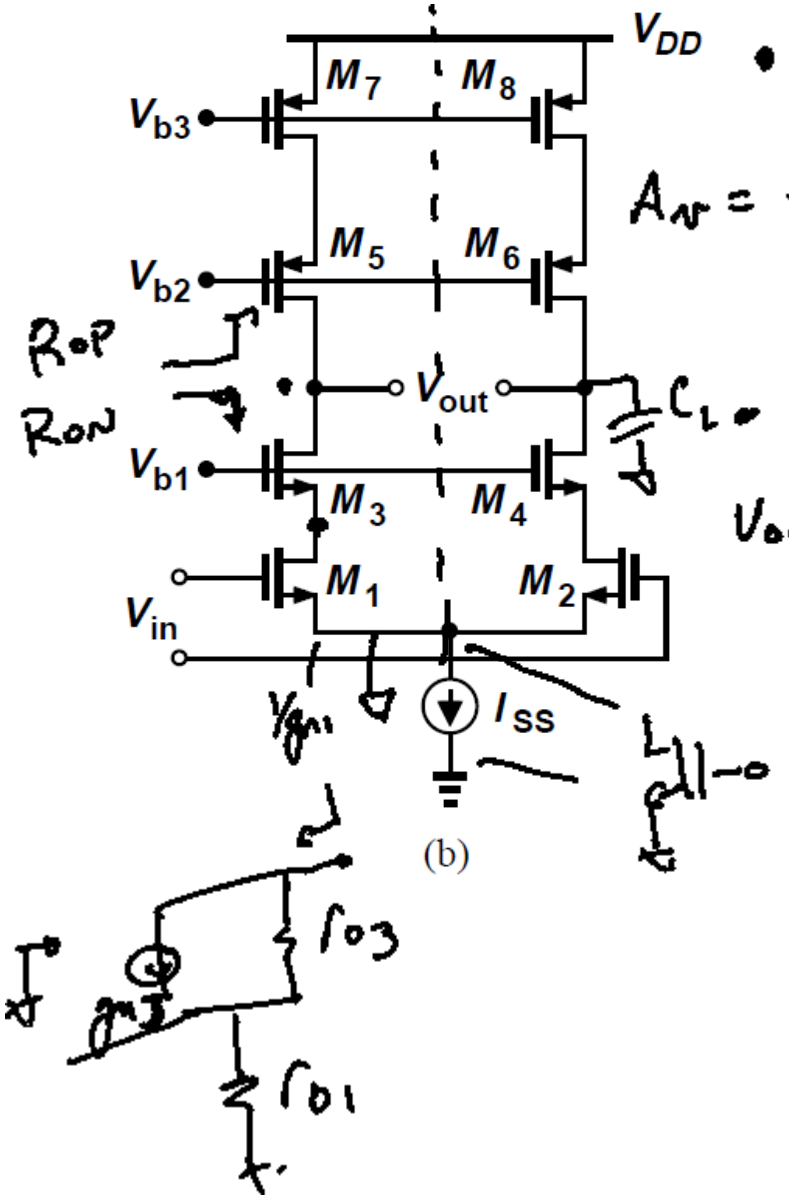
# Lecture #16, Feb 14th, 2022

- We will bounce between chapters 8 (Feedback) and 9 (Op Amp design).
- CAD 4 now out, due Thursday.
- Quiz #2 postponed until Wednesday.
  - Results:
    - High = 3 x 50  Nice work!
    - Mean = 39
    - Standard Deviation = 11
- Project 1 due tomorrow!
- Project 2 coming very soon.
- Today:
  - Opamp Topologies
    - Common-Source
    - Telescopic
    - Folded-Cascode
    - Two-Stage Op Amp
  - Regulated Cascodes (Active Cascode)

# Telescopic Cascode Op Amps




- VOLTAGE GAIN

$$A_V = -g_{m1}\cdot(g_{m3}\cdot r_{03}\cdot r_{01} \,//\, g_{m5}\cdot r_{05}\cdot r_{07})$$

INTRINSIC (10-100)

- OUTPUT SWING

$V_{out,max} = V_{DD} - 5V_{DSAT}$ ; POOR OUTPUT SWING

$(V_{DS} - V_{DSAT})$

- BW

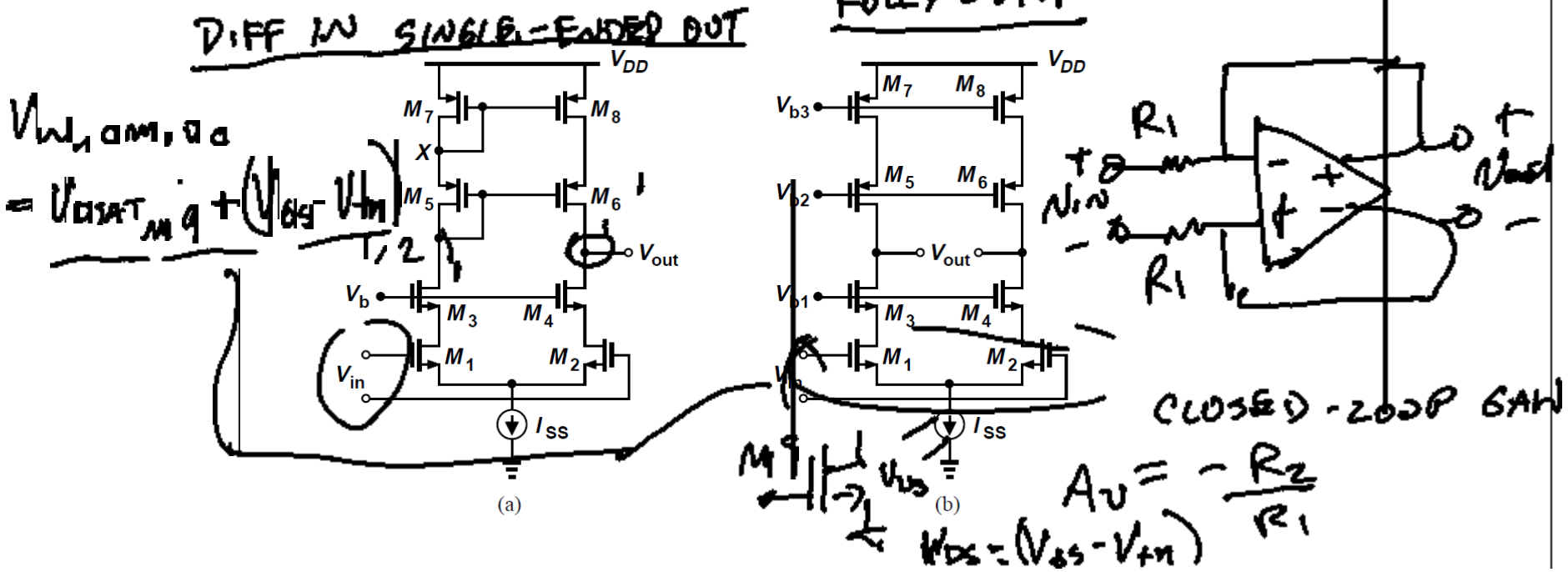
$$P = \frac{1}{2\pi (R_{ON} // R_{OP})\cdot C_L}$$

DOMINATE POLE

STABLE

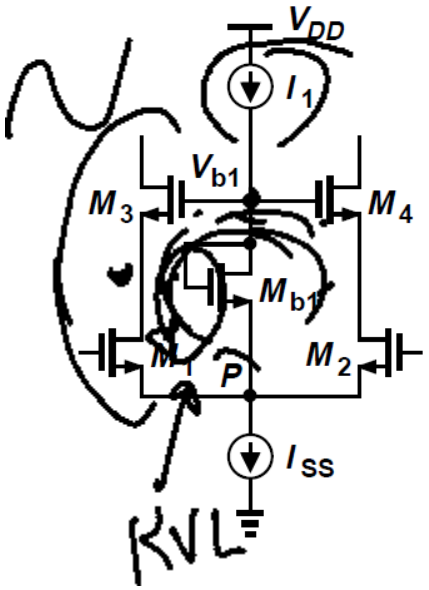
# Telescopic Cascode Op Amps

- **Low-frequency gain:** $g_{mN}[(g_{mN}r_{ON}^2)\|(g_{mP}r_{OP}^2)]$
- **Speed: Additional poles**
- **Output Swing (single-side): VDD-5Overdrive**
- **Mirror pole in single-ended**
- **Difficult to short telescopic op amp output to input**
- **Power and noise: good, input noise mainly has four devices contribution**



# Gate Bias Voltage Generation

- Ensure bias voltage to track the input CM level
- Choose Mb1 to be a narrow, long, "weak" device




KVL

$V_{GSb1} - V_{GS3} - V_{DSM1} = 0$

WANT $V_{DSM1} = (V_{GS} - V_{tn})_{M1}$

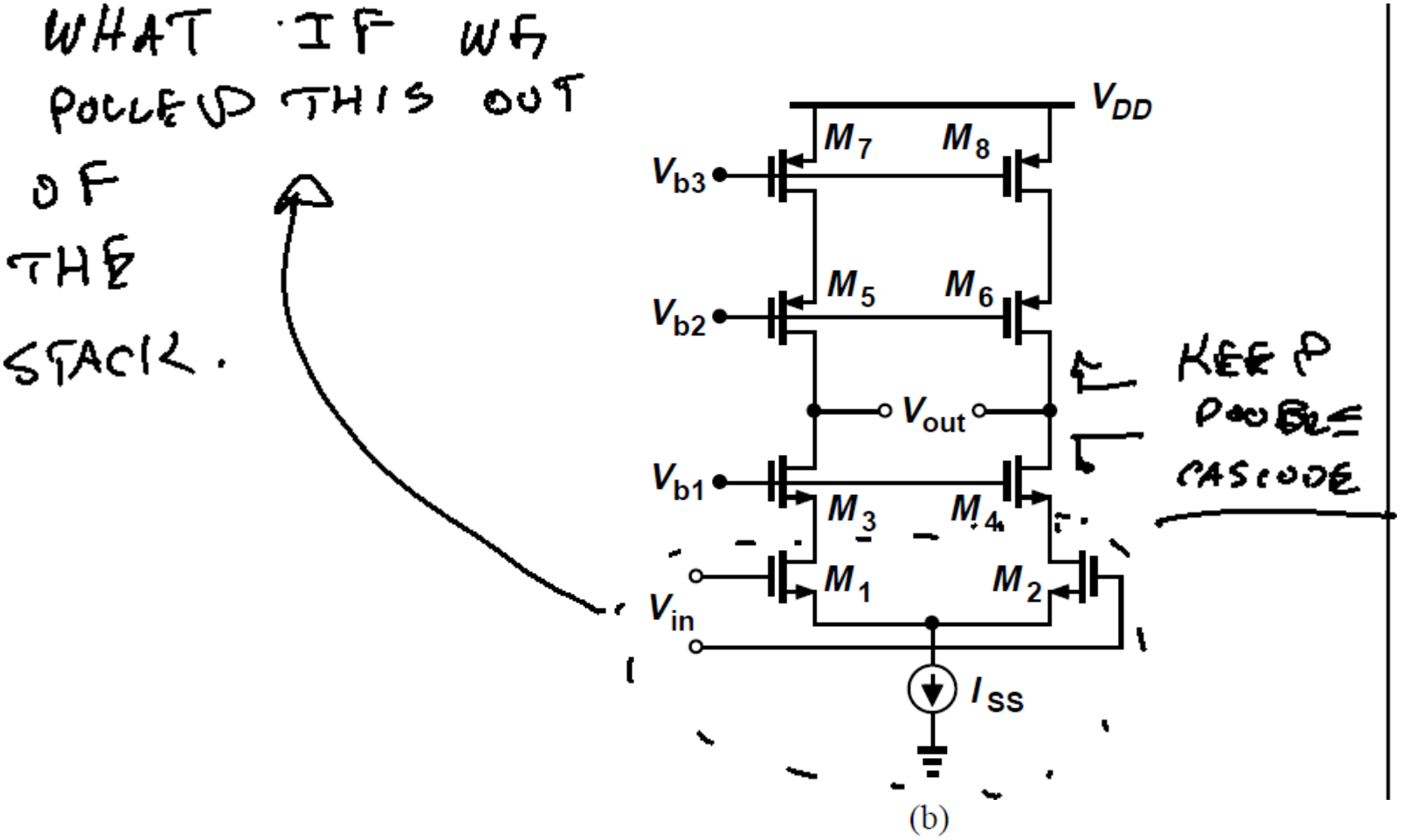
$V_{GSb1} = V_{GS3} + V_{DSM1}$

$= (V_{GS} - V_{tn})_1 + V_{GS3}$

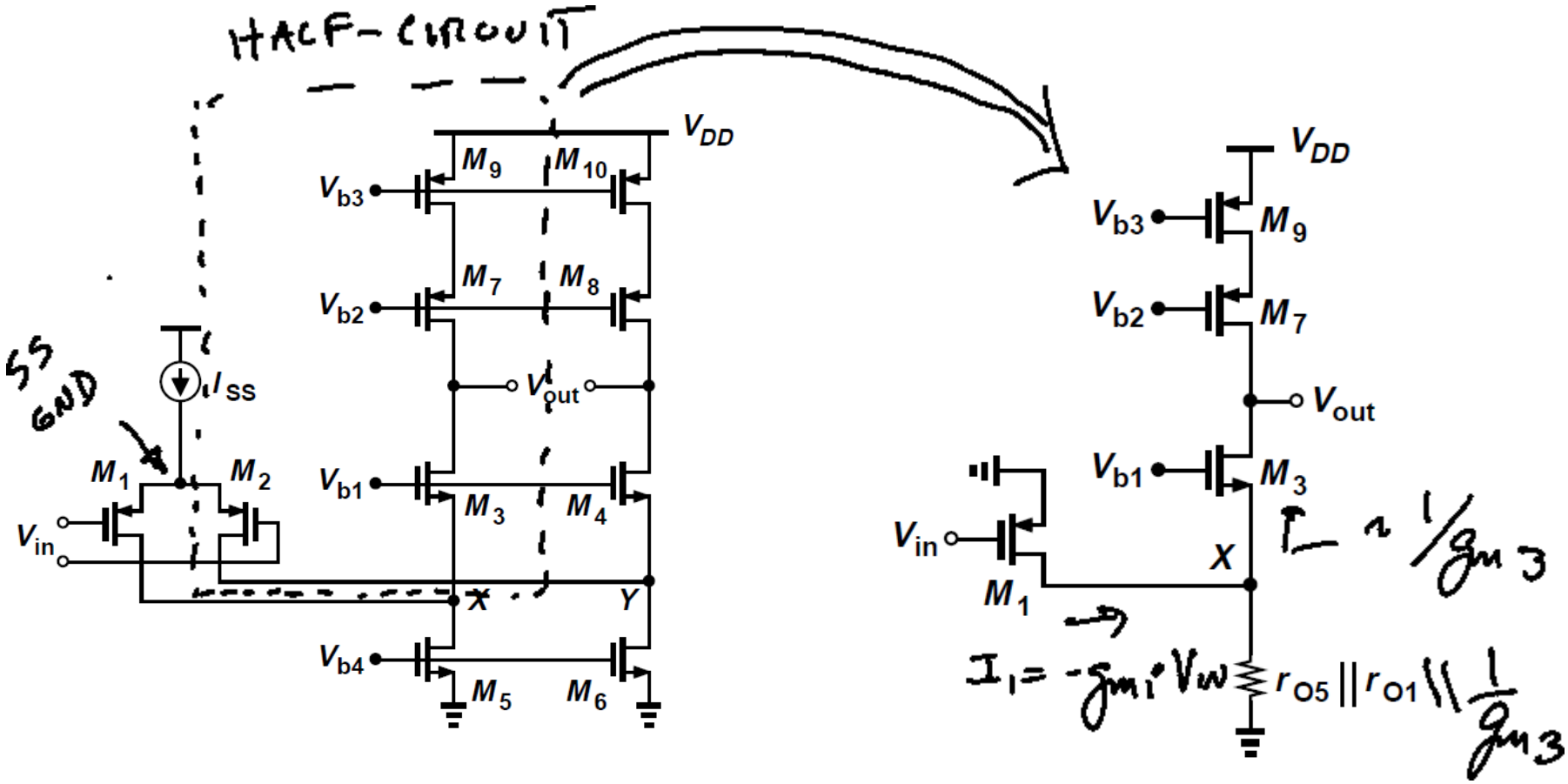
$V_{b1} = V_P + V_{GS,b1}$

$$V_{GS,b1} = (V_{GS1,2} - V_{TH1,2}) + V_{GS3,4}$$

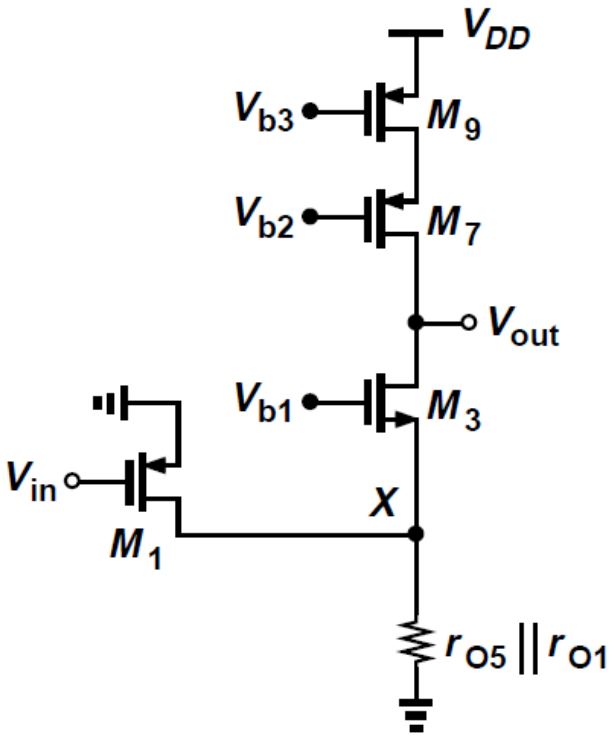
# Removing the Diff Pair From the Stack



# Folded Cascode



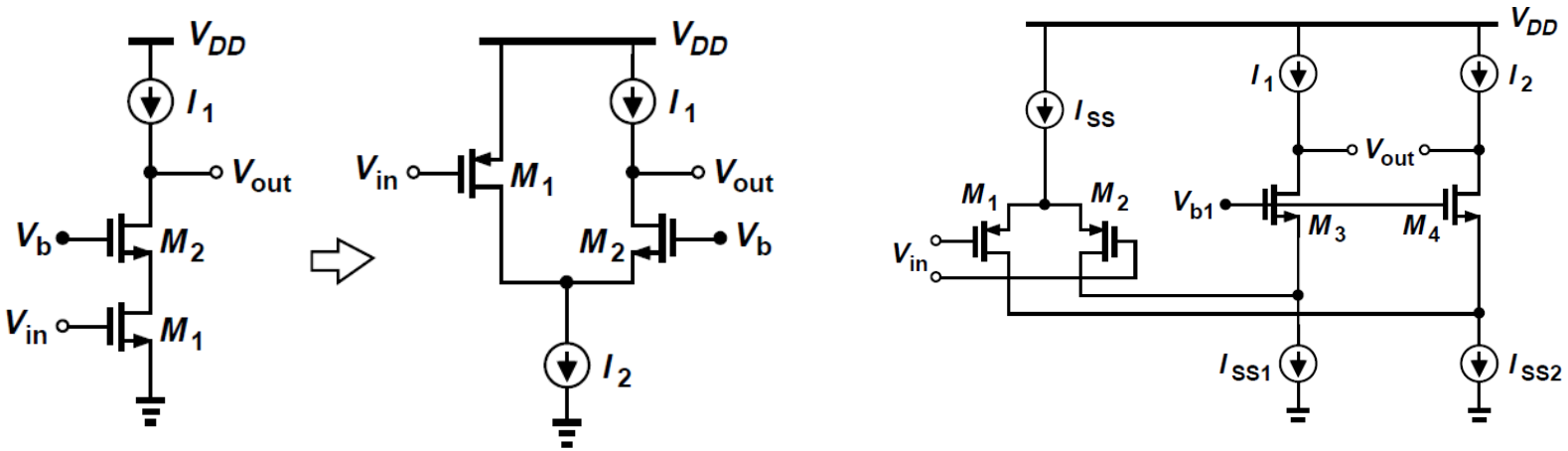
# Folded Cascode Voltage Gain



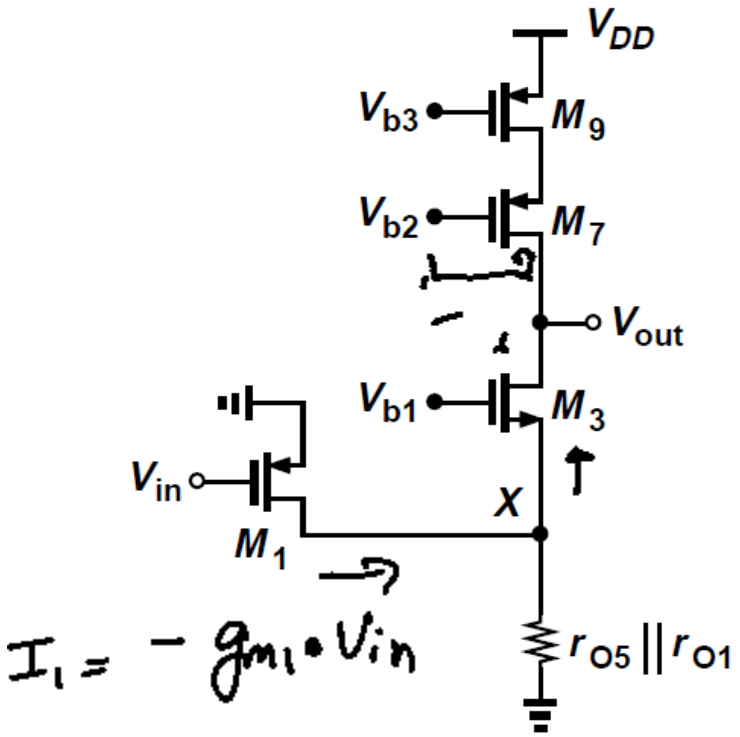
# Folded Cascode Op Amps

**Recall Folded Cascode**

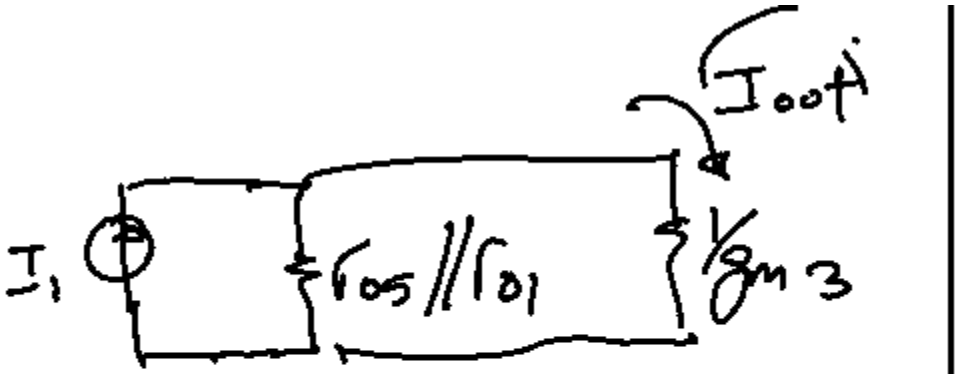
- **Not "stack" the cascode transistor on the input device**
- **Consume higher power**
- **Output Voltage Swing: VDD-4overdrive**
- **Output and input could short together**



# SS Current from Diff Pair Shunted Up In Cascode




$I_1 = -g_{m1} \cdot V_{in}$

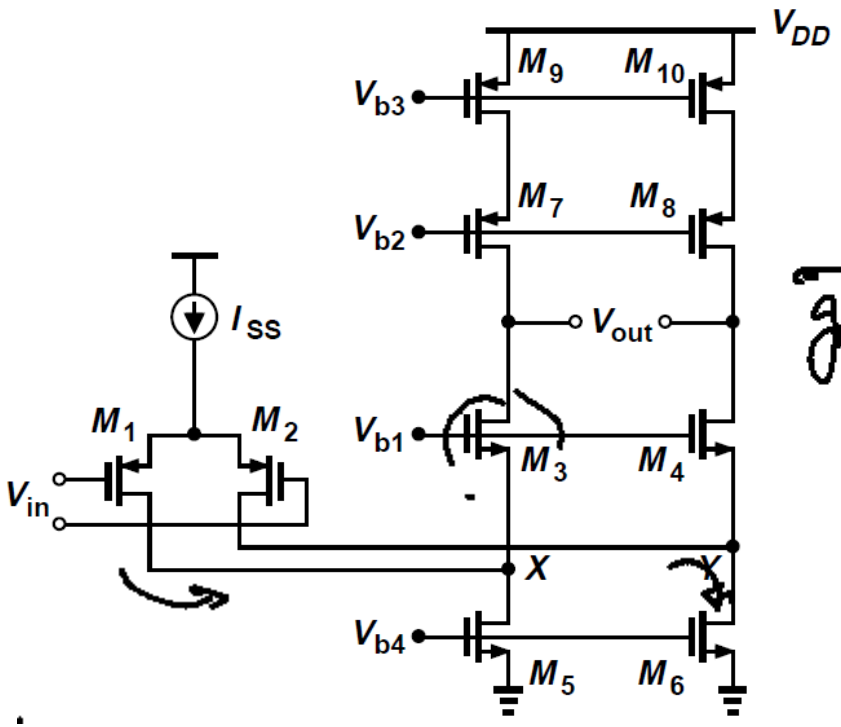


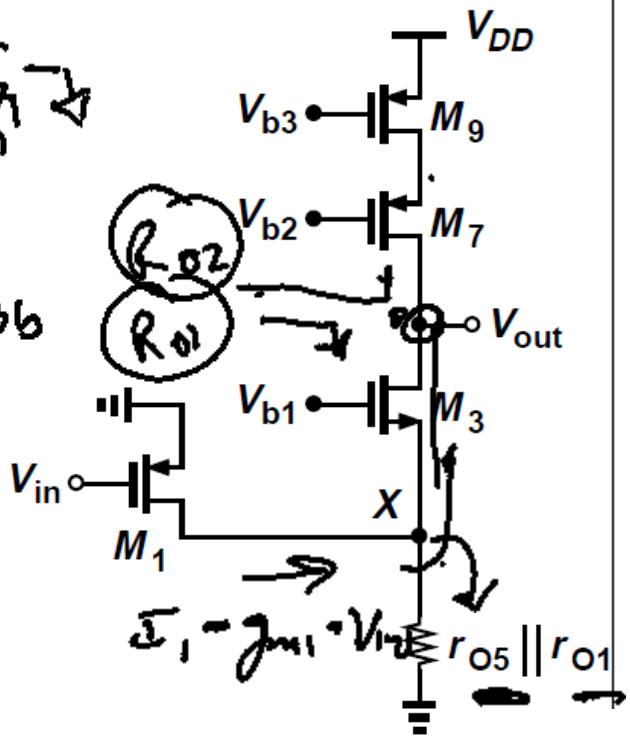

$$I_{out} = \frac{r_{O5} \| r_{O1}}{1/g_{m3} + r_{O5} \| r_{O1}} \cdot I$$

# Folded Cascode Voltage Gain

$$|A_v| = G_m R_{out}$$

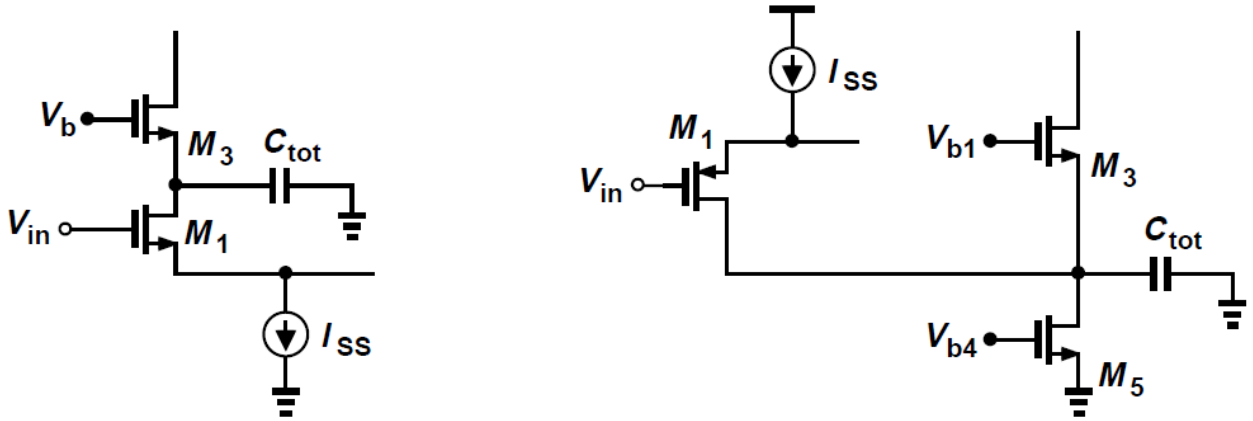
- **Since** $(g_{m3} + g_{mb3})^{-1} \| r_{O3} \ll r_{O1} \| r_{O5}$, **thus** $G_m \approx g_m$
- $|A_v| \approx g_{m1}\{[(g_{m3} + g_{mb3}) r_{O3} (r_{O1} \| r_{O5})] \| [(g_{m7} + g_{mb7}) r_{O7} r_{O9}]\}$
- **Two or three times lower than a telescopic topology**



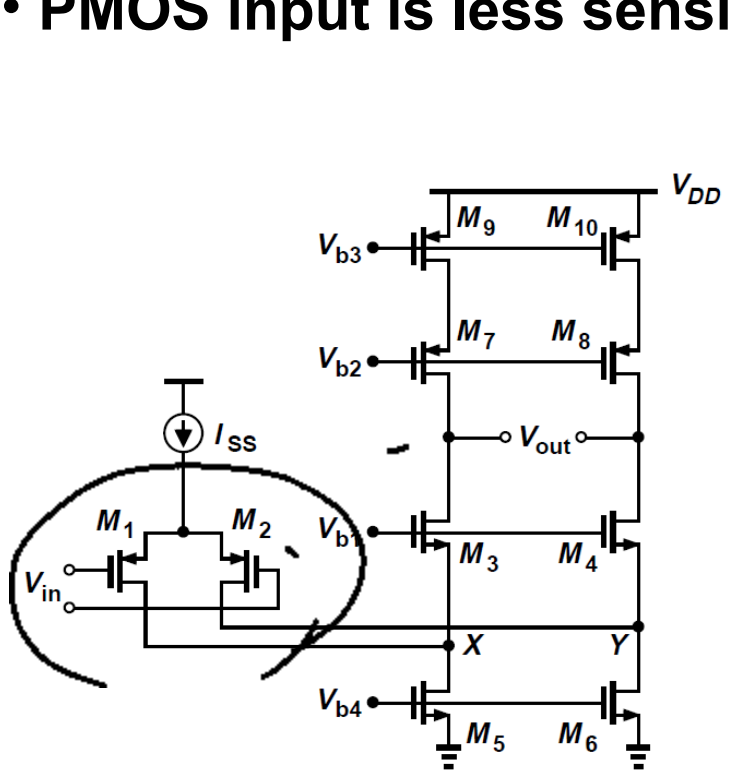
# Effect capacitance on the nondominant pole

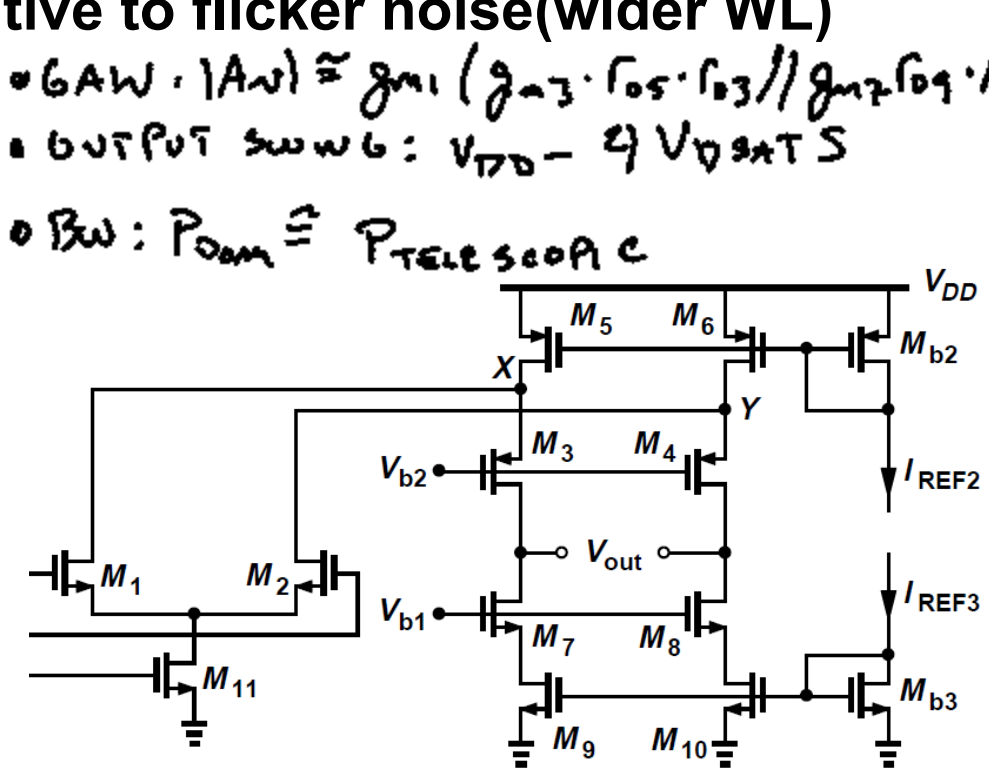
- **At "folding point", a large capacitance due to a large current device M5 would be added to the total capacitance.**



# NMOS vs. PMOS input

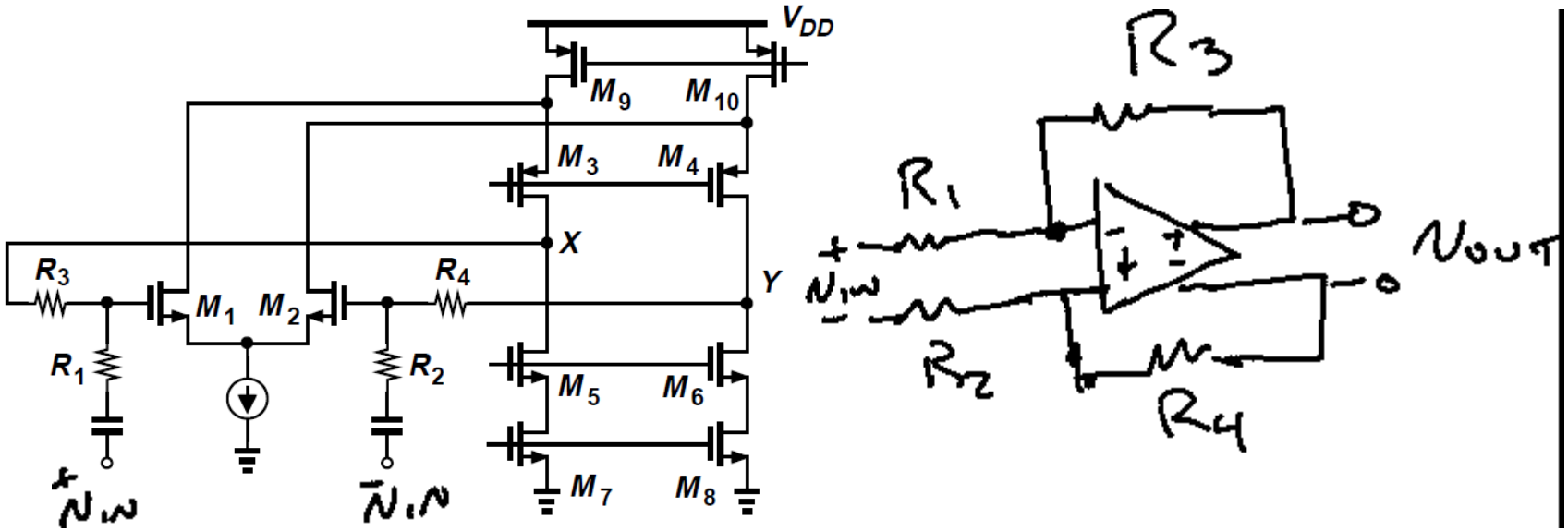
- **Greater mobility from NMOS input leads to higher gain**
- **Lowering the pole at folding point**
- **PMOS input is less sensitive to flicker noise(wider WL)**



# Folded Cascode Properties

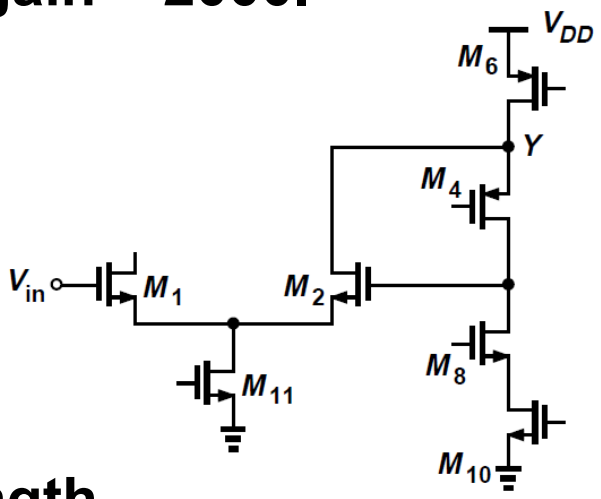
- **Slighter Higher Output Swing than telescopic**
- **Higher Power dissipation, lower voltage gain, lower pole frequency and higher noise**
- **Input and output can be shorted: 2overdrive from bound**
- **A better input CM range**



# Example 9.9

**Design a folded- cascode op amp with an NMOS pair.**

**Specifications: VDD = 3V, differential output swing = 3V, Power dissipation = 10mW, voltage gain = 2000.**




**Solution:**

**(1)Current allocation**

**(2)Overdrive voltage allocation**

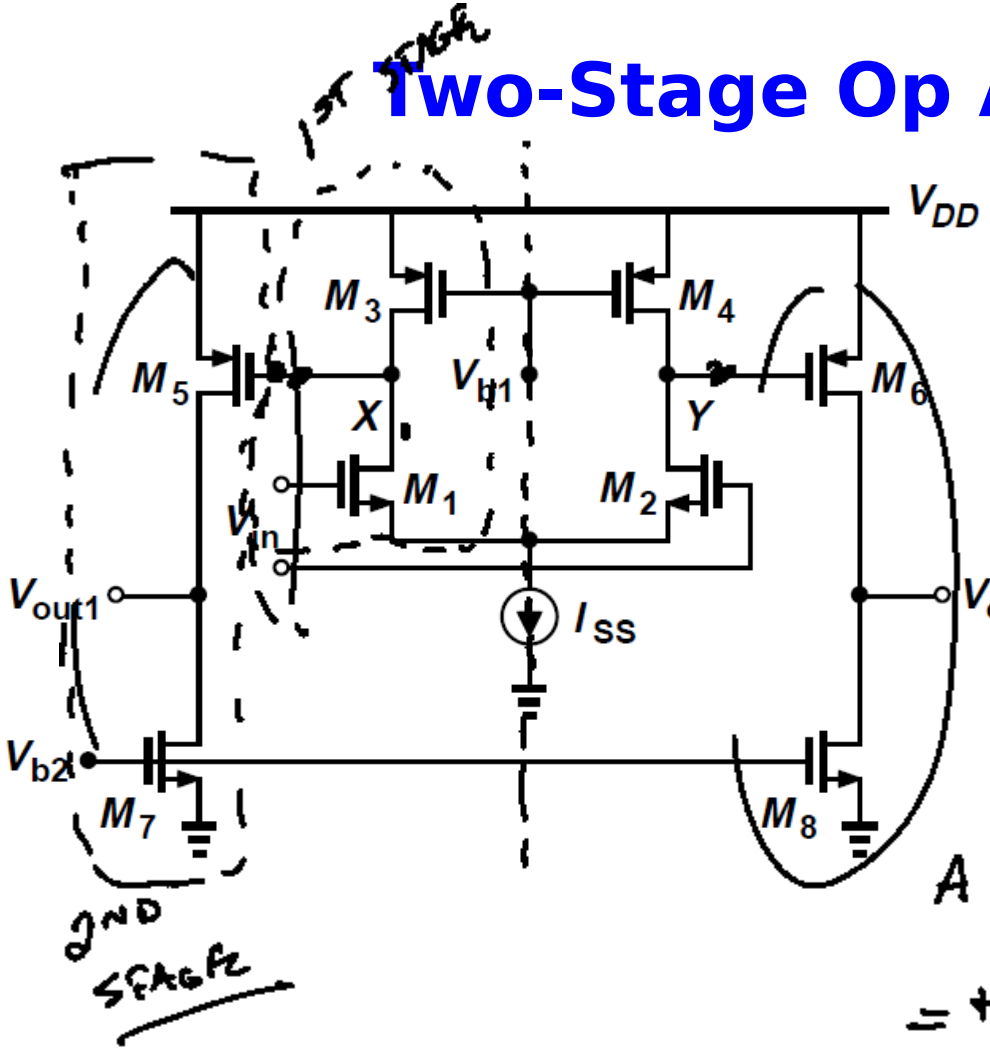
**(3)Aspect ratio calculation**

**(4)Small-signal gain with minimal length**

**(5)Iteration by increase M5/M1/M4 in turns**

**Note that the folding point capacitance may limit here.**

# Two-Stage Op Amps – Gain




1ST STAGE

$$A_{1ST} \cong -g_{m1} \cdot (r_{o1} \| r_{o3})$$

2ND STAGE

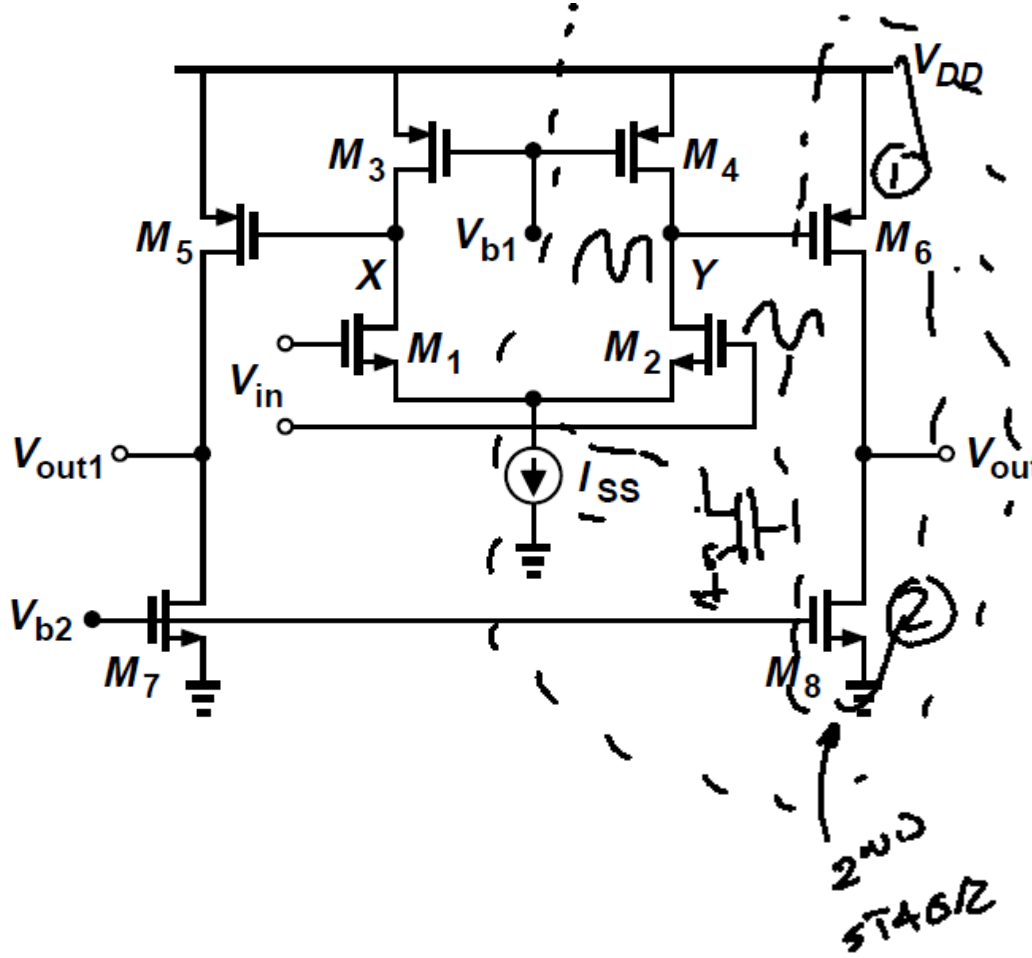
$$A_{2ND} \cong -g_{m5} \cdot (r_{o7} \| r_{o5})$$

$$A = A_{1ST} \cdot A_{2ND}$$

$$= +g_{m1} \cdot g_{m5} (r_{o3} \| r_{o1}) (r_{o5} \| r_{o7})$$

$$A \propto (g_m \cdot r_o)^2$$

# Output Swing Two-Stage Op Amps




OUTPUT SWING 1ST STAGE

MONEY

$V_{OUT,MAX} = V_{DD} - 3V_{DSAT}$

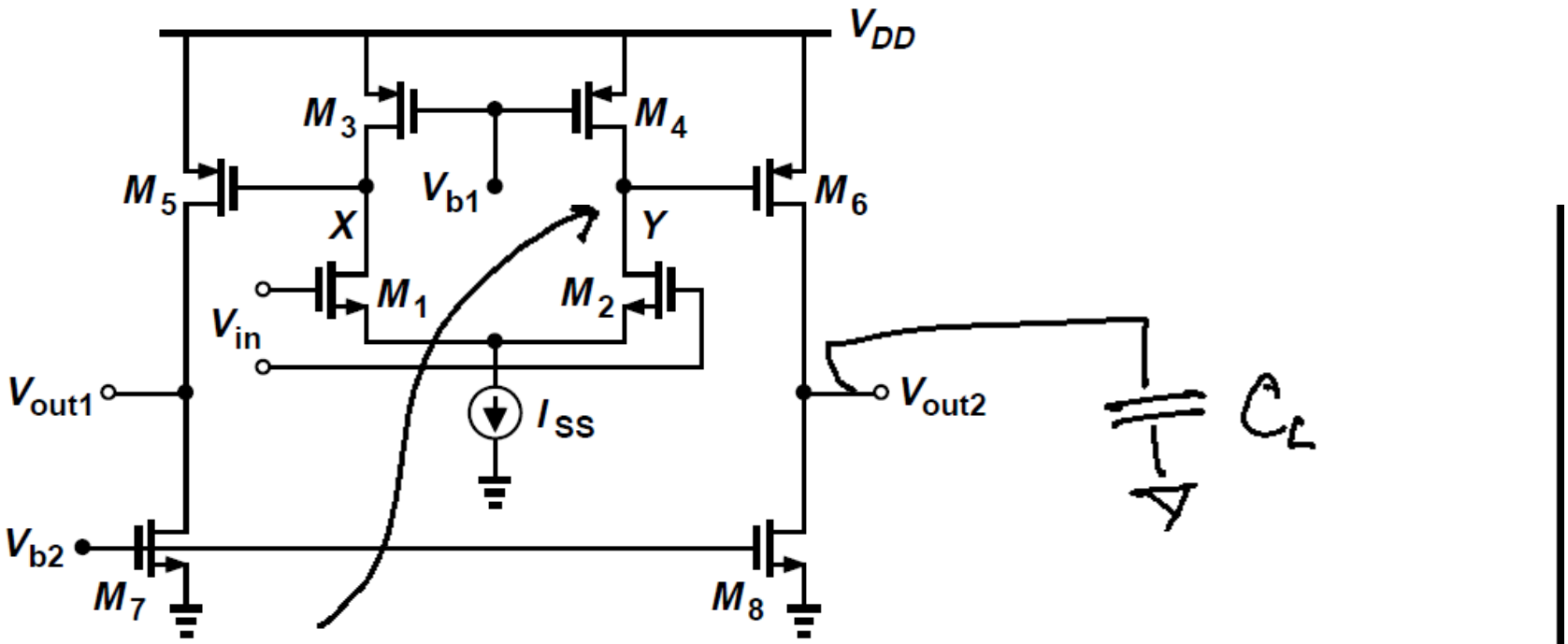
OUTPUT SWING 2ND STAGE

$V_{OUT,MAX} = V_{DD} - 2V_{DSAT}$

WHAT IS THE OVERALL HEADROOM?

ANS: 2ND STAGE → 2ND STAGE SETS HEADROOM BECAUSE OF GAIN IN 2ND STAGE

# Bandwidth: Two-Stage Op Amps

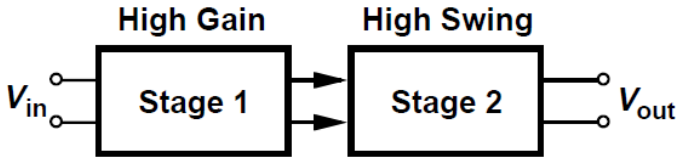


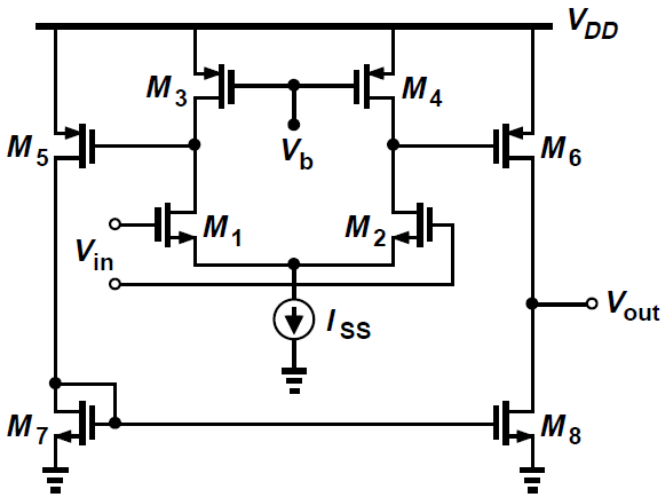

$$P_1 \approx \frac{1}{2\pi (r_{O4} \,//\, r_{O2})(C_{DB4} + C_{DB2} + C_{GL})}$$

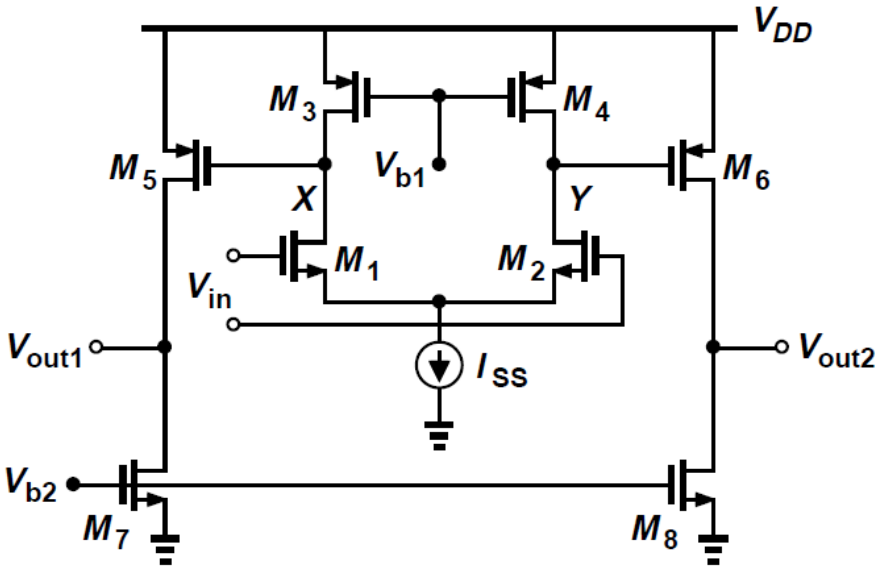
$$P_2 \approx \frac{1}{2\pi (r_{O6} \,//\, r_{O8}) \cdot (C_{DB} + C_{O6} + C_L)}$$

# Two-Stage Op Amps

- **Voltage headroom in today's design is constrained with low supply voltage and large output swing**
- **Gain:** $g_{m1,2}(r_{O1,2} \| r_{O3,4})\ g_{m5,6}(r_{O5,6} \| r_{O7,8})$
- **Output Swing: Vdd-2Overdrive**

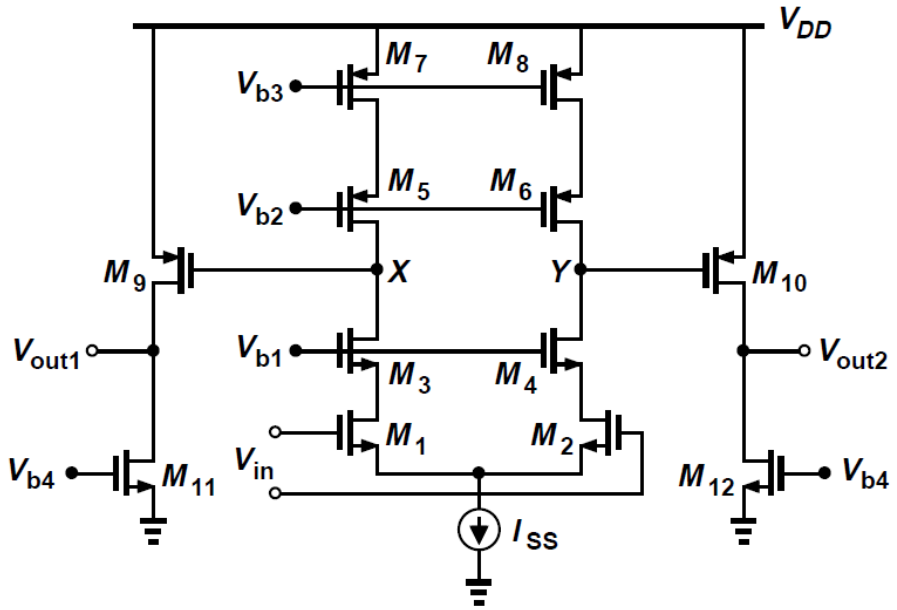


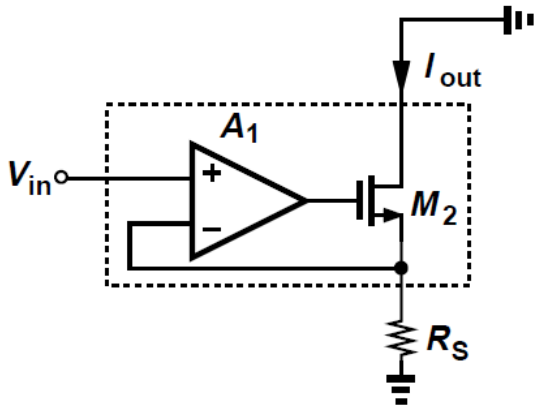



# Two-Stage Op Amps with cascode devices

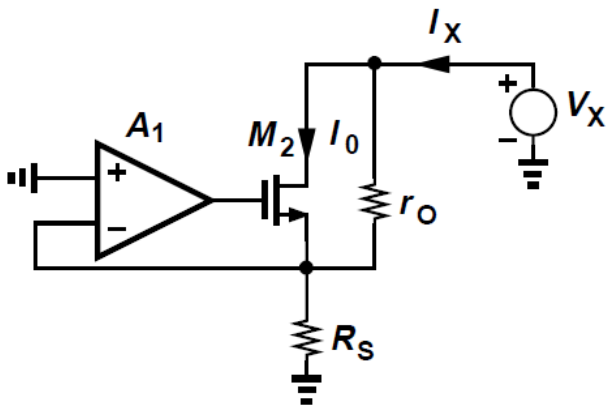
- Voltage headroom in today's design is constrained with low supply voltage and large output swing
- Gain: $A_v \approx \{g_{m1,2}[(g_{m3,4}+g_{mb3,4})r_{O3,4}r_{O1,2}]||[(g_{m5,6}+g_{mb5,6})r_{O5,6}r_{O7,8}]\} \times [g_{m9,10}(r_{O9,10}||r_{O11,12})]$.
- Can we have more stages? Feedback stability limits



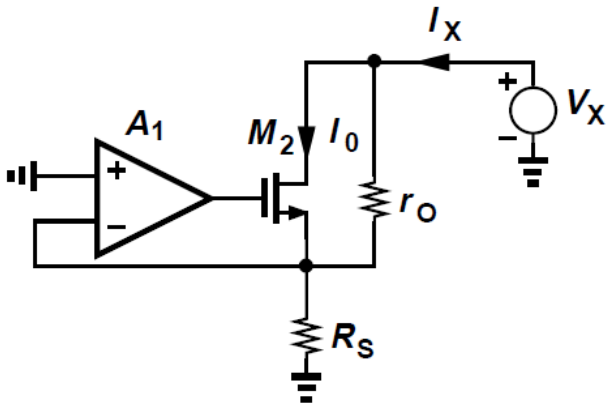
# Gain Boosting Techniques: Effective



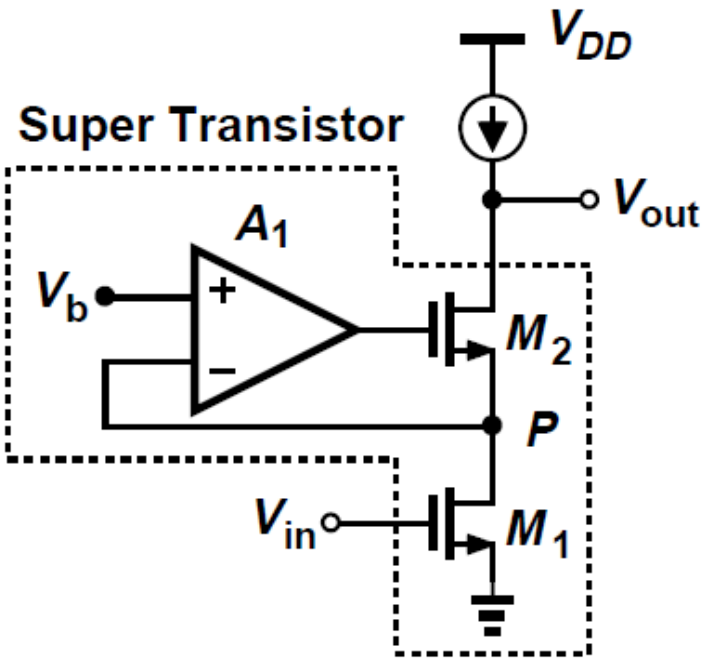
# Output Resistance of Gain Boosting Stage



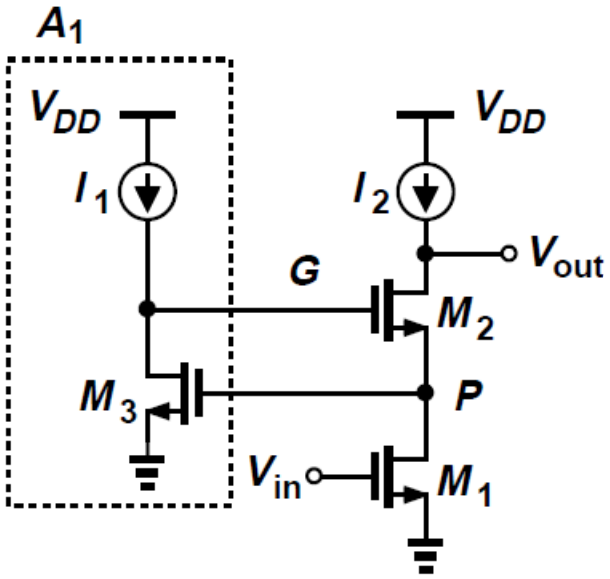
# Output Resistance of Gain-Boosted Stage



# Gain-boosting with Active/Regulated Cascode



# Example Implementations

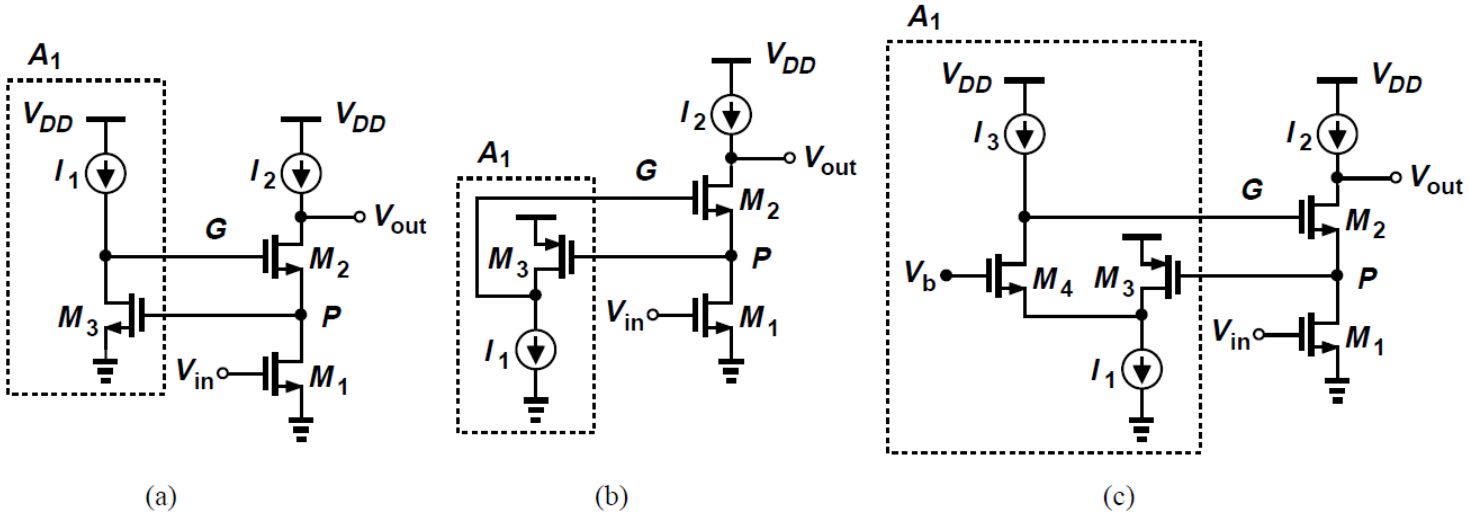


# Gain Boosting Circuit Implementation

- Simplest a common-source stage

$$|V_{out}/V_{in}| \approx g_{m1}r_{O1}g_{m2}r_{O2}(g_{m3}r_{O3}+1)$$

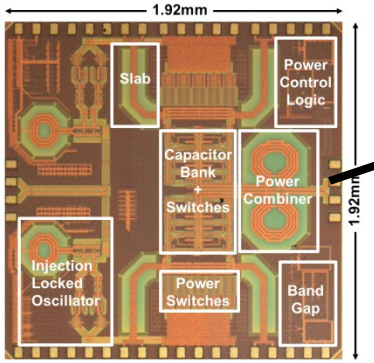
- Avoid headroom limitation, PMOS common-source stage is better, but M3 could go in triode
- Folded-cascode inserts one more stage

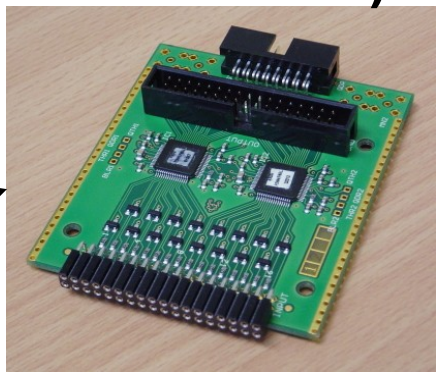


Scintillator

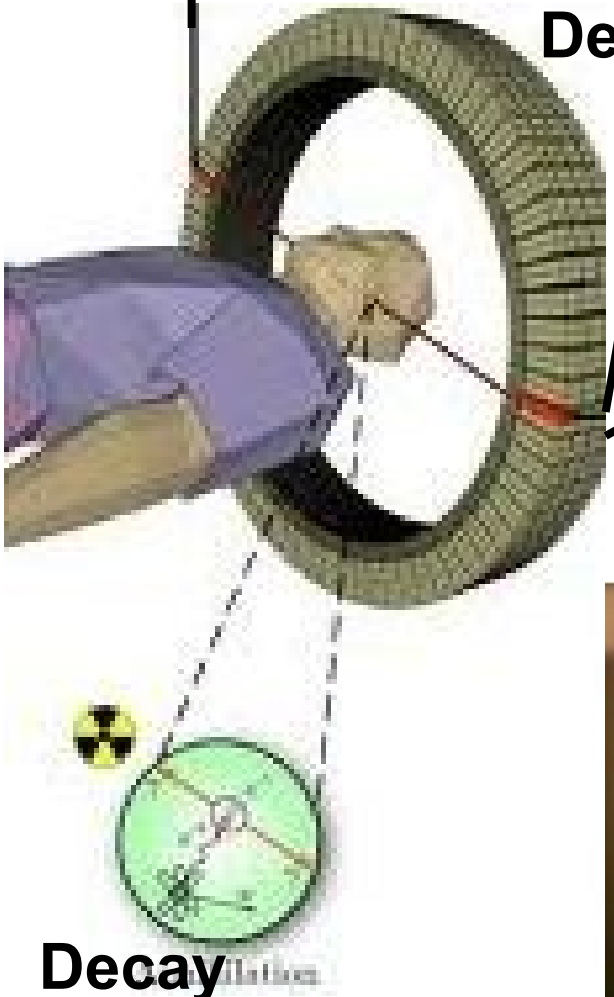
Detector

ADC / FPGA(Phase Electronics)



PET Readout Electronics



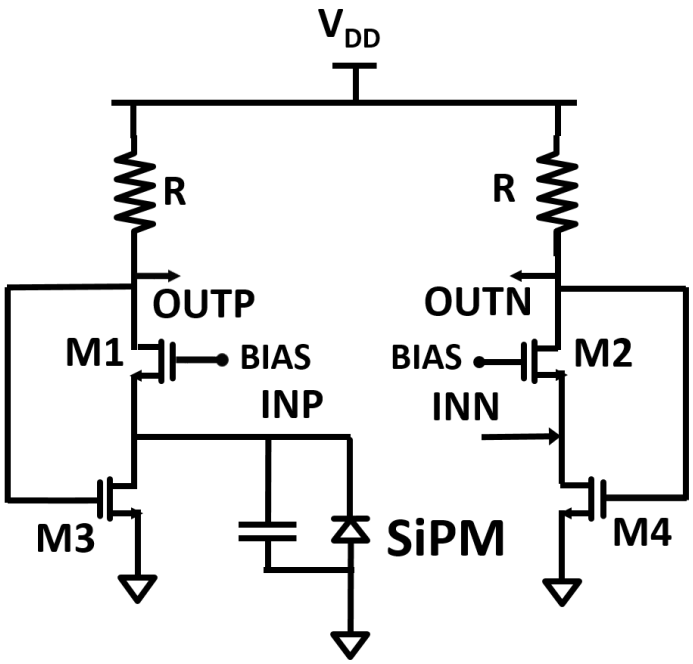
Decay Event

Image

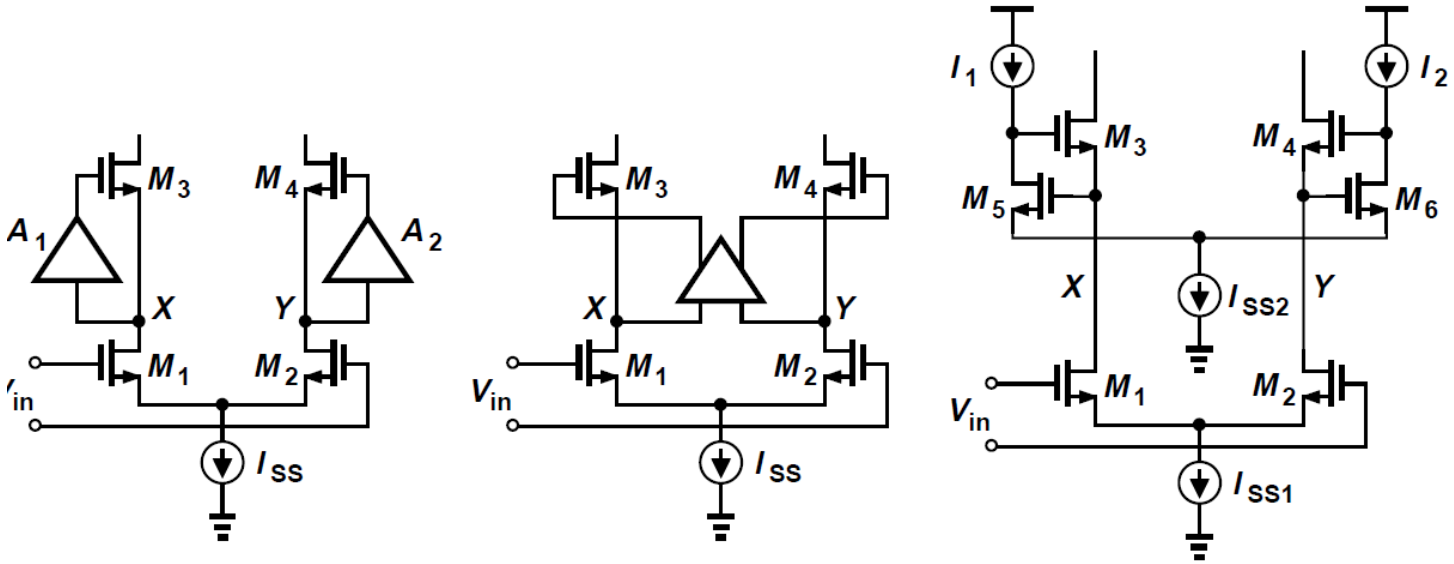
# Example from UW – PET Imaging Front-end

A Front-End Interface ASIC for SiPM based PET Imaging

Samrat Dey, *Student Member,* Thomas K. Lewellen, *Fellow*, Robert S. Miyaoka, *Senior Member*, and Jacques C. Rudell, *Senior Member, IEEE*

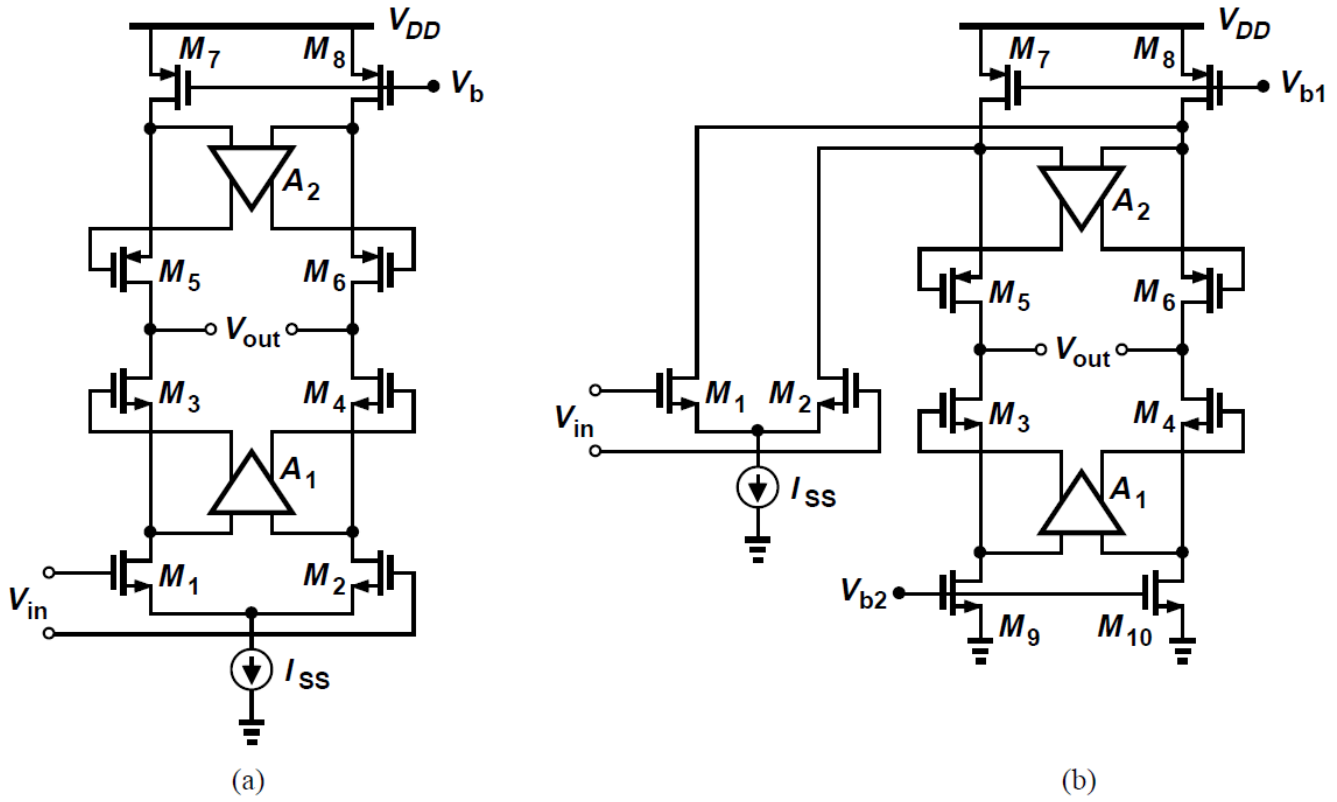


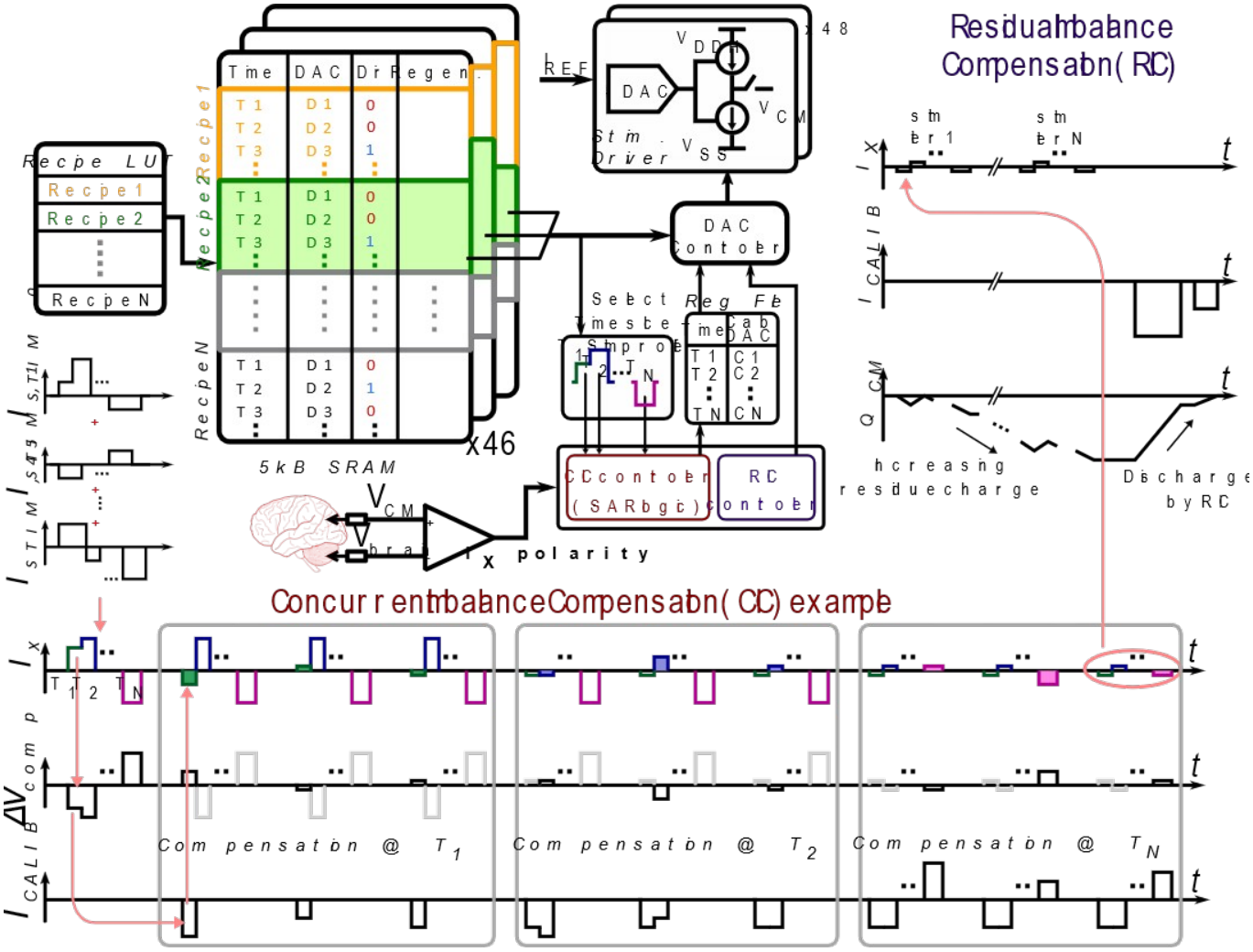
# Gain Boosting with a Differential Pair



# Gain Boosting in Signal Path and Load

- Gain boosting can be utilized in the load current source
- To allow maximum swings, A2 employs NMOS-input.




Recipe LUT
Recipe1
Recipe2
RecipeN
Time
DAC
Dir
Regen
5kB SRAM
x46
x48
DAC
Stim. Driver
DAC Controller
Select Register File
Timestep Sample DAC
CC controller (SAR logic)
RC controller
Vx polarity
Residual Imbalance Compensation (RC)
stim per 1
stim per N
Increasing residue charge
Discharge by RC
Concurrent Imbalance Compensation (CC) example
Compensation @ T1
Compensation @ T2
Compensation @ TN