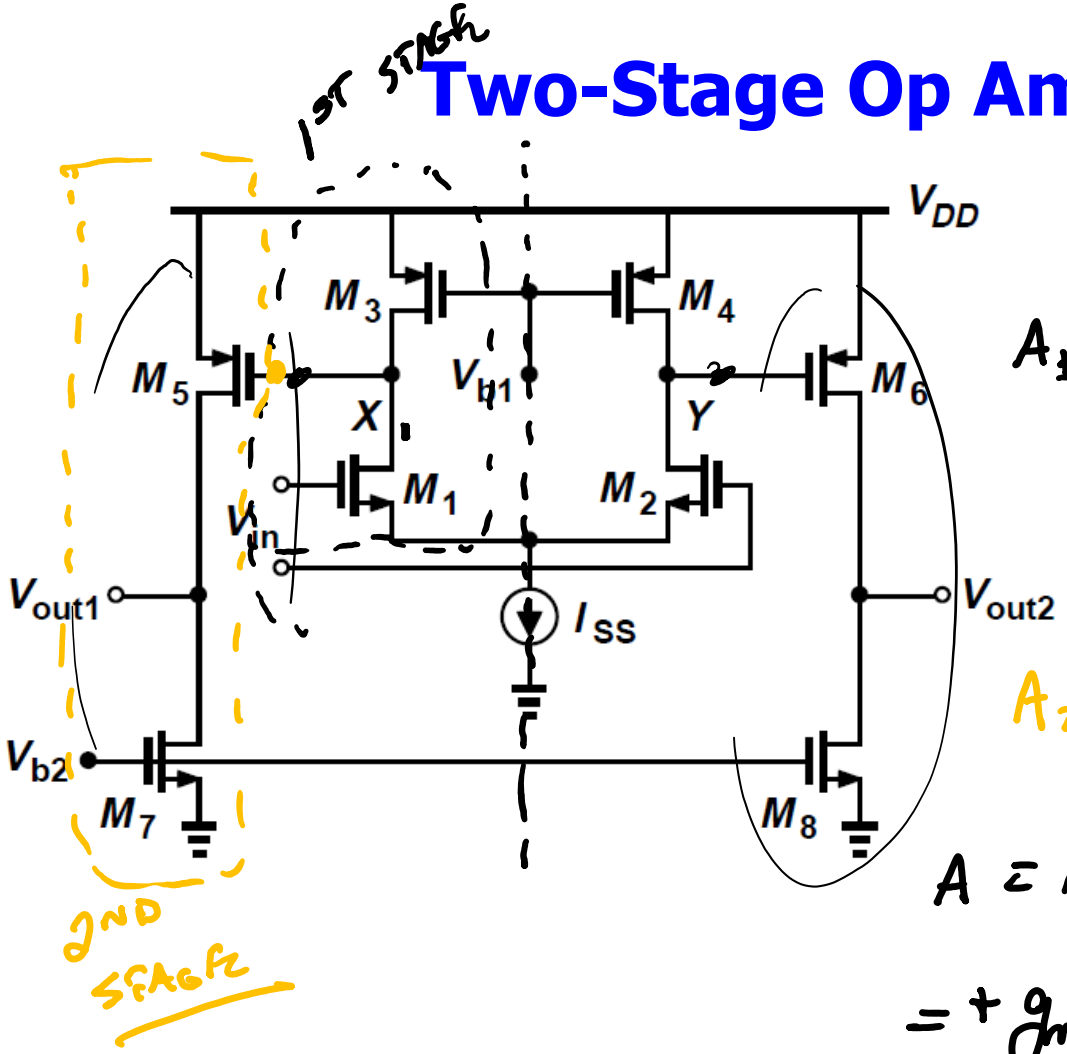
# Lecture #17, Feb 16th, 2022

- We will bounce between chapters 8 (Feedback) and 9 (Op Amp design).
- CAD 4 now out, due Thursday.
- Quiz #2 Today.
- New Homework and Project 2 coming very soon/today.
- Today:
  - Continue with Op Amps
  - Regulated Cascodes

# Two-Stage Op Amps – Gain




1ST STAGE

$$A_{1ST} \cong -g_{m1} \cdot (r_{o1} \| r_{o3})$$

2ND STAGE

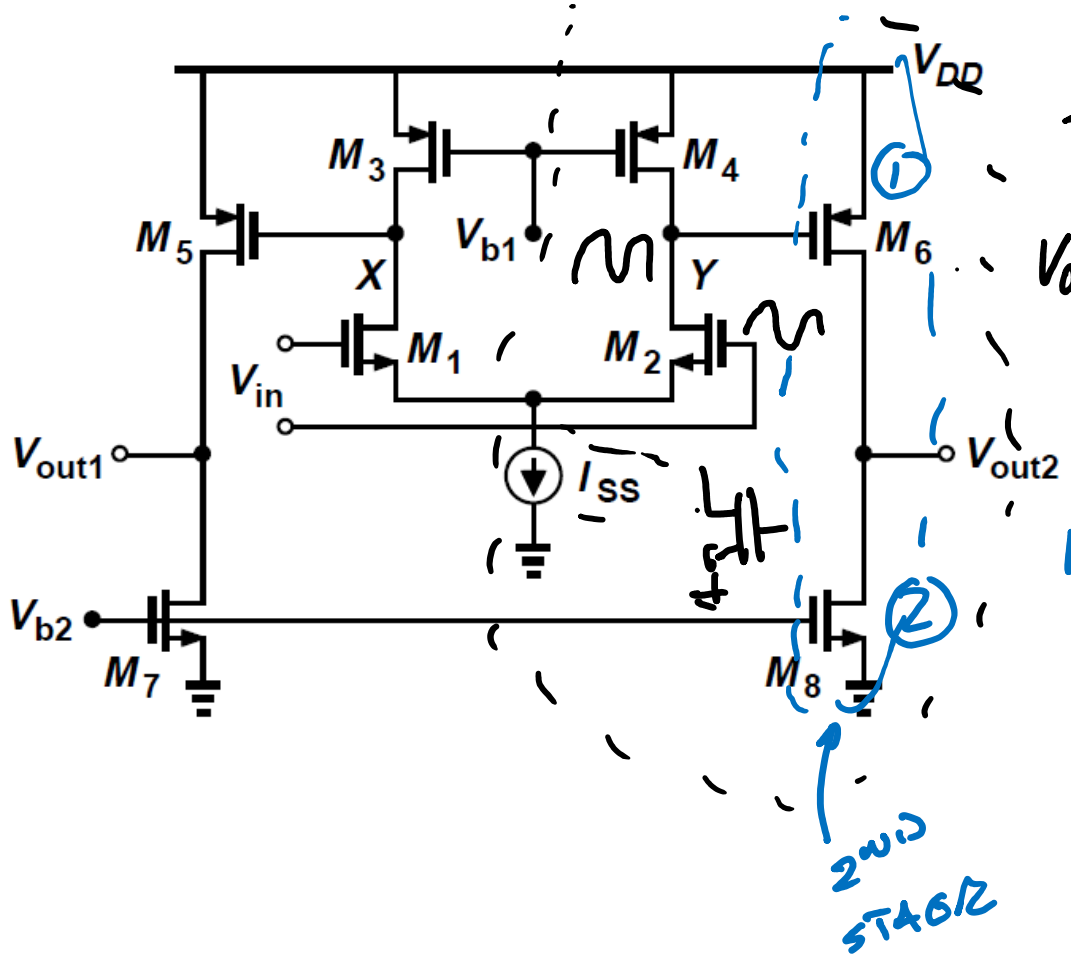
$$A_{2ND} \cong -g_{m5} \cdot (r_{o7} \| r_{o5})$$

$$A = A_{1ST} \cdot A_{2ND}$$

$$= +g_{m1} \cdot g_{m5} (r_{o3} \| r_{o1}) (r_{o5} \| r_{o7})$$

$$A \propto (g_m \cdot r_o)^2$$

# Output Swing Two-Stage Op Amps




OUTPUT SWING 1ST STAGE

NOISY

$V_{OUT,MAX} = V_{DD} - 3V_{DSAT}$

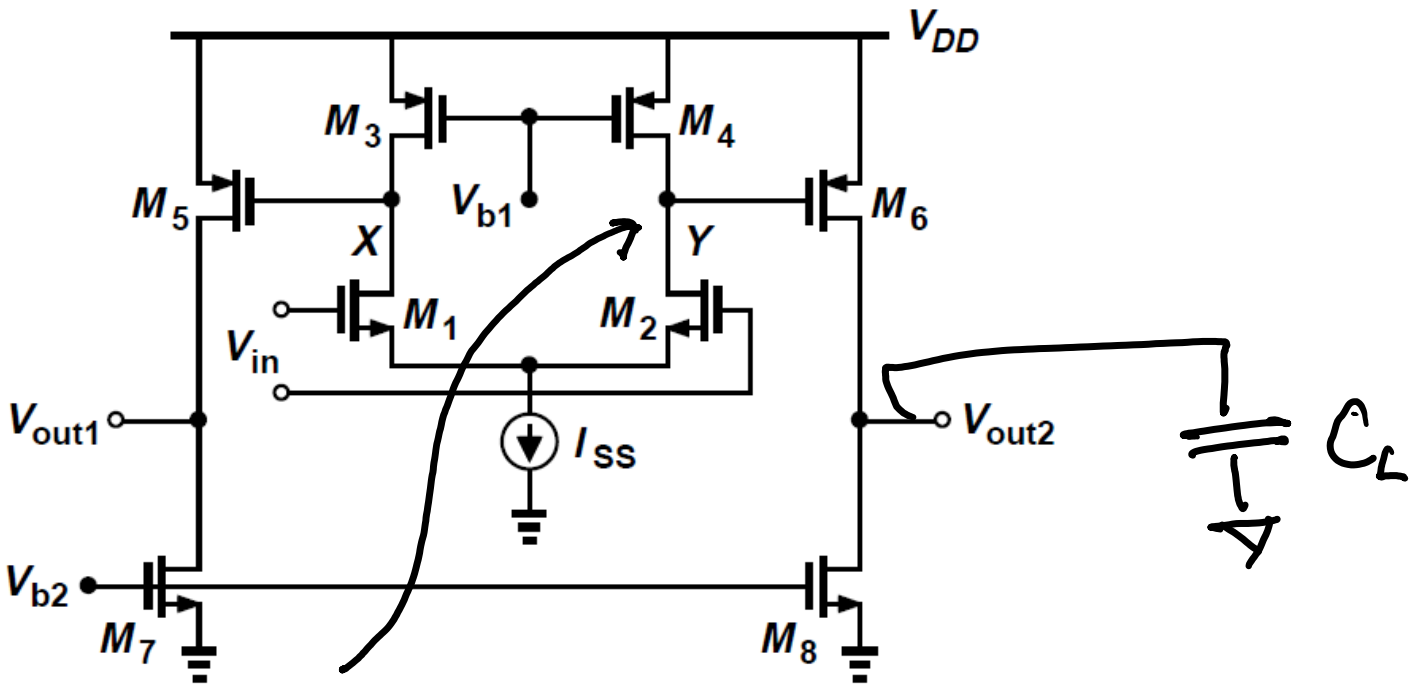
OUTPUT SWING 2ND STAGE

$V_{OUT,MAX} = V_{DD} - 2V_{DSAT}$

WHAT IS THE OVERALL HEADROOM?

ANS: 2ND STAGE → 2ND STAGE SETS HEADROOM BECAUSE OF GAIN IN 2ND STAGE.

# Bandwidth: Two-Stage Op Amps

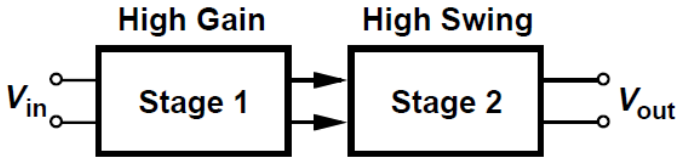


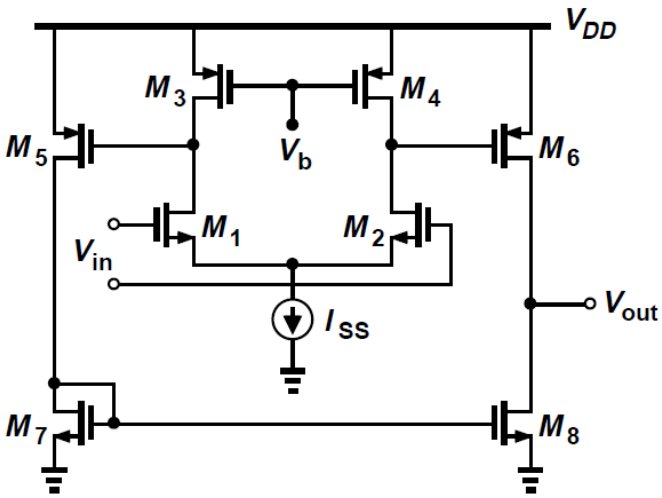

$$p_1 \cong \frac{1}{2\pi (r_{O4} \,//\, r_{O2})(C_{DB4} + C_{DB2} + C_{G6})}$$

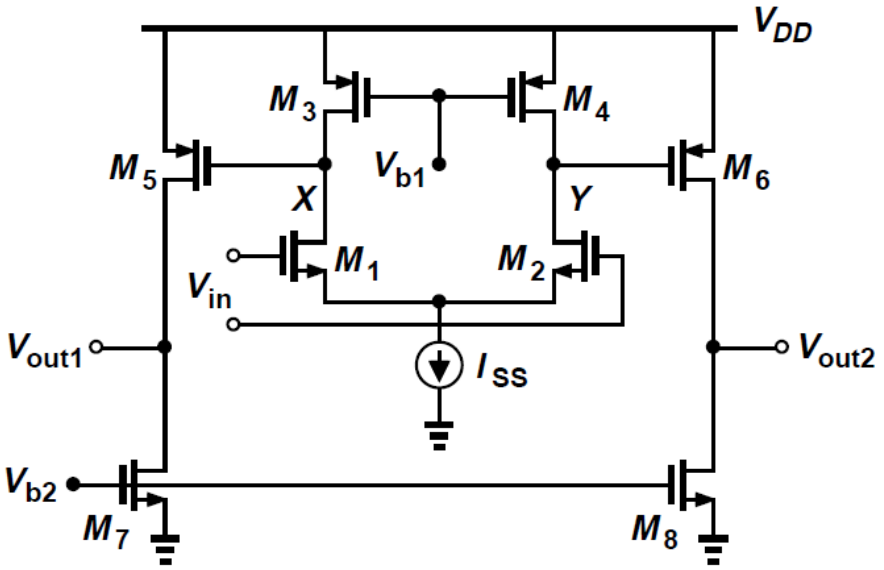
$$p_2 \cong \frac{1}{2\pi (r_{O6} \,//\, r_{O8}) \cdot (C_{DB8} + C_{DB6} + C_L)}$$

# Two-Stage Op Amps

- **Voltage headroom in today's design is constrained with low supply voltage and large output swing**
- **Gain:** $g_{m1,2}(r_{O1,2} \| r_{O3,4})\ g_{m5,6}(r_{O5,6} \| r_{O7,8})$
- **Output Swing: Vdd-2Overdrive**

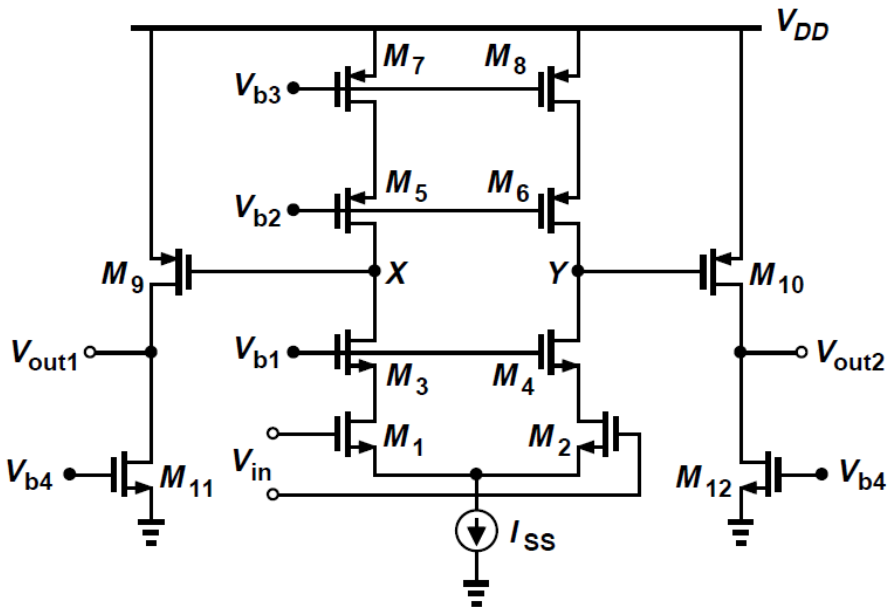


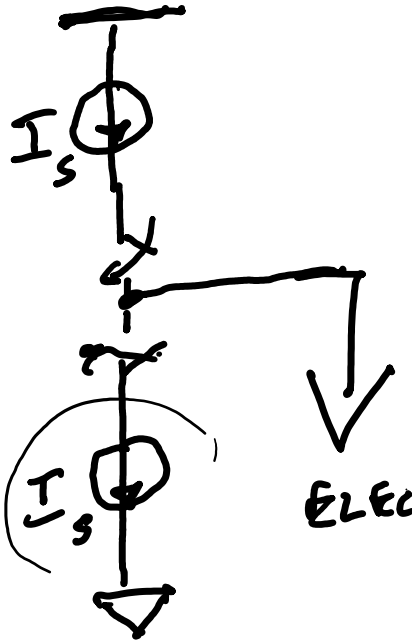



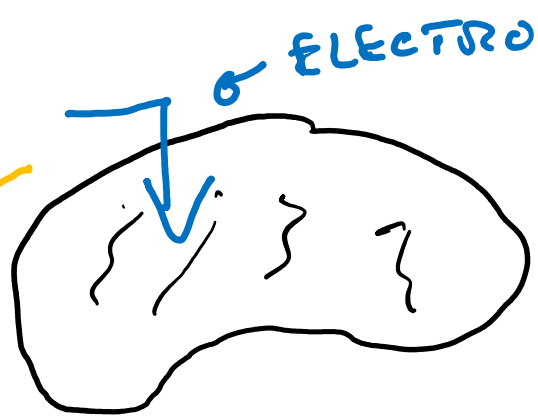
# Two-Stage Op Amps with cascode devices

- **Voltage headroom in today's design is constrained with low supply voltage and large output swing**
- **Gain:** $A_v \approx \{g_{m1,2}[(g_{m3,4}+g_{mb3,4})r_{O3,4}r_{O1,2}]\|[(g_{m5,6}+g_{mb5,6})r_{O5,6}r_{O7,8}]\} \times [g_{m9,10}(r_{O9,10}\|r_{O11,12})].$
- **Can we have more stages? Feedback stability limits**
- **Another low-voltage, high-gain example, A 1.1V, 5-6GHz Reduced-Component Direct-Conversion Transmit Signal Path in 45nm CMOS, ISSCC 2009, Rudell et al.**

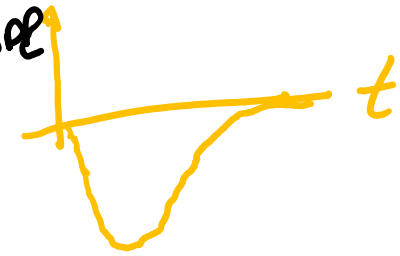


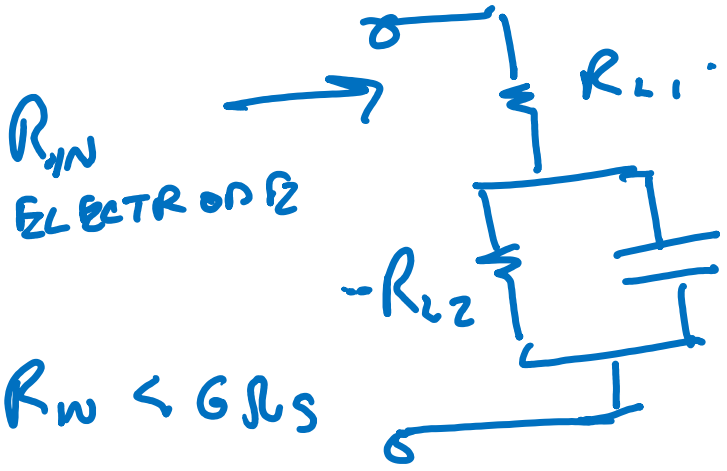
# STIM DRIVER ELECTRONICS

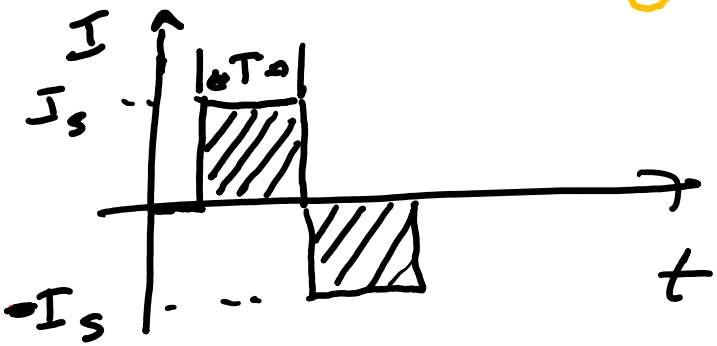



ELECTRODE MODEL

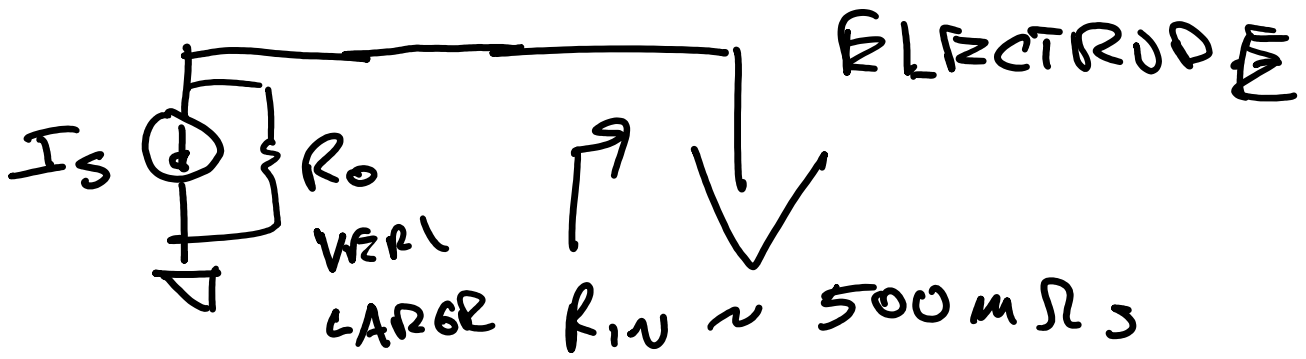


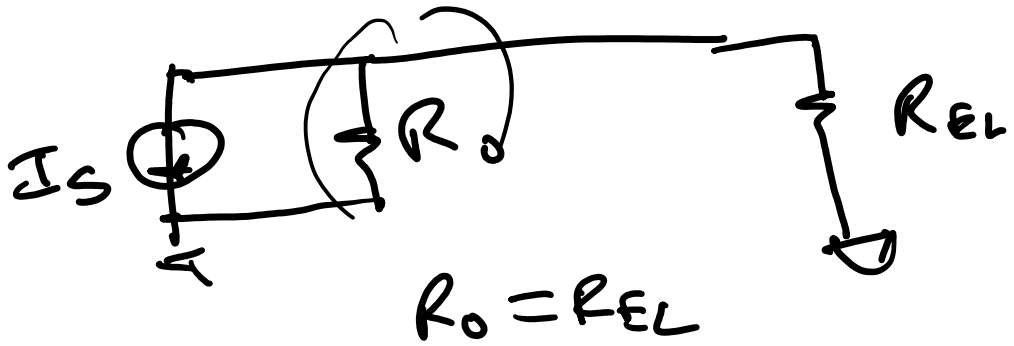




$100\,M R_S \leq R_W < G R_S$

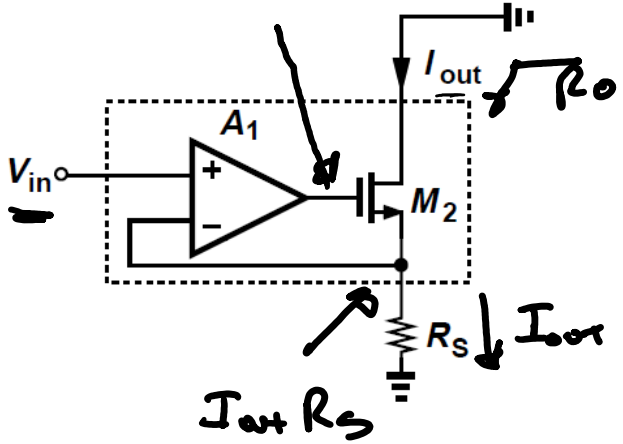
$Q = I_s \cdot T$


ELECTRODE
$I_S$
$R_0$
VERY
LARGE
$R_{IN} \sim 500\,M\Omega$


$I_S$
$R_0$
$R_{EL}$
$R_0 = R_{EL}$

# Gain Boosting Techniques: Effective Gm

$V_G = A_1 (V_{IN} - I_{out} R_S)$




$V_{GS} = A_1 (V_{IN} - I_{out} R_S) - I_{OUT} R_S$

$I_{out} = g_m \cdot V_{GS}$

$I_{out} = g_m [A_1 (V_{IN} - I_{out} R_S) - I_{out} R_S]$

$= g_m A_1 V_{IN} - g_m A_1 I_{out} R_S - g_m I_{out} R_S$

$I_{out} (1 + g_m A_1 R_S + g_m R_S) = g_m \cdot A_1 \cdot V_{IN}$

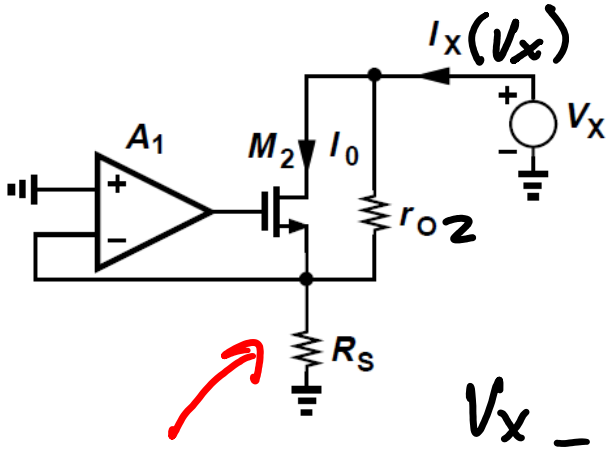
FOR $1 << A_1$

$G_m = \frac{I_{out}}{V_{IN}} = \frac{g_m \cdot A_1}{(1 + g_m R_S (1 + A_1))}$

FOR $1 \ll A_1$

$G_m \cong 1/R_S$

# Output Resistance of Gain Boosting Stage




REPLACE W/ PENCIL

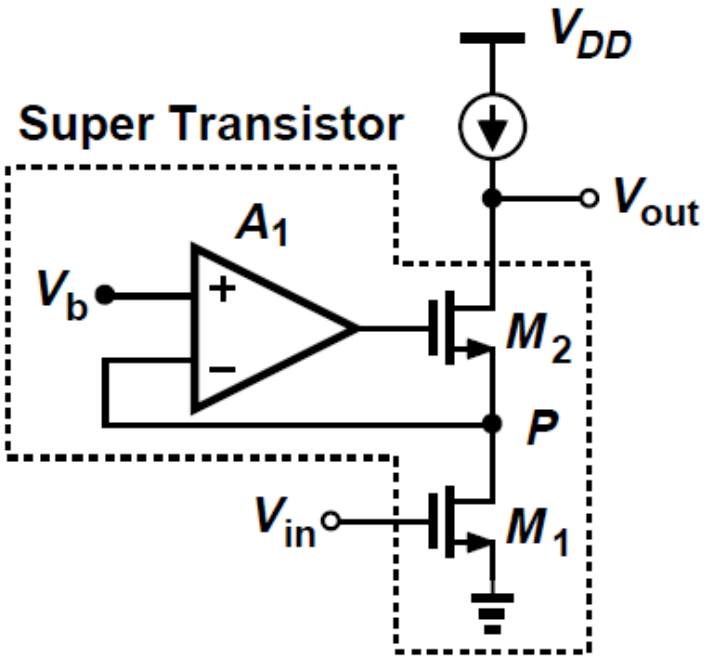
$$\frac{V_X}{I_X} = \frac{(1 + g_{m2} R_S (1 + A_1) + R_S / r_{O2})}{1/r_{O2}}$$

$$= r_{O2} + g_{m2} R_S r_{O2} (1 + A_1) + R_S$$

$$r_{O2}, R_S \ll g_{m2} R_S r_{O2} (1 + A_1)$$

$$R_O \simeq g_{m2} R_S r_{O2} (1 + A_1) \approx g_{m2} R_S r_{O2} A_1$$

# Gain-boosting with Active/Regulated Cascode



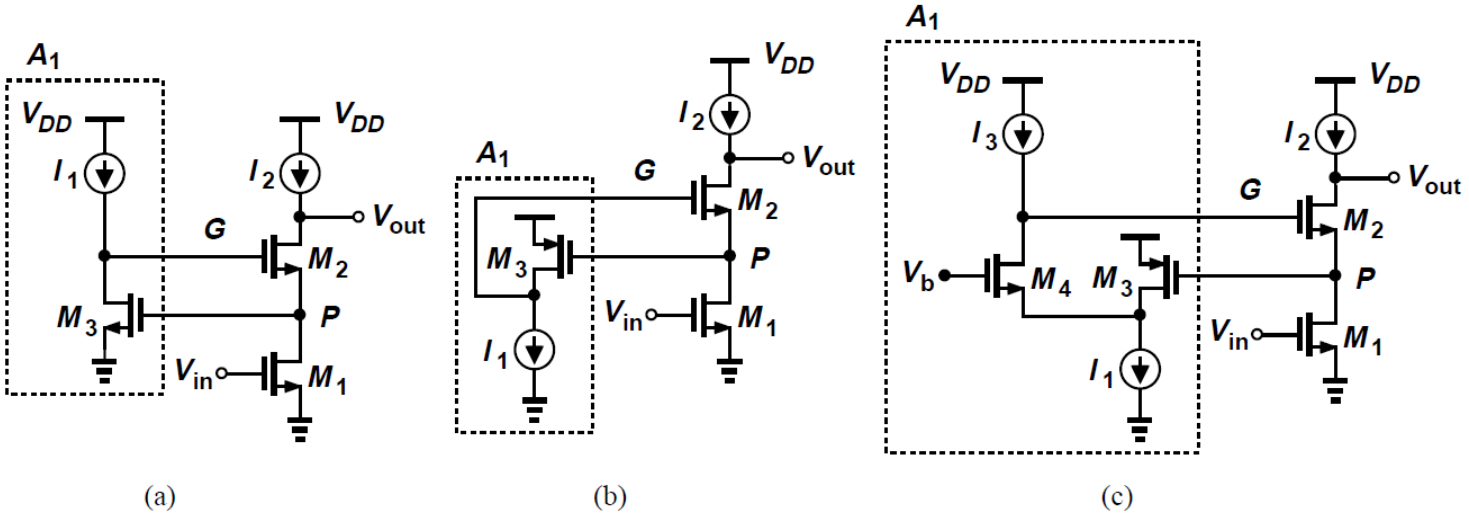

$$R_o \simeq g_{m2} r_{o1} \cdot r_{o2} \cdot A_1$$

# Gain Boosting Circuit Implementation

- **Simplest a common-source stage**

$$|V_{out}/V_{in}| \approx g_{m1}r_{O1}g_{m2}r_{O2}(g_{m3}r_{O3}+1)$$

- **Avoid headroom limitation, PMOS common-source stage is better, but M3 could go in triode**
- **Folded-cascode inserts one more stage**



# Gain Boosting in Signal Path and Load

- Gain boosting can be utilized in the load current source
- To allow maximum swings, A2 employs NMOS-input.