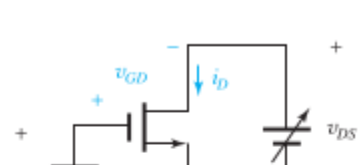
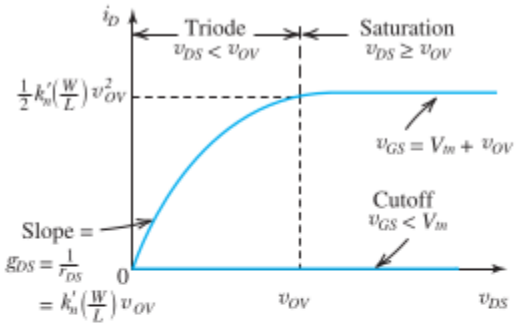
Review

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor





- $v_{GS} < V_{tn}$: no channel; transistor in cutoff; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

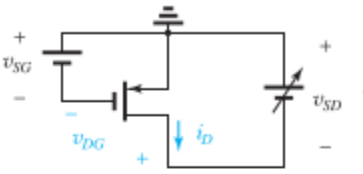
Then

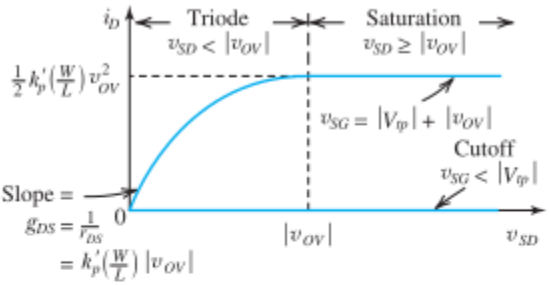
$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently,

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

Table 5.2 Regions of Operation of the Enhancement PMOS Transistor





- $v_{SG} < |V_{tp}|$: no channel; transistor in cutoff; $i_D = 0$
- $v_{SG} = |V_{tp}| + |v_{OV}|$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{DG} > |V_{tp}|$$

or equivalently

$$v_{SD} < |v_{OV}|$$

Then

$$i_D = k_p'\left(\frac{W}{L}\right)\left[(v_{SG} - |V_{tp}|)v_{SD} - \frac{1}{2}v_{SD}^2\right]$$

or equivalently

$$i_D = k_p'\left(\frac{W}{L}\right)\left(|v_{OV}| - \frac{1}{2}v_{SD}\right)v_{SD}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{DG} \leq |V_{tp}|$$

or equivalently

$$v_{SD} \geq |v_{OV}|$$

Then

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(v_{SG} - |V_{tp}|)^2$$

or equivalently

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)v_{OV}^2$$

Table 7.1 Systematic Procedure for the Analysis of Transistor Amplifier Circuits

1. Eliminate the signal source and determine the dc operating point of the transistor.
2. Calculate the values of the parameters of the small-signal model.
3. Eliminate the dc sources by replacing each dc voltage source by a short circuit and each dc current source by an open circuit.
4. Replace the transistor with one of its small-signal, equivalent-circuit models. Although any of the models can be used, one might be more convenient than the others for the particular circuit being analyzed. This point will be made clearer in the next section.
5. Analyze the resulting circuit to determine the required quantities (e.g., voltage gain, input resistance).

Table 7.2 Small-Signal Models of the MOSFET

Small-Signal Parameters

NMOS transistors

- **Transconductance:**

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{OV}}$$

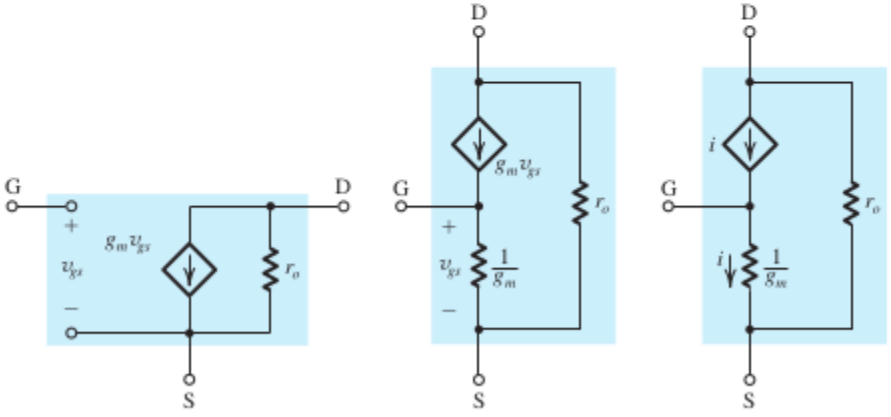
- Output resistance:

$$r_o = V_A / I_D = 1/\lambda I_D$$

PMOS transistors

Same formulas as for NMOS *except* using $|V_{OV}|$, $|V_A|$, $|\lambda|$ and replacing μ_n with μ_p.

Small-Signal, Equivalent-Circuit Models



Hybrid-π model T models

Table 7.4 Characteristics of MOSFET Amplifiers

Amplifier type	Characteristics[a] R_{in}	A_{vo}	R_o	A_v	G_v
Common source (Fig. 7.35)	∞	$-g_m R_D$	R_D	$-g_m(R_D \| R_L)$	$-g_m(R_D \| R_L)$
Common source with R_s (Fig. 7.37)	∞	$-\frac{g_m R_D}{1+g_m R_s}$	R_D	$\frac{-g_m(R_D \| R_L)}{1+g_m R_s}$ $-\frac{R_D \| R_L}{1/g_m + R_s}$	$-\frac{g_m(R_D \| R_L)}{1+g_m R_s}$ $-\frac{R_D \| R_L}{1/g_m + R_s}$
Common gate (Fig. 7.39)	$\frac{1}{g_m}$	$g_m R_D$	R_D	$g_m(R_D \| R_L)$	$\frac{R_D \| R_L}{R_{sig} + 1/g_m}$
Source follower (Fig. 7.42)	∞	1	$\frac{1}{g_m}$	$\frac{R_L}{R_L + 1/g_m}$	$\frac{R_L}{R_L + 1/g_m}$

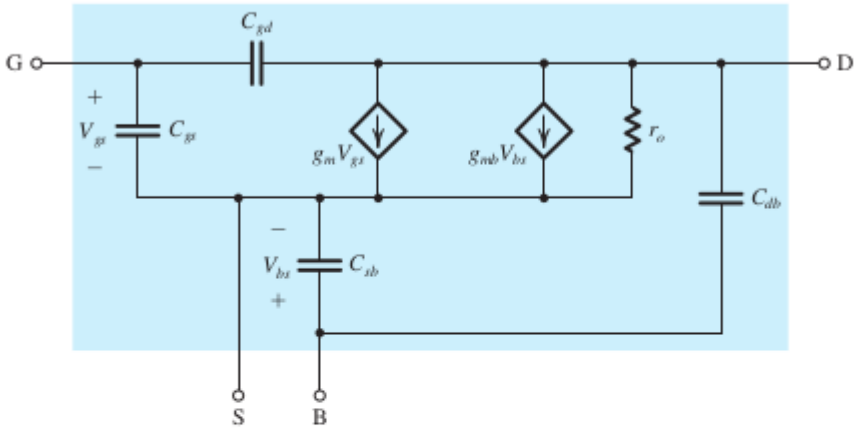
[a] For the interpretation of R_{in}, A_{vo}, and R_o, refer to Fig. 7.34(b).

Table 8.1 Gain Distribution in the MOS Cascode Amplifier for Various Values of R_L

Case	R_L	R_{in2}	R_{d1}	A_{v1}	A_{v2}	A_v
1	∞	∞	r_o	$-g_m r_o$	$g_m r_o$	$-(g_m r_o)^2$
2	$(g_m r_o) r_o$	r_o	$r_o/2$	$-\frac{1}{2}(g_m r_o)$	$g_m r_o$	$-\frac{1}{2}(g_m r_o)^2$
3	r_o	$\frac{2}{g_m}$	$\frac{2}{g_m}$	-2	$\frac{1}{2}(g_m r_o)$	$-(g_m r_o)$
4	0	$\frac{1}{g_m}$	$\frac{1}{g_m}$	-1	0	0

Table 10.1 The MOSFET High-Frequency Model

Model



Model Parameters

$$g_m = \mu_n C_{ox} \frac{W}{L} |V_{OV}| = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{|V_{OV}|}$$

$$g_{mb} = \chi g_m, \quad \chi = 0.1 \text{ to } 0.2$$

$$r_o = |V_A|/I_D$$

$$C_{gs} = \frac{2}{3} WLC_{ox} + WL_{ov} C_{ox}$$

$$C_{gd} = WL_{ov} C_{ox}$$

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1 + \frac{|V_{SB}|}{V_0}}}$$

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{|V_{DB}|}{V_0}}}$$

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}$$

Table G.3 Comparison of the MOSFET and the BJT

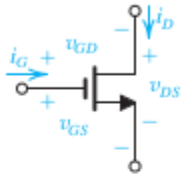
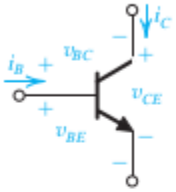
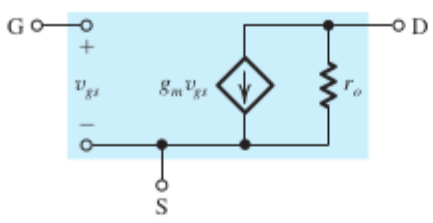
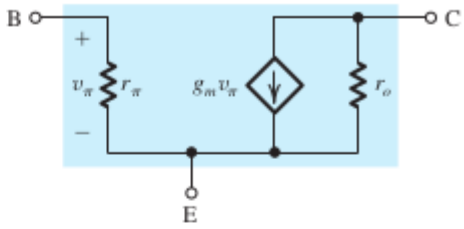
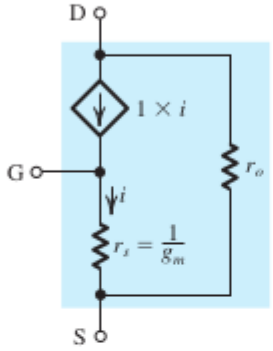
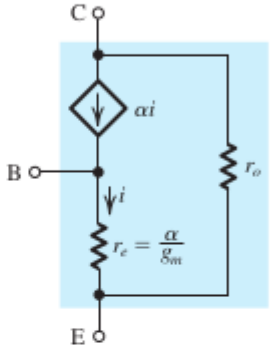
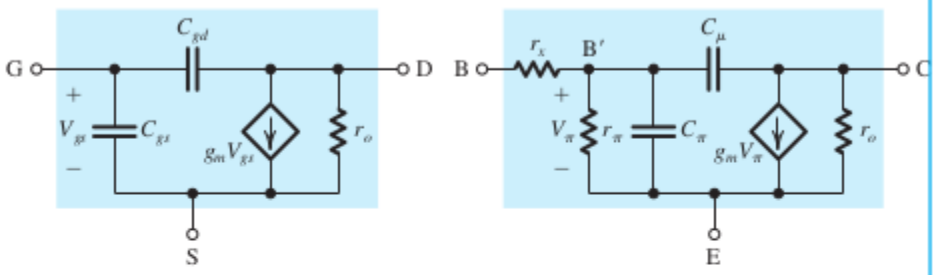
	NMOS	*npn*
Circuit Symbol		
To Operate in the Active Mode, Two Conditions Have to Be Satisfied	(1) *Induce a channel*: $v_{GS} \geq V_t$, $V_t = 0.3$–$0.5\,\text{V}$ Let $v_{GS} = V_t + v_{OV}$ (2) *Pinch-off channel at drain*: $v_{GD} < V_t$ or equivalently, $v_{DS} \geq V_{OV}$, $V_{OV} = 0.1$–$0.3\,\text{V}$	(1) *Forward-bias EBJ*: $v_{BE} \geq V_{BEon}$, $V_{BEon} \simeq 0.5\,\text{V}$ (2) *Reverse-bias CBJ*: $v_{BC} < V_{BCon}$, $V_{BCon} \simeq 0.4\,\text{V}$ or equivalently, $v_{CE} \geq 0.3\,\text{V}$
Current–Voltage Characteristics in the Active Region	$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2\left(1 + \frac{v_{DS}}{V_A}\right)$ $= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2\left(1 + \frac{v_{DS}}{V_A}\right)$ $i_G = 0$	$i_C = I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right)$ $i_B = i_C/\beta$

Table G.3 *continued*

	NMOS	*npn*
Low-Frequency, Hybrid-π Model		
Low-Frequency T Model		
Transconductance g_m	$g_m = I_D/(V_{OV}/2)$ $g_m = (\mu_n C_{ox})\left(\frac{W}{L}\right)V_{OV}$ $g_m = \sqrt{2(\mu_n C_{ox})\left(\frac{W}{L}\right)I_D}$	$g_m = I_C/V_T$
Output Resistance r_o	$r_o = V_A/I_D = \frac{V_A' L}{I_D}$	$r_o = V_A/I_C$
Intrinsic Gain $A_0 \equiv g_m r_o$	$A_0 = V_A/(V_{OV}/2)$ $A_0 = \frac{2V_A' L}{V_{OV}}$ $A_0 = \frac{V_A'\sqrt{2\mu_n C_{ox} WL}}{\sqrt{I_D}}$	$A_0 = V_A/V_T$
Input Resistance with Source (Emitter) Grounded	∞	$r_\pi = \beta/g_m$

(continued)

Table G.3 *continued*

	NMOS	*npn*
High-Frequency Model		
Capacitances	$C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox}$ $C_{gd} = WL_{ov}C_{ox}$	$C_\pi = C_{de} + C_{je}$ $C_{de} = \tau_F g_m$ $C_{je} \simeq 2C_{je0}$ $C_\mu = C_{\mu 0} \Big/ \left[1 + \frac{V_{CB}}{V_{C0}}\right]^m$
Transition Frequency f_T	$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$ For $C_{gs} \gg C_{gd}$ and $C_{gs} \simeq \frac{2}{3}WLC_{ox}$, $f_T \simeq \frac{1.5\mu_n V_{OV}}{2\pi L^2}$	$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$ For $C_\pi \gg C_\mu$ and $C_\pi \simeq C_{de}$, $f_T \simeq \frac{2\mu_n V_T}{2\pi W_B^2}$
Design Parameters	I_D, V_{OV}, L, $\frac{W}{L}$	I_C, V_{BE}, A_E (or I_S)
Good Analog Switch?	Yes, because the device is symmetrical and thus the i_D–v_{DS} characteristics pass directly through the origin.	No, because the device is asymmetrical with an offset voltage $V_{CE,off}$.