EE 473/538 CAD Lab 4 Winter 2022

Due on Thursday, Feb. 17th at 5pm. Please submit electronically in CANVAS.

Analog Simulation Tutorial

Introduction

This tutorial introduces common simulation practices for analog circuits, with a single-stage, fully-differential op-amp as an example. This tutorial covers MOSFET parameters, schematic set-up, and several types of simulation in Cadence Virtuoso. Each step will be accompanied with illustrative screen captures. Capture colors may be inverted or altered to make the document printable.

Report

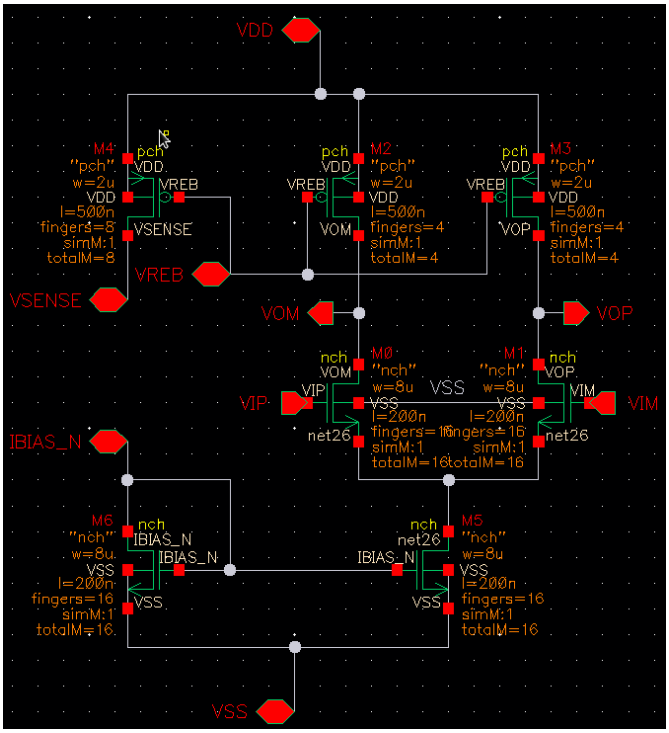
For your report, please do a screen capture of all simulation results, including annotating your circuit for the (Vgs-Vth), DC operating voltages and currents as well as any simulation plots. For each screen capture, please write 2-4 sentences about your observations and anything interesting that you may have learned.

Setup

This tutorial assumes that you have configured a working directory for Cadence Virtuoso with the TSMC 65nm Process Design Kit (PDK). Creating a new library is recommended, but this design can be built in any library attached to the tsmcN65 technology library.

Op-Amp Schematic

Create a new schematic in your working library. The schematic in this example is named "opamp_replica." Create a schematic configured like the one shown below:

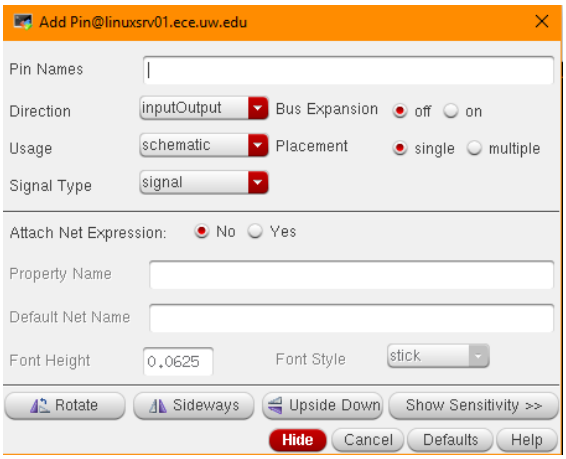


The top "pch" devices load the circuit and M4 is used as the sensing point for replica biasing. VREB and VSENSE will go to an ideal opamp in the testbench. The VSENSE pch on the left has 8 fingers, and the two load devices have 4 fingers. All three devices have: W/L = 2u/500n.

The amplifying "nch" devices provide transconductance. This pair must be symmetrical to boost common mode rejection and offset. Parameters: W/L = 8u/200n and 16 fingers.

The bottom devices form a current mirror biasing the differential pair. These devices must also match. Parameters: W/L = 8u/500n and 16 fingers.

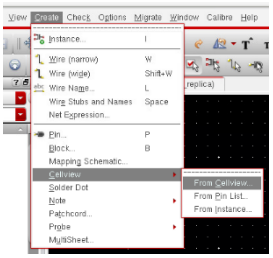
To create pins for the inputs and outputs of the circuit, press “p” hotkey to bring up the pin menu.



- VSENSE, VREB, IBIAS_N, VDD, and VSS will have a direction of “inputOutput”
- VIP and VIM will have a direction of “input”
- VOP and VOM will have a direction of “output”

Place these pins in their respective places as seen in the circuit diagram above.

Op-Amp Symbol

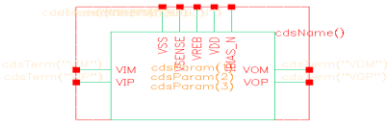


In the schematic editor window, select:

Create → Cellview → From Cellview

and hit “OK” on any windows that open to automatically generate a symbol view. If a “black box” schematic does not immediately open, check the library manager to see if a symbol schematic was created.

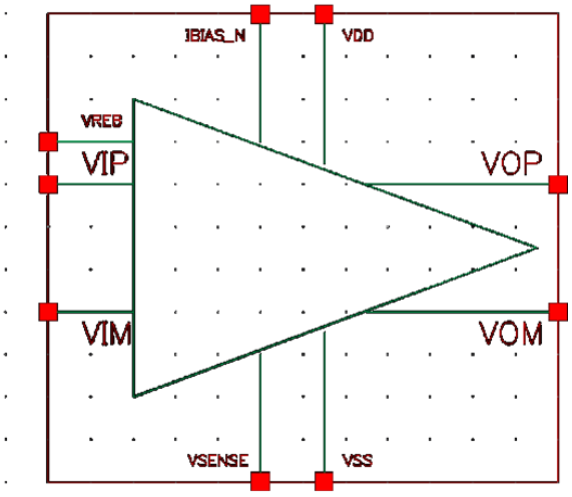
Opening the symbol will show you something to the left. This “black box” figure isn’t particularly useful or descriptive of what the circuit does so usually we have to draw our own symbol.



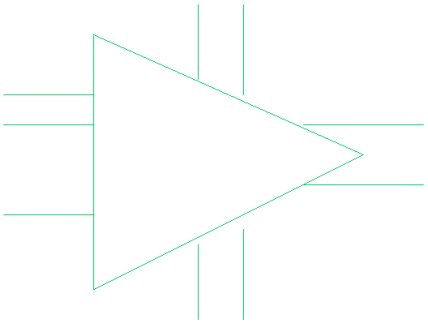
It is good practice to draw a symbol that describes your circuit. Every designer has different conventions, but it is important that everything you draw can be interpreted by others. An example symbol is shown below. It follows some basic rules:

- Higher voltages should be on top. IBIAS_N and VDD are sinking current and in general, current goes from top to bottom.
- Inputs are on the left and outputs are on the right. We consider VREB an input in this case, because it is the PMOS gate driven by the ideal opamp output.

Current flows out of VSENSE and VSS; they should be placed on the bottom.



To begin drawing the new symbol, use these options in the header of the schematic:

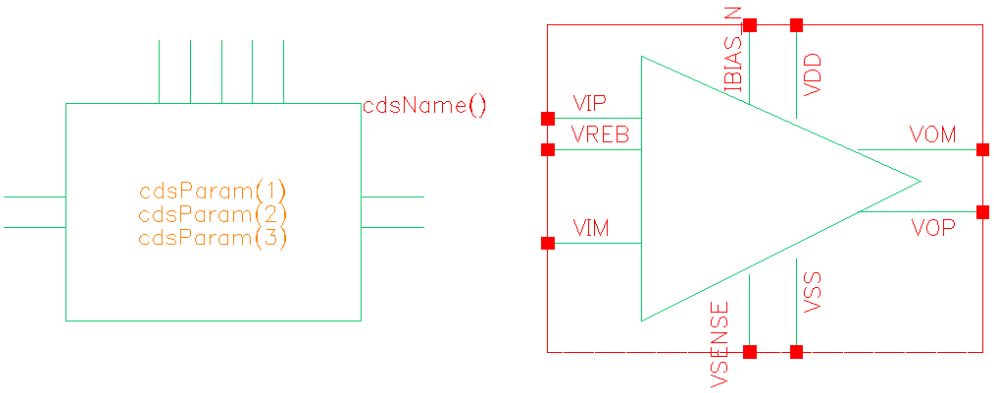


The “Create Line” option was used to create the symbol on the right.

Move the red pins from the generated “black box” symbol onto the new symbol following the guidelines mentioned above. You can delete the cdsTerms that are attached to each pin.

After the pins have been moved onto the new symbol, find the red box that is still on the initial generated symbol. Move the red box onto the new drawn symbol, making sure that each side of the red box is touching the red pins.

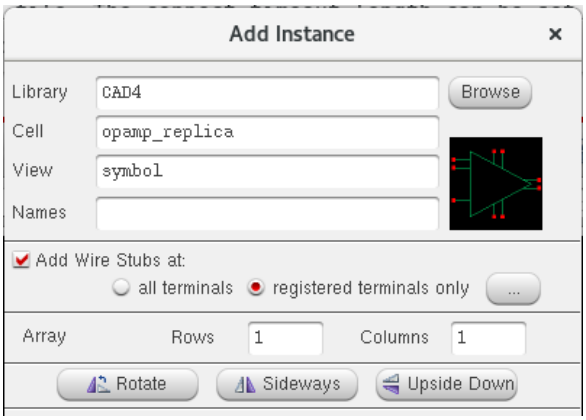
The new drawn symbol should look something like below:



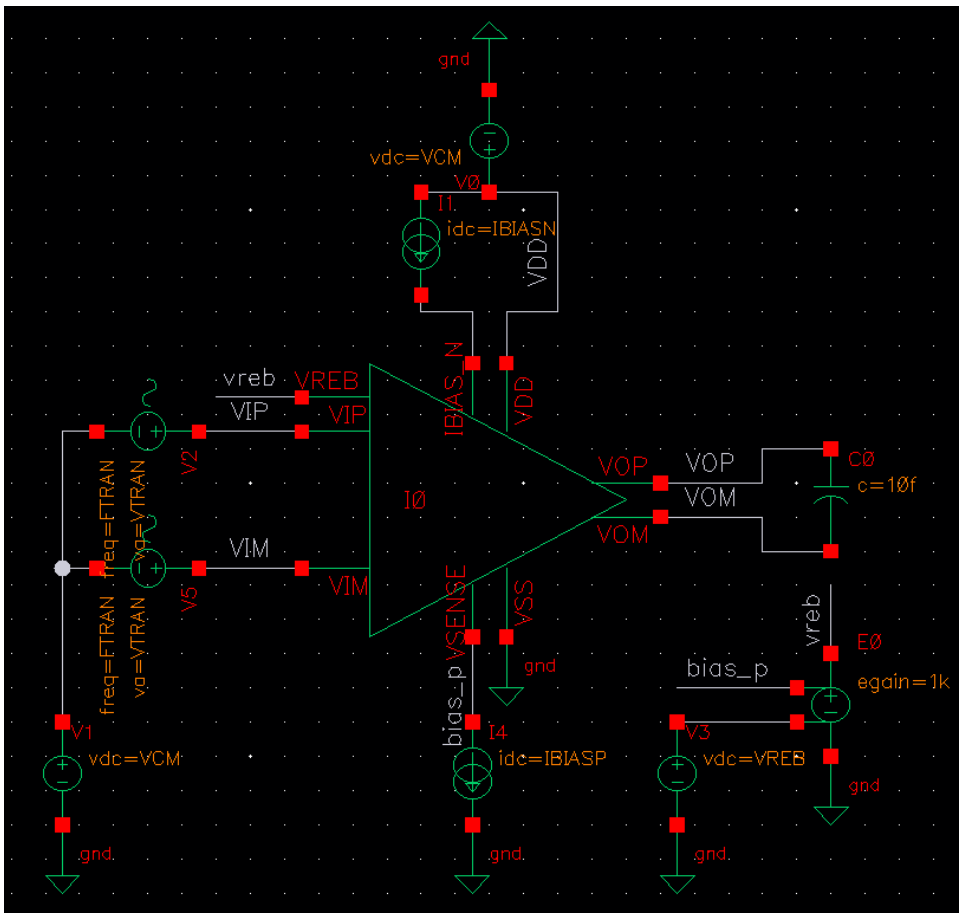
Delete the generated symbol on the left and save the symbol schematic. Now you have a drawn symbol that looks something like a traditional opamp symbol. Next, we will use the newly drawn symbol in a testbench

Testbench

Create a new schematic cellview named “opamp_replica_test’; this will be your testbench. To place the symbol in the new the schematic, press “I” to add a new instance. Type in the library in which the symbol is in along with the name of the cellview.

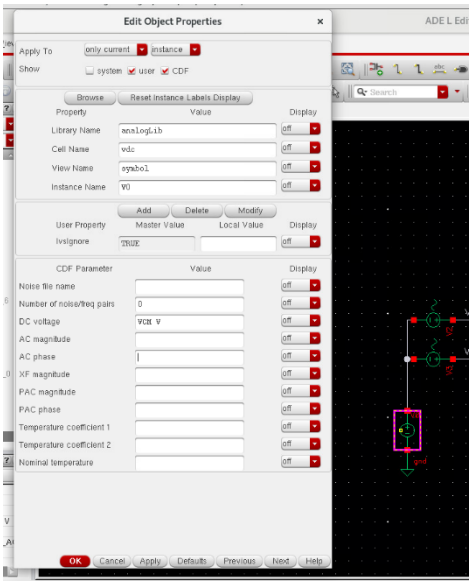


A picture of the symbol you just made should show up in the icon on the right. Place the symbol into schematic and construct a testbench based on the picture below using components from the analogLib library. Component parameters will be explained in detail. (Please note that VIP is connected to the AC source despite what the diagram shows)



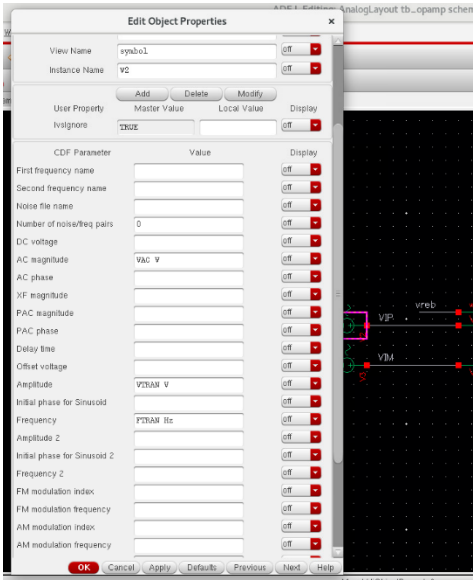
Common-mode DC voltage bias “vdc”

DC Voltage: VCM



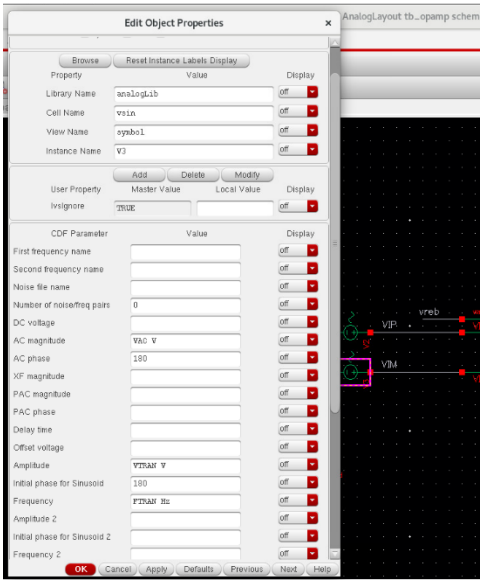
Positive input voltage source “vsin”

AC Magnitude: VAC
Amplitude: VTRAN
Frequency: FTRAN



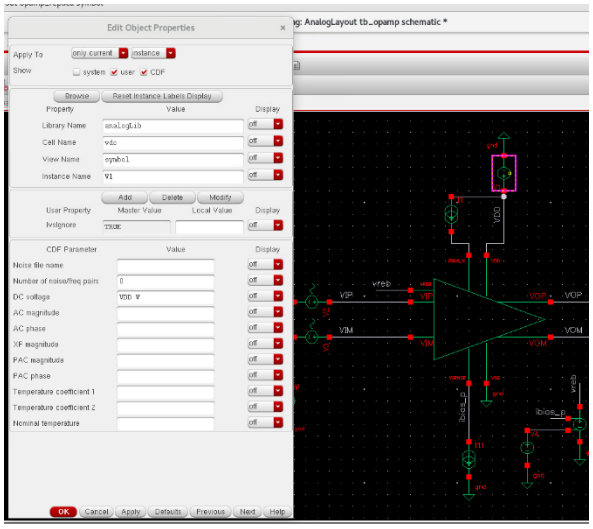
Negative input voltage source “vsin”

AC Magnitude: VAC
AC Phase: 180
Amplitude: VTRAN
Initial Phase for Sinusoid: 180
Frequency: FTRAN

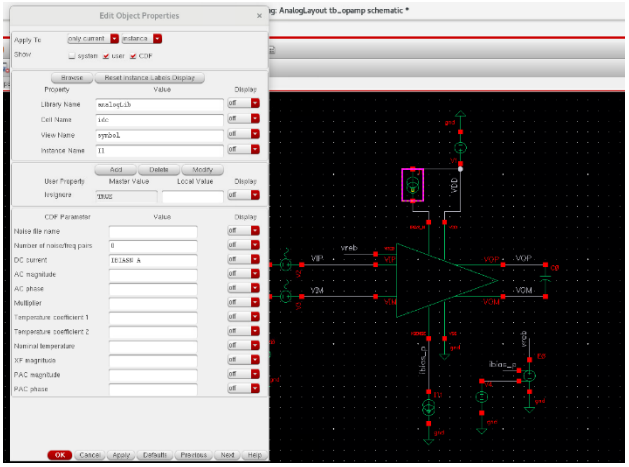


Power voltage source “vdc”

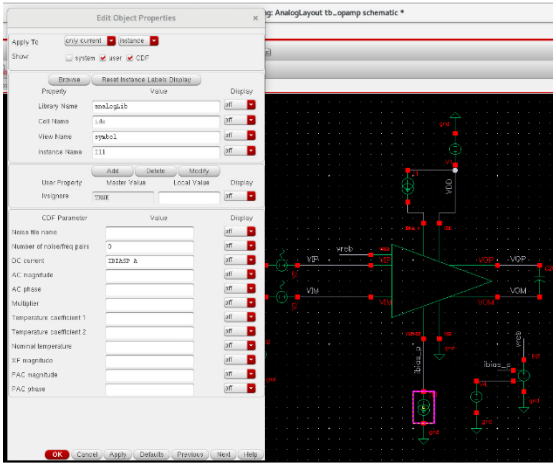
DC Voltage: VDD



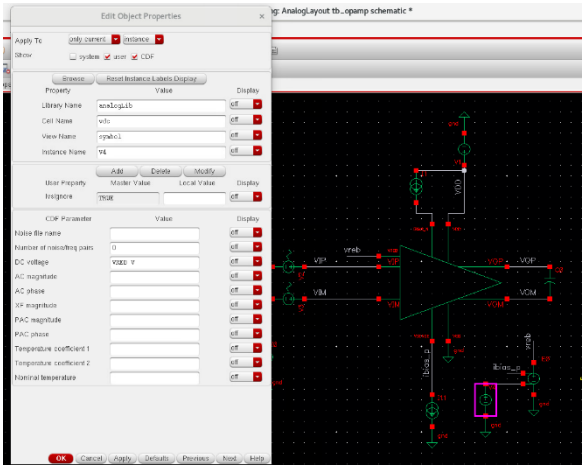
NMOS current bias “idc”
DC Current: IBIASN



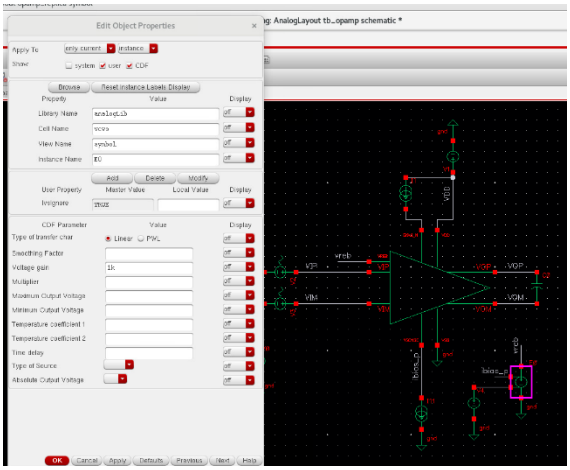
PMOS current bias “idc”
DC Current: IBIASP



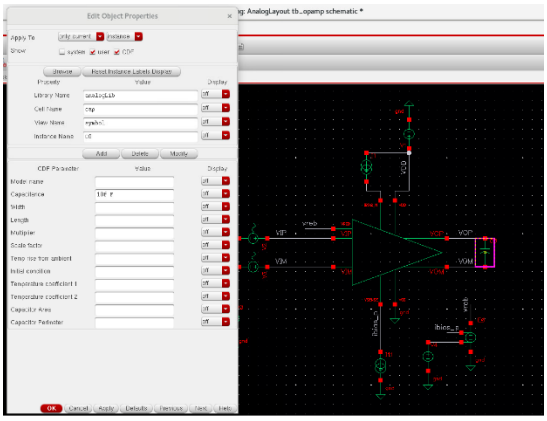
Replica bias voltage reference “vdc”
DC Voltage: VREB



Replica bias ideal op-amp “vcvs”
Voltage Gain: 1k



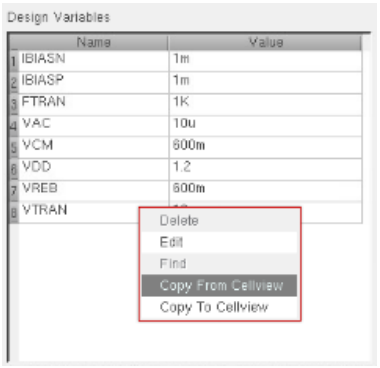
Load capacitor “cap”
Capacitance: 10f



Schematic Simulation

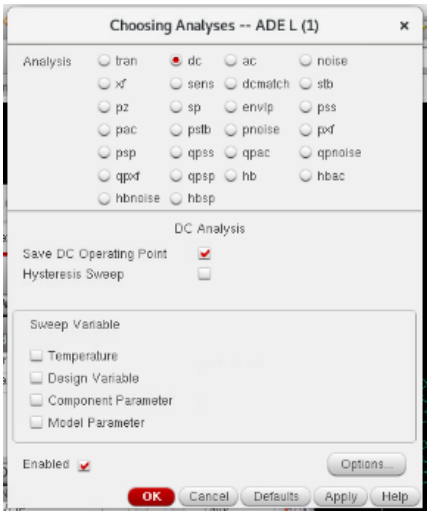
Start the ADE simulator from the schematic editor window with Launch → ADE L

Pull in the parameters used in the testbench by right-clicking in the "Design Variables" box and selecting "Copy from Cellview." This will populate the parameter names. Fill in the parameters as follows:

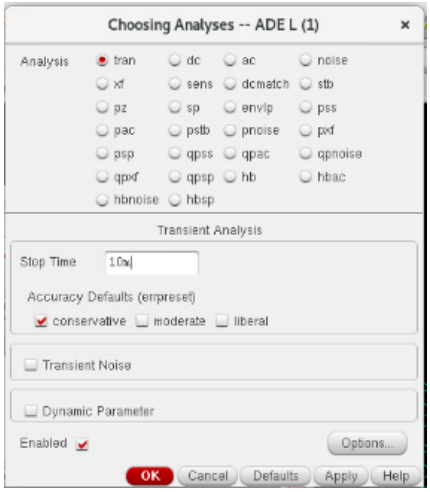


IBIASN, IBIASP:	1m
FTRAN:	1k
VAC:	10u
VCM:	600m
VDD:	1.2
VREB:	600m
VTRAN:	10u

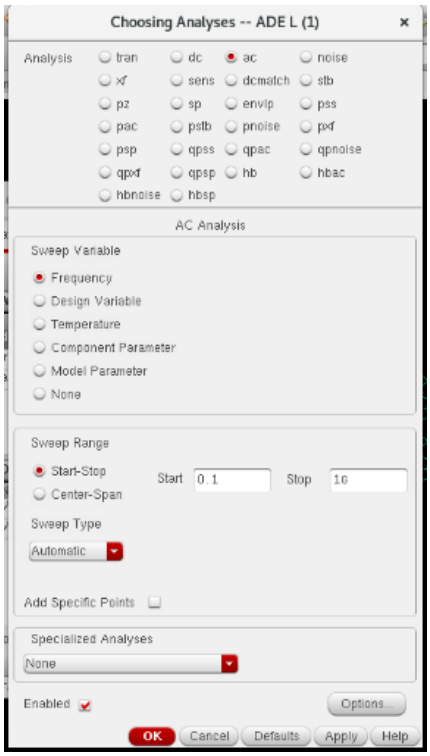
Next, right click in the "Analyses" box and "Edit" to select simulation types. Configure a dc, ac, and tran simulations as shown below:



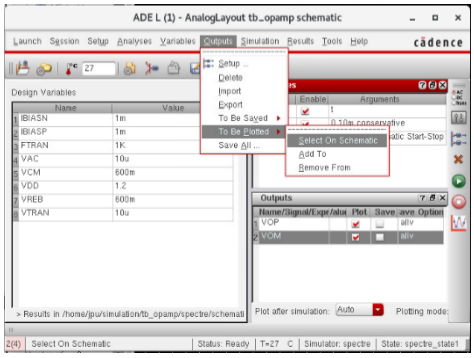
tran Stop Time: 10m



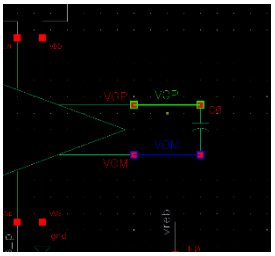
AC Start-Stop: 0.1 – 1G



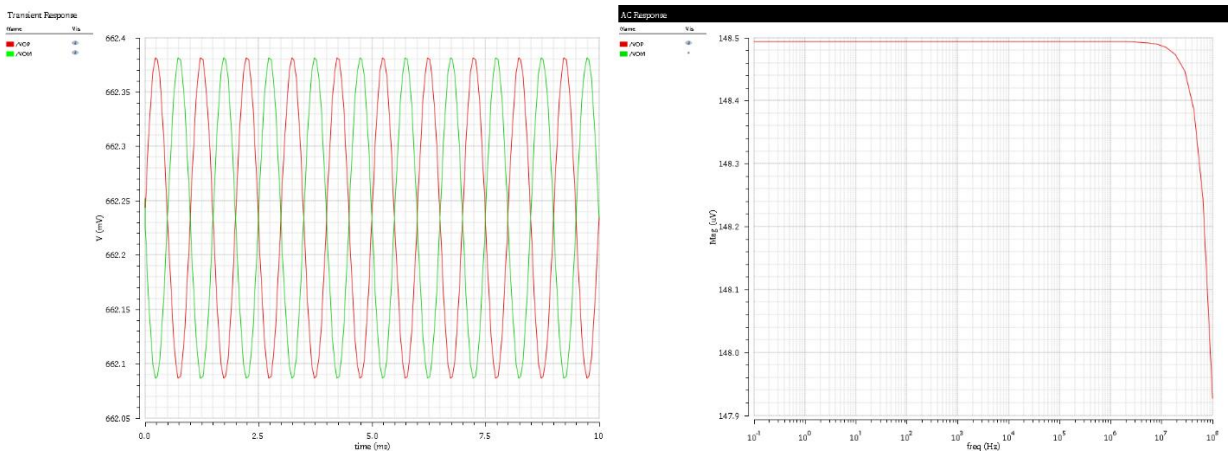
Next, add outputs to your simulation by selecting “Outputs → To Be Plotted → Select on Schematic”



Click on VOP and VOM in the testbench schematic to add them to your outputs.

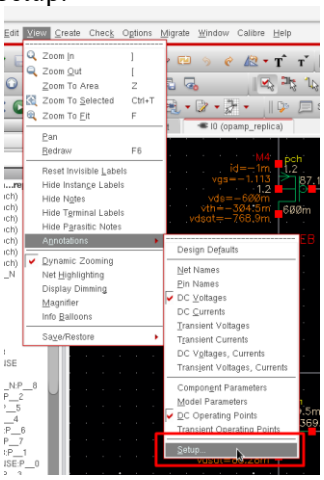


This will generate an output like the one below:

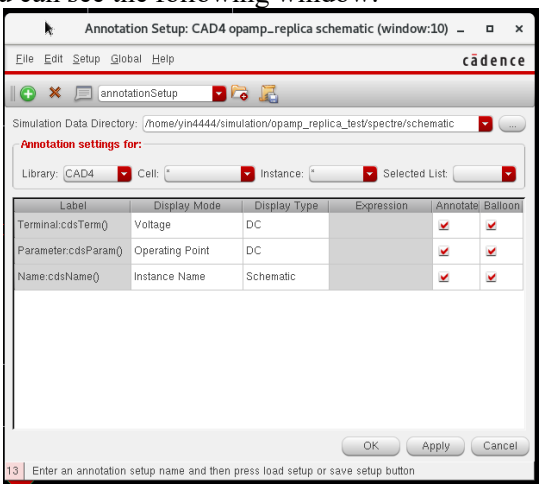


Notice a gain of approximately 15 (150uV AC output with a 10uV AC input).

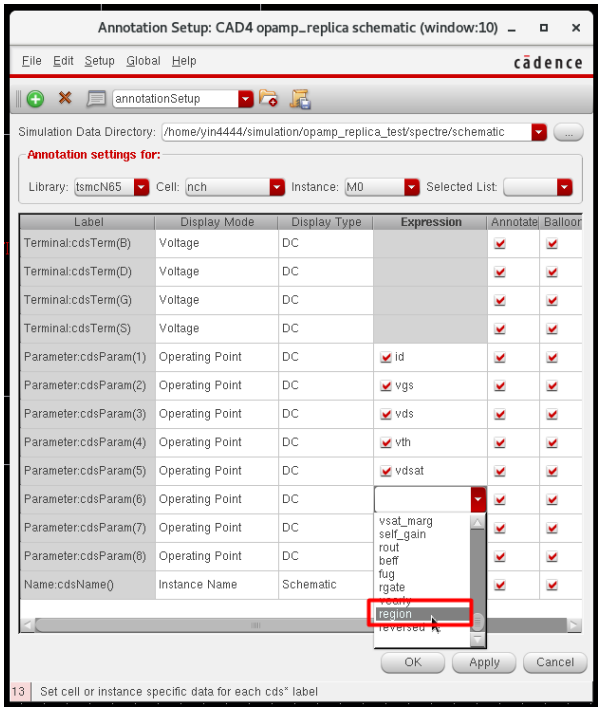
To view the calculated DC operating points, add annotations to your schematic after simulation. Enter the placed op-amp symbol in your testbench with “Descend Edit.” Either use shift-E and click on the symbol or right-click and hit “Descend Edit.” Now, select “View → Annotations” to add DC Voltage and DC Operating Point annotations. You can add additional Operating Point annotations, such as “gm” or “rout” by selecting “View → Annotations → Setup.”



After click on the “Setup”, you can see the following window:



For example, in order to add the DC operating region of M0 into the annotation, choose “tsmcN65” for “Library”, “nch” for “Cell”, and “M0” for “Instance”. Finally, double-click on one of the empty parameters and choose “region” to be illustrated:



If you examine the DC operating points, notice that the PMOS load devices are in triode (|VDS| < |VGS-VTH|) and the NMOS devices are in saturation (|VDS| > |VGS-VTH|). This is an all-MOSFET implementation of a fully differential, resistively loaded common-source amplifier.

Report

For your report, please do a screen capture of all simulation results, including annotating your circuit for the (Vgs-Vth), DC operating voltages and currents as well as any simulation plots. For each screen capture, please write 2-4 sentences about your observations and anything interesting that you may have learned.