EE 473/538 Project 1 Winter 2022

Title: Design a Bandgap Reference Circuit with minimal Temperature Dependence.

Due Date: Tuesday, February 15th at 5pm. Please submit online.

Description: You are to design a Bandgap voltage reference circuit with minimal temperature variation from $-40\ C^o$ to $+120\ C^o$. You should use the 65nm TSMC PDK for all your components except the opamp. You will be allowed to use an ideal opamp in your cadence schematic from the "AnalogLib" library. The open-loop gain of the opamp can be no greater than 500V/V. All other components used in your schematic need to come from the 65nm library of devices. You are to design your bandgap to achieve minimal voltage variation over the given temperature range.

You should include a plot of the output voltage versus temperature, with voltage on the y-axis and temperature on the x-axis. You will be graded on the quality and robustness of your design, in addition to the minimization of $\Delta V_{out}(T)$. In your plot of V_{out} vs. T (in Celsius), please use the curser and marks to show the maximum and minimum voltage over the temperature range. Please report in a table, all the device sizes used in your bandgap, the current flowing down any branch and compute to include in your table:

$$\frac{\Delta V_{out}}{V_{out}}$$

You should write a two-page report that contains the following content:

- **Introduction:** which describes the challenges of building your circuit and what alternative solutions have been published.
- **Design:** a detailed description of your design, please emphasize any novelty in your design.
- **Results:** please use clear figures to show your Cadence simulation results with a clear discussion of the results.
- **Conclusions:** Type up a brief paragraph of concluding comments. You may add another paragraph to describe what you would have done differently if you had more time to design this circuit.
- **Appendix:** You may use an additional page for figures.