EE 473/538 Linear IC Design (HW 1) January 21, 2022

Kevin Egedy

Unless otherwise stated, in the following problems, use the device data shown in Table 2.1 and assume that $V_{DD} = 3$ V where necessary. All device dimensions are effective values and in microns.

Table 2.1 Level 1 SPICE models for NMOS and PMOS devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

3.1. For the circuit of Fig. 3.13, calculate the small-signal voltage gain if $(W/L)_1 = 50/0.5$, $(W/L)_2 = 10/0.5$, and $I_{D1} = I_{D2} = 0.5$ mA. What is the gain if M_2 is implemented as a diode-connected PMOS device (Fig. 3.16)?

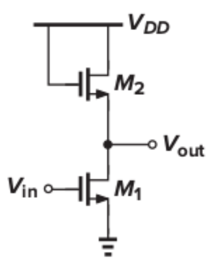

Figure 3.13 CS stage with diode-connected load.

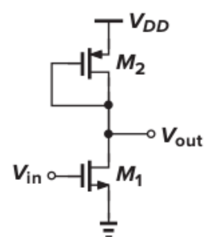

Figure 3.16 CS stage with diode-connected PMOS device.

3.2. In the circuit of Fig. 3.18, assume that $(W/L)_1 = 50/0.5$, $(W/L)_2 = 50/2$, and $I_{D1} = I_{D2} = 0.5$ mA when both devices are in saturation. Recall that $\lambda \propto 1/L$.

(a) Calculate the small-signal voltage gain.

(b) Calculate the maximum output voltage swing while both devices are saturated.

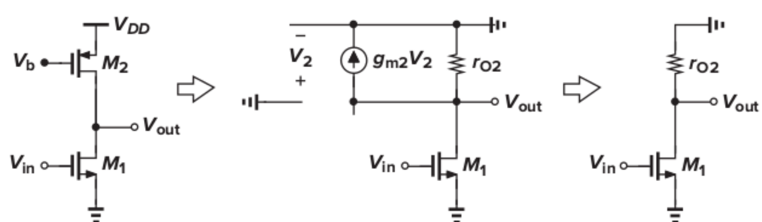

Figure 3.18 CS stage with current-source load.

3.3. In the circuit of Fig. 3.4(a), assume that $(W/L)_1 = 50/0.5$, $R_D = 2$ kΩ, and $\lambda = 0$.

(a) What is the small-signal gain if M_1 is in saturation and $I_D = 1$ mA?

(b) What input voltage places M_1 at the edge of the triode region? What is the small-signal gain under this condition?

(c) What input voltage drives M_1 into the triode region by 50 mV? What is the small-signal gain under this condition?

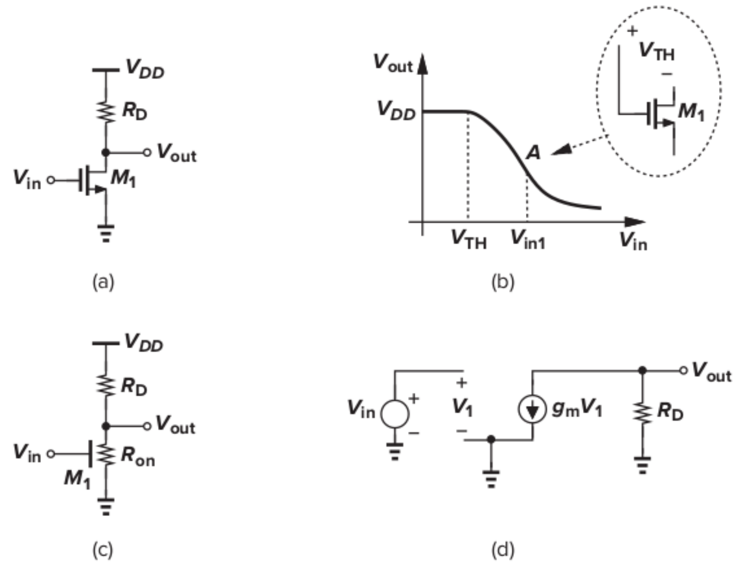

Figure 3.4 (a) Common-source stage, (b) input-output characteristic, (c) equivalent circuit in the deep triode region, and (d) small-signal model for the saturation region.

3.20. Assuming all MOSFETs are in saturation, calculate the small-signal voltage gain of each circuit in Fig. 3.83 ($\lambda \neq 0, \gamma = 0$).

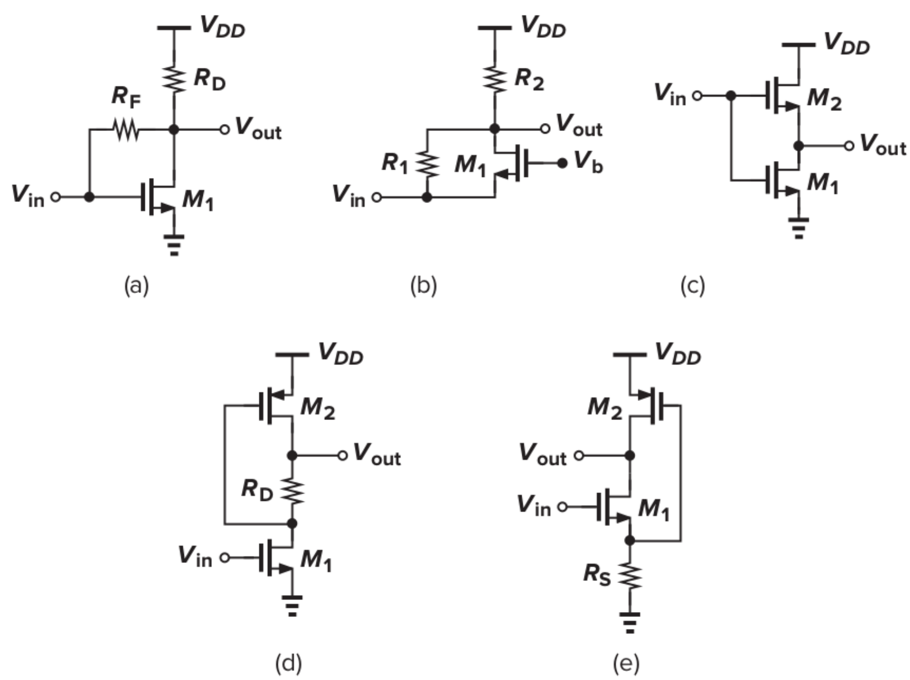

Figure 3.83

3.27. A source follower can operate as a level shifter. Suppose the circuit of Fig. 3.37(b) is designed to shift the voltage level by 1 V, i.e., $V_{in} - V_{out} = 1$ V.

(a) Calculate the dimensions of M_1 and M_2 if $I_{D1} = I_{D2} = 0.5$ mA, $V_{GS2} - V_{GS1} = 0.5$ V, and $\lambda = \gamma = 0$.

(b) Repeat part (a) if $\gamma = 0.45\ \mathrm{V}^{-1}$ and $V_{in} = 2.5$ V. What is the minimum input voltage for which M_2 remains saturated?

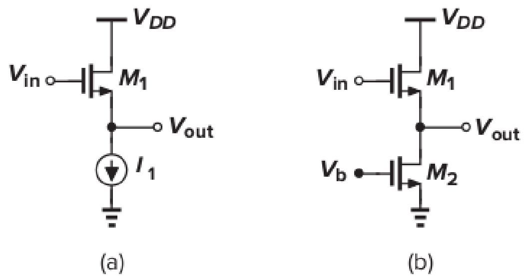

Figure 3.37 Source follower using (a) an ideal current source, and (b) an NMOS transistor as a current source.

3.32. In the circuit shown in Fig. 3.86, prove that

$$\frac{V_{out1}}{V_{out2}} = \frac{-R_D}{R_S} \tag{3.148}$$

where V_{out1} and V_{out2} are small-signal quantities and $\lambda,\ \gamma > 0$.

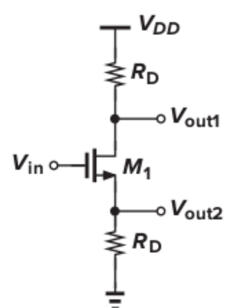

Figure 3.86

3.34. Calculate the voltage gain of a source follower using the lemma $A_v = -G_m R_{out}$. Assume that the circuit drives a load resistance of R_L and $\lambda,\ \gamma > 0$.