UNIVERSITY OF WASHINGTON
ELECTRICAL ENGINEERING

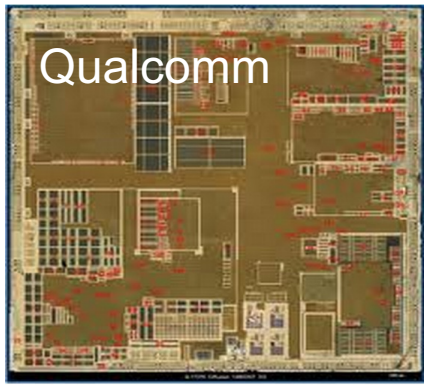
Lecture 1: Introduction

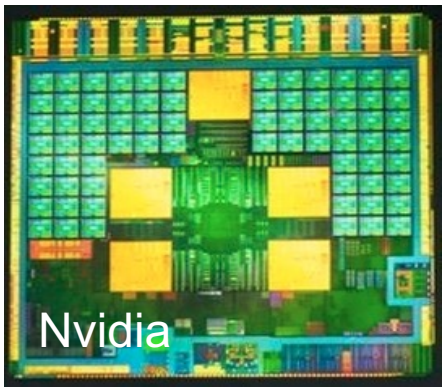
VLSI-0: Introduction to VLSI Systems

Diego Peña-Colaiocco

Based on material prepared by prof. Visvesh S. Sathe

A first-step into the world of IC design





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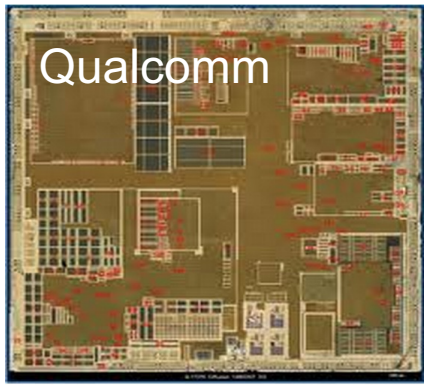

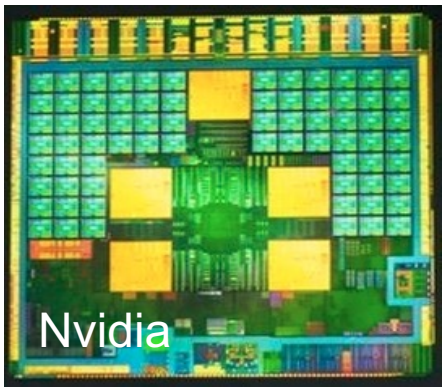

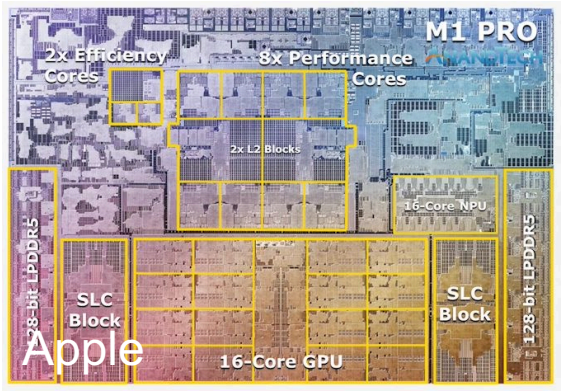

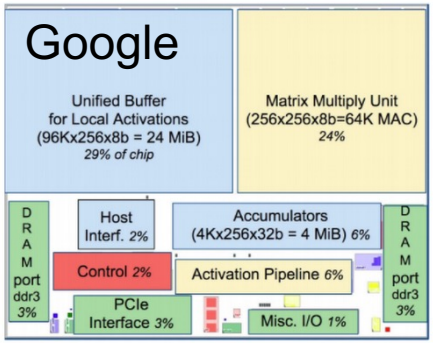

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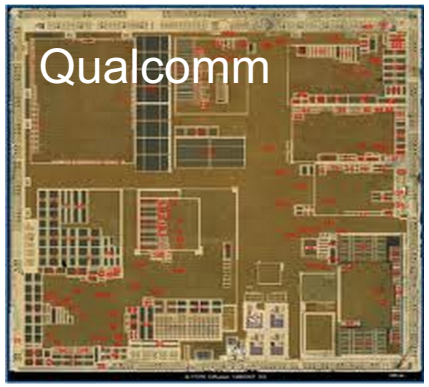
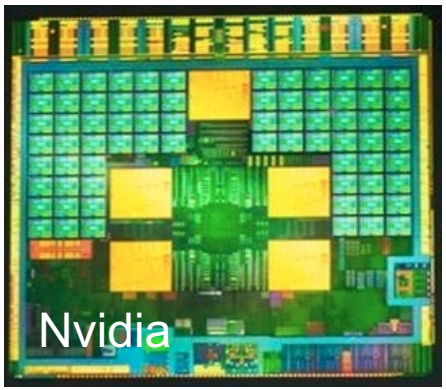
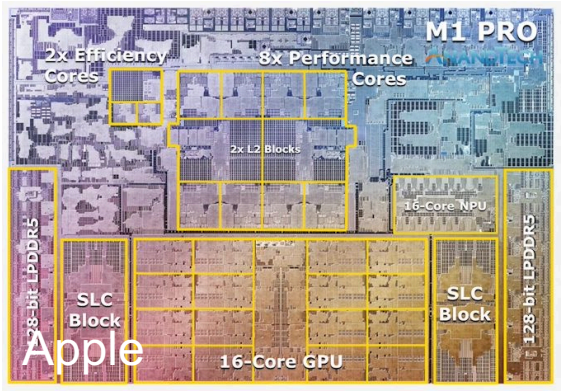
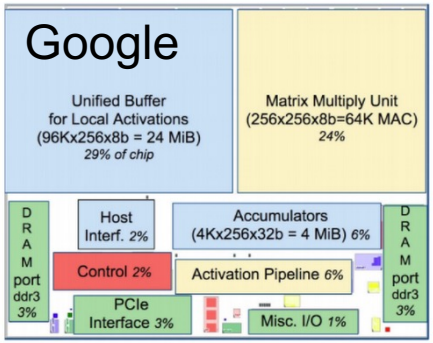
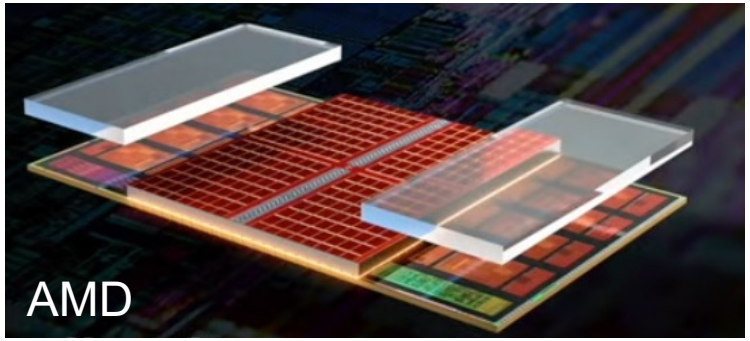
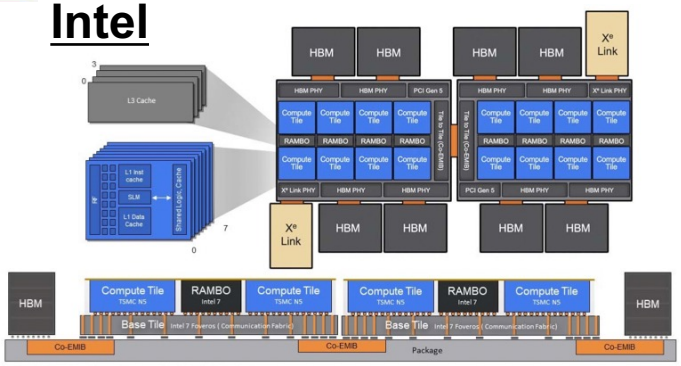


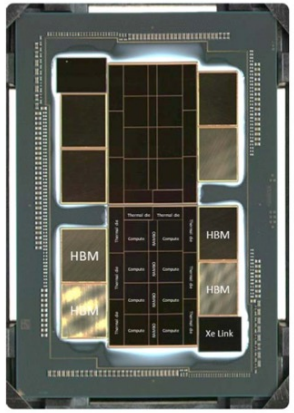












Acknowledgements

All class materials (lectures, assignments, etc.) based on material prepared by Prof. Visvesh S. Sathe, and reproduced with his permission

Visvesh S. Sathe
Associate Professor
Georgia Institute of Technology
https://psylab.ece.uw.edu

UW (2013-2022)
GaTech (2022-present)

Who is this class for?

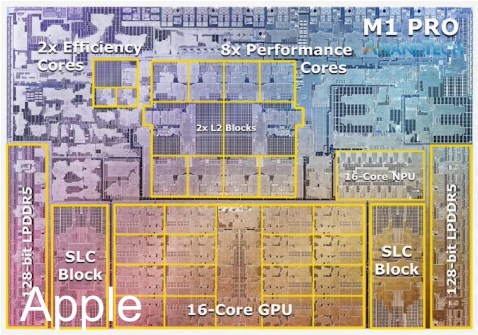
- Anyone interested in integrated circuits!
  - RTL, custom digital, mixed signal, analog, computer architecture, etc.
- What to expect of the next quarter? The next year?

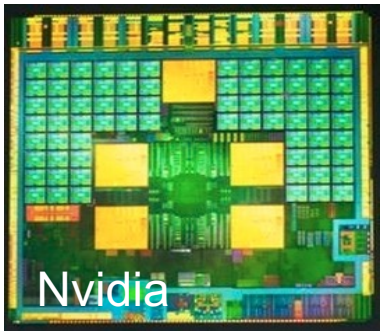
Course Objectives

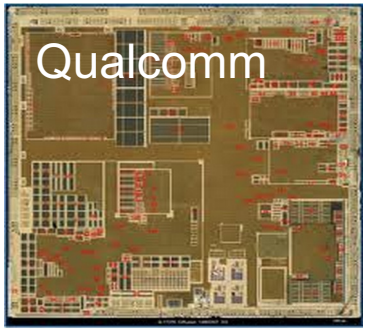
- Understand the **basics** of designing digital CMOS ICs
  - The MOS transistor
    - Levels of abstraction
    - Basic fabrication process (Going from a mask design to working silicon)
  - CMOS logic design: The building blocks of complex systems
    - Key characteristics of CMOS logic gates (Power, delay, noise immunity etc.)
    - Mask layout (Preparing a design for manufacturing)
  - Common VLSI structures (Datapath, Memory)
- "Breadth-First" approach to understanding of how digital systems are implemented as efficient CMOS ICs
  - Digital circuit design
  - Pipelining and parallel processing
  - Timing
  - Simulation and verification
  - Datapath and memory elements
  - Broader design principles (Hierarchy, modularity, regularity, managing scale)

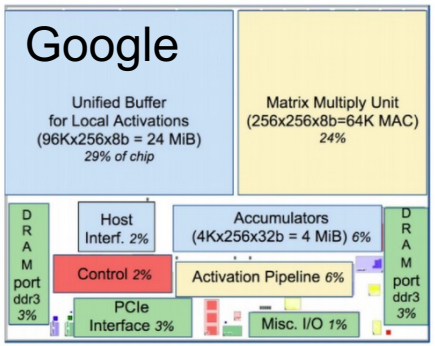
Objectives (contd.)

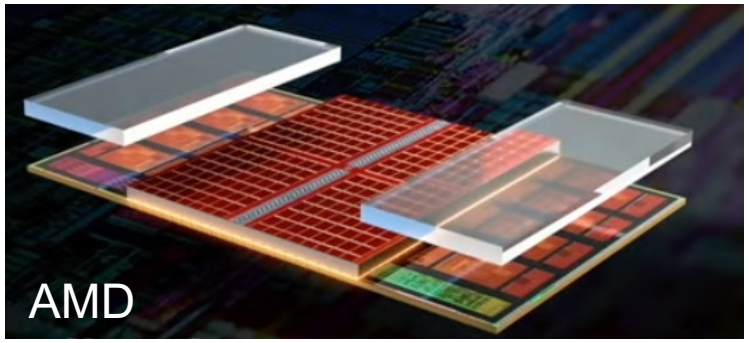
- Focus will be on
  - Equipping you to understand, analyze and design VLSI systems
  - Building a foundation toward a real VLSI design experience (EE477, EE526)
- A first-step into the world of IC design

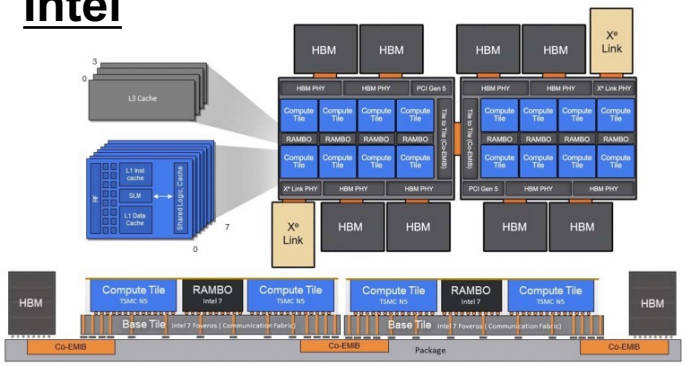


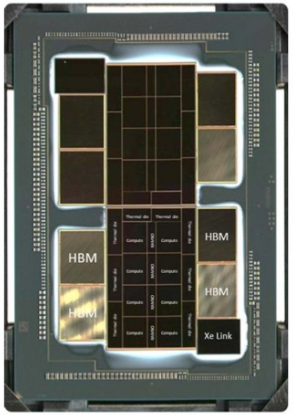










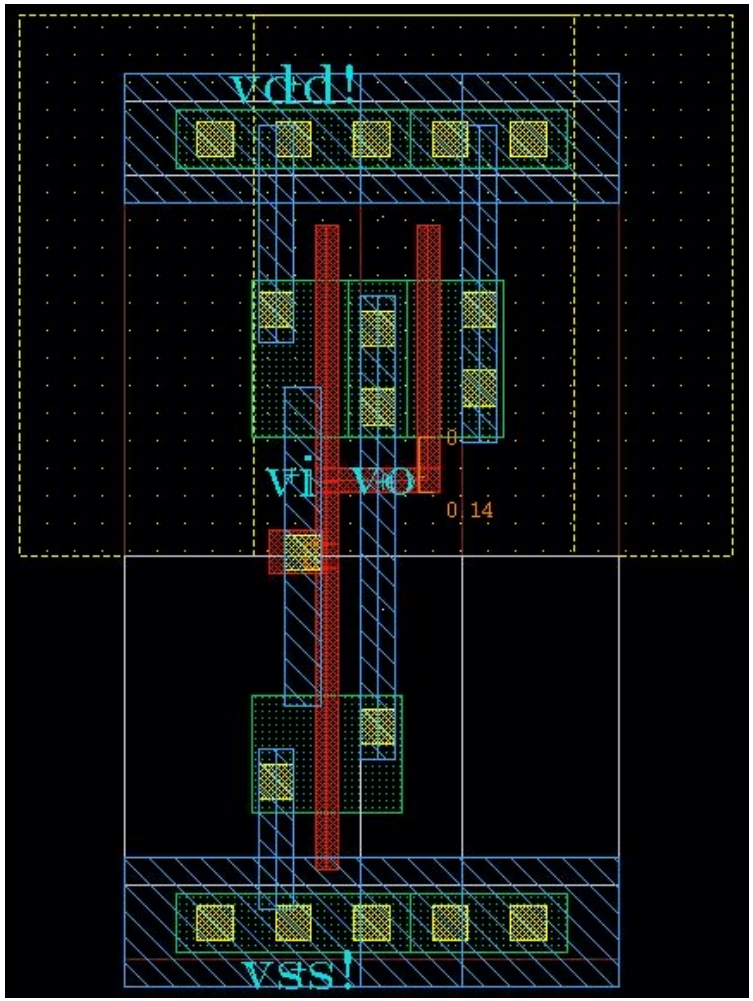


Objectives (contd.)

- This course is **not**
  - Going to make up for earlier basic circuit theory classes (I'm assuming you've learned what you needed to learn there.)
  - A course on MOSFET theory (We will use only the most basic MOSFET model)
  - A course on detailed VLSI design

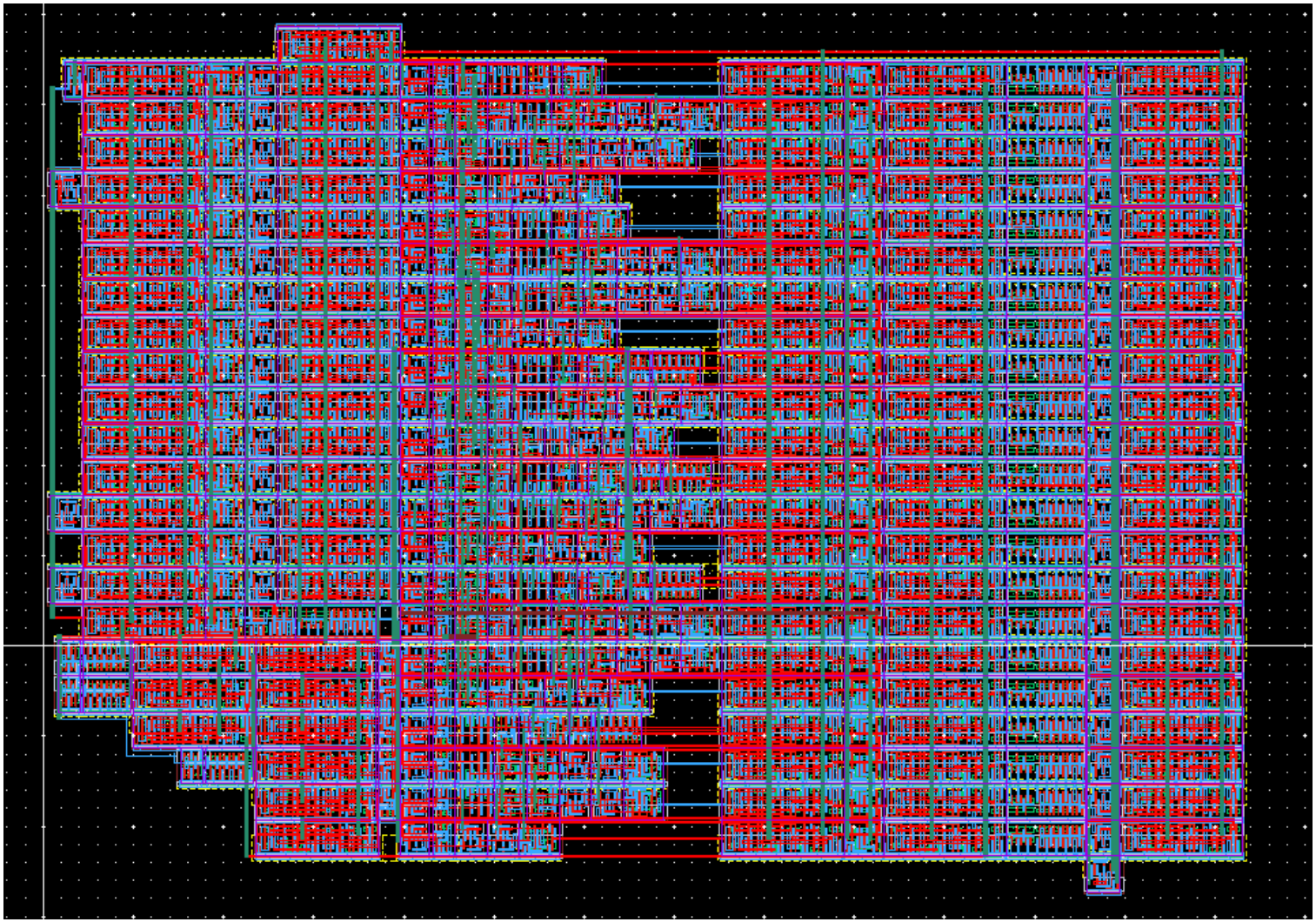
- This course is
  - A first view into VLSI design
  - Some MOSFET, some transistor level design, some managing of complexity
  - A reasonable amount of work compared to earlier 476 offerings
    - Somewhat less than last year offering ☺

Now and Then…



- One week from now

Now and Then …



- 10 weeks from now…

Assignments, CAD assignments and Homework

- Homework due each week (6 weeks): **Not required. Not graded**
  - Related to material in lecture, reading assignments and midterms
  - Solutions are provided
  - These are useful only if you take the time to look through them individually or in groups

- 4 CAD assignments + 2 mini projects
  - Design assignments
  - *Due on Fridays at 2am*
  - Performed using provided standard design flow
  - Will be time consuming (especially in the beginning)
  - **Tip: The better you are at CAD tools now, the more time you'll save later**
  - Refer to canvas page for due dates

- 2 mini-projects
  - Regfile
  - Datapath (sch-only)
  - Final presentation, privately with course staff

Grade breakdown

- CADs 0, 1 and 2: 10%
- CAD 3: 10%
- CAD 4: 10%
- Mini project 1: 20%
- Mini project 2 and final presentation: 30%
- Midterm: 10%
- Final Exam: 10%

CAD assignment flow

- Allocate enough time (coming from experience)
- Form study groups
- TAs will grade based on measurements + design quality

- First 10 students to volunteer to use HYAK will get a 0.2 grade bonus (out of 4.0)

Week No.	Lecture (Led by Instructor)	Disc. Session (TAs, Instructor)	CAD
0	Introduction	CMOS Logic (Lecture)	Linux Overview (Optional)
1	MOS devices, Basic Fabrication	Tutorial walkthrough	0: Tutorial
2	Basic Fabrication, Inverter (DC Characteristics, Delay)	Spice I/Silicon-Explorer	1: Inverter
3	Timing-element Design	Timing Element Design	2: Nand/RO
4	**TA_Lecture (**Layout Tips and Tricks, Inverter overview and live-demo). LFSR/Signature Analyzer	Inverter Sizing/Power	3: Flip flop, LFSR, **Group formation**
5	Inverter sizing and power, Regfile Design	Design Planning	
6	CMOS Scaling , Pipelining		4: RegFile
7	Memory Structures, Adders	Spice II	5: ROM (sch) (SOLO)
8			
9	Low power design: An introduction	Track-planning	6: Datapath (sch)
10	Project Delivery, Final		
11	**Get back to your other classes ☺**		

- EE476 is a lot of work
  - **Design is a practitioner's art**, but grounded in basic circuits and logic principles => We'll be learning and doing at the same time
  - We are aware – the workload is not reasonable and we're not proud of it
  - Course is hard not by intent but by consequence
  - Please don't take 3 courses this quarter if you are taking EE476
  - EE476 is not a class you want to be stuck in mid-quarter
- Attending lectures live is recommended but **NOT required**
  - Please stay home if you're not feeling well
  - Lectures will be recorded and made available on canvas

Course Philosophy

> "I Hear and I Forget, I **See** and I Remember,
> I **Do** and I **Understand**"

- Where you are and where you need to get to
  - Course is hard not by intent but by consequence
  - Lots to cover -> we cannot just do theory and firming through practice. Get out of your comfort zone and you'll be doing a bit of learning by practice already.
- Fundamentally different from any class most have taken
  - Learning by design
  - You will learn from your peers and teams and actually do

- **<u>The goal is to NOT weed out students</u>** but to enable them to be successful in this class, and eventually engineering leaders who know how to build complicated systems that will work
- This course is not intellectually taxing, but is drinking from a firehose. It will be deeply unsettling for some. At first.

Logistics…

- Friday lecture slot
  - TA-led discussion session AND/OR Lecture/Q&A driven by us jointly AND/OR make-up lecture if we're running behind
  - Discussion session will complement course material
    - Unix, schematic/layout design
    - SPICE simulation
    - Good design practices
    - Scripting

- Reading assignments (Textbook: West and Harris 4th edition)
  - Given at the end of each lecture. **For your benefit, read these before coming to the class** (Much more efficient use of your time)
  - Optional reading will **never** appear on any graded material **BUT** highly recommended if you want to proceed to take 477, 526

  - Additional reference: S. Kang and Y. Leblebici. "CMOS Digital Integrated Circuits." McGraw-Hill Education (2003).

…and more Logistics….

- Office hours
  - Instructor office hours during the week (total 3 hours)
    - Online or in person (ECE 253 F)
    - 1.5 hours drop-in slot
    - 1.5 hours by booking only
  - TA office hours (total 3 hours)
    - 2 hours in Linux labs
    - 1 hour online, by booking only
  - Course staff might take 24 hours or more to answer your emails
  - Logistics on Linux labs to be announced

- Class communication through MS Teams

…and more Logistics….

- All computer access must happen on either the main linux server, the linux lab machines, or hyak
  - E.g. ssh linuxsrv01.ece.uw.edu or
  - ssh linux-lab-001.ece.uw.edu (for machine number 1. You have machines 001 to 040)
- Anatomy of a lecture ***(from previous years)***
  - Q&A (CAD/Assignment/Prior-lecture) – 20m
  - Break – 5m
  - Lecture (part 1) – 35m
  - Break – 5m
  - Lecture (part 2) – 35m
  - Q&A and/or worked examples – 10m

…Seriously?? is there going to be any learning today?

- Will be using FreePDK 45nm for the assignments

- **You must have an EE account**
  - If you don't have it, get it **TODAY**
  - Used to create your linux directory, where you'll be doing all your work. (They were created yesterday, reach out to us if you can't find it)

Course grading and late policy

- Late policy:
  - You **MUST***** inform the TA by email that you are late (Overcommunicate!)
    - Else he will grade you for what you have
    - Lose 10% of the **residual** credit for every 6-hour late window.
    - Late delivery of project. Same as above, but hard stop at grade-delivery deadline
- Grading policy
  - CAD Assignments (30%)
  - Midterm and final (20%)
  - Mini-project 1 (20%)
  - Mini-project 2 (30%)
- Grading on a curve (Mean shifts based on overall class performance)
- Bonus problems/design tasks
  - 0.2 extra in the awarded grade per 1 bonus credit (fractions apply)
  - Calculation done **after** all grades are assigned based on curve
  - Not doing them will **not** hurt the awarded grade
  - E.g. If you accumulate 0.4 bonus credits. I'll add 0.08 to your awarded grade and round-off (you get a 0.1 bump in this case)

Course grading (new)

- If you submit at least one week early, the TA will grade you by next Tuesday, with feedback, and you're allowed to resubmit.
  - Will only provide grades and feedback on complete CADs (maybe completed tasks as well, TBD)

Get Good with Tools ….

- VL**S**I - Tools play a crucial role
  - The 80%-20% corollary ….
- Tool-flow in 476
  - Design Schematic Entry – Cadence Virtouso
  - Design Simulation – Hspice (Synopsys)
  - Design Mask-Layout – Cadence Virtuoso
  - LVS/DRC – Calibre (Mentor) but integrated within Virtuoso environment
  - Parasitic Extraction – xRC (Mentor) but within Virtuoso environment
- Other required skills
  - Working knowledge of Unix (dir navigation, .cshrc). If you're new to Unix/Linux, **spend the time on a tutorial**
  - Text editor : vi, emacs, sublimetext (gedit if you **absolutely** must)
- Very highly recommended
  - Scripting (Python, Perl)

…. So you have more time to Think

- HSpice
  - Spend the time to learn how to control and implement simulations
  - sweeps/measure_statements/parameter definitions/patterns
  - Be productive with the waveform viewer

- Use resources to use the tools well .. Don’t just get by
  - Canvas
  - Panopto (recordings on Canvas) : Lots of helpful short-cuts
  - User-guides (available in the course-directory on canvas)
  - Stack-overflow
  - Your TA, Instructor (last line of defence)
  - Youtube

Assignments (Reading, CAD, Homework)

- We are in week 0 …
- Reading assignment 1: Text. 1.1-1.4
- Optional reading assignment 1: Text. 1.6, 1.8

- 0.1 bonus credits for every bug
- Kevin must acknowledge as significant bug. First reporter takes all…
  - If you report misplet text, you get our sincere thanks but not points

We're Almost Done….Last Comments

Course Eval'19

SUMMATIVE ITEMS

	N	Excellent (5)	Very Good (4)	Good (3)	Fair (2)	Poor (1)	Very Poor (0)	Median	Adjusted Median
The course as a whole was:	17	65%	35%					4.7	4.4
The course content was:	17	65%	35%					4.7	4.4
The instructor's contribution to the course was:	17	71%	24%	6%				4.8	4.5
The instructor's effectiveness in teaching the subject matter was:	17	71%	24%	6%				4.8	4.5

STUDENT ENGAGEMENT

Relative to other college courses you have taken:	N	Much Higher (7)	(6)	(5)	Average (4)	(3)	(2)	Much Lower (1)	Median
Do you expect your grade in this course to be:	17	18%	59%	12%	12%				6.0
The intellectual challenge presented was:	17	53%	35%	6%	6%				6.6
The amount of effort you put into this course was:	17	82%	18%						6.9
The amount of effort to succeed in this course was:	17	82%	12%	6%					6.9
Your involvement in course (doing assignments, attending classes, etc.) was:	17	76%	24%						6.8

On average, how many hours per week have you spent on this course, including attending classes, doing readings, reviewing notes, writing papers and any other course related work?

Class median: 22.0 Hours per credit: 4.4 (N=17)

Under 2	2-3	4-5	6-7	8-9	10-11	12-13	14-15	16-17	18-19	20-21	22 or more
							12%		12%	12%	65%

From the total average hours above, how many do you consider were valuable in advancing your education?

Class median: 18.0 Hours per credit: 3.6 (N=17)

Under 2	2-3	4-5	6-7	8-9	10-11	12-13	14-15	16-17	18-19	20-21	22 or more
		6%			6%	6%	29%		12%	12%	29%

What grade do you expect in this course?

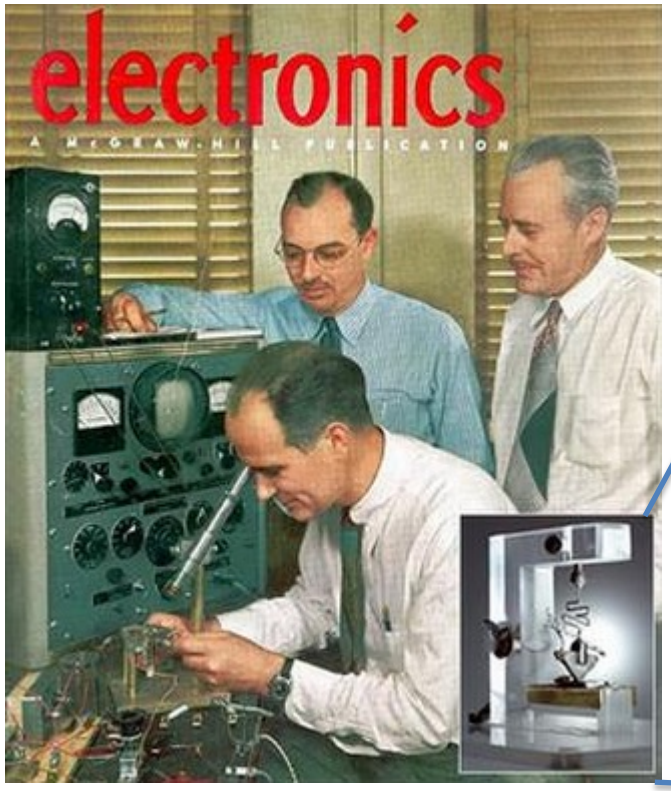
Class median: 3.7 (N=17)

A (3.9-4.0)	A- (3.5-3.8)	B+ (3.2-3.4)	B (2.9-3.1)	B- (2.5-2.8)	C+ (2.2-2.4)	C (1.9-2.1)	C- (1.5-1.8)	D+ (1.2-1.4)	D (0.9-1.1)	D- (0.7-0.8)	F (0.0)	Pass	Credit	No Credit
24%	65%	6%	6%											

- This course will take up a lot of your time – not the class to be stuck in
- Being a good peer, teammate matters. Immensely.

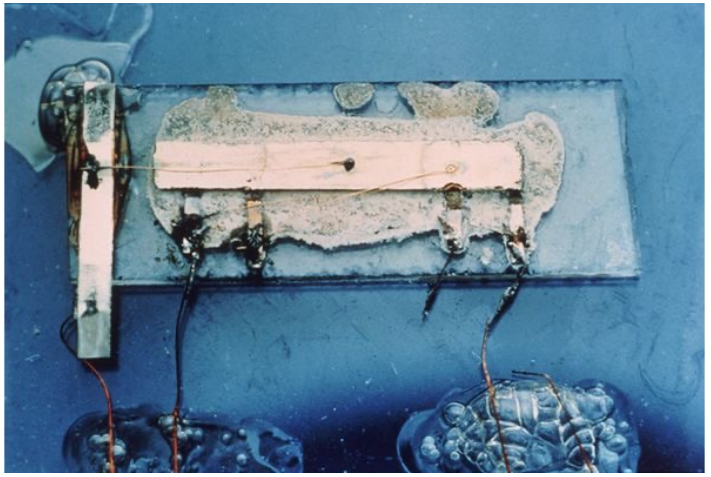
VLSI Design – A look back

- Invention of the Transistor in 1947 (Bardeen, Brattain, Shockley)
- Nobel Prize (1956)
- Point contact transistor



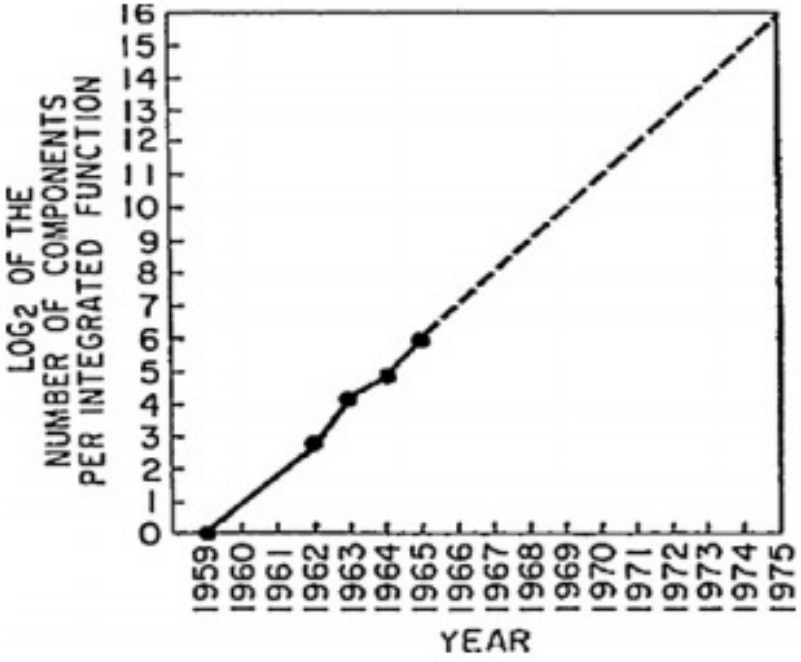
Advances in integration

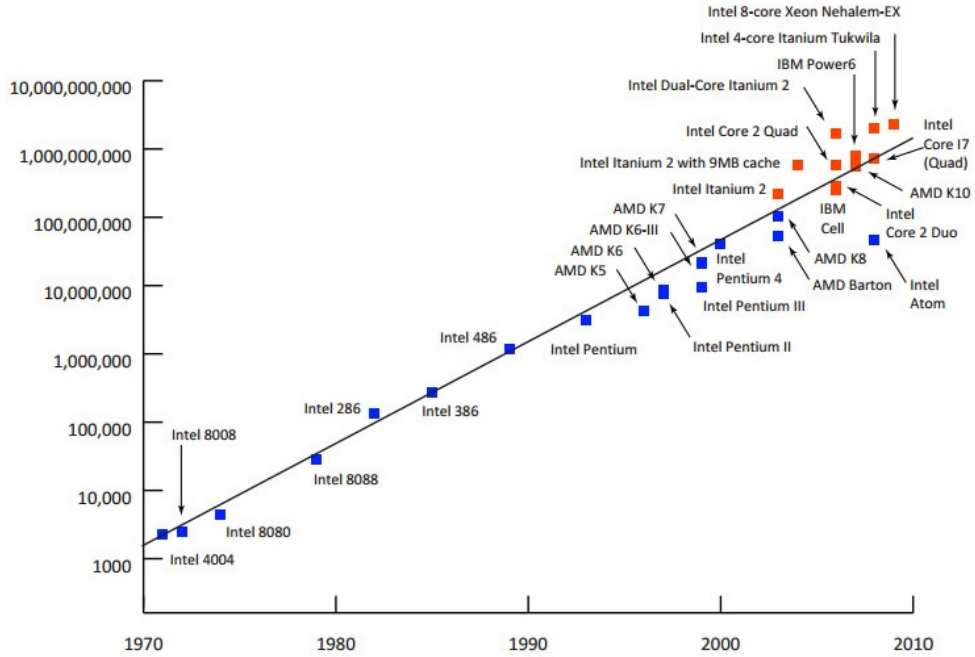
- 1958 - Jack Kilby built the first integrated circuit at Texas Instruments
  - Two transistor flip-flop
  - Integrated Tx, R and C (**Wires not integrated**)
  - Nobel Prize (2000)



The first integrated circuit (2 tx)

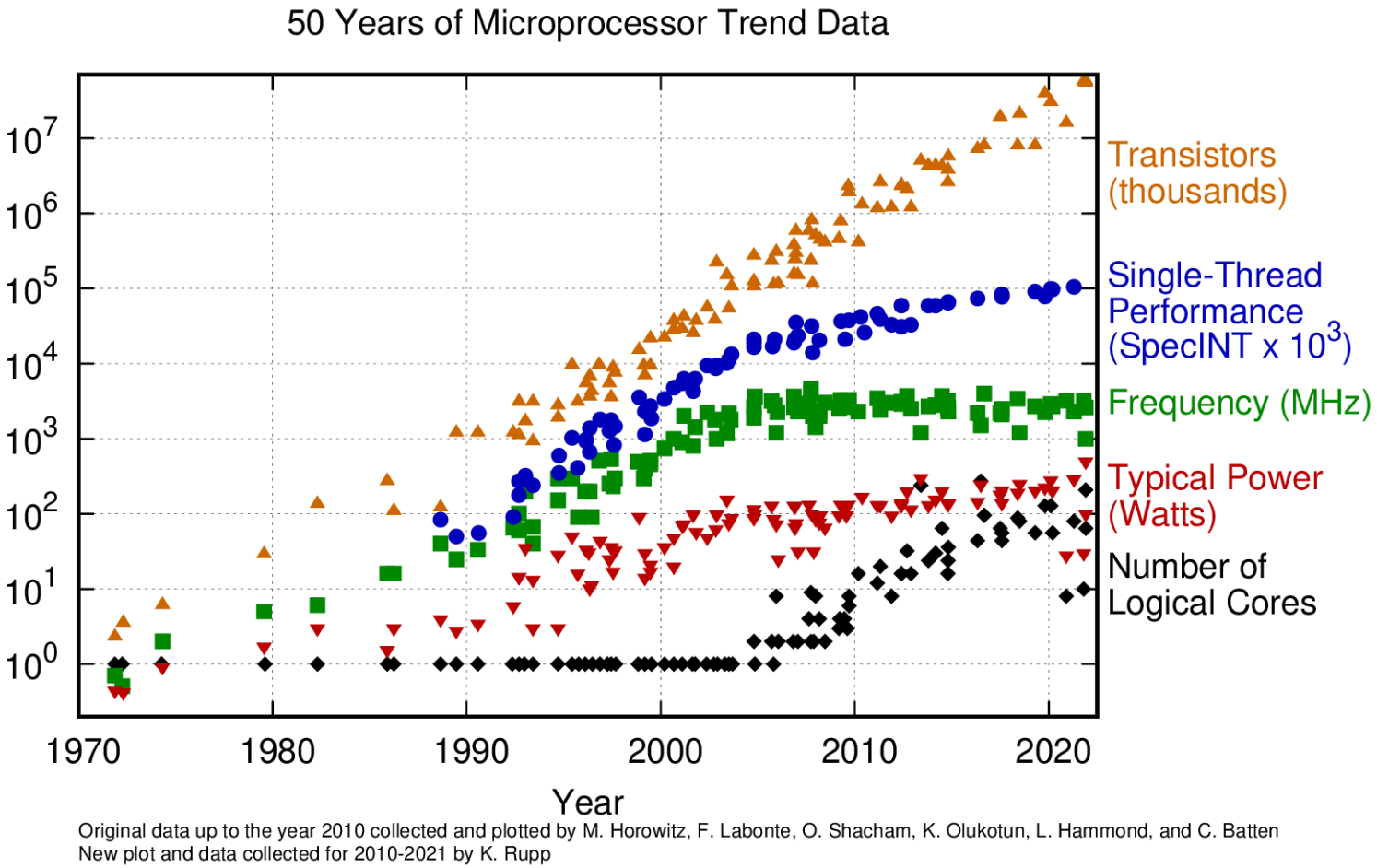
Moore's law*





- Transistor **count** on integrated circuits will double every 18 months
- In large part, drove progress in computational performance over the past 4 decades (Historically, ~10x every 5 years)

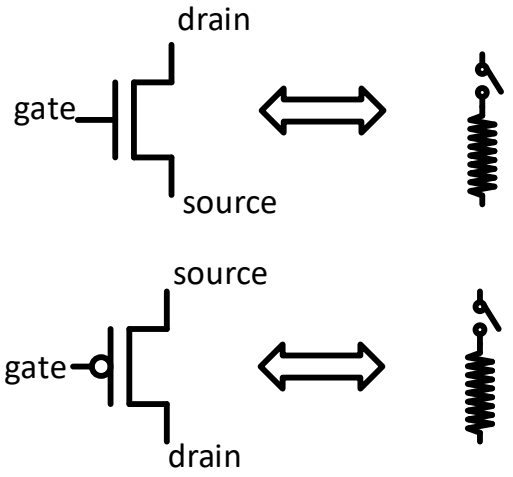
* Not to be confused with Dennard's law



- Taken from https://github.com/karlrupp/microprocessor-trend-data

The MOS transistor abstraction

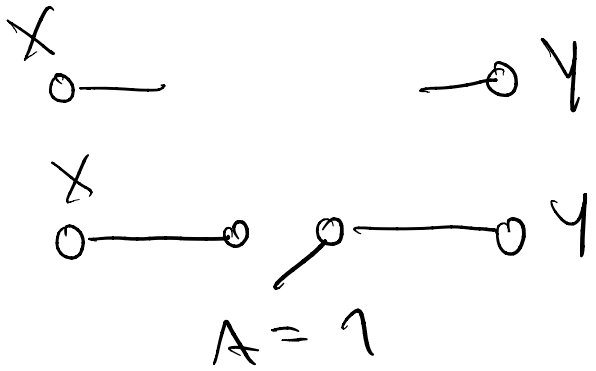
- Programmable switch: 3-terminals
  - Drain: “Destination” of charge carriers of controllable switch
  - Source : Source of charge carriers of controllable switch
  - Gate : “Controlling” terminal. Decides whether the switch conducts between Source and Drain
- Operation
  - “Resistive Switch” View
    - NMOS: If $V_{gate} > (V_{drain}$ or $V_{source}) \rightarrow$ Switch conducts
    - PMOS : If $V_{gate} < (V_{drain}$ or $V_{source}) \rightarrow$ Switch conducts



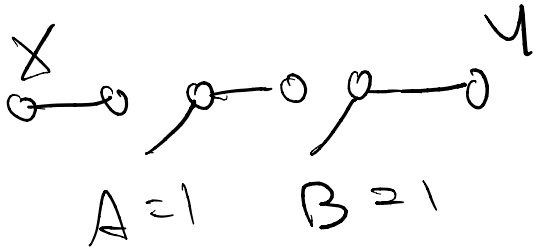
Using switches as relays (Break-out)

- Given inputs A and B, and 2 points X, Y. Connect X, Y subject to:
  - A & B
  - A | B
  - $\bar{A}$ & $\bar{B}$
  - (A&B)|(C&D)
  - $\overline{((A\&B)|(C\&D))}$

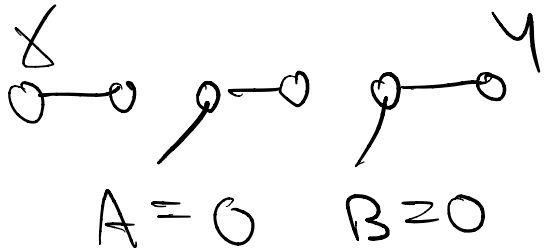
1) A :



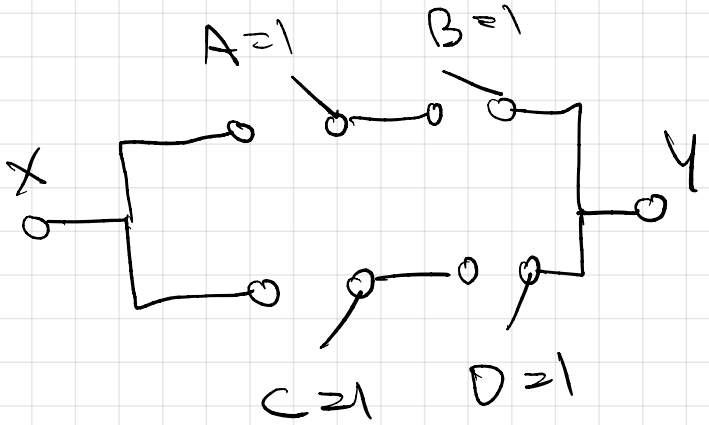
2) A & B



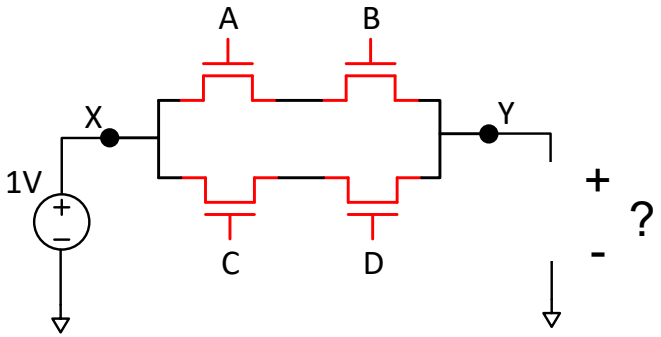
3) $\bar{A}$ & $\bar{B}$



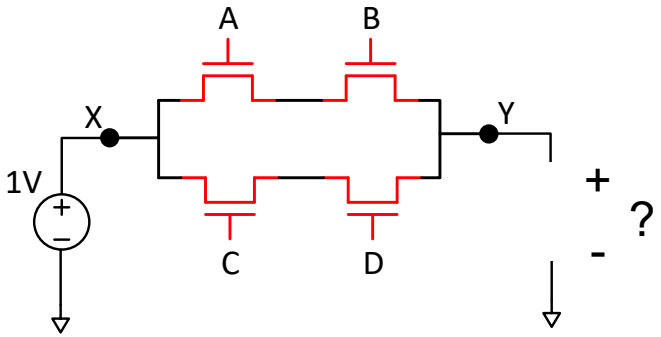
4) (A & B) || (C & D)



Short Aside: Current Flow in Relay Networks

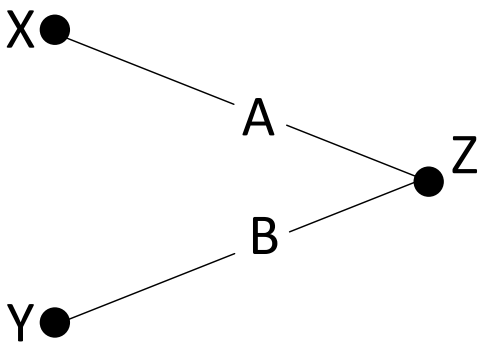


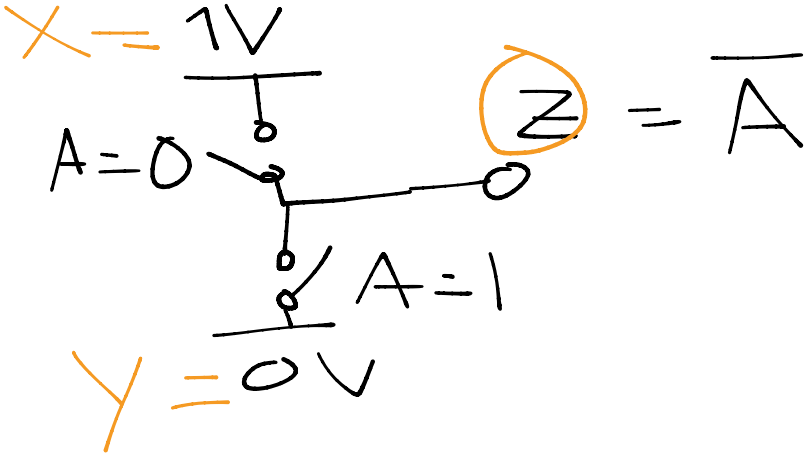
Short Aside: Current Flow in Relay Networks



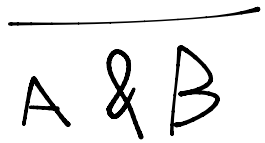
What happens if X→0
After charging Y?

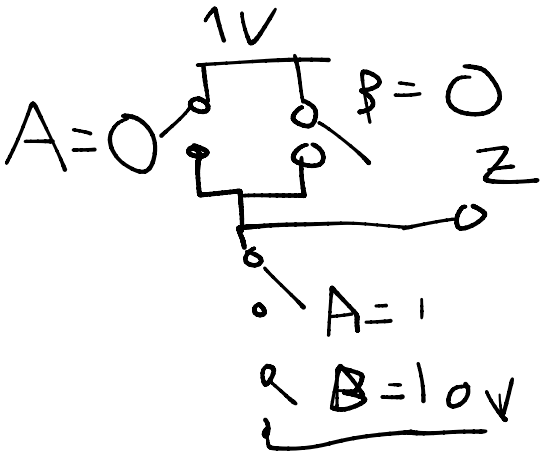
Connecting Multiple Evaluation Trees





- Build a network with the following properties
  - 3 nodes: X,Y,Z ; 2 inputs: A, B
  - Connect X to Z if (A==1)
  - Connect Y to Z if (B==1)

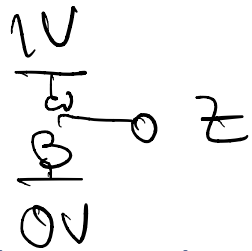


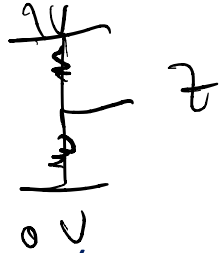


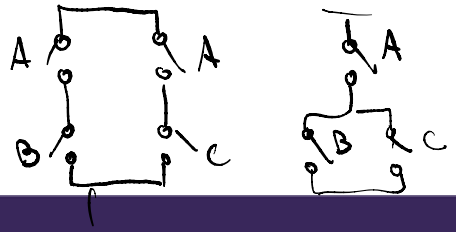
Implementing Boolean Functions

- Connection between points is nice….
- ….But how do I translate it to implementing logical functions?

- Boolean Functions: $Z = f(X_1, X_2, X_3, \ldots X_n)$, $X_i = 0|1$
- One possible implementation:
  - For each combination of $X_1, X_2, X_3, \ldots X_n$ s.t Z=1, "connect Z to V_{dd}" (Logic 1)
  - For each of the remaining combinations, "connect Z to 0" (Logic 0)
  - Possibility of contention?
  - Number of trees = 2^n
- Two observations:
  - CMOS gates are not implemented with more than 3-4 inputs (more on this later in the course)
  - Factoring of prime-implicants simplifies topologies







$AB + AC$

$= A(B + C)$

Reading Assignment

- Section 1.1-1.4 (Cmos logic)
- Optional 1.6, 1.8, 2.1-2.3