CAD 3: Ring Oscillator

EE 476 | University of Washington

Notes

1. Use a 1.4um height (height from the top edge of the top contact row, to the top edge of the bottom contact row) for all cells. The 1.4um cell height should be used for all future CAD's as well.

2. Unless stated otherwise, assume a `VDD` of 1.2 V.

3. From this CAD on, assume input signals are ideal, unless otherwise stated.

Setup

Use the same general directory structure as in CAD 1 and CAD 2, review *Tutorial 1* for details.

CAD 3 Overview

In this CAD assignment, students will build and characterize several ring oscillators[1]. Part 1 involves the creation and test of a NAND gate, which can then be reused in the ring oscillator designs (Parts 4-6). The regularity of the ring oscillator structure creates the opportunity for more design reuse, and this CAD introduces the importance of hierarchical designs. Students will also experiment with gate sizing, as well as supply voltage levels, and observe the effects on ring oscillator operating frequency. Besides the above, students continue to build competence with HSPICE, Cadence Virtuoso and other standard industry tools.

[1] https://en.wikipedia.org/wiki/Ring_oscillator

1 NAND Schematic Design and Test

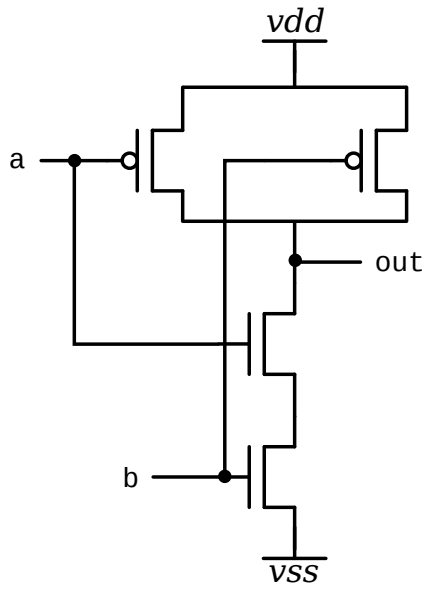

Figure 1

a. Create the schematic for the two-input NAND in Figure 1, and use the NAND to build the circuit in Figure 2; for this Part, use 50nm / 250nm for the PMOS devices and 50nm / 300nm for the NMOS devices. Call the NAND sub-circuit `NAND2` in Figure 1, and the circuit in Figure 2 `loaded_nand`. **Please name the NMOS instances `NMOS0` and `NMOS1`, and the PMOS instances `PMOS0` and `PMOS1`** (order is not important). To do this, select the transistor or instance in question, hit 'q', and change the name in the field "Instance Name". Similarly, name the NAND gate that is directly connected to the `a`, `b` and `z` pins `DUT`[2].

When designing your schematic, remember that all NMOS devices are fabricated on the same p-type substrate. Therefore, they will all share one body connection. The NMOS body voltage should be tied to the lowest voltage your circuit will see: `VSS`. Similarly, all PMOS devices should have their body connected to `VDD`.

[2]This makes it easy for you, and the grader, to measure current through individual transistors

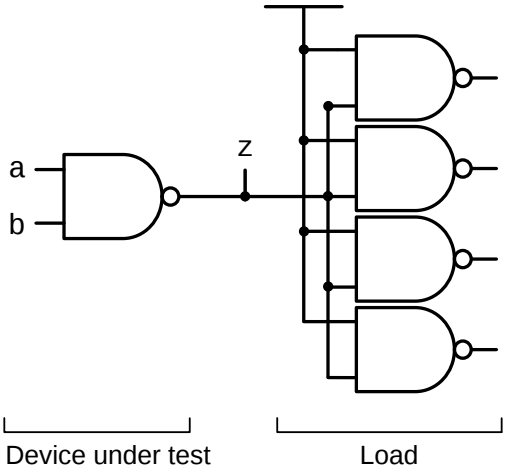

Figure 2: The NAND is used for both the device under test, and the load.

b. Collect the measurements listed in Table 1 for the `loaded_nand` circuit. For generating output transitions to take measurements on, and for the input capacitance measurements, tie the `a` input high and toggle the `b` input. For instance, to generate the transition $(z = 0) \rightarrow (z = vdd)$ the input pattern would look like $(a = vdd, b = vdd) \rightarrow (a = vdd, b = 0)$. Energy measurements should only include energy consumed directly by the device-under-test (DUT).

Measurement	**Description**
`rise_delay`	Rise delay, 50% to 50% (a.k.a. propagation delay low-to-high)
`fall_delay`	Fall delay, 50% to 50% (a.k.a. propagation delay high-to-low)
`rise_time`	Rise time, 20% to 80%
`fall_time`	Fall time, 20% to 80%
`rise_en_dissip`	Energy consumed by a low-to-high output transition
`fall_en_dissip`	Energy consumed by a high-to-low output transition
`input_cap`	Input capacitance **on the `b` pin** of the `loaded_nand` circuit
`output_cap`	Output capacitance **on the `z` pin** of the `loaded_nand` circuit

Table 1

Delivery

a.-b. The schematic netlist for `loaded_nand`, and the measurements in Table 1

2 NAND Layout (and Test)

a. Create the layout for the `loaded_nand` circuit in Part 1. To do this, create the layout for the `NAND2` cell first, making sure that the cell can be tiled without violating DRC rules. During the subsequent layout of the `loaded_nand`, make sure to create *instances* of the NAND gate layout - not copies (use the 'i' key to insert instances while in layout view). Note: Since we are reusing the `NAND2` layout for a larger design, you can remove the welltap then place it again when the layout of the `loaded_nand` is complete.

b. Collect the same measurements as in Part 1, but for the post-layout `loaded_nand`. For the parasitics extraction, use `C+CC`.

Delivery

a. The netlist for the post-layout `loaded_nand`, and the generated DRC/LVS reports

b. The corresponding measurements from Table 1

3 NAND Circuit Tuning

Since the drive strength of NMOS and PMOS devices is intrinsically different (NMOS having greater charge-carrier mobility), one might expect the PMOS to be slower by the NMOS by some factor close to β. However, since the NMOS is in series, the difference in rise time and fall time may not be pronounced as expected.

a. Create a copy of the `NAND2` design from Part 1, and call it `NAND2_balanced`. Modify the width of the PMOS devices to make the rise time and fall time equal to within 15% difference. Only balance the `NAND2` gate at the schematic level - don't redo the layout.

When balancing, assume no output load and worst-case transitions. e.g. the worst-case rise time will be when only one PMOS device is active, so balance that case versus the worst-case fall time.

Delivery

a. The schematic netlist for `NAND2_balanced` (no measurements needed)

4 Ring Oscillator Schematic

a. Create the schematic for the ring oscillator design in Figure 3, named `ring_osc`. For the inverter and NAND, use the `INVD1` cell from CAD 2 (copy over from CAD 2 to keep the design files between CAD's independent), and the `NAND2` from Parts 1 and 2 of this CAD.

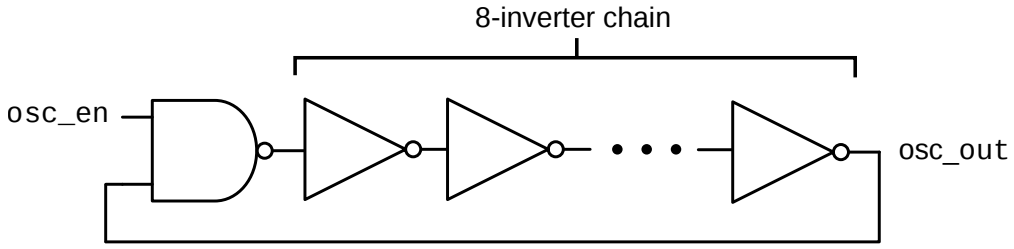

Figure 3

b. Collect the measurements in Table 2 for the ring oscillator schematic. The average power consumption should be measured over the 4ns immediately after `osc_en` transitions to logic '1'. The power measurement should be taken over the entirety of Figure 3 (i.e. it should include the sum of power consumed by both the NAND gate and all 8 inverters).

Measurement	**Description**
`osc_freq`	Oscillation frequency
`avg_pow`	Average power consumption

Table 2

Delivery

a.-b. The schematic netlist for `ring_osc`, and the measurements from Table 2

5 Ring Oscillator Layout

a. Complete the layout for the ring oscillator from Part 4. As with the `loaded_nand`, make sure to use instances, and promote hierarchy. Students are encouraged to create additional levels of hierarchy so long as the name and pins of the top-level design are not affected.

b. Repeat the measurements from Table 2 for the post-layout ring oscillator.

Delivery

a. The post-layout netlist for `ring_osc`, and DRC/LVS reports

b. The measurements from Table 2 for the post-layout netlist

6 Double-width Ring Oscillator Schematic

a. Create a copy of the ring-oscillator schematic called `ring_osc_2x`, and modify the copy such that all transistors are double the widths of those in the original `ring_osc`. Collect the same measurements for frequency and power (Table 2) for this modified schematic. Do not redo your ring oscillator layout.

Delivery

a. The schematic netlist for `ring_osc_2x`, and the corresponding measurements from Table 2

7 Additional Questions

a. For the `ring_osc` schematic, `ring_osc` layout, and `ring_osc_2x` schematic, generate plots for oscillation frequency v.s. VDD, for VDD $\in [0.7\text{V}, 1.2\text{V}]$. The granularity of the curves is not important, but if done "correctly" in HSPICE there should be no difference between generating 5 points and 50 points.

b. Identify at least 2 reasons for differences between the frequency v.s. VDD curves collected above.

Delivery

a.-b. Nothing (questions should be answered in the report)

File Submission

Plots and answers to questions should be submitted in a report named `cad3_report.pdf`. Measurements should be submitted using the provided `specifications.json` file, and files should be in the specified locations (see the *CAD Submission* document for more information).