

E E 476 – Introduction to VLSI Design  
 Mid-term examination  
 November 4<sup>th</sup>, 2022

I have not received nor obtained help from anyone in the completion of this examination. During the course of this mid-term examination, I have not engaged with any form of communication with my peers on any aspect of the contents of this exam. I understand that strict action will be taken resulting from my failure to comply with the mid-term examination policy. I also understand that it is my duty to not only adhere to the mid-term exam policy, but also report any other individual(s) who are violating this policy.

Name: \_\_\_\_\_

Signature: \_\_\_\_\_

**The use of notes, calculators, or any electronic devices is not allowed during this midterm examination.**

Duration: 50 minutes

Assume that all devices have 0 leakage current. Unless otherwise stated, the following default parameters apply:

$V_{dd}$	1.2 V	$C_{ox} = \frac{\epsilon_r \cdot \epsilon_0}{t_{ox}} = 0.01 \text{ F/m}^2$  $\mu_n \cdot C_{ox} = 0.5 \text{ mA}$ $\mu_p \cdot C_{ox} = 0.25 \text{ mA}$  $\mu_n \cdot C_{ox} \cdot \frac{W_n}{L} = 10 \text{ mA}$ $\mu_p \cdot C_{ox} \cdot \frac{W_p}{L} = 10 \text{ mA}$
$\epsilon_r$ (Silicon-di-oxide)	3.8	
$\epsilon_0$	$8.85 \cdot 10^{-12} \text{ F/m}$	
$\lambda$	0	
$t_{ox}$	$33.63 \text{ A} = 3.363 \text{ nm}$	
$\mu_n$	$500 \text{ cm}^2/\text{V}$	
$\mu_p$	$250 \text{ cm}^2/\text{V}$	
$V_{th,n} = V_{th,p} = V_{th}$	0.2 V	
$W_n$	1 $\mu\text{m}$	
$W_p$	2 $\mu\text{m}$	
Beta ratio = $\frac{\mu_n}{\mu_p}$	2	
$L_n = L_p = L$	50 nm	

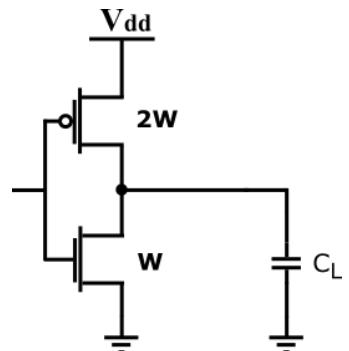
### NMOS transistor:

Cut-off	$V_{GS} \leq V_{th}$	$I_D = 0$
Linear/Triode	$V_{GS} > V_{th}$ and $V_{DS} \leq V_{GS} - V_{th}$	$I_D = \mu_n \cdot C_{ox} \cdot \frac{W_n}{L} \left[ (V_{GS} - V_{th}) \cdot V_{DS} - \frac{1}{2} V_{DS}^2 \right]$
Saturation	$V_{GS} > V_{th}$ and $V_{DS} > V_{GS} - V_{th}$	$I_D = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W_n}{L} (V_{GS} - V_{th})^2 (1 + \lambda \cdot V_{DS})$

### PMOS transistor:

Cut-off	$V_{SG} \leq V_{th}$	$I_D = 0$
Linear/Triode	$V_{SG} > V_{th}$ and $V_{SD} \leq V_{SG} - V_{th}$	$I_D = \mu_p \cdot C_{ox} \cdot \frac{W_p}{L} \left[ (V_{SG} - V_{th}) \cdot V_{SD} - \frac{1}{2} V_{SD}^2 \right]$
Saturation	$V_{SG} > V_{th}$ and $V_{SD} > V_{SG} - V_{th}$	$I_D = \frac{1}{2} \cdot \mu_p \cdot C_{ox} \cdot \frac{W_p}{L} (V_{SG} - V_{th})^2 (1 + \lambda \cdot V_{SD})$

1 .- (5 points) Consider the inverter in the figure to the right, where  $C_L = 100 \text{ fF}$ . Is it true that we can make the propagation delay of this gate as small as we want by increasing  $W$ ? Why or why not?

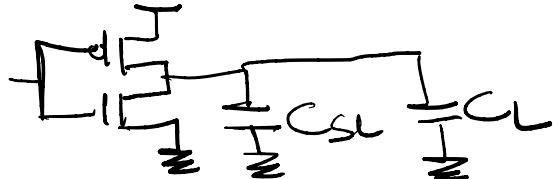


$$\tau = P_d + R_{eff} C_L$$

↑  
inp.  
of  $W$

↑  
 $\propto 1/W$

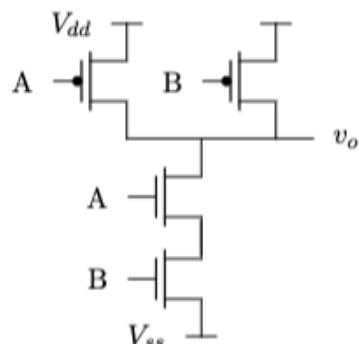
No, it cannot go below  $P_d$



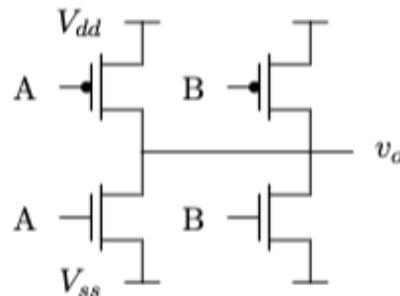
$$\tau = \frac{C V_{dd}}{2 I_S} = \frac{C_{se} V_{dd}}{2 I_S} + \frac{C_L V_{dd}}{2 I_S}$$

$C = C_{se} + C_L$

2 .- (5 points) Which of the following circuits is an acceptable implementation of CMOS logic? Why?

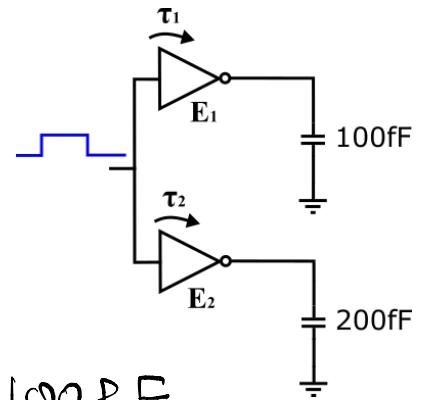


NAND Gate  
✓



If  $A = 1$  ( $V_{dd}$ )  
and  $B = 0$  ( $Gnd$ )  
⇒ we have connected  
 $V_{dd}$  to  $Gnd$   
⇒ PDN and the  
PDN aren't  
complementary  
⇒ not a valid CMOS gate

3.- (5 points) Consider the figure to the right, where the two inverters are identical.  $\tau_1$  and  $\tau_2$  are the propagation times for each inverter. Similarly,  $E_1$  and  $E_2$  are the energies consumed by each inverter when their input transitions twice, as shown with the blue waveform.



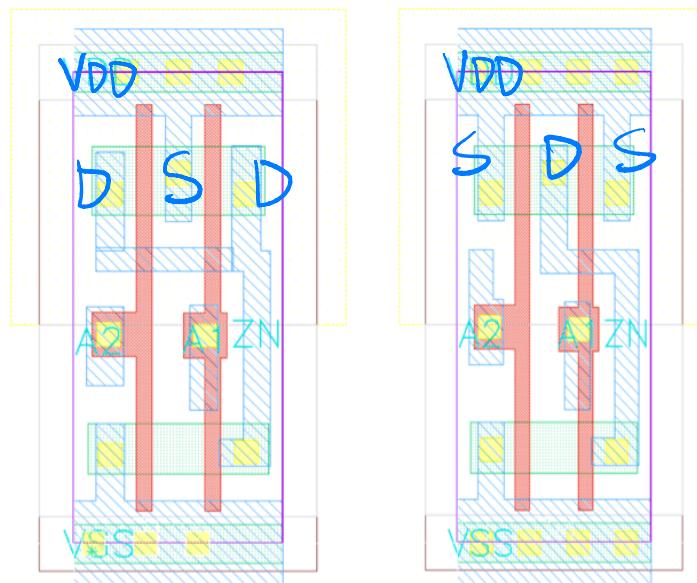
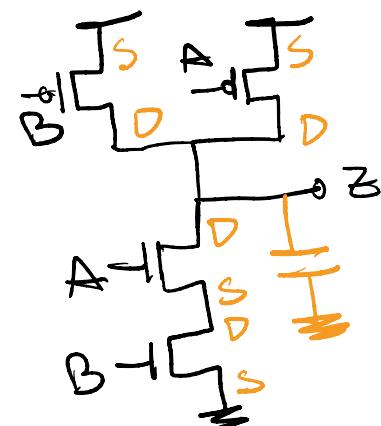
- a) Are the two delays equal? If not, which is greater,  $\tau_1$  or  $\tau_2$ ?

$$\tau = P_d + R_{\text{app}} \cdot C_L ; \quad 200 \text{ fF} > 100 \text{ fF} \\ \Rightarrow \tau_2 > \tau_1$$

- b) If we assume that the inverters don't have any parasitic capacitance, what is the value of the ratio  $\frac{E_2}{E_1}$ ?

$$E = CVdd^2 \Rightarrow E_1 = 100 \text{ fF } Vdd^2 \Rightarrow \frac{E_2}{E_1} = 2 \\ E_2 = 200 \text{ fF } Vdd^2$$

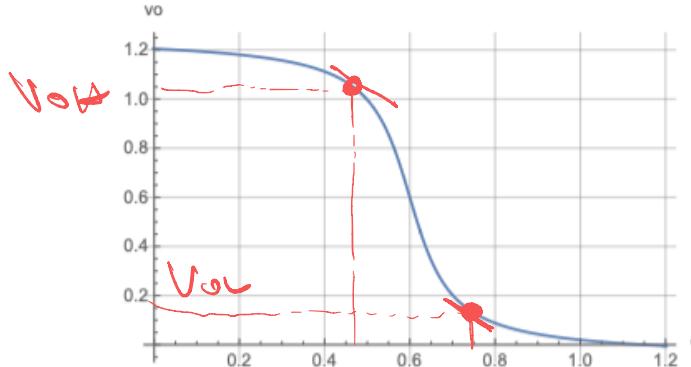
4.- (5 points) Which of the following two layouts of a NAND gate takes advantage of "drain sharing"?



$\uparrow$   
This one  
doesn't

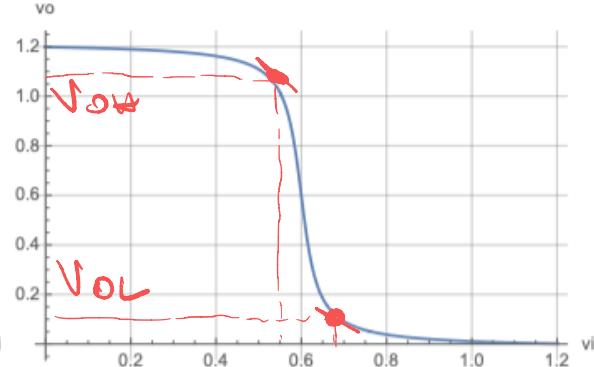
$\uparrow$   
This layout takes  
advantage of  
sharing

5 .- (5 points) Consider the following voltage-transfer curves for two separate inverters. Based on the curves, which inverter is more immune to noise in the input? Why?



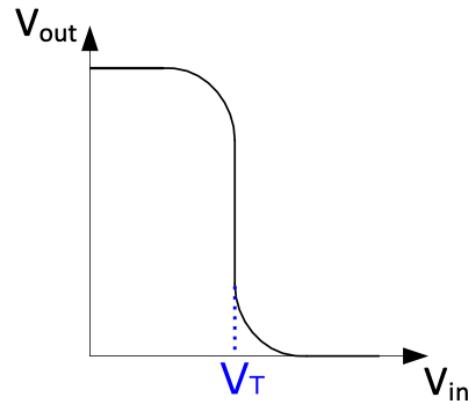
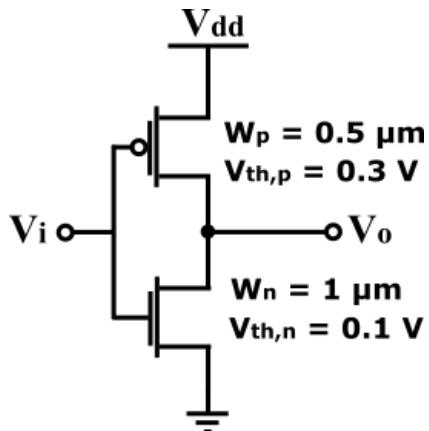
$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$



$\Rightarrow$  Higher noise margins  
 $\Rightarrow$  more immune to noise in the input

6 .- (10 points) The figure below shows an inverter, and a sketch of its DC voltage transfer characteristic. What is the value of  $V_T$ ?



When  $V_{in} = V_T$  both transistors are in saturation

$$\frac{1}{2} \mu_n C_{ox} \frac{W_n}{L} (V_{GS} - V_{th})^2 = \frac{1}{2} \mu_p C_{ox} \frac{W_p}{L} (V_{SG} - V_{th})^2$$

$$\mu_n = 2\mu_p$$

$$W_n = 2W_p$$

$$\Rightarrow \frac{\mu_n W_n}{\mu_p W_p} = 4$$

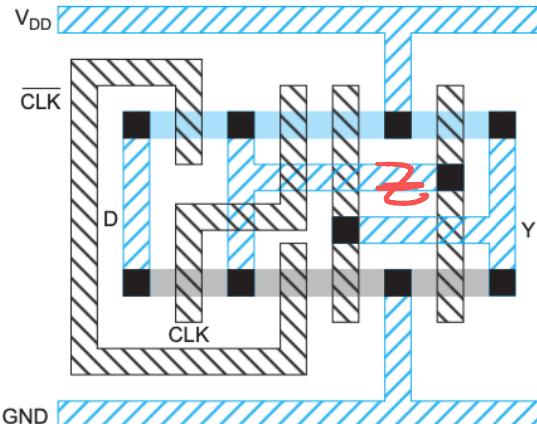
$$\Rightarrow 4(V_T - 0.1)^2 = (V_{dd} - V_T - 0.3)^2$$

$$= 0.38$$

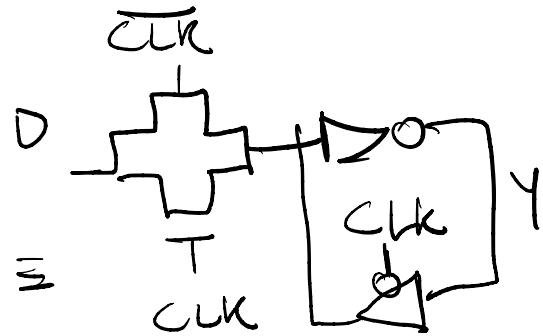
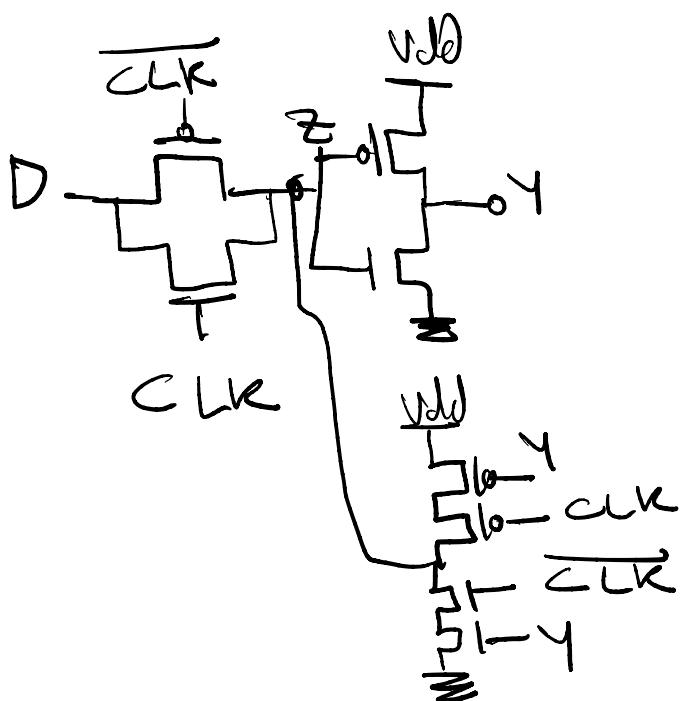
$$\Rightarrow 2V_T - 0.2 = 1.2 - V_T - 0.3$$

$$\Rightarrow 3V_T = 1.2 + 0.2 - 0.3 = 1.1 \Rightarrow V_T = \frac{1.1}{3}$$

6 .- (15 points) Draw the transistor-level schematic that corresponds to the stick diagram in the figure below  
 (BONUS: 5 points) What is the function of this circuit?

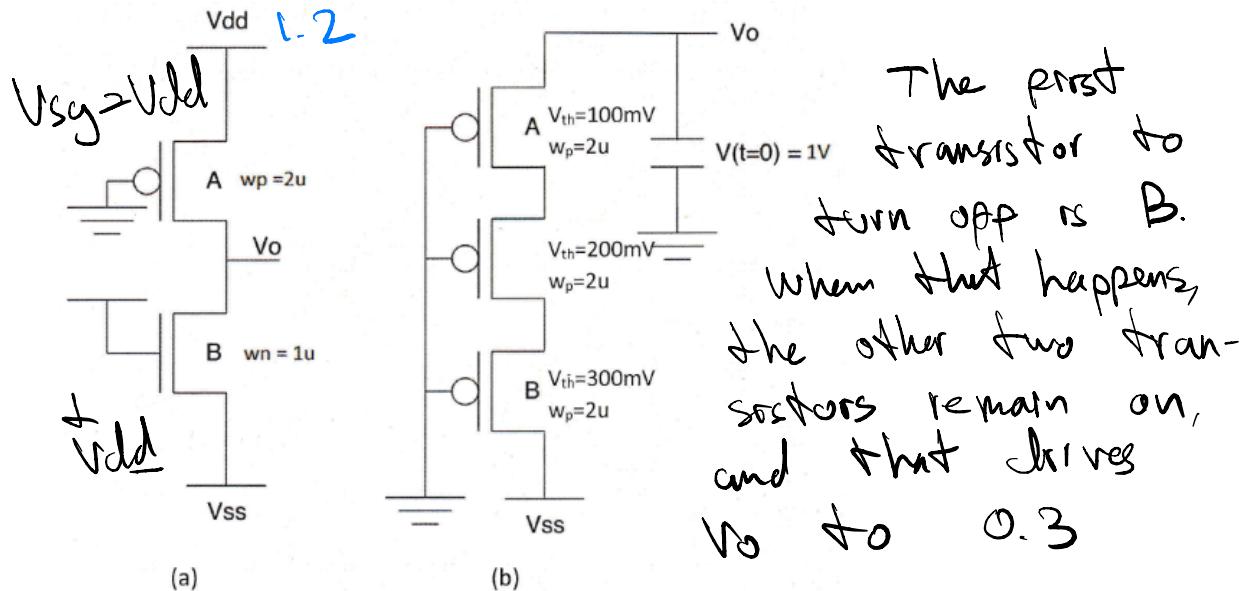


Contact  
 Metal1  
 pdiff  
 ndiff  
 Polysilicon



$\Rightarrow$  Latch

7 . - (10 points) For the given circuits in the figure below, (a) and (b), find  $V_o$  and the state in which devices A and B are (linear/saturation/cutoff). Assume no leakage in the transistors. Fill up Table 1 to indicate your answers, and briefly explain how you deduced them.



	$V_o$	State of device A	State of device B
(a)	0.6	Linear	Linear
(b)	0.3	Linear	Cutoff

(e) We guess that both devices are in the linear region (transistors are balanced)

$$\begin{aligned}
 (V_{DS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^2 &= (V_{SD} - V_{th}) V_{SD} - \frac{V_{SD}^2}{2} \\
 1 \cdot V_{DS} - \frac{1}{2} V_{DS}^2 &\geq 1 - V_{SD} - \frac{V_{SD}^2}{2} \\
 V_o - \frac{1}{2} V_o^2 &= 1 - V_o - \frac{(1 - V_o)^2}{2} \\
 V_o - \frac{1}{2} V_o^2 &= 1 - V_o - 0.72 + 1.2 V_o - \frac{V_o^2}{2} \\
 \Rightarrow 0.8 V_o &= 0.48 \\
 \Rightarrow V_o &= \frac{0.48}{0.8} = \frac{48}{100} \cdot \frac{10}{8} = \frac{1}{10} \cdot \frac{48}{8} = 0.6
 \end{aligned}$$

$V_o = 0.6$