Grade: /90

E E 476 – Introduction to VLSI Design
Final examination
December 12th, 2022

I have not received nor obtained help from anyone in the completion of this examination. During the course of this final examination, I have not engaged with any form of communication with my peers on any aspect of the contents of this exam. I understand that strict action will be taken resulting from my failure to comply with the final examination policy. I also understand that it is my duty to not only adhere to the final exam policy, but also report any other individual(s) who are violating this policy.

Name: _____

Signature: _____

The use of a non-programmable calculator is allowed. The use of notes or any other electronic devices is not allowed during this final examination.

Duration: 110 minutes

Assume that all devices have 0 leakage current. Unless otherwise stated, the following default parameters apply:

V_{dd}	1.2 V	$C_{ox} = \frac{\epsilon_r \cdot \epsilon_0}{t_{ox}} = 0.01\ \mathrm{F/m^2}$
ϵ_r (Silicon-di-oxide)	3.8	
ϵ_0	$8.85 \cdot 10^{-12}$ F/m	
λ	0	
t_{ox}	$33.63\ A = 3.363$ nm	$\mu_n \cdot C_{ox} = 0.5$ mA $\mu_p \cdot C_{ox} = 0.25$ mA
μ_n	$500\ \mathrm{cm^2/V}$	
μ_p	$250\ \mathrm{cm^2/V}$	
$V_{th,n} = V_{th,p} = V_{th}$	0.2 V	$\mu_n \cdot C_{ox} \cdot \frac{W_n}{L} = 10$ mA $\mu_p \cdot C_{ox} \cdot \frac{W_p}{L} = 10$ mA
W_n	1 µm	
W_p	2 µm	
Beta ratio $= \frac{\mu_n}{\mu_p}$	2	
$L_n = L_p = L$	50 nm	

NMOS transistor:

Cut-off	$V_{GS} \leq V_{th}$	$I_D = 0$
Linear/Triode	$V_{GS} > V_{th}$ and $V_{DS} \leq V_{GS} - V_{th}$	$I_D = \mu_n \cdot C_{ox} \cdot \frac{W_n}{L}\left[(V_{GS} - V_{th}) \cdot V_{DS} - \frac{1}{2}V_{DS}^2\right]$
Saturation	$V_{GS} > V_{th}$ and $V_{DS} > V_{GS} - V_{th}$	$I_D = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W_n}{L}(V_{GS} - V_{th})^2(1 + \lambda \cdot V_{DS})$

PMOS transistor:

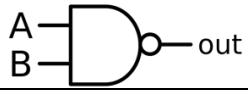
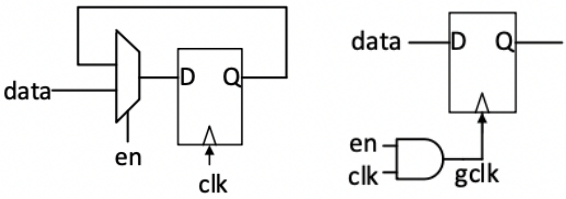
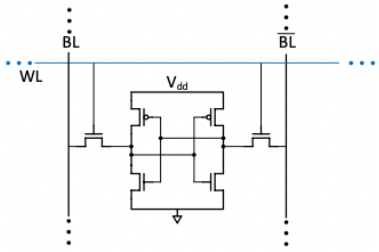
Cut-off	$V_{SG} \leq V_{th}$	$I_D = 0$
Linear/Triode	$V_{SG} > V_{th}$ and $V_{SD} \leq V_{SG} - V_{th}$	$I_D = \mu_p \cdot C_{ox} \cdot \frac{W_p}{L}\left[(V_{SG} - V_{th}) \cdot V_{SD} - \frac{1}{2}V_{SD}^2\right]$
Saturation	$V_{SG} > V_{th}$ and $V_{SD} > V_{SG} - V_{th}$	$I_D = \frac{1}{2} \cdot \mu_p \cdot C_{ox} \cdot \frac{W_p}{L}(V_{SG} - V_{th})^2(1 + \lambda \cdot V_{SD})$

True/False (12 points, 1 each)

No.	Assertion	True/False
1	The Miller coupling coefficient can be as high as 3x when analyzing energy dissipation for a gate driving a load coupled with other loads	
2	The switching activity of a node is defined as the probability that the corresponding node has a transition (from 0V to Vdd or vice versa) during a clock cycle	
3	Switching activities can be arbitrarily large	
4	Consider a battery driving a CMOS inverter. The current flow out of the "+" (positive) terminal is not instantaneously equal to the "–" (negative) terminal but the overall integrated charge is always equal over one cycle.	
5	Crowbar current in an inverter increases with input loading (i.e., increases if we increase the wire capacitance connected to the input of the inverter)	
6	Cross-coupled inverters (e.g., as used in latches) only have 2 DC equilibrium points. That is why we use them to store bits	
7	Hold violations in Flip Flop and latches are only a concern for academics. In practice, designers never need to worry about them	
8	For a pipelined design, adding more pipeline stages eventually stops being effective (that is, we stop seeing any frequency improvements)	
9	Designers only need to worry about clock uncertainty when they don't spend enough time designing the clock distribution (e.g., a clock tree)	
10	Funnel shifters are inherently better than barrel shifters and should always be preferred	
11	DRAMs are typically not compatible with most CMOS fabrication processes, that is why they are usually in a different chip	
12	For a given input and output load, a chain of three inverters in series is always slower than a single inverter	

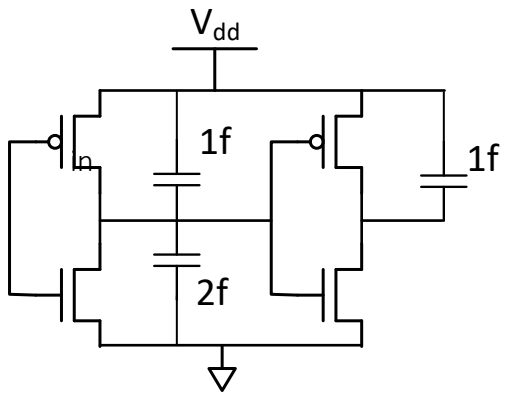
Short Answers (8 points, 1 each)

No.	Question	Answer
1	Assume you have a very fine-grained block of combinational logic, with a minimum delay of 50ps, and a maximum delay of 1000ps, and flip-flops with t_{setup}=t_{CQ}=25ps. What is the maximum frequency that you can achieve if you divide this combinational logic into 4 pipeline stages?	
2	The complexity (in terms of delay) for an N-bit carry-propagate adder is $O(\sqrt{N})$, while for a tree adder it is $O(\log(N))$. Is there any case where we would prefer a carry-ripple adder over a tree adder? If yes, give an example. If not, why?	

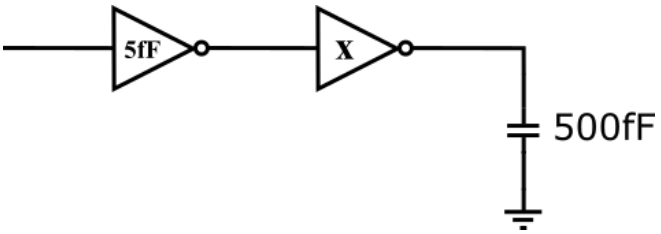
3	Is it possible to have overflow when subtracting two signed N-bit numbers (using 2's complement)? If not, why? If yes, give an example	
4	For the following NAND gate, we know that the probability that A is 1 is 0.5, and the probability that B is 1 is 0.2. What is the probability that the output is 1? 	
5	The power consumption of a circuit is 100mW. If we reduce the clock frequency by a factor of 2, and increase Vdd by a factor of 2, what will the power consumption of the circuit be?	
6	From a digital logic point of view, the following two circuits are equivalent:  The one on the right is known as "clock gating". Name one advantage of clock gating when compared to the implementation on the left	
7	The following SRAM bit cell is usually called a 6T SRAM bit cell. Why? 	
8	If we assume that Vdd >> Vth, and we increase Vdd by 20%, by how much can we increase the frequency of our circuit?	

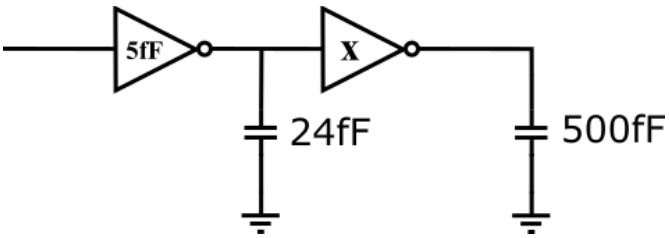
1. [10 points] For the circuit shown below complete the table below for energy delivered by the supply and energy dissipated for each transition

Input Transition	Energy delivered by supply	Energy dissipated in circuit
Rising		
Falling		



2. [20=10+10 points] For the following circuits, find the optimal input capacitance x of the second inverter. Make sure to write down how you obtained your answer

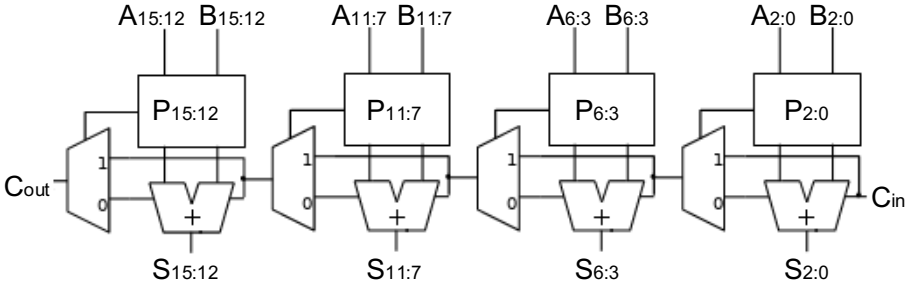




3. [10 points] Consider the 16-bit carry skip adder that is shown in the figure below (note the non-uniform group sizes). For this example, assume

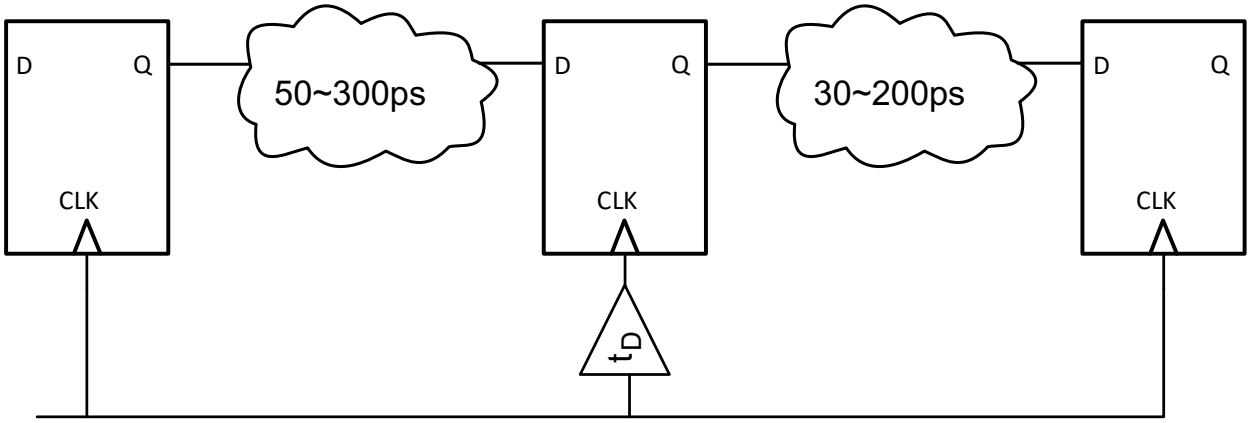
1. Propagates within each block are generated by producing individual bit propagates, then merged in parallel using 2-input AND gates only.
2. Assume all gate delays are equal, including the full-adder cells in the add blocks

a. Which gates does the critical path travel through? (Sketch and annotate the path over the block diagram below).



b. What is the **worst-possible delay** of this adder? Write your answer as the sum of unit gate delays making the path (random example to illustrate what we mean: 3(group-prop delay) + 2(mux delay) + 1(xor delay) = 6 delay units total)

4. [15 points] (Note that for all questions except for c, t_D=0, and in those cases the pipeline is exactly like the one we studied in class). In the clouds corresponding to combinational logic, the smallest number corresponds to the delay of the shortest path (contamination delay), and the largest number corresponds to the delay of the critical path (propagation delay)



Consider the Datapath shown above. The throughput is not optimal due to constraints on logic delay granularity. The designer plans to fix the design by deliberately inserting delay in the clock distribution as shown. (Timing properties of such a flip-flop are: T_{setup} = 30ps, T_{hold} = 40ps, T_{cq} = 50ps. $T_{clk,U}$=20ps=clock uncertainty)

a. [2 points] What is the current minimum achievable operating cycle-time **(t_D=0)**?

b. [3 points] What is the current hold-slack in the design **(t_D=0)**?

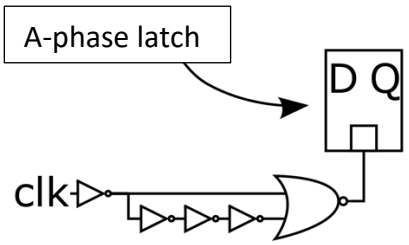
c. [5 points] What is the maximum achievable functionally correct performance that can be achieved by purely tuning the delay of the distribution (i.e., by changing t_D)?

d. [5 points] Assuming a square-law current model, and with $\mathbf{t_D=0}$ again, what is the percentage dynamic energy-per-cycle dissipation reduction achieved by voltage scaling the pipeline until it operates at 1GHz.

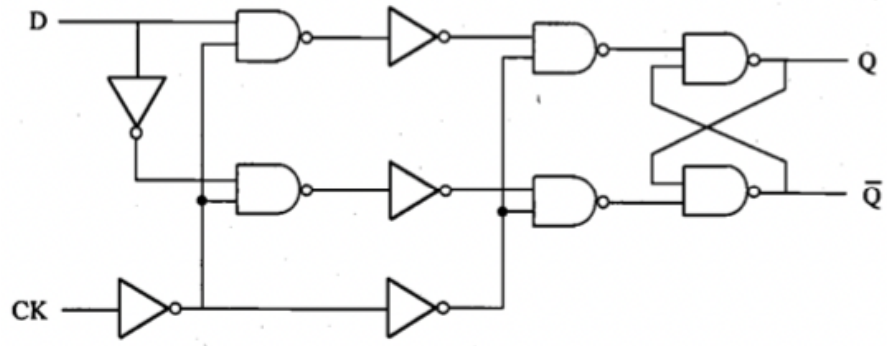
e. [Bonus: 3 points] What is the impact of the voltage scaling in question "d" above on leakage power for the pipeline? Answer in this form: (It will be <pick one word: Higher or lower or unchanged> because <no more than 20 words>

5. [5+10 points] The following circuits correspond to D Flip-Flops. They are different implementations than the one we studied in class. Explain how they work, and if they are triggered by the positive edge of CK, by the negative edge of CK, or both. Assume all the gates have the same propagation delay of T seconds. Do not worry about setup or hold.
Hint: check that the flop keeps its state when CLK=0 and CLK=1. Then consider what happens during a CLK transition. Specifically, track how the signals propagate through the circuits. It might help to draw a timing diagram, considering what happens after intervals of T seconds

a)



b)



[BONUS: 10 points] Cross-talk analysis: Consider the following circuit, in which two wires are coupled through a couple capacitance C_C. The victim wire is being held at 0V (GND) through the holding resistance R_H of an NMOS transistor (for this problem, assume that this resistance is constant). The capacitance between the victim wire and GND has a value of C_W. The aggressor wire sees a voltage change, from 0V to V_0. The change is linear, and with a total duration of Δt seconds. Due to the coupling among the two lines, the change in the aggressor causes a pulse in the victim wire. Determine the maximum height V_h of this pulse. (You may assume that V_h is small enough that to compute the current flowing C_C, we may approximate the voltage on the victim as being constant and equal to 0V. If we go with this hypothesis, we might assume that C_C behaves as a piecewise constant current source)