

EE476 Midterm Examination

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12/9/21

I have not received nor obtained help from anyone in the completion of this examination. During the course of this mid-term examination I have not engaged with any form of communication with my peers on any aspect of the contents of this exam. I understand that strict action will be taken resulting from my failure to comply with the mid-term examination policy. I also understand that it is my duty to not only adhere to the mid-term exam policy, but also report any other individual(s) who are violating this policy.

Name: _____

Signature: _____

Duration: 1 h 50m

Assumed that all devices have 0 leakage current. Unless otherwise stated, the following default parameters apply:

Vdd	1V
ϵ_r (Silicon-di-Oxide)	3.8
ϵ_0	8.85 E-12 F/m
λ	0
T_{ox}	100A
μ_n	500cm ² /V
μ_p	250cm ² /V
$V_{thn} = V_{thp}$	0.2V
W_n	1μm
W_p	2μm
Beta-ratio	2
$L_n=L_p$	60nm

N-channel MOSFET

Cut Off	$V_{GS} \leq V_T$	$I_{DS} = 0$
Linear	$V_{GS} > V_T, V_{DS} \leq V_{GS} - V_T$	$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right]$
Saturation	$V_{GS} > V_T, V_{DS} > V_{GS} - V_T$	$I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$

1. [3+3 points] For the circuit given below (Figure 1), assuming all the gates have the same delay of 2ps, calculate the latest arrival time at any of the outputs if:

- All signals arrive at the same time, $t=0\text{ps}$
- Signals arrive at the following times ($a=0\text{ps}$, $b=10\text{ps}$, $c=2\text{ps}$, $d=2\text{ps}$, $e=0\text{ps}$)

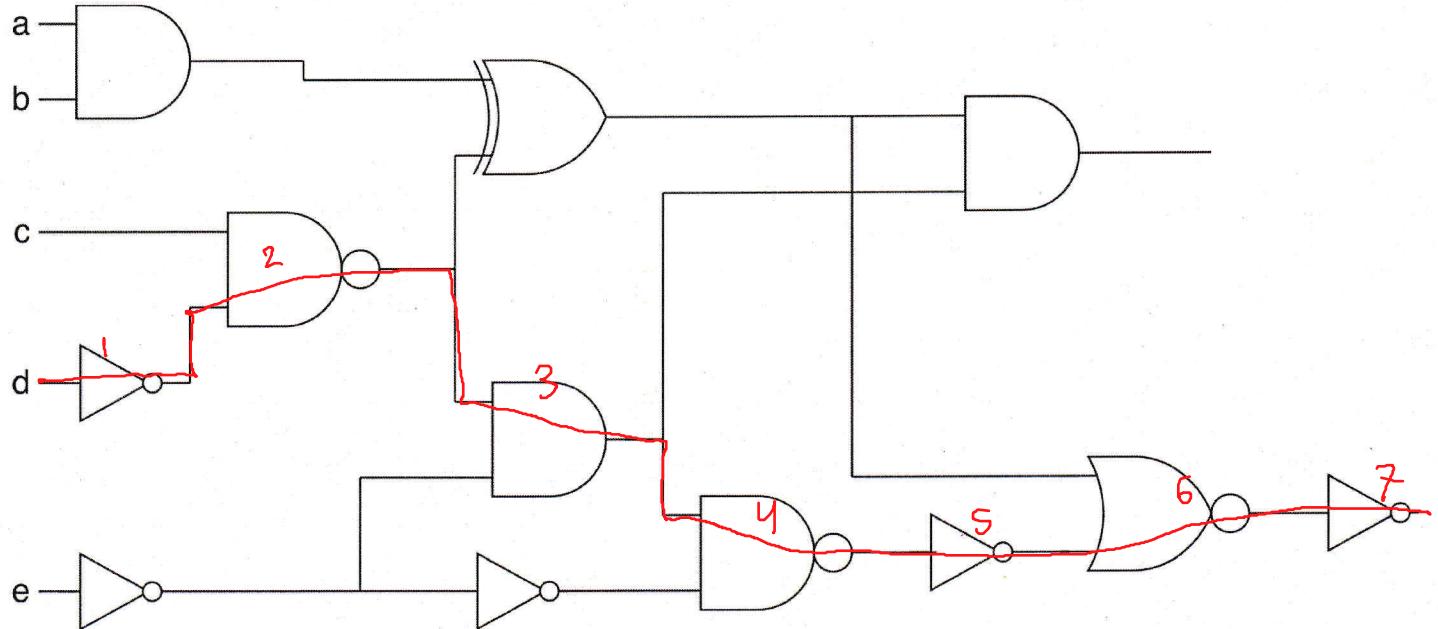


Figure 1

a Find longest path (colored red) $7 \text{ gates} \cdot 2 \text{ ps} = \boxed{14 \text{ ps}}^1_a$

b Find longest path from each starting point, add arrival times, then choose the longest

$$a = 0\text{ps} + 4 \cdot 2\text{ps} = 8\text{ps}$$

$$b = 10\text{ps} + 4 \cdot 2\text{ps} = \boxed{18\text{ps}}^1_b$$

$$c = 2\text{ps} + 6 \cdot 2\text{ps} = 14\text{ps}$$

$$d = 2\text{ps} + 7 \cdot 2\text{ps} = 16\text{ps}$$

$$e = 0\text{ps} + 6 \cdot 2\text{ps} = 12\text{ps}$$

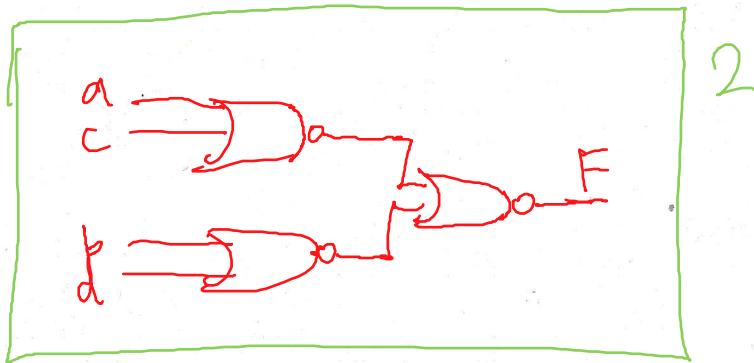
2. [6 points] Write down the CMOS implementation of the following Boolean function in as few 2-input **nand** and **nor** gates as possible. You may use inverters if needed but no other gates are allowed.

$$F = ab + cd + bc + ad$$

group then DeMorgan

$$\overline{(a+c)(b+d)} \rightarrow \overline{\overline{a+c}} + \overline{\overline{b+d}}$$

$$a(b+d) + c(b+d) = (a+c)(b+d)$$



3. [5 points] If the delay for a unit step input for the **loaded inverters** in Figure 2 (a) and (b) are as follows, what is the delay for (c)?

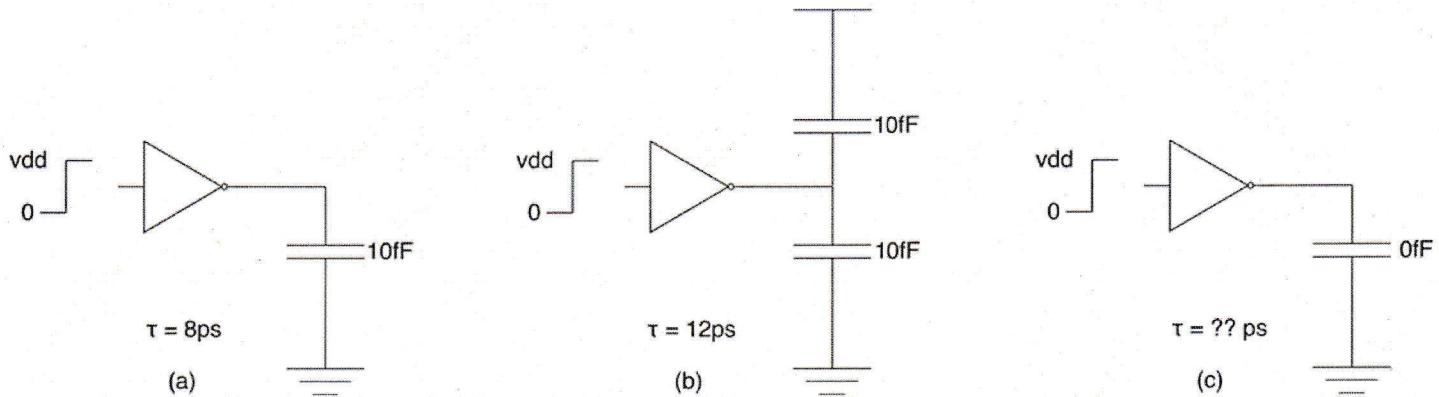
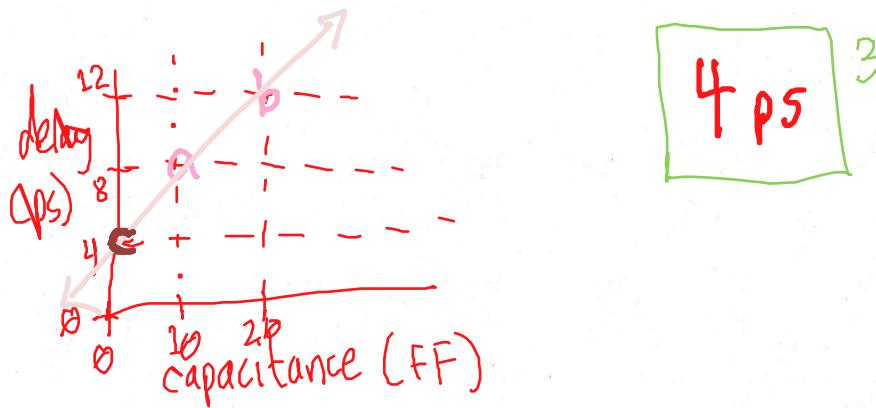


Figure 2

Is a linear function based the points we are given



4 ps

3

4. [8 points] For the following circuit (Figure 3), assuming the **inverters** are sized such that the rising waveforms at b and c are identical, and the falling waveform at a has the same 50% crossover point and transition time as b and c. Find the rise delay for the given transition at **b**.

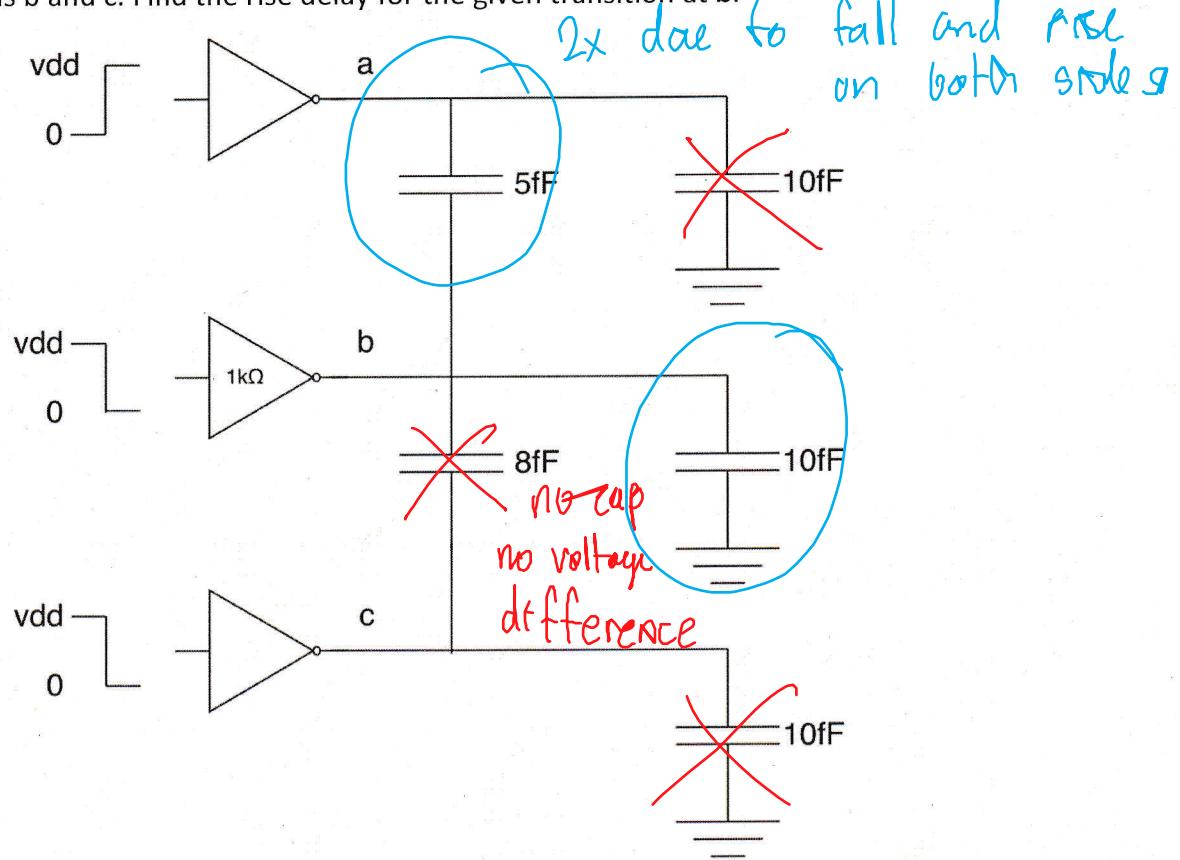


Figure 3

$$10\text{fF} + 2 \cdot 5\text{fF} = 20\text{fF}$$

$$20\text{fF} \cdot 1000\Omega = 20\text{ps}$$

4

5. [5+4+4+2 points] For the following circuit (Figure 7)

- a. draw the transfer function. Label only the the points that mark transitions in operating region for the inverter (i.e. where any of the devices changes its mode of operation such as from linear to saturation for example). **Do not** solve for V_{out} when $V_{in}=0$ or $V_{in}=V_{dd}$. Note, V_{th} is -0.2 for both nmos and pmos. Your sketch will be graded on the general shape of the curve.

P3

- b. When pmos is at the edge of saturation/linear

P1

- c. When nmos is at the edge of saturation/linear

P2

- d. $V_i = V_{dd}/2$

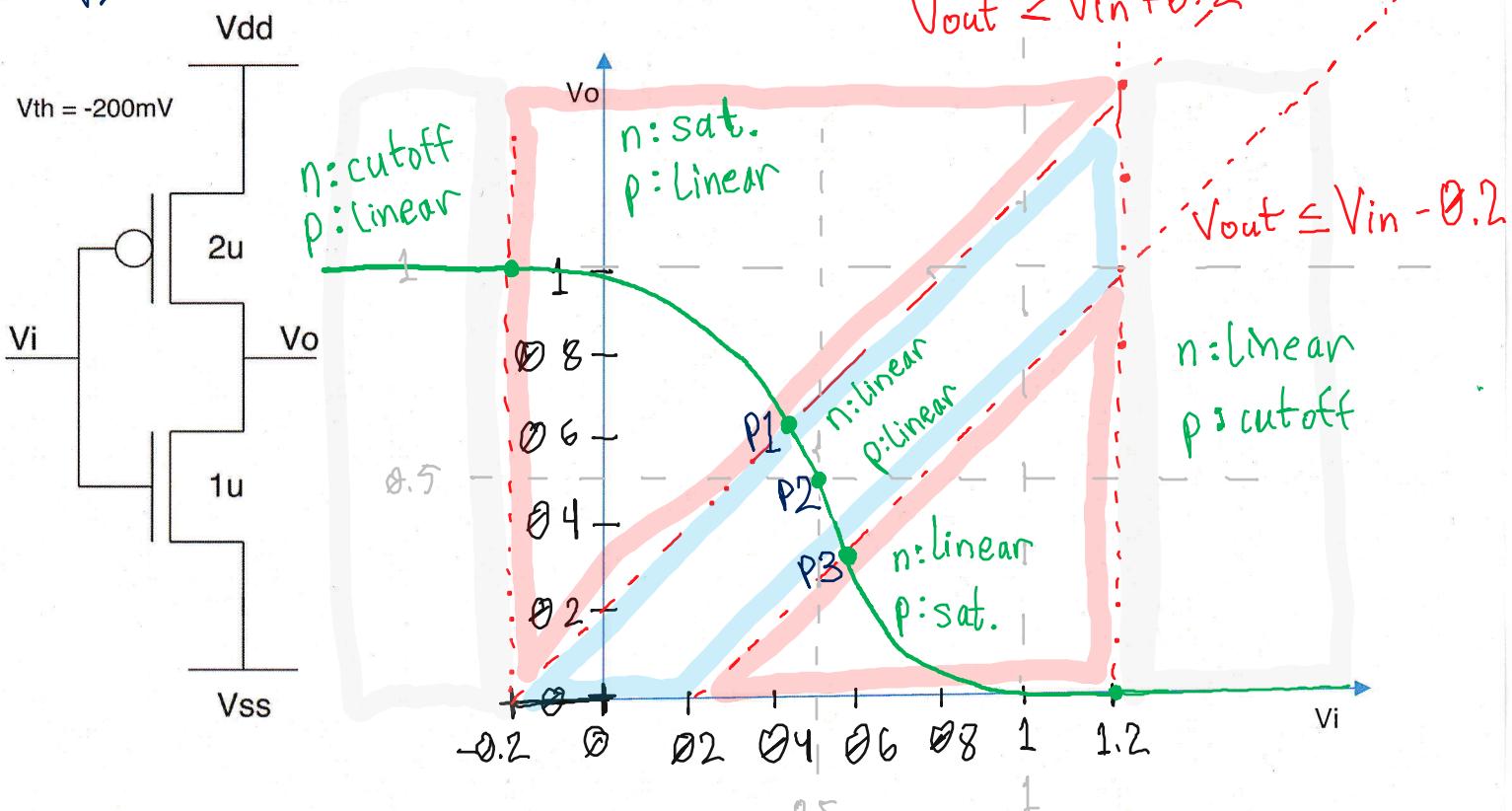


Figure 4

EE 476 midterm 1 problem 5 calculation

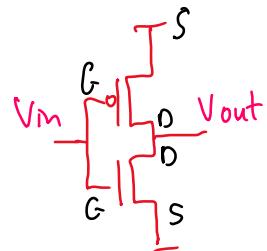
b. PMOS at edge sat/linear \rightarrow at $V_{out} = V_m - 0.2$

use sat equation to get PMOS current:

$$I_p = \frac{1}{2} \mu_p C_{ox} \frac{W_p}{L_p} (V_{gs} - V_T)^2 \quad (\cancel{1+2V_{ds}})$$

$$I_p = \frac{1}{2} \cdot 250 \cdot 100 \cdot \frac{2 \cdot 10^{-6}}{60 \cdot 10^{-9}} (V_{gs} + 0.2)^2$$

Please ignore C_{ox} in these equations.
I accidentally used T_{ox} as C_{ox} , but it cancels during solving so the answers are still correct.



we know currents are equal so set up equation for linear current through nmos and solve for voltage value. V_{gs} is in reference to PMOS so $V_{gs} = (1 - V_{gs})$ for NMOS

$$I_n = \mu_n C_{ox} \frac{W}{L} [(V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2}]$$

$$I_n = 500 \cdot 100 \cdot \frac{10^{-6}}{60 \cdot 10^{-9}} [(1 - V_{gs}) + 0.2] \cdot (0.8 - V_{gs}) - \frac{(0.8 - V_{gs})^2}{2}$$

$$I_n = I_p$$

\downarrow solve for V_{gs}

$$V_{gs} = 0.4428571$$

(PMOS)

$V_{in} = 1 - V_{gs} =$ (pmos)	0.557 V	Sb
$V_{out} = V_m - 0.2 =$	0.357 V	Vout

C nmos at edge sat linear. $V_{out} = V_{in} + 0.2$

set up equations again.

$$I_n = I_{sat} = \frac{1}{2} \cdot 500 \cdot 100 \cdot \frac{10^{-6}}{60 \cdot 10^{-9}} \cdot (V_{gs} + 0.2)^2$$

$$I_p = I_{lin} = 250 \cdot 100 \cdot \frac{2 \cdot 10^{-6}}{60 \cdot 10^{-9}} \cdot \left[[(1 - V_{gs}) + 0.2] \cdot (0.8 - V_{gs}) - \frac{(0.8 - V_{gs})^2}{2} \right]$$

$$I_n = I_p$$

↓ solve

$$V_{gs} = 0.4428571 \quad (nmos)$$

$$\rightarrow \begin{array}{|c|c|} \hline V_{gs} & V_{in} \\ \hline (nmos) & 0.443V \\ \hline V_{out} & V_{out} \\ \hline V_{out} = V_{in} + 0.2 & 0.643V \\ \hline \end{array} \quad 5c$$

d balanced inverter ($u_n w_n = u_p w_p$) so $V_i = V_o$ at $\frac{V_{dd}}{2} = V_i$

$$\boxed{(V_i, V_o) = (0.5V, 0.5V)} \quad 5d$$

6. [10 + 5 = 16 points] Consider the novel gate topology proposed in Figure.
- Sketch the DC transfer function of such a gate assuming $V_{dd}=1V$. Label all points of transition in the operating region of either transistor. **Do not solve for V_{out} values when $V_{in}=0$** (too much repetitive work). You will be evaluated based on the shape of the curves and labeling of key points.
 - What is the disadvantage of implementing long cascades of such a logic gate in terms of voltage values corresponding to logic 1 and logic 0 (Write your answer down in **no more than 10 words**)

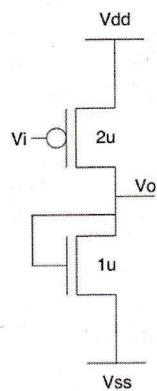
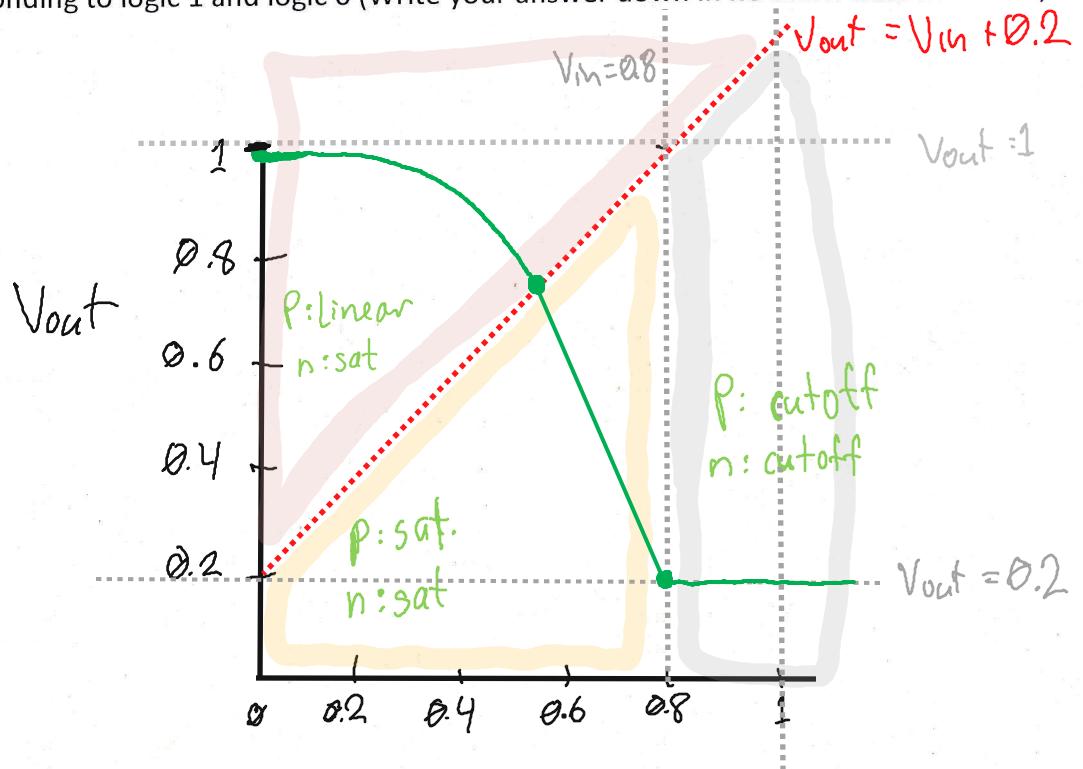


Figure 5



b. logic 1 degrades with each stage (infinite delay possible)
logic 0 cannot go below $V_{th}(0.2V)$

Allow up to 20 words

7. [2+6 points] For the given circuits in Figure 9, (a) and (b), find V_o and the state in which device A and B is in (linear/saturation/cutoff). Assume no leakage in the transistors. Fill up Table 1 to indicate your answers.

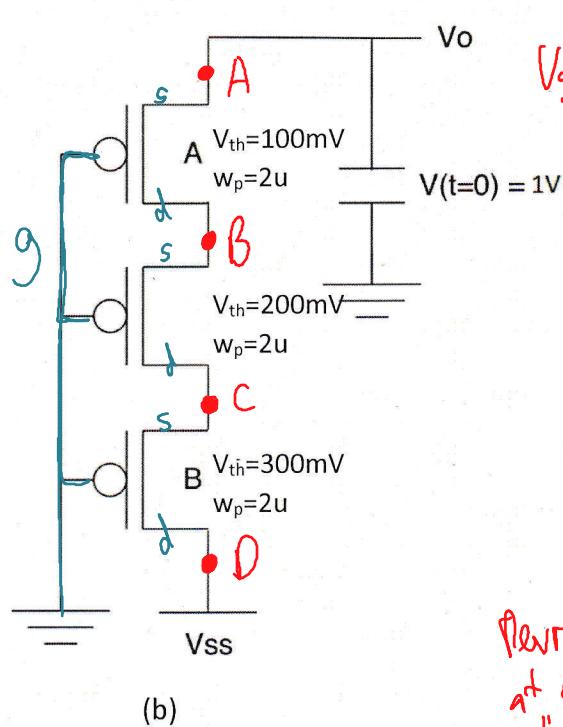
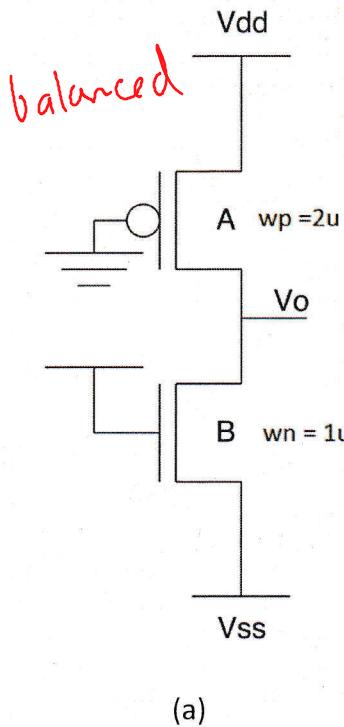


Figure 6

V_{gs} must drop below V_{th} , all gates tied ground so for device A source (net A) must drop below 0.1 V to enter cutoff. Device B is the first to enter cutoff. Since device B is on bottom so at 0.3V, nets A-C can no longer discharge to ground.

Table 1

	V_o	State of device A	State of device B
(a)	0.5	Linear	Linear
(b)	0.3	Linear	Cutoff

8. [3+4+2 points] For the circuit in Figure 10 (a), a unit step input is applied at $t=0$ s. Assume all load capacitance is 10fF in this problem. **Assume a V_{th} of 0.5V.**
- What should be the value of W for which current through the NMOS at $t=0+$ is equal in Fig. 7a and Fig. 7b?
 - What is the time at which $V_c=0.5\text{V}$ for Fig. 7a?
 - What is the time at which $V_c=0.5\text{V}$ for Fig. 7b?

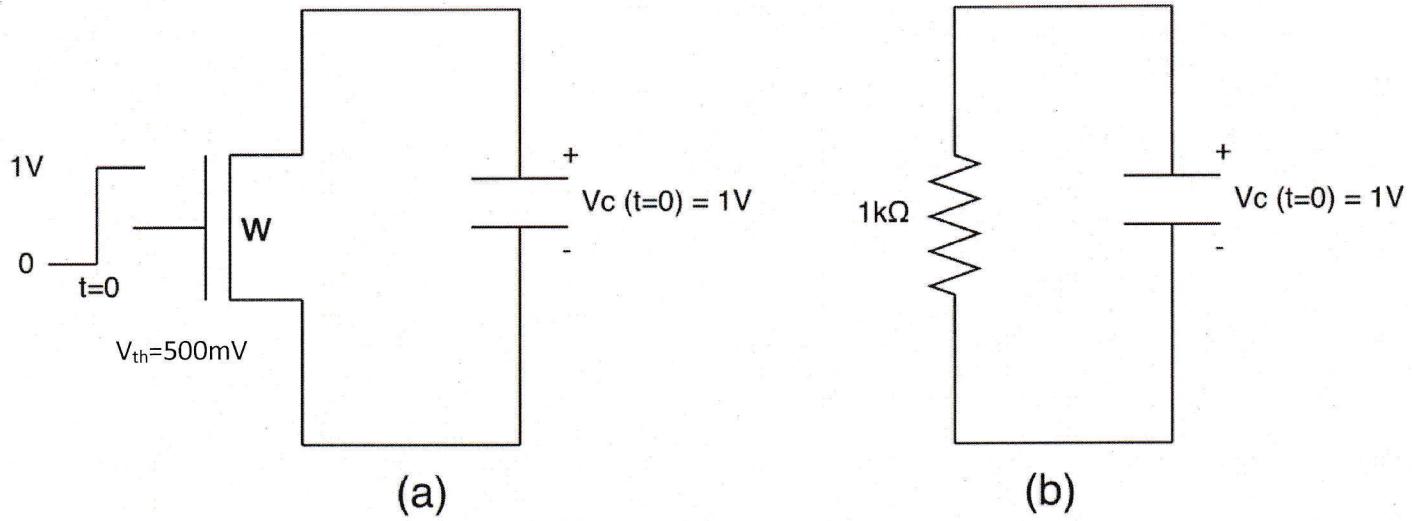


Figure 7

8.

$$a) I_{sat} = \frac{1}{2} \mu_n C_{ox} \frac{W_n}{L_n} (V_{DS} - V_{TH})^2 = \frac{1 \text{ V}}{1 \text{ k}\Omega}$$

$$\Rightarrow W_n = 2(1 \times 10^{-3} \text{ A}) L_n / \mu_n \cdot C_{ox} \cdot (V_{DS} - V_{TH})^2$$

$$\begin{aligned} \mu_n \cdot C_{ox} &= (500 \text{ cm}^2/\text{V}\cdot\text{s}) \left(\frac{\epsilon_r \cdot \epsilon_0}{T_{ox}} \right) = \frac{500 \text{ cm}^2}{\text{V}\cdot\text{s}} \cdot \frac{3.8 \cdot 8.85 \times 10^{-12} \text{ F}}{100 \text{ cm} \cdot 10^{-6} \text{ cm}} \\ &= \frac{5 \cdot 3.8 \cdot 8.85 \times 10^{-12} \times 10^6 \text{ C}}{\text{V}^2 \cdot \text{s}} = \frac{168.15 \times 10^6 \text{ C}}{\text{V}^2 \cdot \text{s}} \cdot \frac{4}{\text{V}^2} \end{aligned}$$

$$W_n = \frac{2 \cdot 60 \times 10^{-9} \cdot 10^{-3} \text{ C} \cdot \text{m}}{8} \cdot \frac{\text{V}^2 \cdot \text{s}}{168.15 \times 10^6 \text{ C}} \cdot \frac{1}{(1 \text{ V} - 0.5 \text{ V})^2}$$

$$W_n = \frac{8 \cdot 60 \times 10^{-12} \text{ m}}{168.15 \times 10^6} = 2.855 \times 10^{-8} \text{ m} = 2.855 \text{ nm}$$

~~AV = 0.5 V~~

$$b) \cancel{I_{sat} = 1 \text{ mA}} \quad I_{sat} = 1 \text{ mA}$$

$$V_c(t) = 1 - \int \frac{i}{C} dt$$

$$V_c(t) = 1 - \frac{1 \text{ mA}}{10 \text{ fF}} t = 0.5 \text{ V}$$

$$\Rightarrow t = \frac{1 - 0.5 \text{ V}}{1 \text{ mA}} \cdot 10 \text{ fF} = 5 \text{ ps}$$

$$c) \text{Discharging RC: } V_c(t) = V_0 e^{-\frac{t}{RC}}$$

$$R = 1 \text{ k}\Omega; \quad C = 10 \text{ fF}$$

$$0.5 \text{ V} = 1 \text{ V} e^{-\frac{t}{RC}}$$

$$\Rightarrow t = -\ln(0.5) RC = 6.93 \text{ ps}$$

9. [8 points] Consider the timing element shown in Fig. 8. When considering the timing implications of this structure, consider it a timing element referenced at the rising edge of clock.

- When does it capture data at its input? *rising edge*
- When does it release data at its output? *Falling edge*
- What is one advantage of such a structure (from a timing perspective)? *More forgiving hold requirement*
- What is one disadvantage of such a structure (from a timing perspective)?
• data comes out 1/2 cycle late, less computation time, more limited bandwidth.

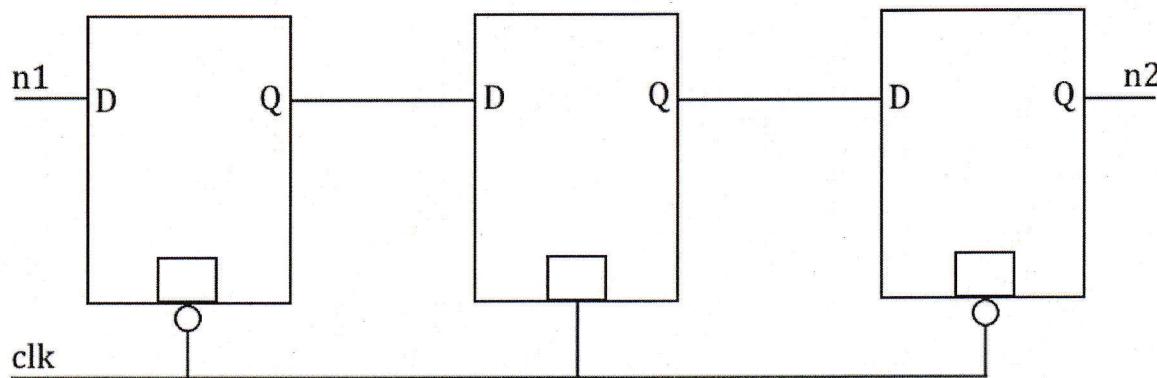


Figure 8