

# Lecture 6: Gate Delay



*Based on material prepared by prof. Visvesh S. Sathe*

# Acknowledgements

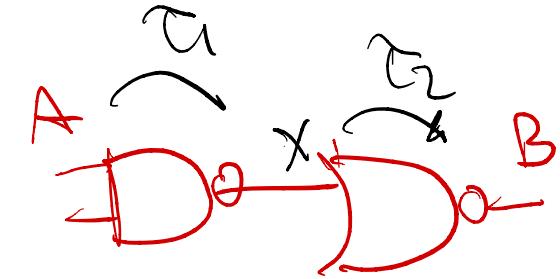
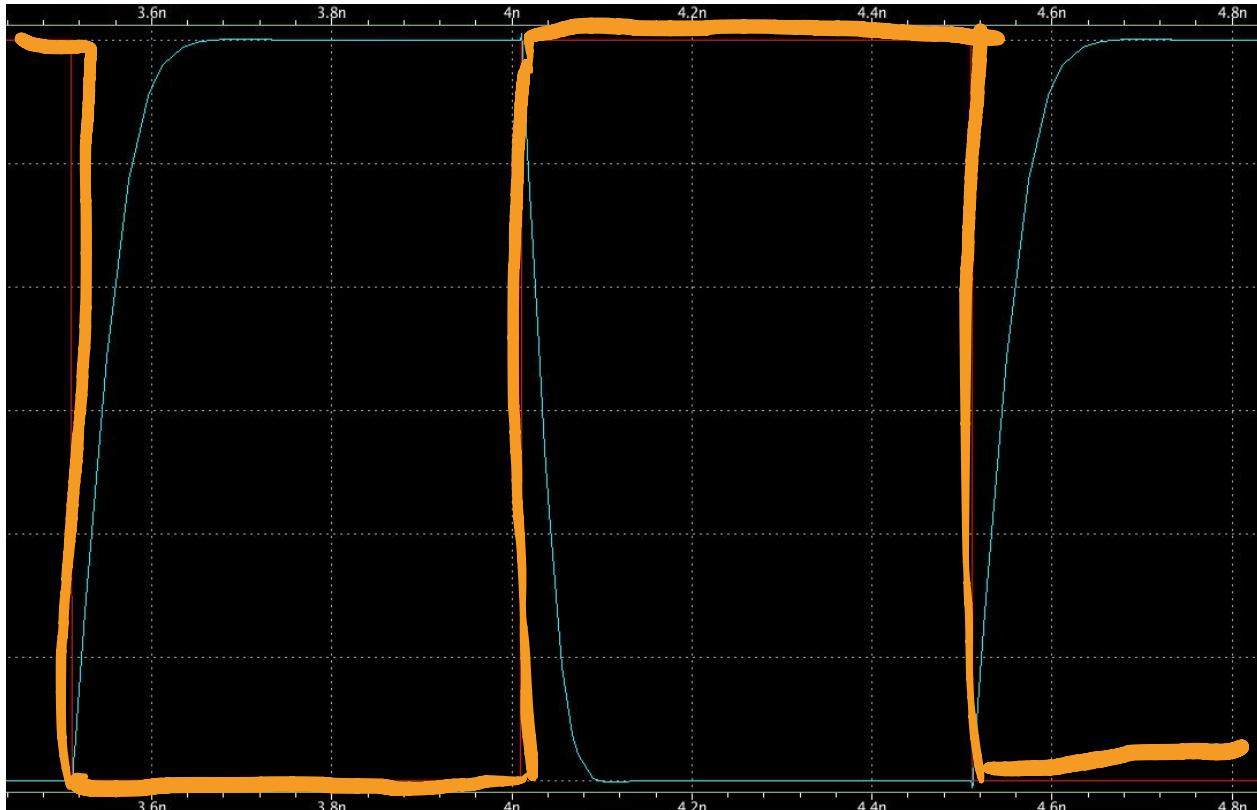
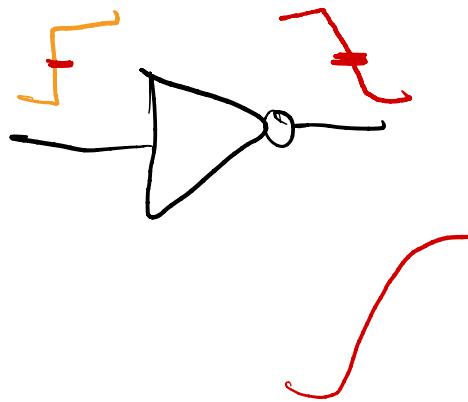
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Visvesh S. Sathe  
Associate Professor  
Georgia Institute of Technology  
<https://psylab.ece.gatech.edu>

UW (2013-2022)  
GaTech (2022-present)

# CMOS Inverter Delay



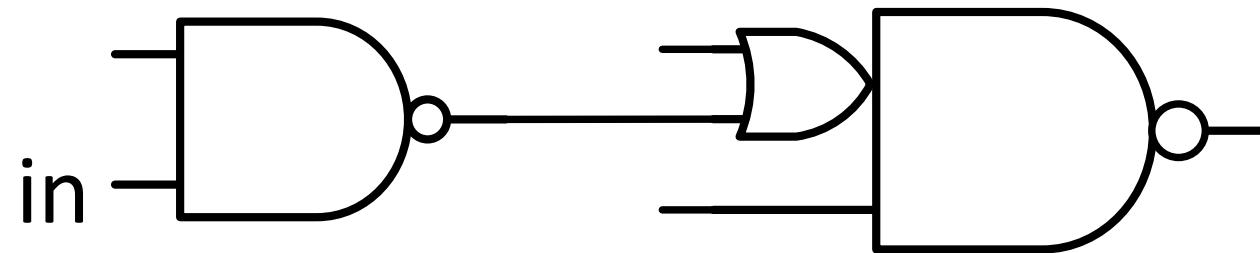
$\tau_1: A \text{ } 50\%$ ,  $\rightarrow$   
 $B \text{ } 50\%$ ,

$\tau_2 \text{ } 50\%$ ,  
 $\rightarrow B \text{ } 50\%$ ,

$\tau_1 + \tau_2$

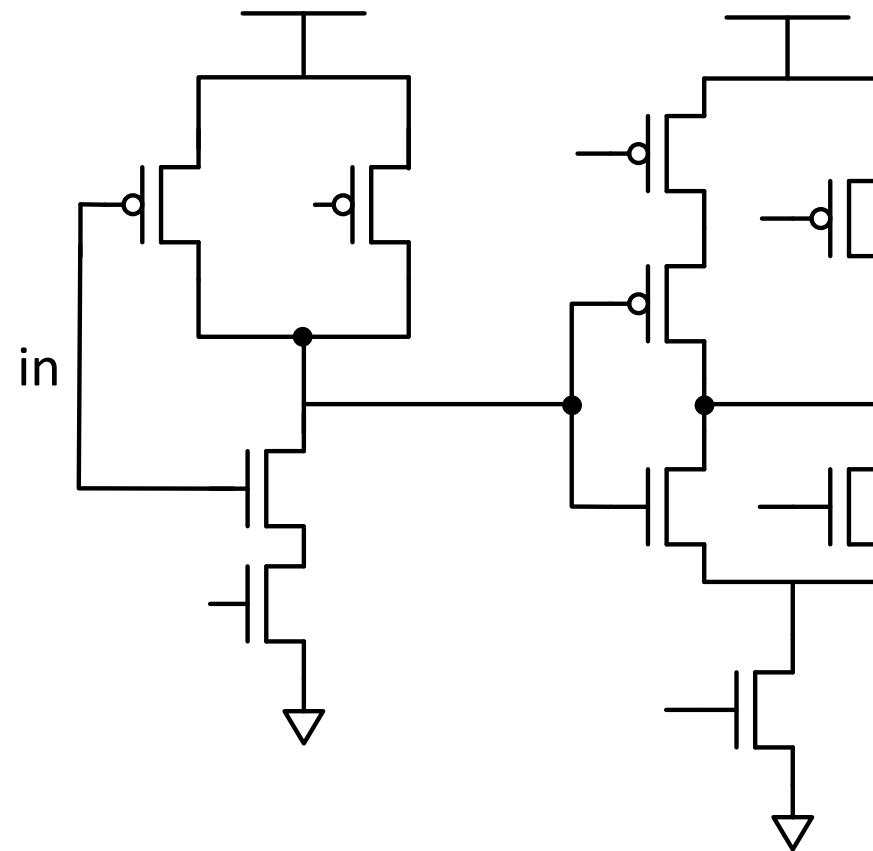
$A \text{ } 50\% \rightarrow B \text{ } 50\%$

# Simple Delay Model



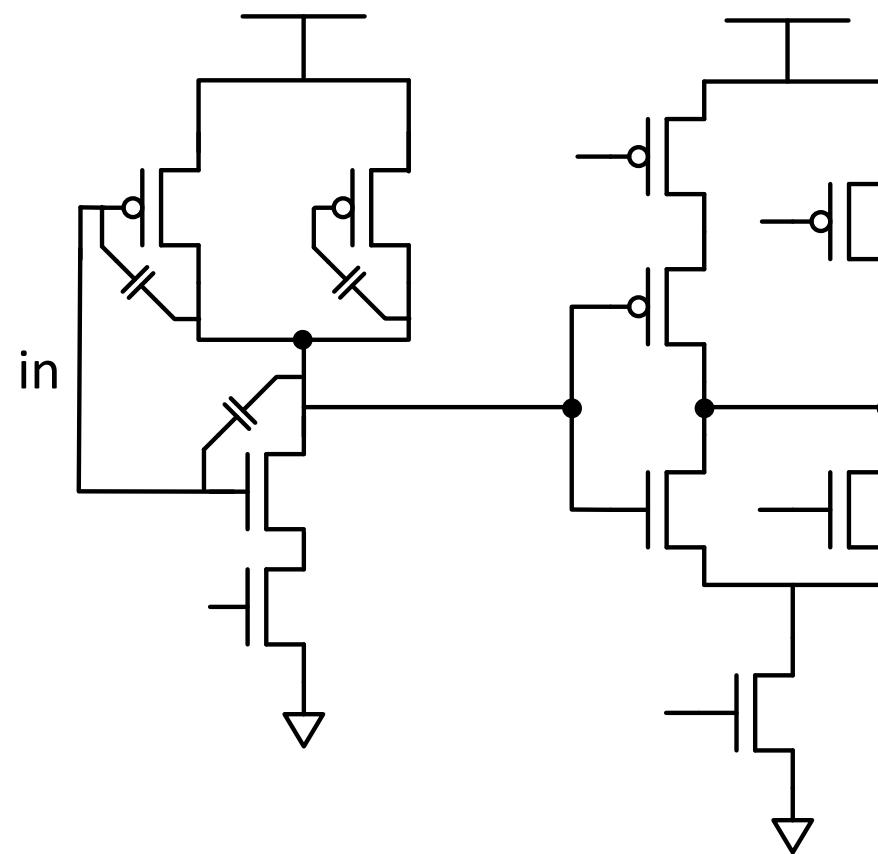
- Gate delays determine the time taken to compute a boolean function

# Simple Delay Model



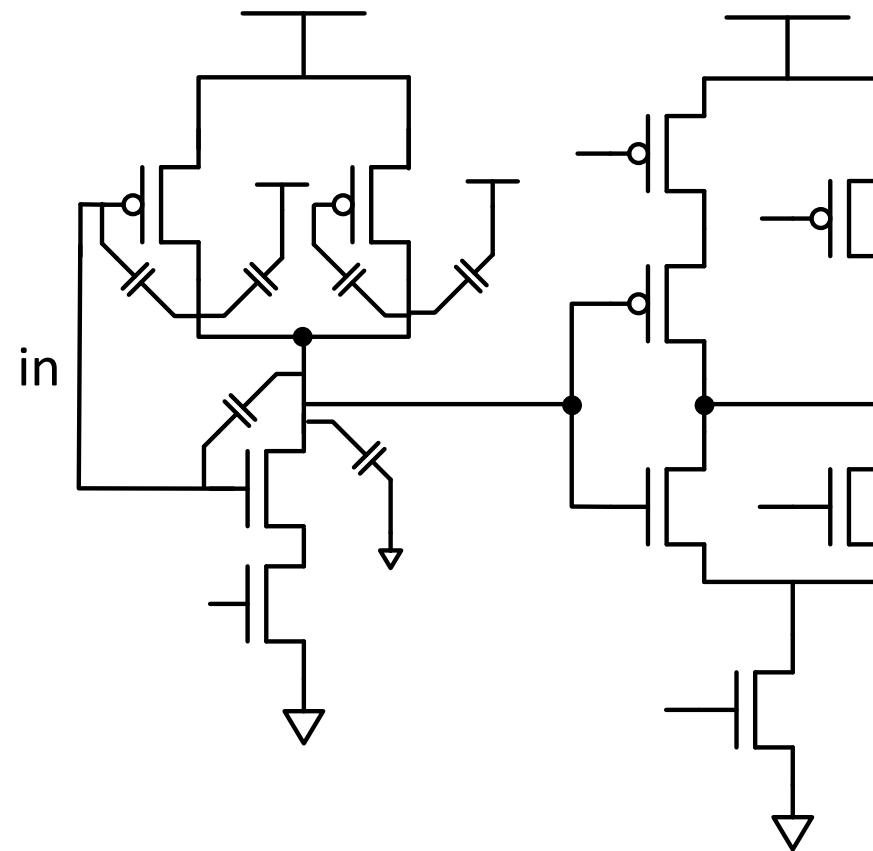
- Pmos or Nmos device drive capacitive load to charge (discharge) output to logic 1 (0)

# Simple Delay Model



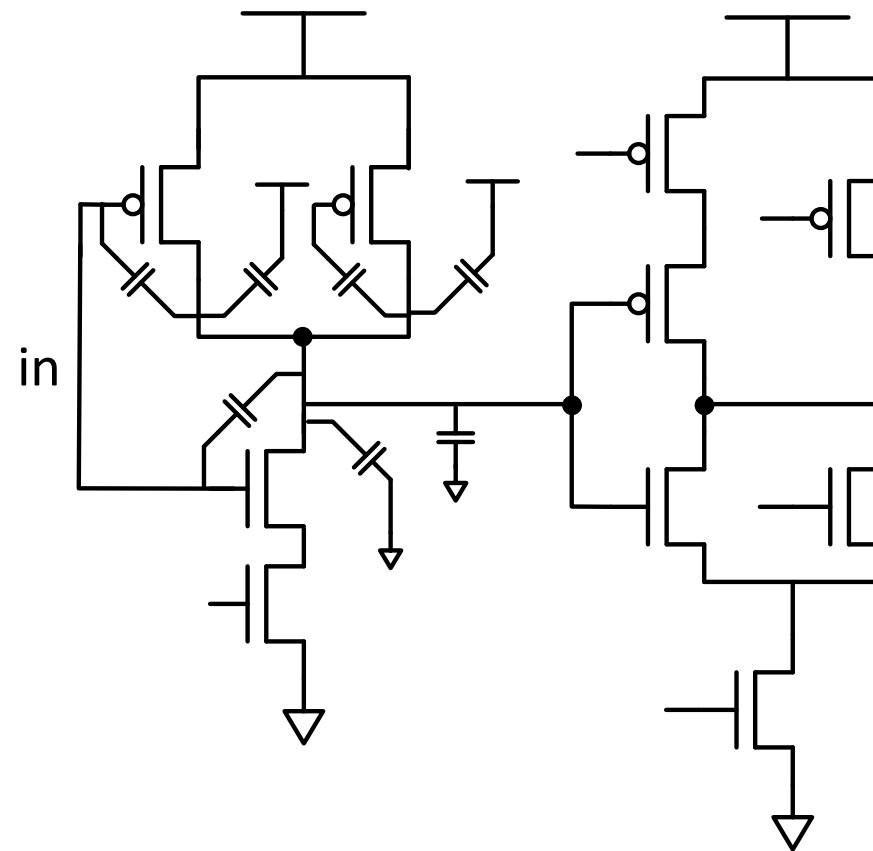
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# Simple Delay Model



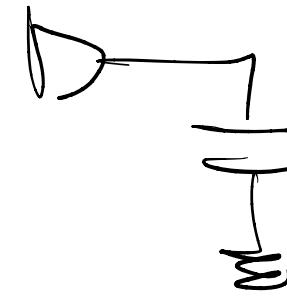
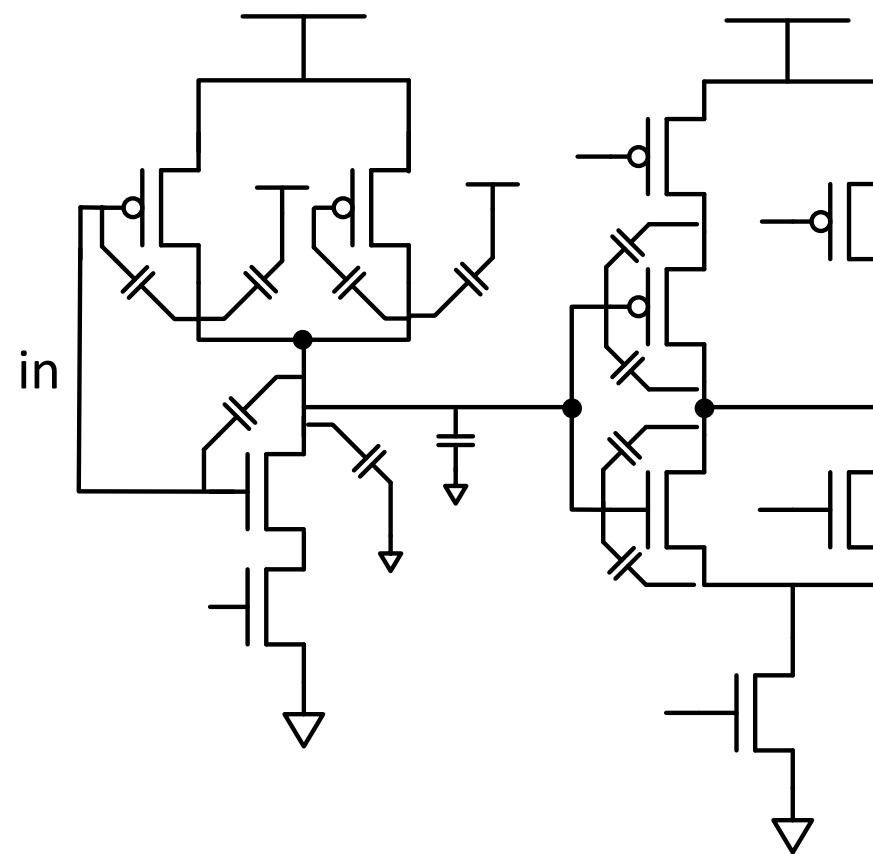
- PMOS or NMOS device drive capacitive load to charge (discharge) output to logic 1 (0)

# Simple Delay Model



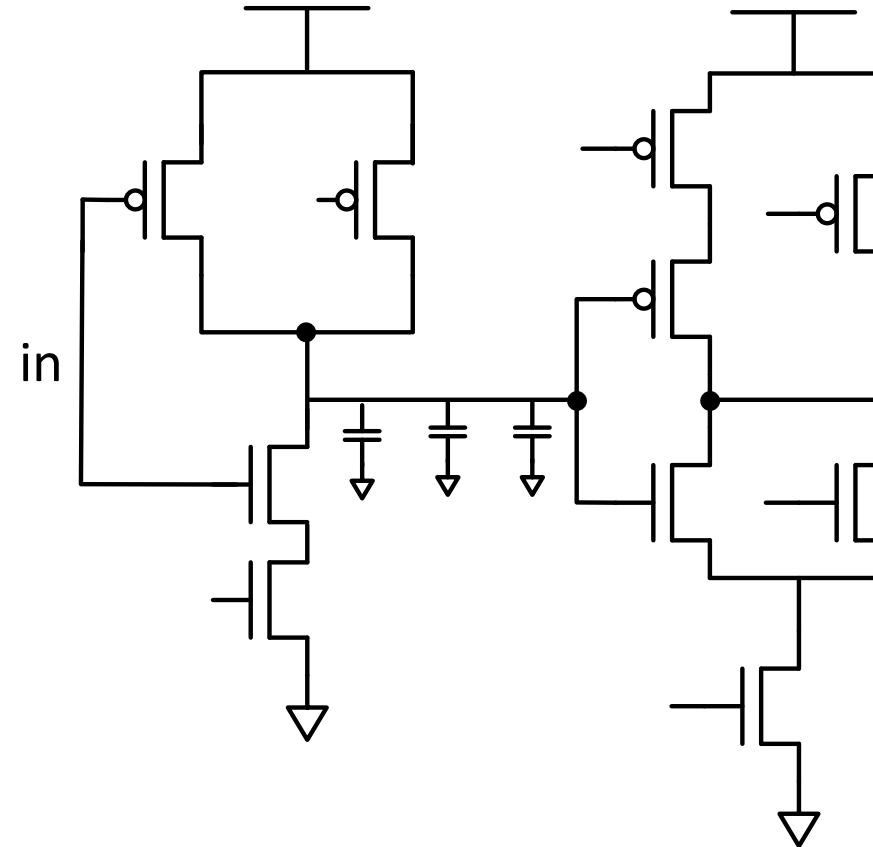
- PMOS or NMOS device drive capacitive load to charge (discharge) output to logic 1 (0)

# Simple Delay Model



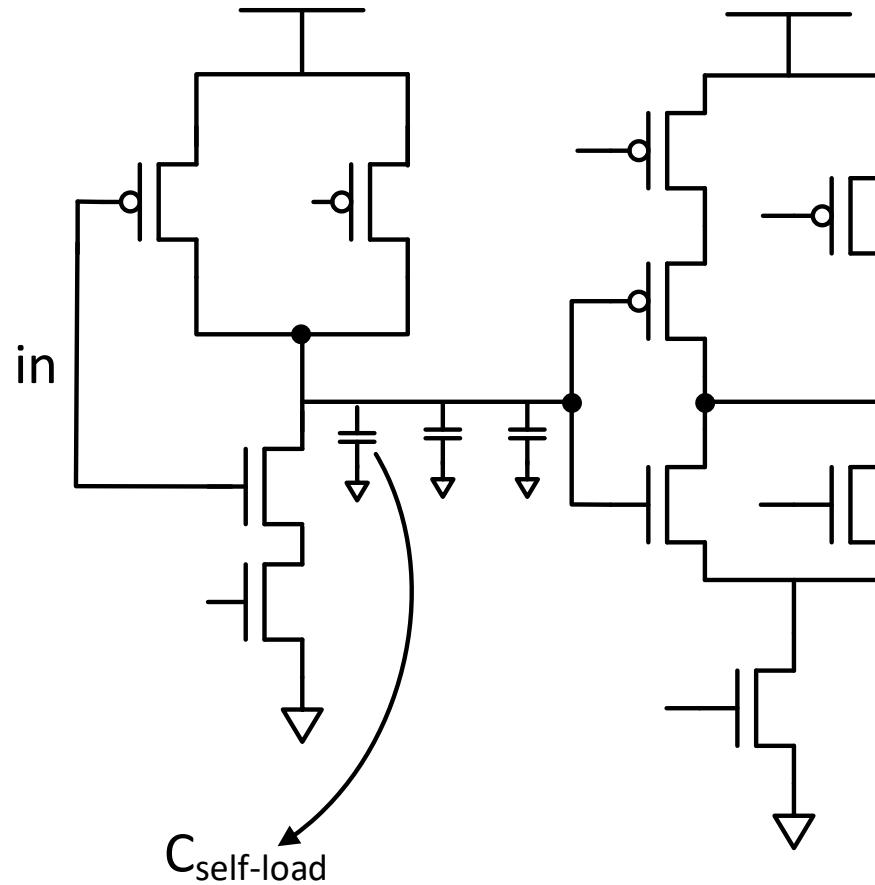
- PMOS or NMOS device drive capacitive load to charge (discharge) output to logic 1 (0)

# Simple Delay Model



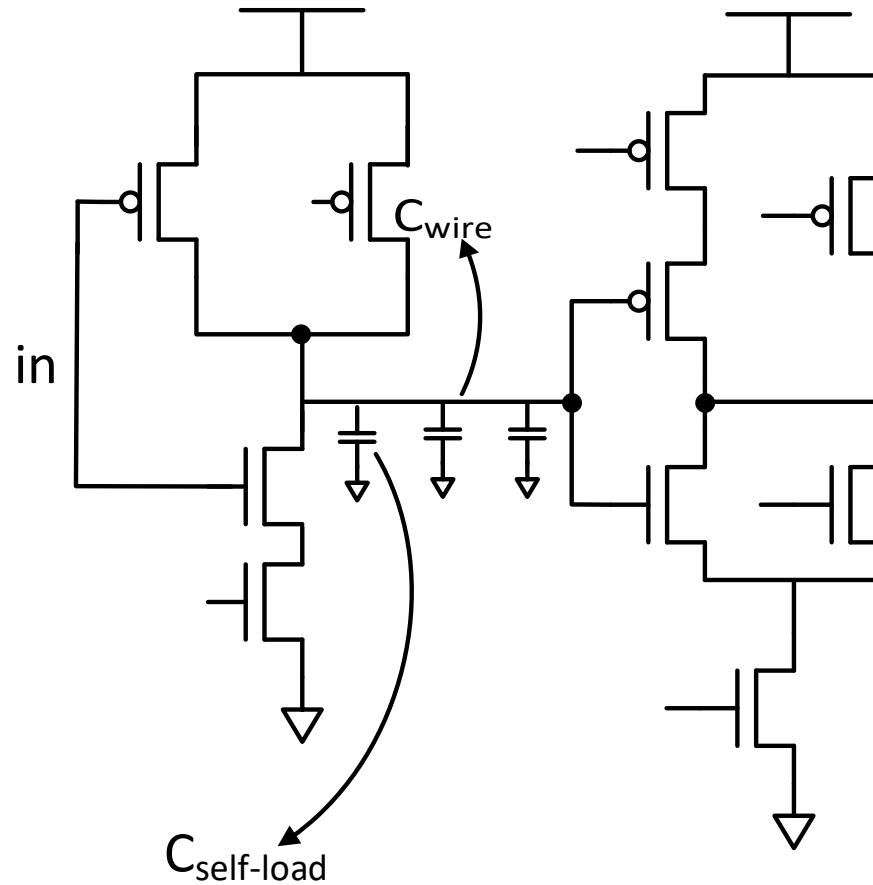
- Effectively 3 components

# Simple Delay Model



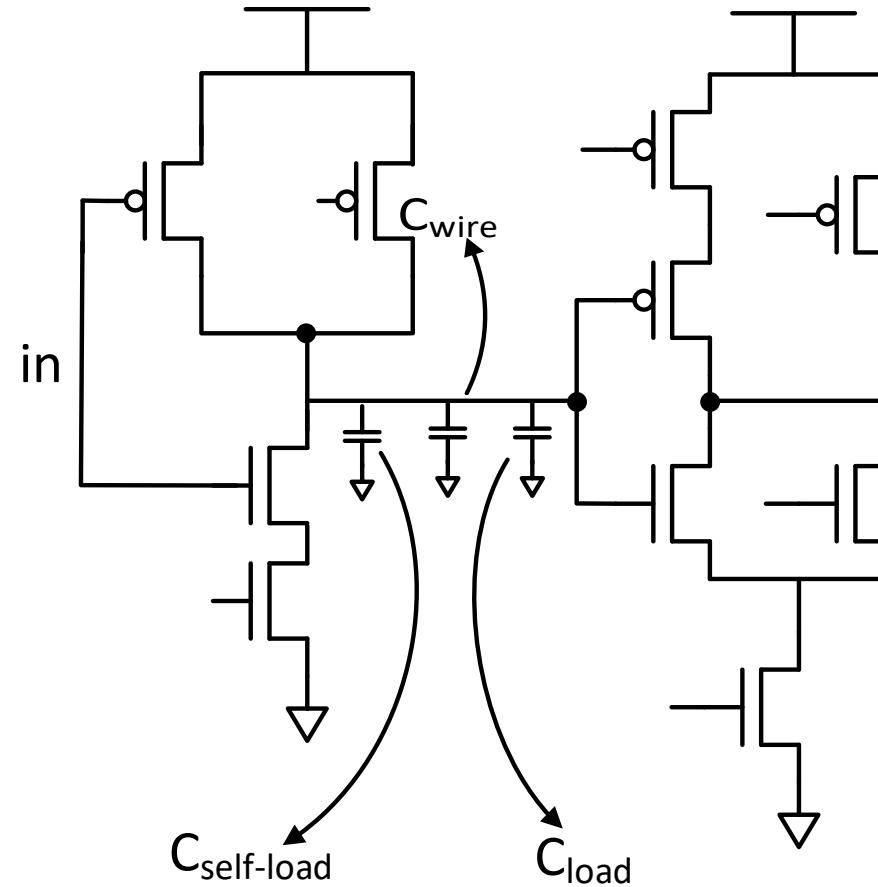
- Effectively 3 components

# Simple Delay Model



- Effectively 3 components

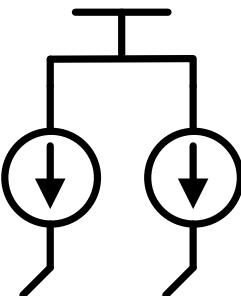
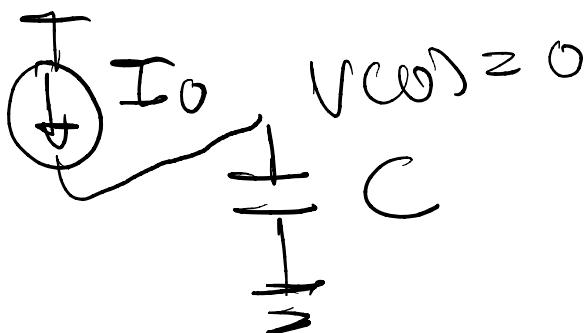
# Simple Delay Model



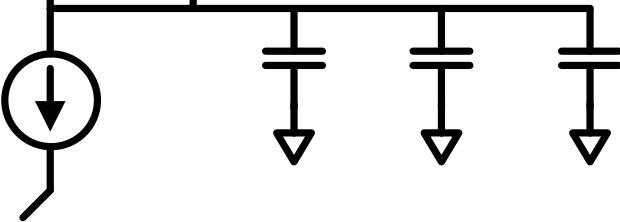
- Effectively 3 components

# Simple Delay Model

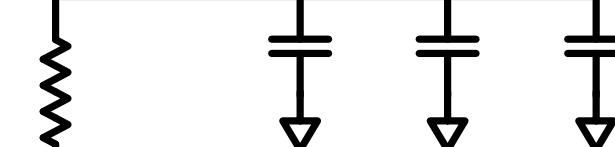
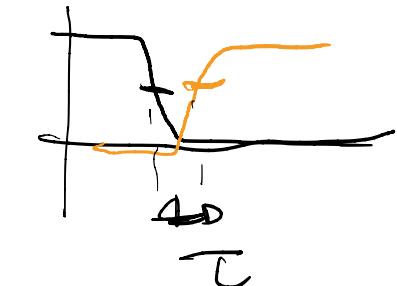
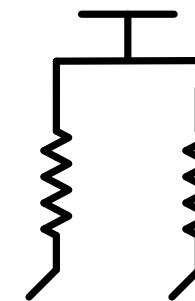
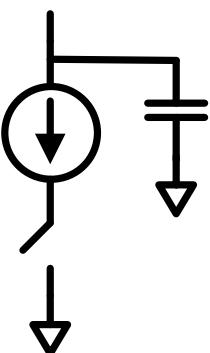
Input 50% → Output 50%



$$V_C(t) \geq \frac{1}{2} V_{dd}$$

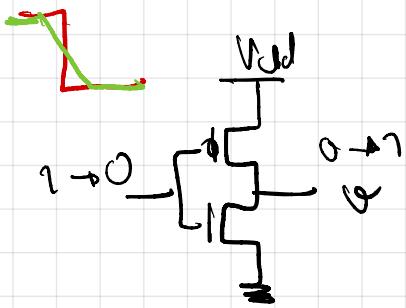


$$\tau = \frac{C V_{dd}}{\frac{1}{2} I_0}$$



$$\begin{aligned} & \int_0^\tau C \frac{dV_C}{dt} = \int_0^\tau I_0 dt \\ & = C \int_0^\tau \frac{dV_C}{dt} dt \\ & \frac{1}{2} C V_{dd}^2 = I_0 \tau \end{aligned}$$

- Circuit delay viewed as
  - Voltage-dependent current source charging/discharging capacitance
  - Voltage-dependent resistance charging/discharging capacitance



$$V(0) = 0V$$

$$V_{SGP} \approx Vdd$$

$$V_{SDP} = Vdd - V$$

$$V_{SDP}(f=0) = Vdd > V_{SG} - V_{th}$$

$$= V_{DD} - V_{th}$$



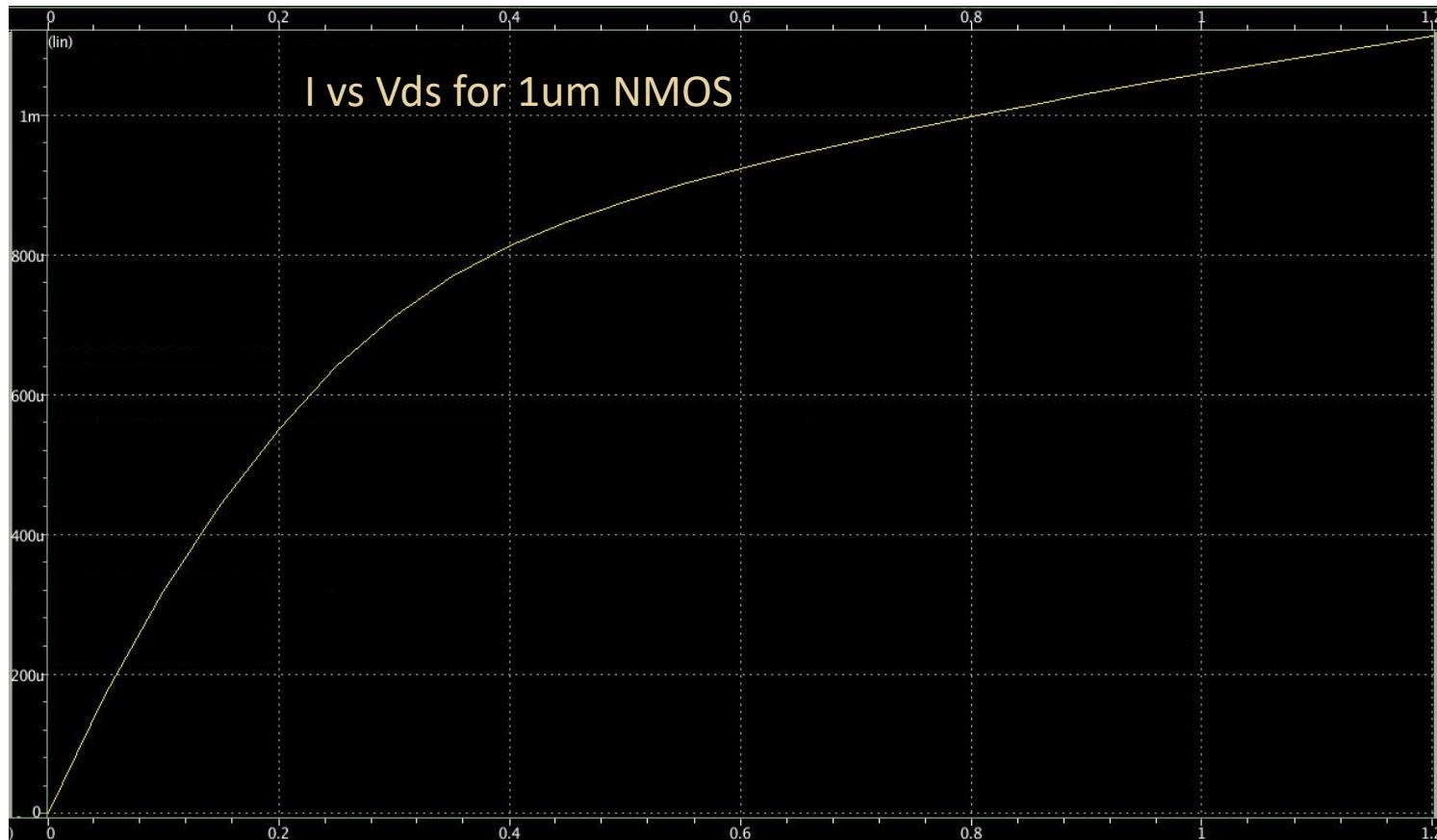
Saturation

How long is this true?

$$Vdd - V > V_{DD} - V_{th}$$

$$V_{th} \geq V$$

# Charging/Discharging Current



$I \propto W$

- Gate evaluating to Vdd
  - PMOS operating in different regions
  - Working out exact equations is not productive
  - Design perspective: Linear or Saturation, current drive scaled by  $W, 1/L$

$$I_s \propto \frac{w}{L}$$

$$\tau = \frac{C}{I_s} \propto \frac{L}{w} C(w)$$

?

$$C_{\text{self-load}} = a w$$

$$\tau = k \frac{L}{w} C(w)$$

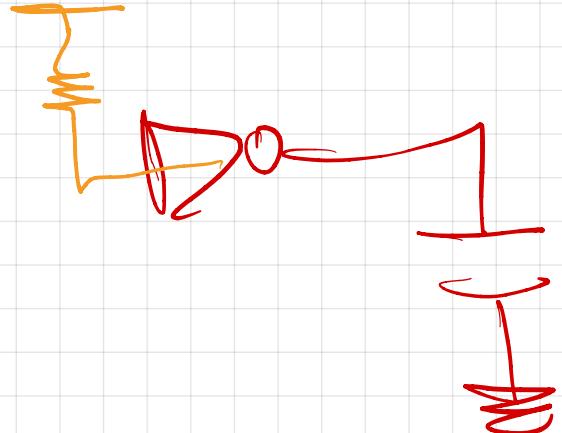
$$= k \frac{L}{w} (C_{\text{self-load}}(w) + C_0)$$

$$= k \frac{L}{w} (aw + C_0) = kL \underbrace{\left(\frac{aw + C_0}{w}\right)}_{\text{constant}}$$

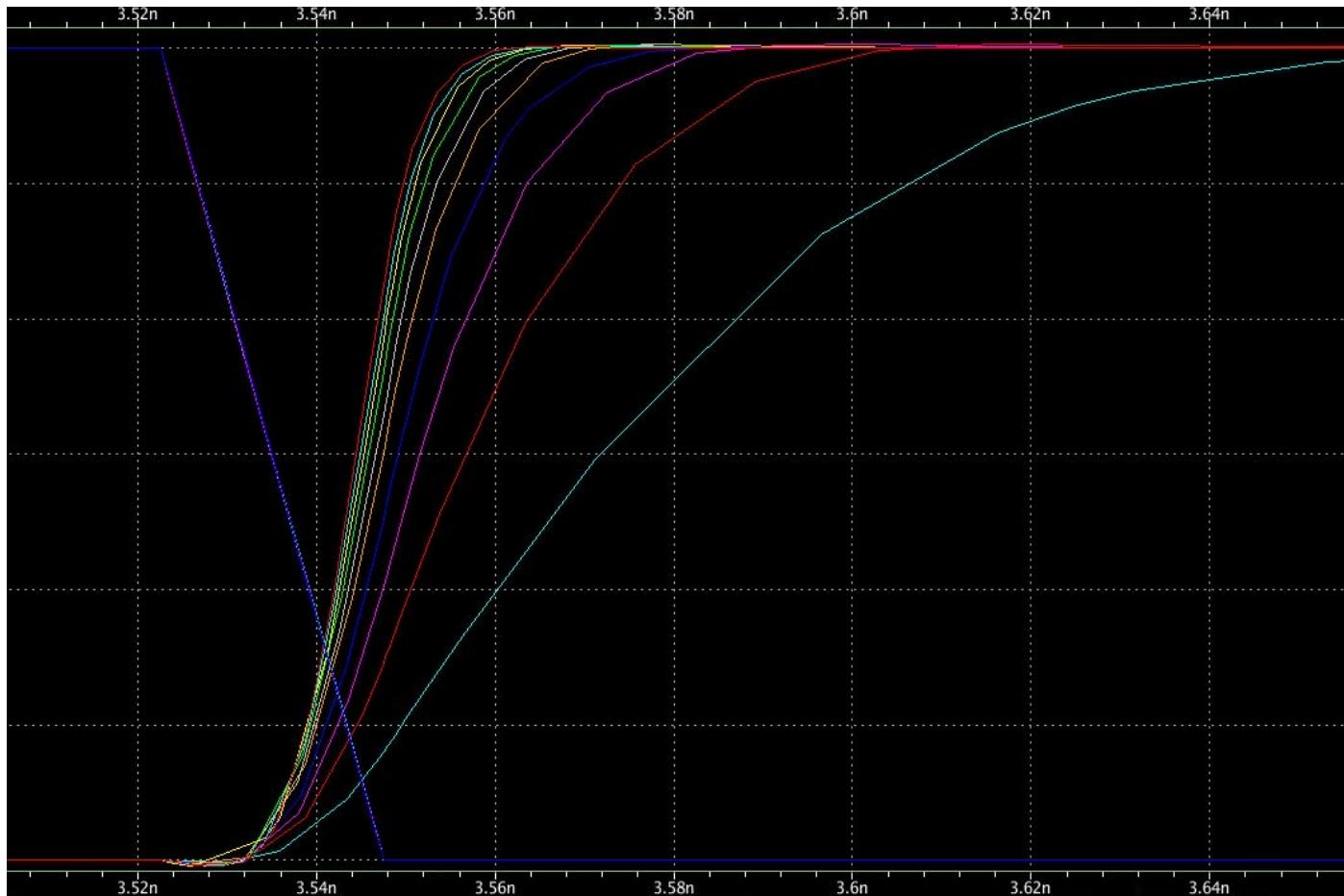
$$V_{\text{eff}} = kL \left(\frac{aw + C_0}{w}\right)$$

$$\tau \propto \frac{1}{w} \quad \times$$

$$\tau \propto \frac{aw + C_0}{w}$$

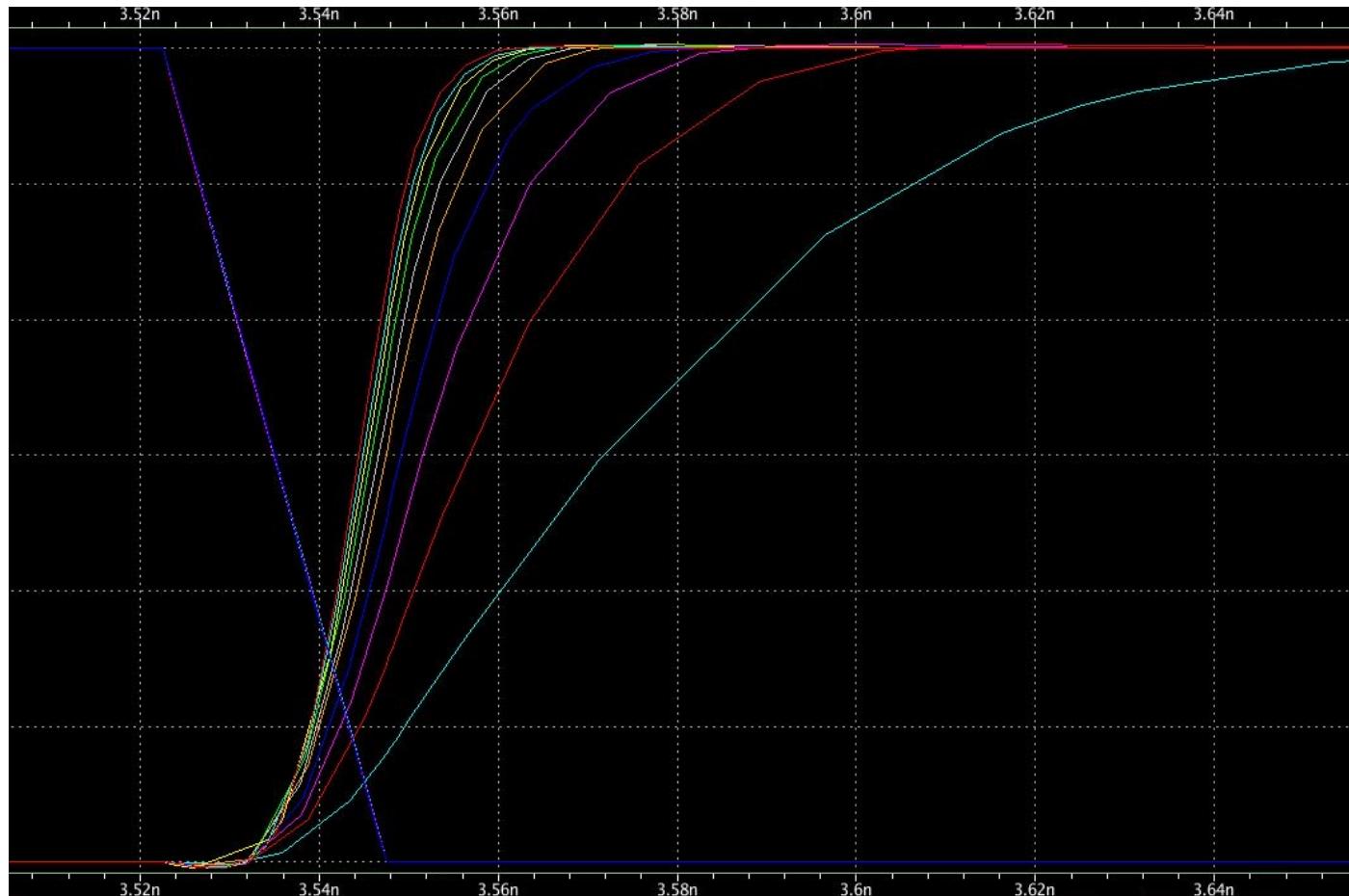


# Delay Dependence on W



- Does delay scale as  $1/W$ ?

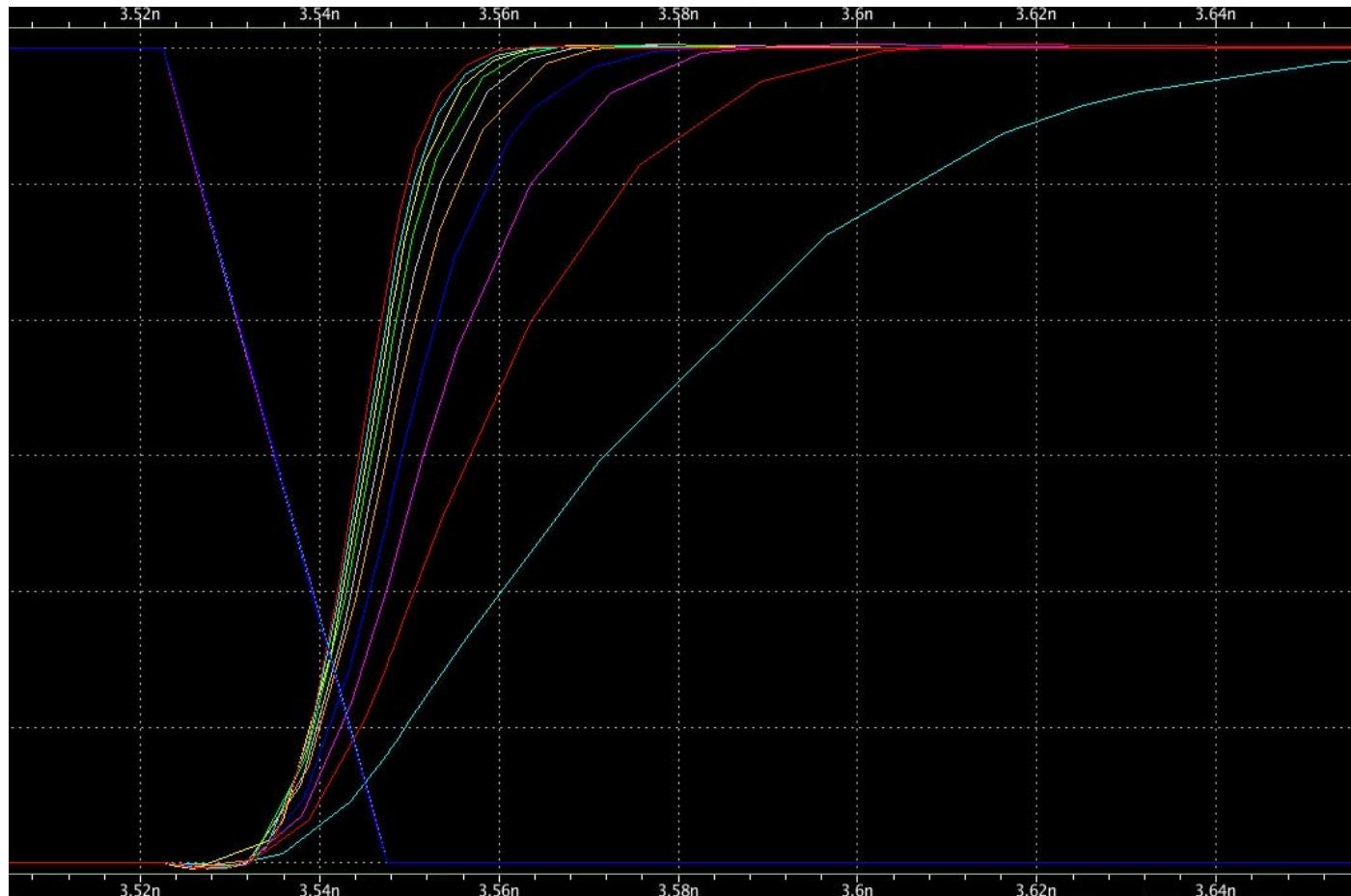
# Delay Dependence on W



If I have 2 cascaded inverters and the scale,  $x$  of the driving inverter is variable, how does the delay vary with  $x$

- Does delay scale as  $1/W$ ?

# Delay Dependence on W



Self-loading!

- Does delay scale as  $1/W$ ?



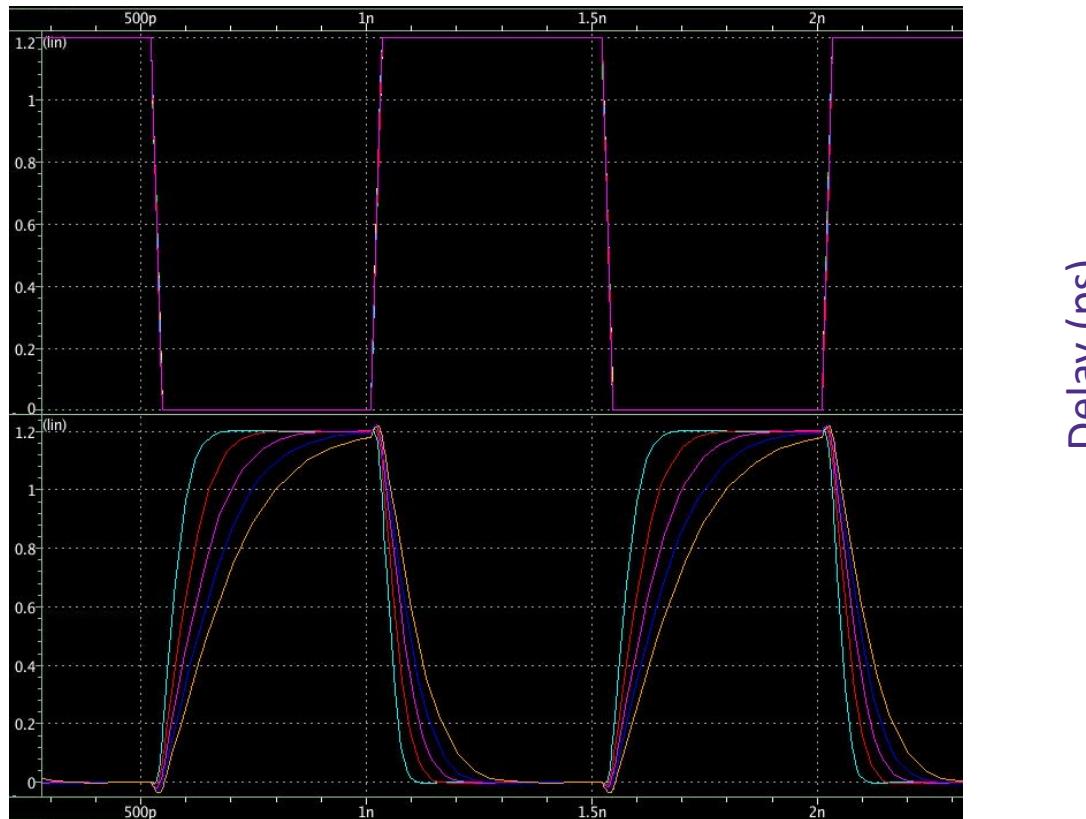
If I have 2 cascaded inverters and the scale, x of the driving inverter is variable, how does the delay vary with x

# Delay Dependence on L

$$I \propto \frac{W}{L}$$

$$\tau \propto \frac{L C}{W}$$

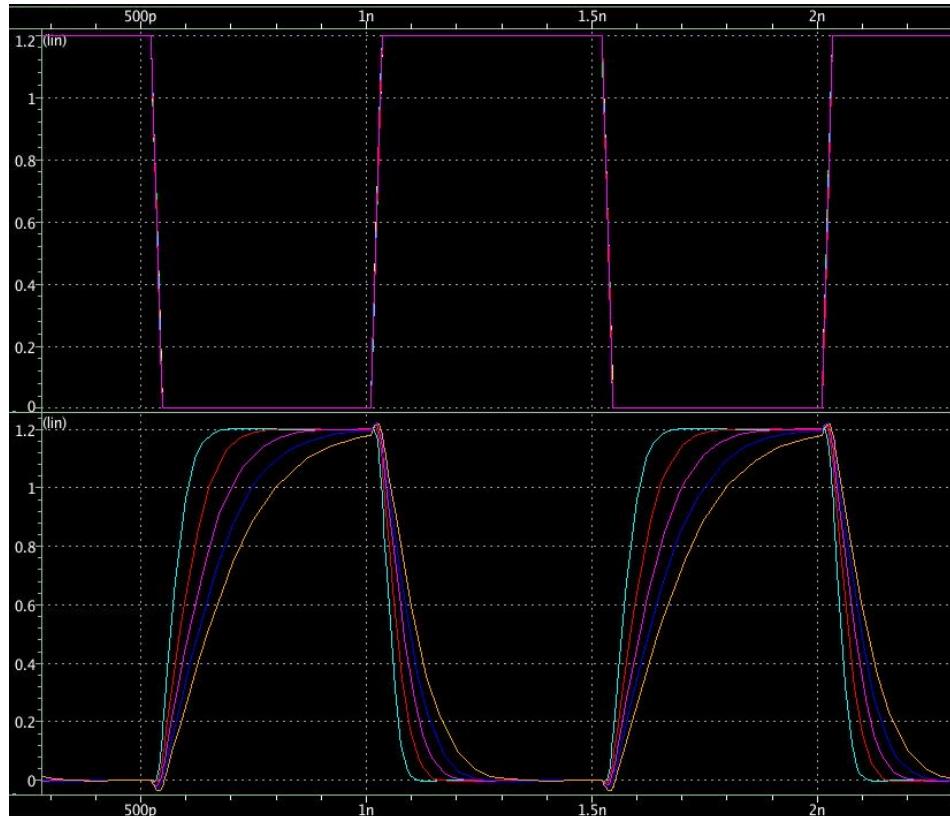
Delay vs. L\_factor



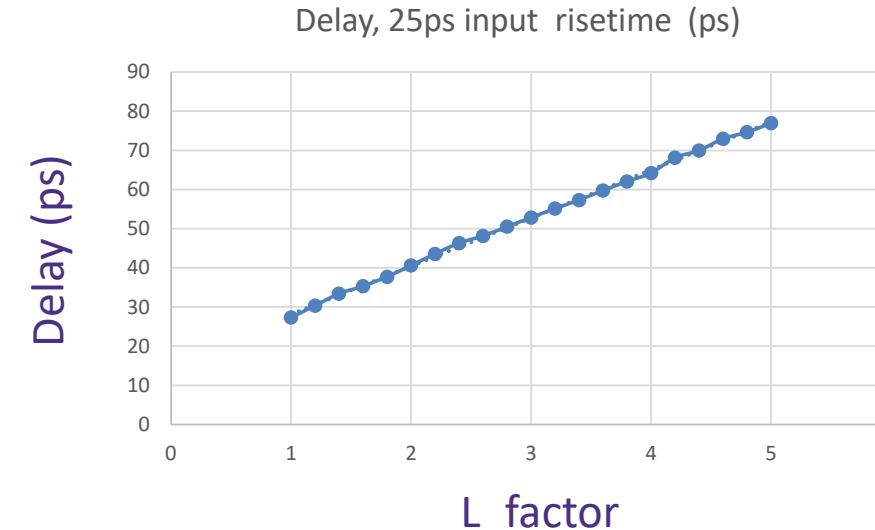
L\_factor

- If W and L are both designer tunable, why do most digital designs tweak only W?

# Delay Dependence on L

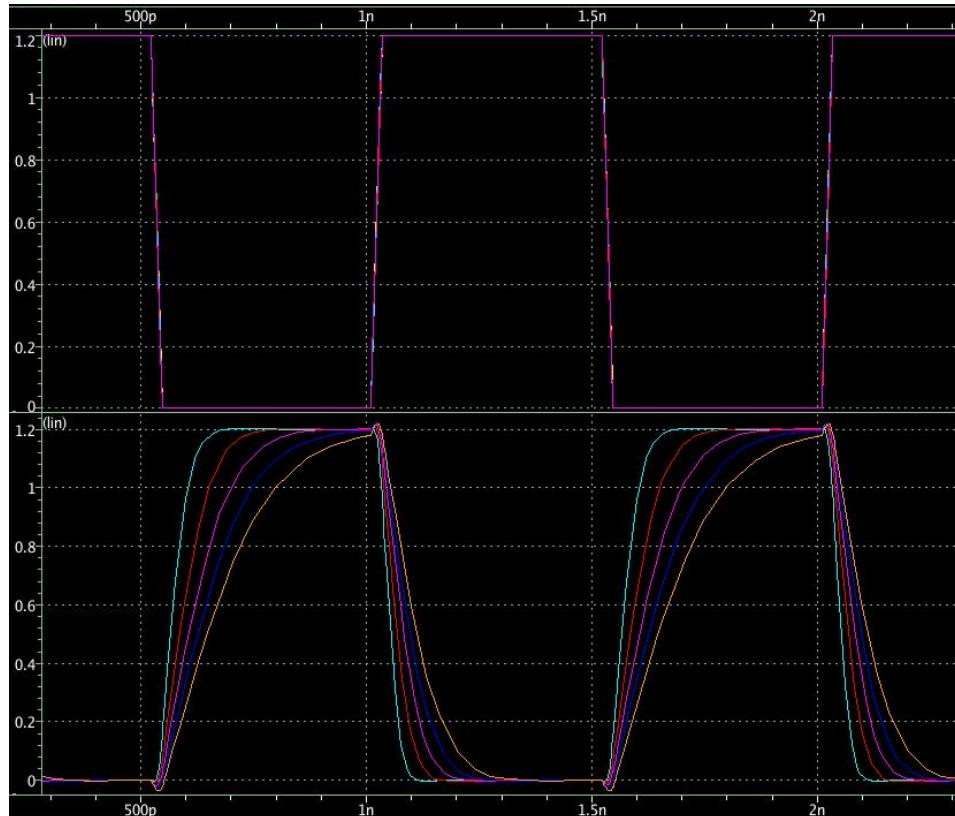


Delay vs. L\_factor



- If W and L are both designer tunable, why do most digital designs tweak only W?

# Delay Dependence on L



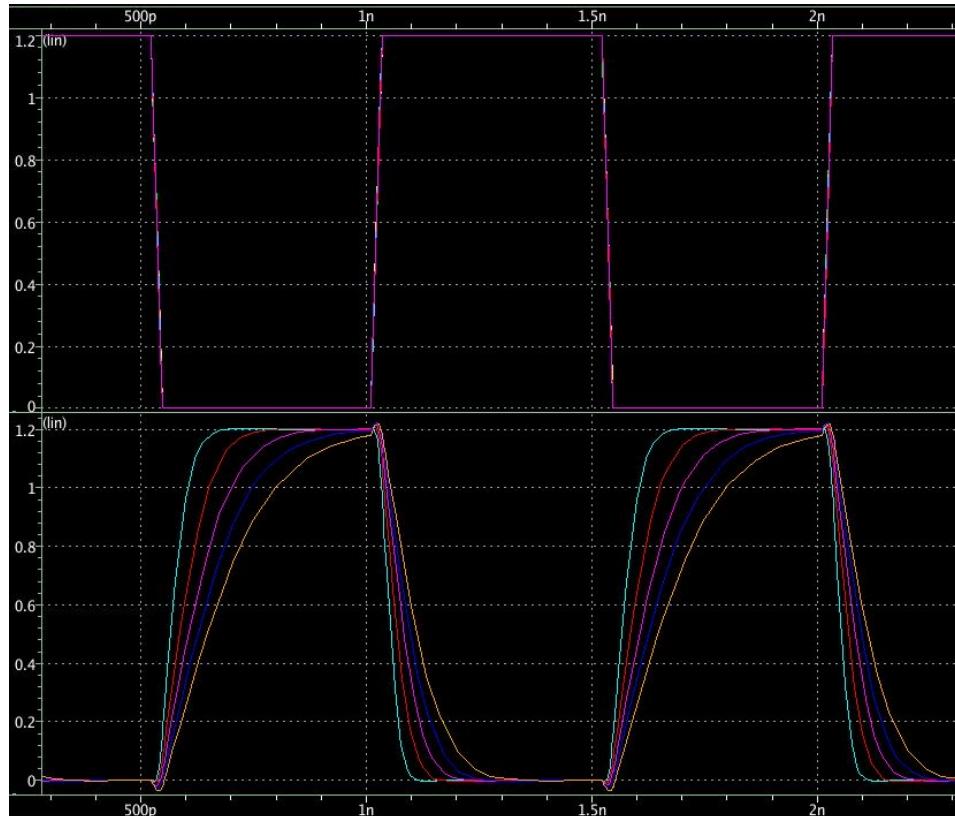
Delay vs. L\_factor

Delay (ps)

L\_factor

- If W and L are both designer tunable, why do most digital designs tweak only W?

# Delay Dependence on L



Delay vs. L\_factor

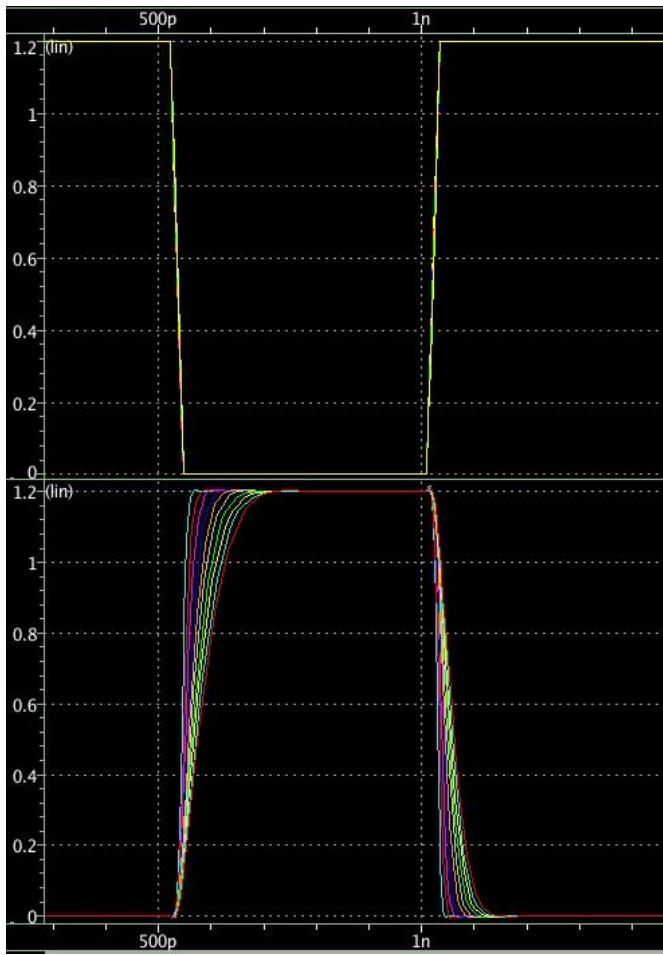
Delay (ps)

L\_factor

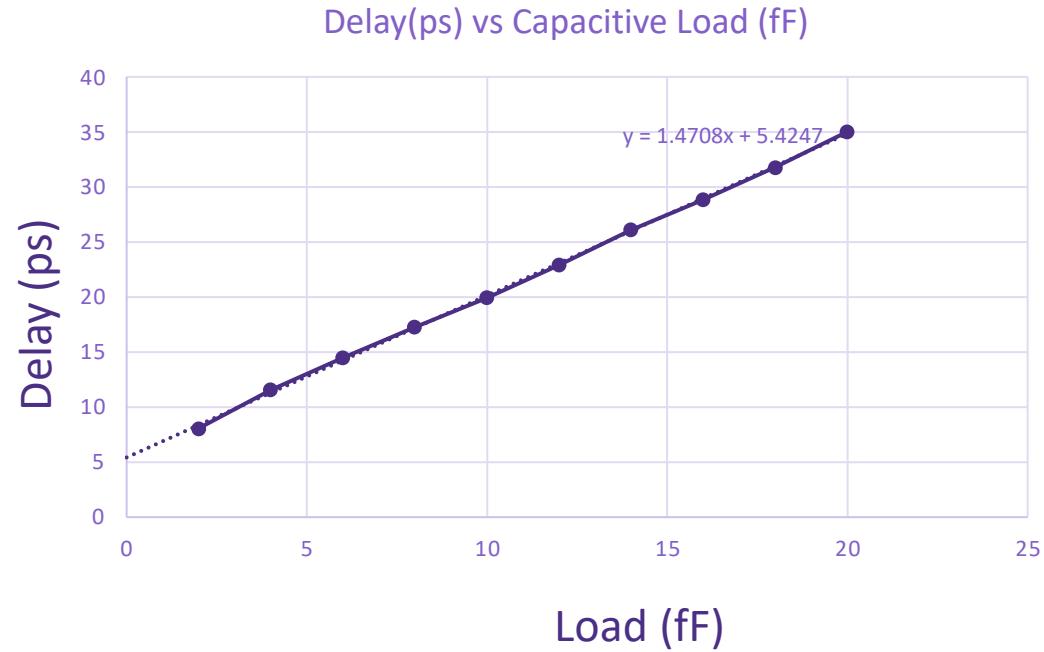
Extra:  
Relationship with  
L is Linear (Affine, y-intercept)

- If W and L are both designer tunable, why do most digital designs tweak only W?

# Delay Dependence on C<sub>Load</sub>

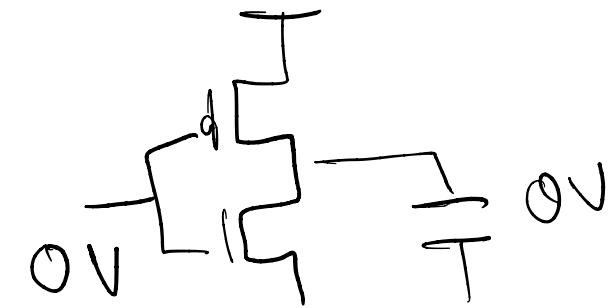


$$\tau \propto \frac{C}{I_S} \alpha (C_{\text{self-load}} + C_{\text{load}})$$



- Self loading causes non-zero intercept

# Delay Dependence on Vdd



$$\tau = \frac{C_{\text{load}} V_{dd}}{2 I_S} \propto \frac{V_{dd}}{(V_{os} - V_{th})^2}$$

SG

$$\propto \frac{V_{dd}}{(V_{dd} - V_{th})^2}$$

$$\frac{1}{V_{dd}} \quad (V_{th} \text{ small})$$

$$(V_{dd} - V_{th})^2 \approx V_{dd}^2$$

# Delay Dependence on Vdd

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- $\uparrow V_{dd} \rightarrow \downarrow \text{Delay}$

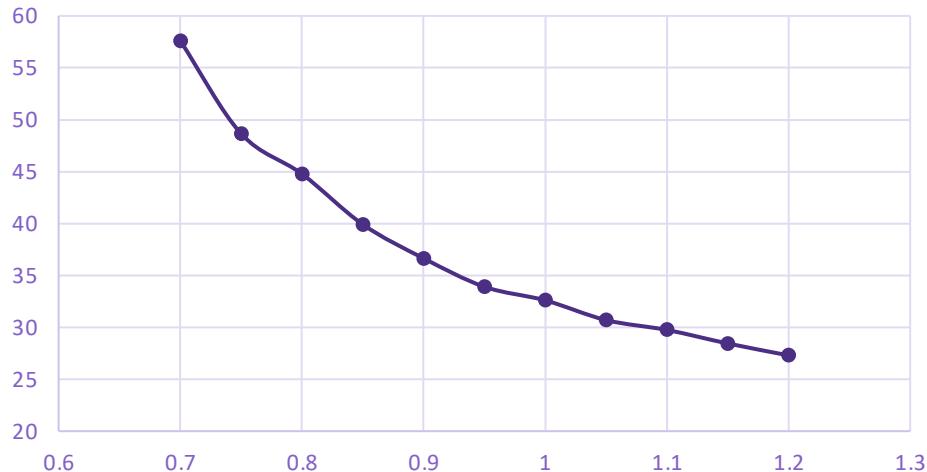
# Delay Dependence on Vdd

---

- $\uparrow V_{dd} \rightarrow \downarrow \text{Delay}$
- $\tau = \frac{Q_{load}}{I} = \frac{C_{load}V_{dd}}{I} = \frac{kC_{load}V_{dd}}{\beta(V_{dd}-V_{th})^\alpha}$

# Delay Dependence on Vdd

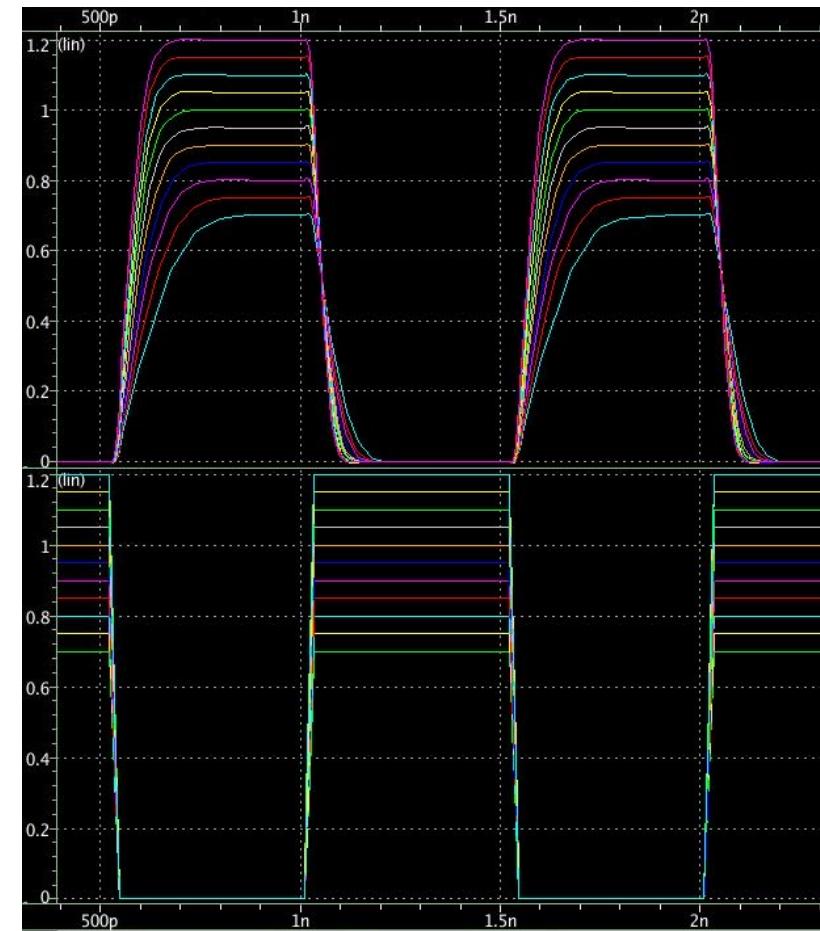
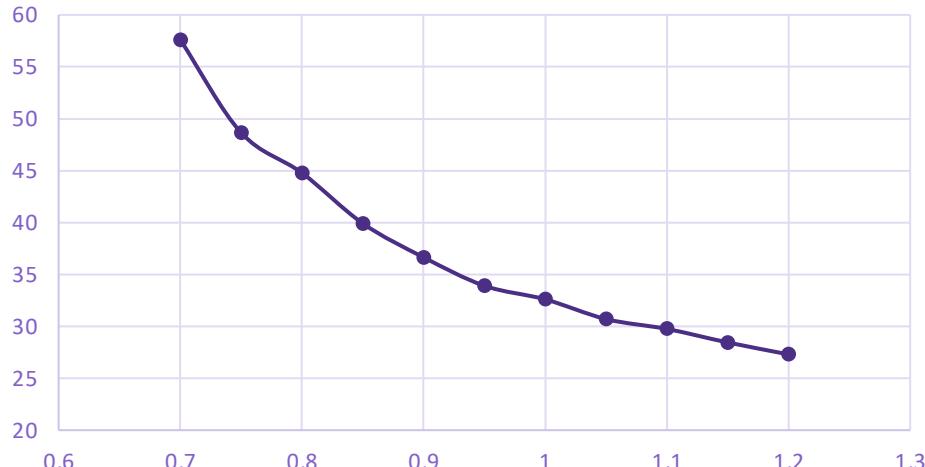
Delay(ps) vs Vdd



- $\uparrow V_{dd} \rightarrow \downarrow \text{Delay}$
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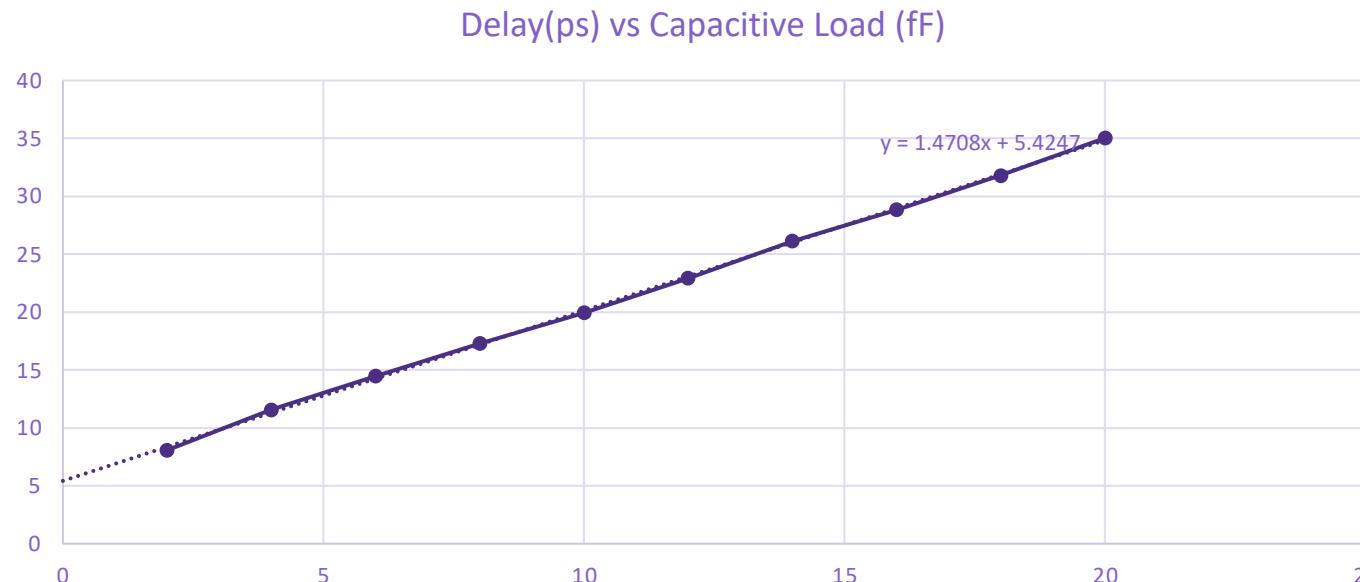
# Delay Dependence on Vdd

Delay(ps) vs Vdd



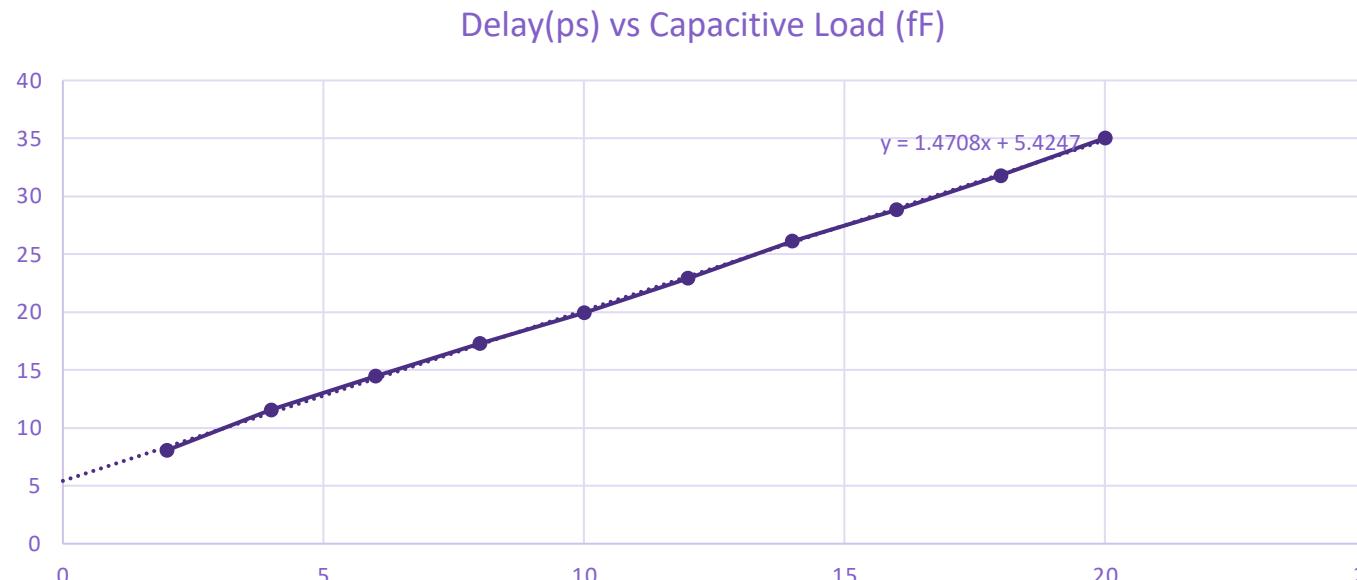
- $\uparrow V_{dd} \rightarrow \downarrow \text{Delay}$
- $$\tau = \frac{Q_{load}}{I} = \frac{C_{load}V_{dd}}{I} = \frac{kC_{load}V_{dd}}{\beta(V_{dd}-V_{th})^\alpha}$$

# CMOS Inverter Delay : Inverter model



- Simplified views:
  - Effective resistance
  - Notice  $2W$  allows twice the current (half the resistance)
  - $2L$  allows half the current
  - Limitations (small signal resistance is diff.)
- Can also think of equivalent current source?
  - Current source a function of  $V_{gs}$ ,  $V_{th}$   $W$ ,  $L$  (No control over  $V_{th}^*$ ,  $\mu$ ,  $C_{ox}$ )
  - Norton resistance for  $\lambda$
  - Typically device operates in saturation while bringing output to 50%

# CMOS Inverter Delay : Inverter model



Estimate  $R(V)$   
 $I_{eff}(V)$

- Simplified views:
  - Effective resistance
  - Notice  $2W$  allows twice the current (half the resistance)
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  - Norton resistance for  $\lambda$
  - Typically device operates in saturation while bringing output to 50%

# Delay analysis : Some Thoughts

- Designers casually refer to the “resistance of the inverter”
  - If this resistance is a constant, what will be the impact of voltage on delay with the RC model?
- Scaled technologies rely on  $\uparrow C_{ox}$  for improved current drive...
  - But what's the point if that increases the load of the transistor?!

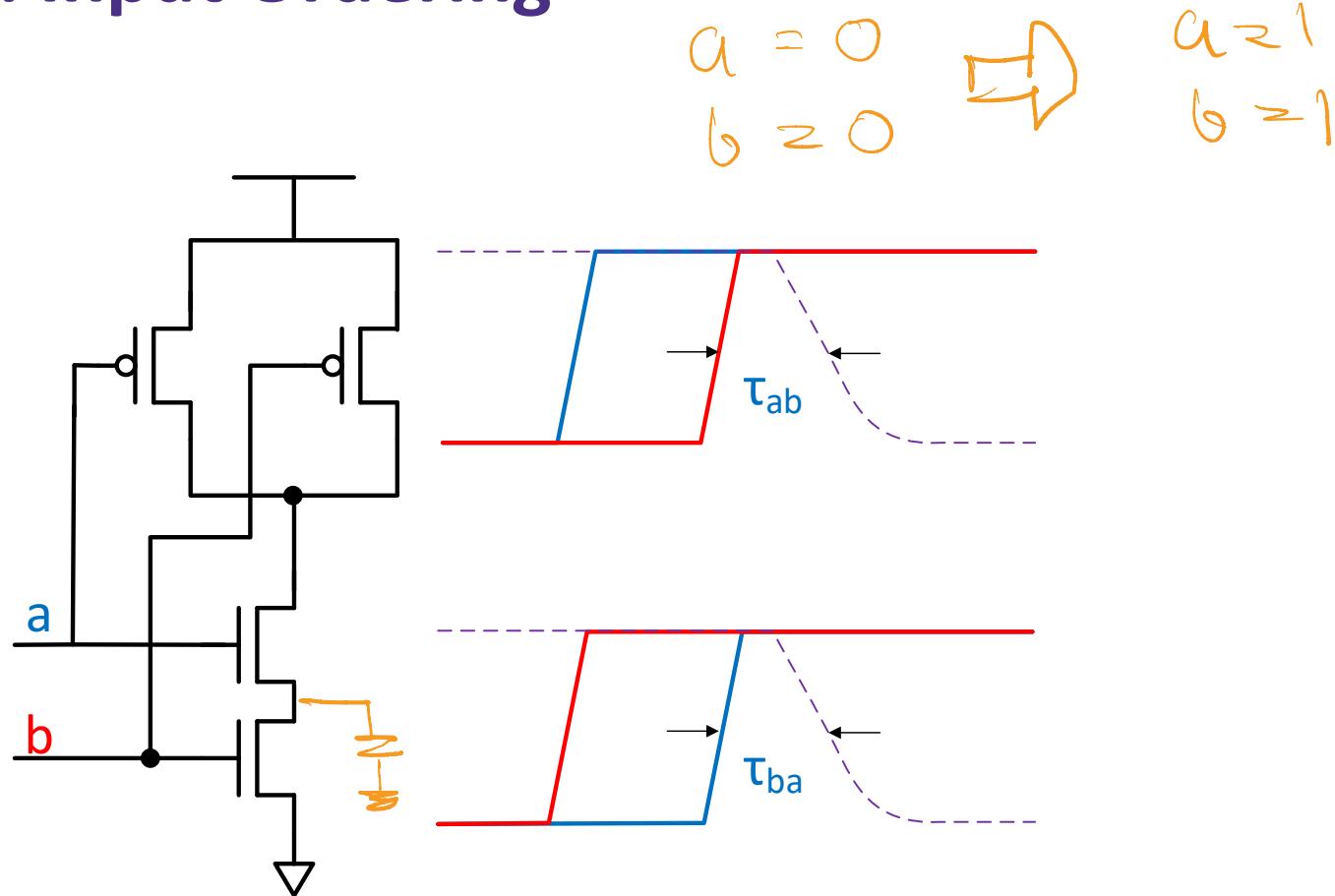
# Delay analysis : Some Thoughts

- Designers casually refer to the “resistance of the inverter”
  - If this resistance is a constant, what will be the impact of voltage on delay with the RC model?
  - Resistance is Voltage Dependent!
- Scaled technologies rely on  $\uparrow C_{ox}$  for improved current drive...
  - But what's the point if that increases the load of the transistor?!

$$I = \frac{1}{2} \beta (V - V_t)^2$$

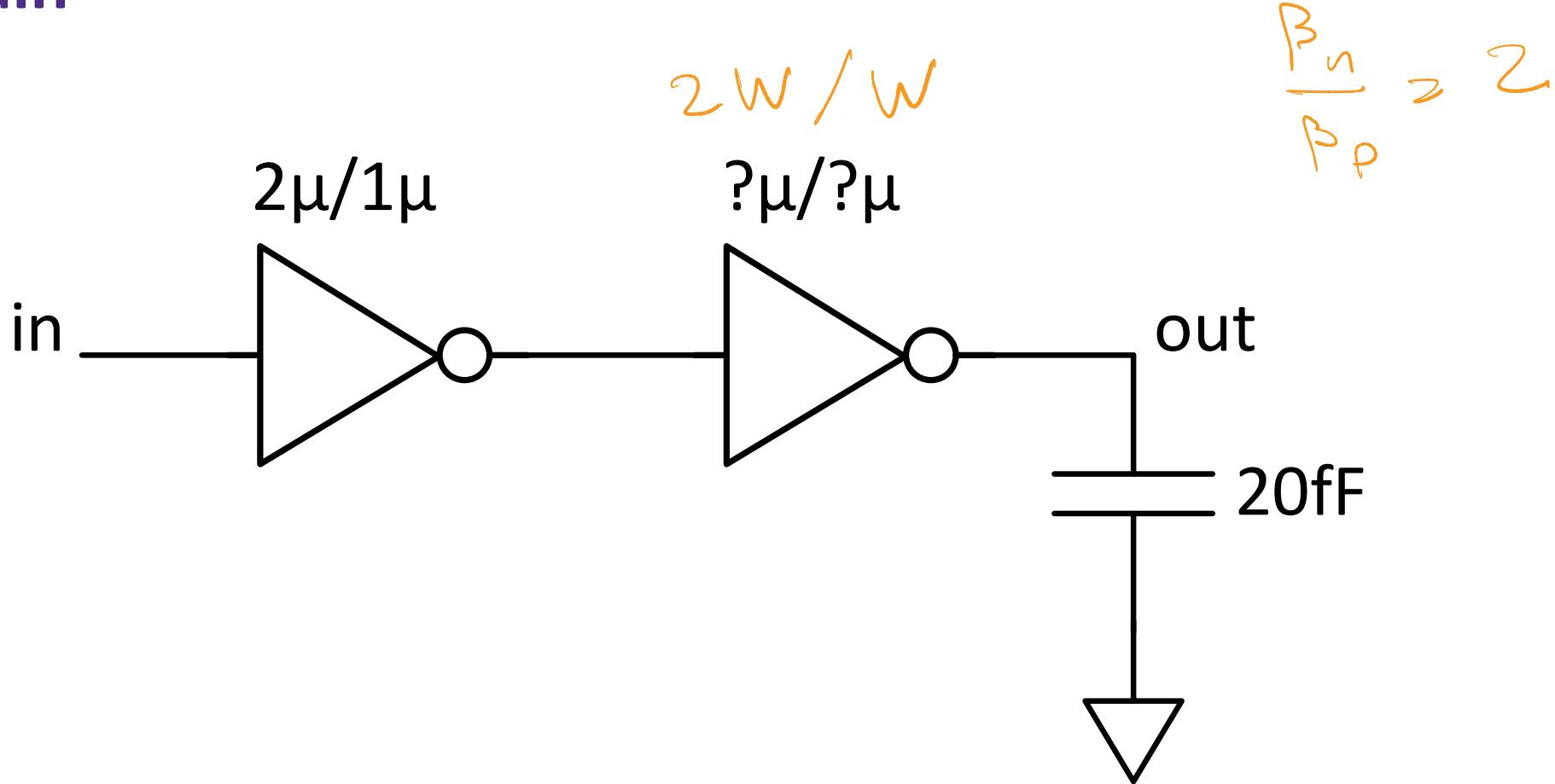
$$\beta = \mu C_{ox} \frac{W}{L}$$

# CMOS Gate Delay : Input Ordering



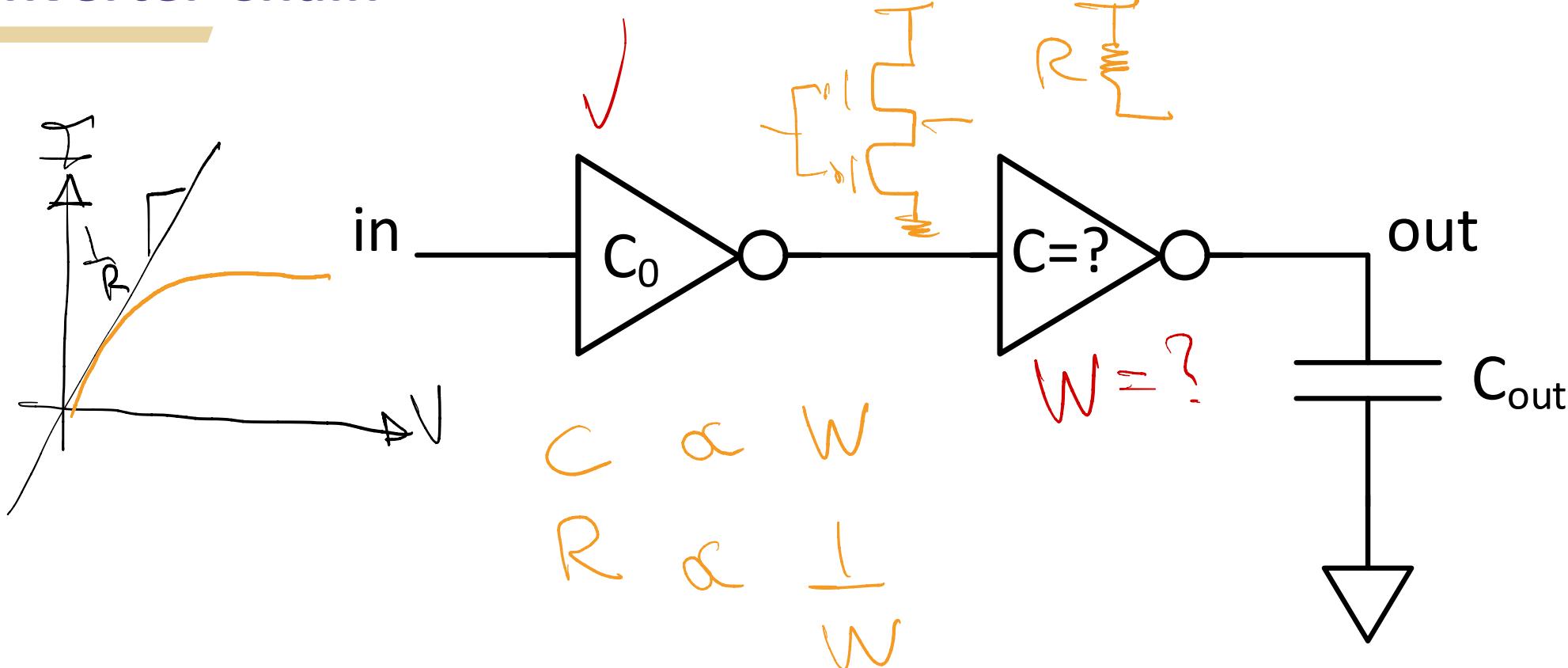
- Which is faster?  $\tau_{ba}$  or  $\tau_{ab}$  ??

# Inverter Chain



- Total delay =  $\sum \tau_i$
- How can we achieve minimum delay?

# Inverter Chain



- In general, given a chain with:
  - Fixed input cap
  - Output load

$RC = \text{constant}$   
→ Does not depend  
on  $W$

# Inverter Chain (contd)

- Assume balanced rise/fall delay

$$\tau = \sum \tau_i = \sum (R_i C_{i+1} + R_d)$$

$$R = k/C$$

$$\tau = R_0 C_1 + R_1 C_{out}$$

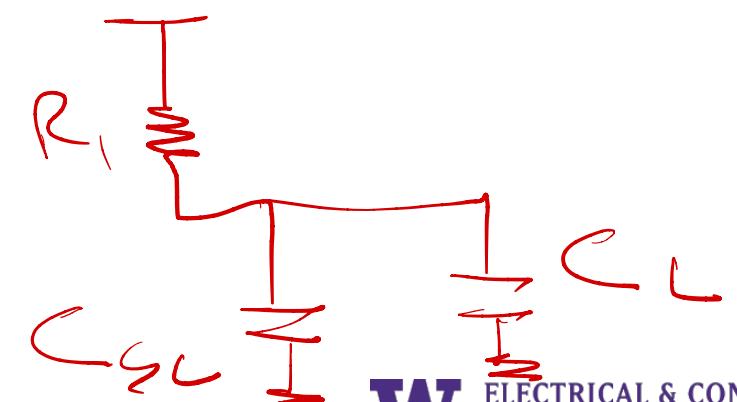
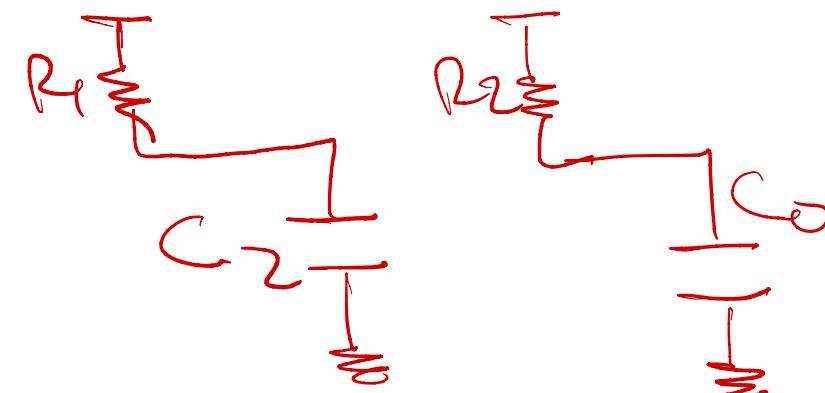
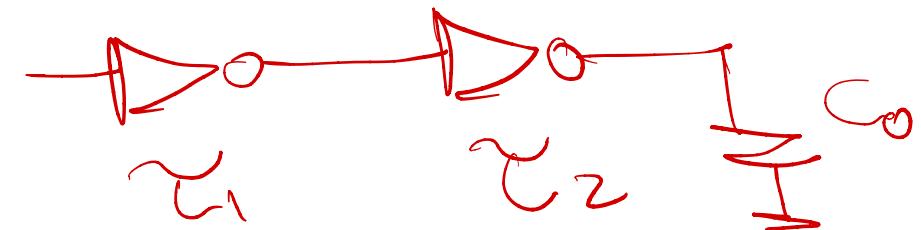
$$+ 2R_d$$

$$= \frac{kC_1}{C_0} + \frac{kC_{out}}{C_1}$$

$$= k \left( \frac{C_1}{C_0} + \frac{C_{out}}{C_1} \right)$$

- Setting  $\frac{\partial \tau}{\partial C_1} = 0$  gives ...

$$R_d + f(w) = \frac{V_W}{R_1(C_{SL} + C_L)} \frac{1}{\frac{1}{R_1} + \frac{1}{C_L}} C_{SL} \leftarrow$$



$$T_i = R_d + R_i C_{i+1}$$



$$R_i \propto \frac{1}{W_i} \Rightarrow R_i = \frac{\tilde{R}}{W_i}$$

$$C_i \propto W_i$$

$$C_i = \frac{1}{\tilde{R}} W_i$$

$$\Rightarrow W_i = C_i \frac{\tilde{R}}{1}$$

$$R_i = \tilde{R} \frac{1}{C_i} \cdot \frac{1}{C_i}$$

$$R_i = R \frac{1}{C_i}$$

$$R_i C_i \approx k \approx R_d$$

$$R_1 C_2 + R_2 C_{out}$$

$$\frac{U}{G_2}$$

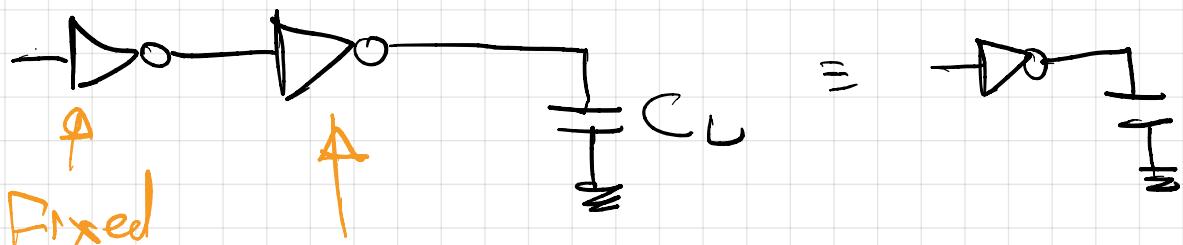
$$= k \frac{C_2}{C_1} + R \frac{C_{out}}{C_2}$$

## Inverter Chain (contd)

- Assume balanced rise/fall delay
- $\tau = \sum \tau_i = \sum R_i C_{i+1}$
- $R = k/C$
- $\tau = R_0 C_1 + R_1 C_{out}$

$$\begin{aligned} &= \frac{kC_1}{C_0} + \frac{kC_{out}}{C_1} \\ &= k \left( \frac{C_1}{C_0} + \frac{C_{out}}{C_1} \right) \end{aligned}$$

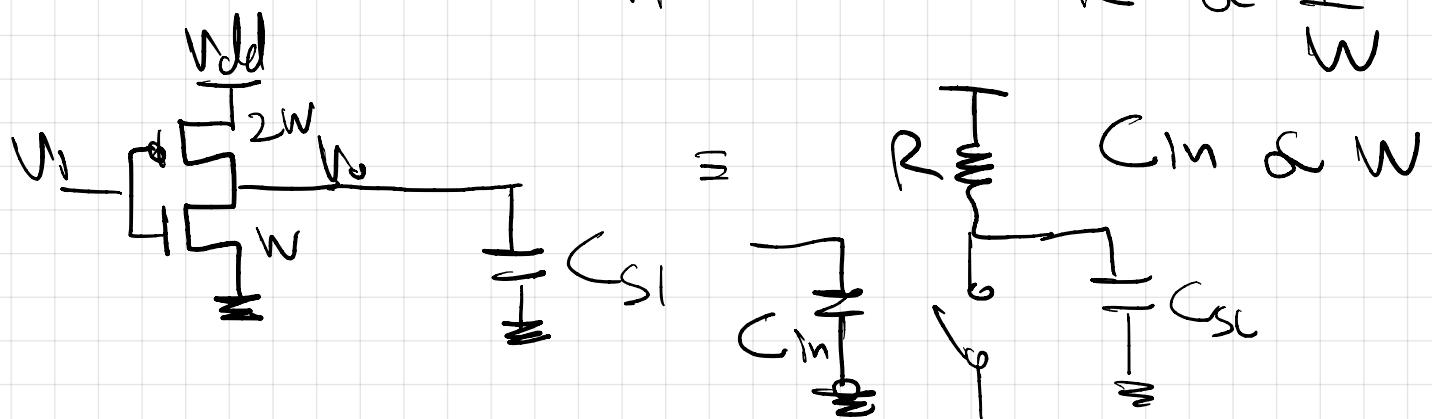
- Setting  $\frac{\partial \tau}{\partial C_1} = 0$  gives ...
- $C_1 = k\sqrt{C_0 C_{out}}$
- $\tau_{min} = 2k\sqrt{C_{out}/C_0}$



Optimal  
size?  
?

$$\frac{\beta_N}{\beta_P} = 2$$

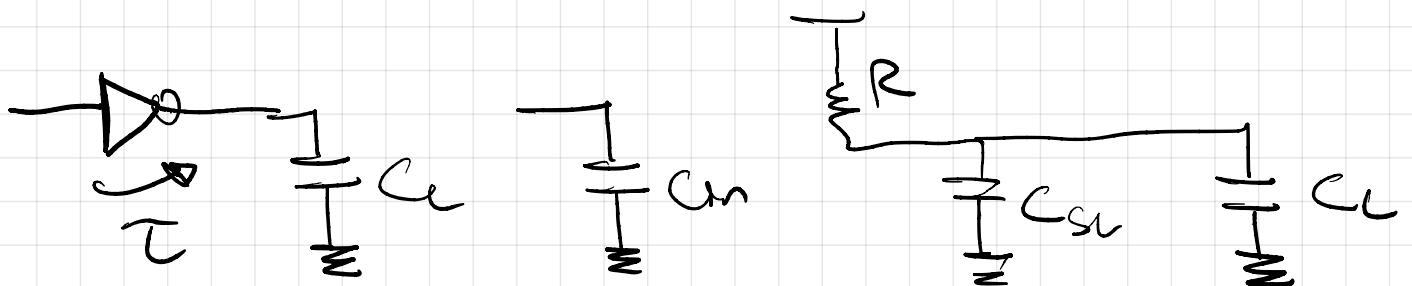
$C_{SL} \propto W$   
 $R \propto \frac{1}{W}$



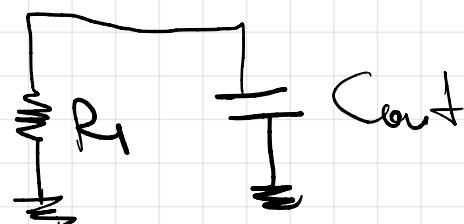
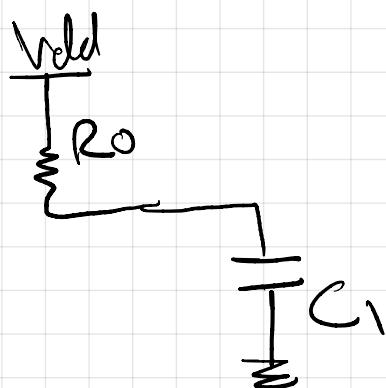
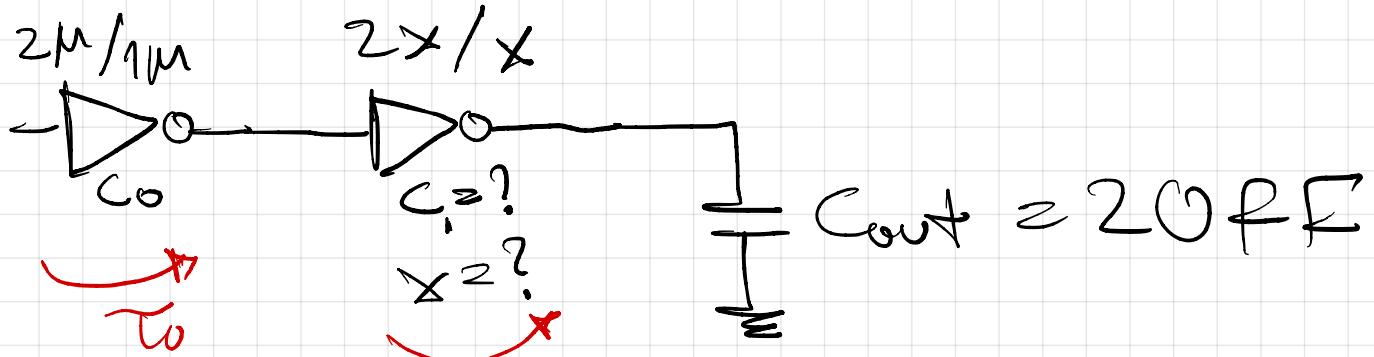
$$R C_{SL} = R_d = \text{propagation delay}$$

$$R C_{IN} = R \quad (\text{independent of } W)$$

From this model



$$\begin{aligned} T &= R (C_{SL} + C_L) \\ &\approx R_d + R C_L \end{aligned}$$



$$C_1 \propto x$$

$$C_1 = k_c \cdot x$$

$$\Rightarrow \frac{C_1}{k_c} \approx x$$

Leaving out  $C_{sc}$

$$\tau = \tau_o + \tau_i = (\underbrace{P_d + R_o C_1}_{\tau_o}) + (\underbrace{P_d + R_1 C_{out}}_{\tau_i})$$

$$R_o C_o = k$$

$$R_1 C_1 = k$$

$$= 2 P_d + \frac{k}{C_o} C_1 + \frac{k}{C_1} C_{out}$$

$$\underbrace{\tau_o}_{R_o} \quad \underbrace{\tau_i}_{R_1}$$

$$\tau(C_1) = 2 P_d + k \left( \frac{C_1}{C_o} + \frac{C_{out}}{C_1} \right)$$

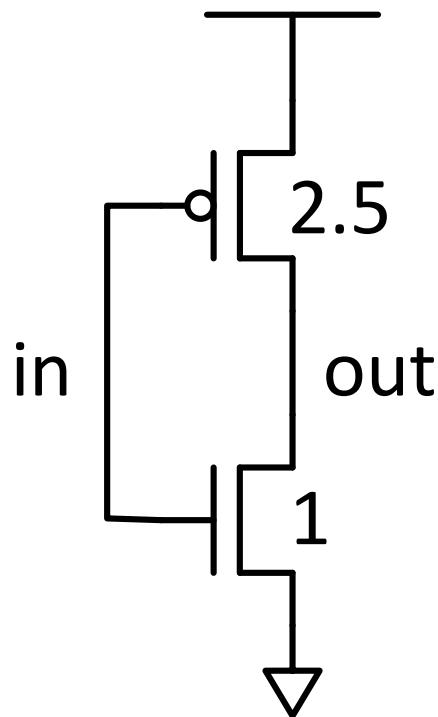
$$0 = \frac{d}{dC_1} \tau = 0 + k \left( \frac{1}{C_o} - \frac{C_{out}}{C_1^2} \right)$$

$$\Rightarrow \frac{1}{C_o} = \frac{C_{out}}{C_1^2} \Rightarrow \frac{C_1}{C_o} = \frac{C_{out}}{C_1} = r$$

$$r^2 = \left( \frac{C_1}{C_o} \right) \left( \frac{C_{out}}{C_1} \right) = \frac{C_{out}}{C_o} \Rightarrow r = \sqrt{\frac{C_{out}}{C_o}} ; C_1 = r C_o$$

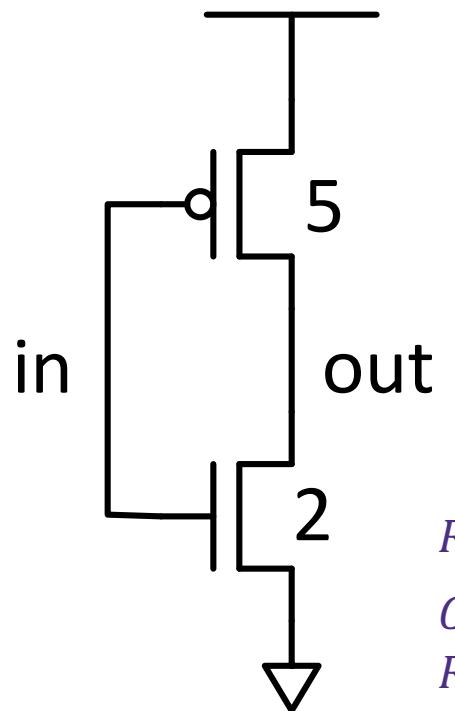
# Intrinsic RC delay

RCin



$$\begin{aligned} R &= k_r/W_n \\ C &= k'_c(W_n + W_p) \\ &= k'_c W_n(1 + \beta) \\ &= k_c W_n \end{aligned}$$

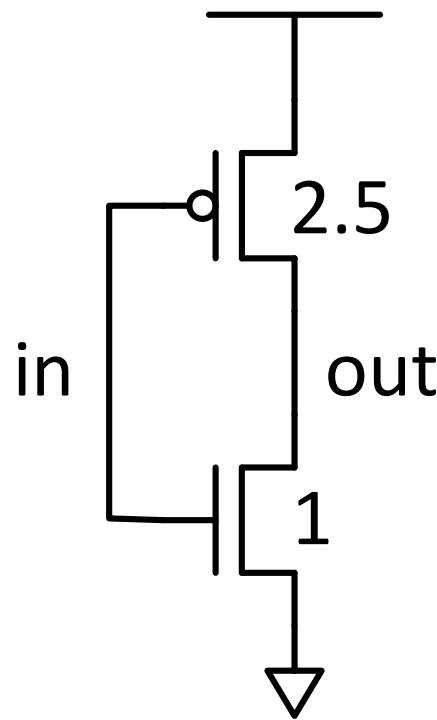
$$\begin{aligned} R_n &= \\ C_{in} &= \\ R_n C_{in} &= \end{aligned}$$



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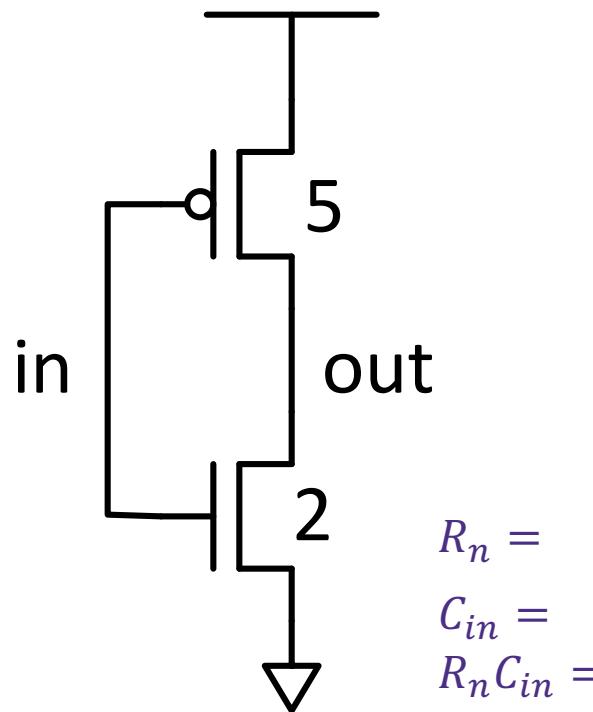
- Not to be confused with self loading
- $R_{\text{eff}}C_{\text{in}}$  product of an inverter (assume balanced inverter)
  - Independent of sizing
  - Topology driven
- Quick exercise: Compute  $R_n C_n$  for a 2 input NOR
  - Repeat  $R_p C_{\text{in}}$  calculation assuming  $\beta=3.5$

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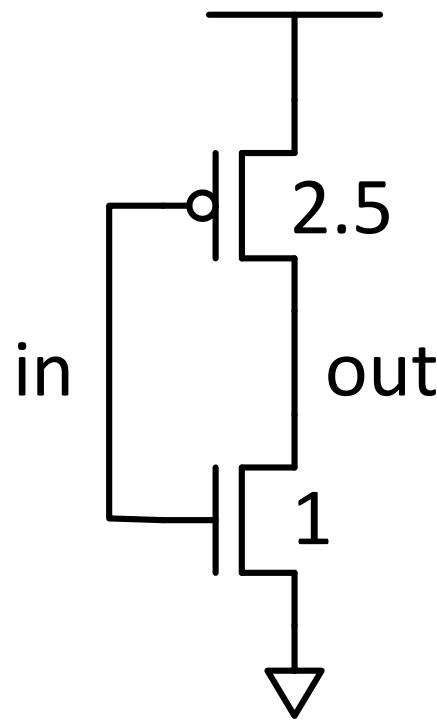
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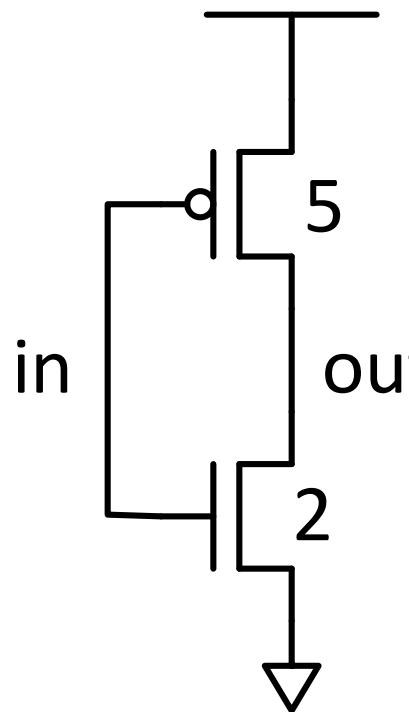
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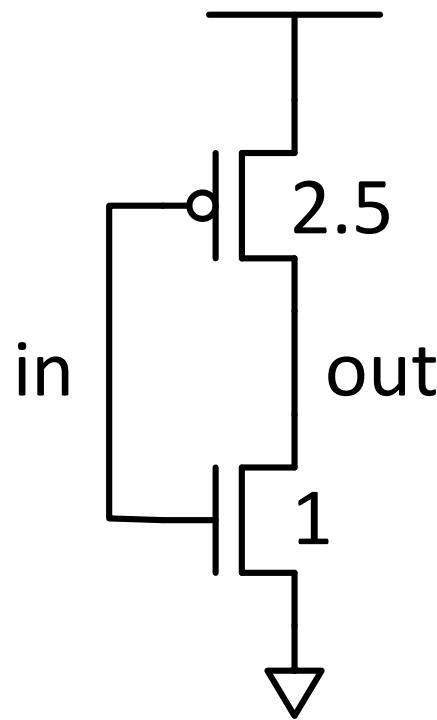
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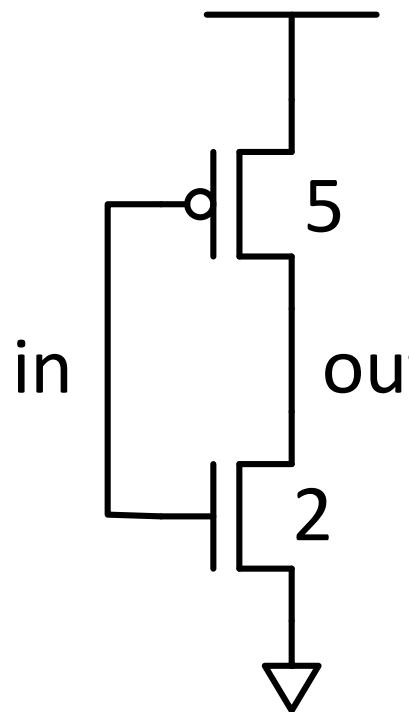
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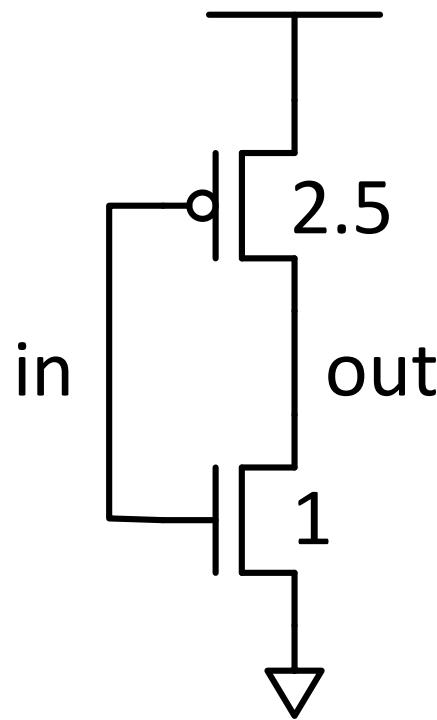
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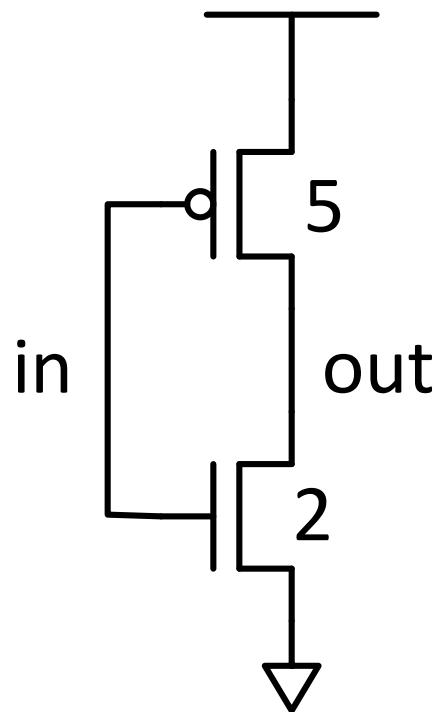
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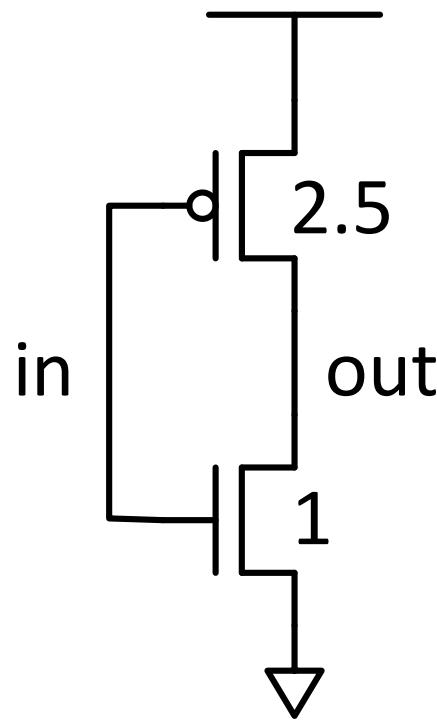
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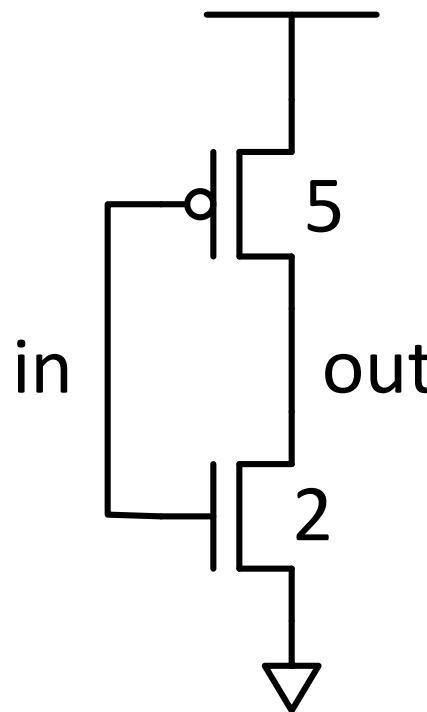
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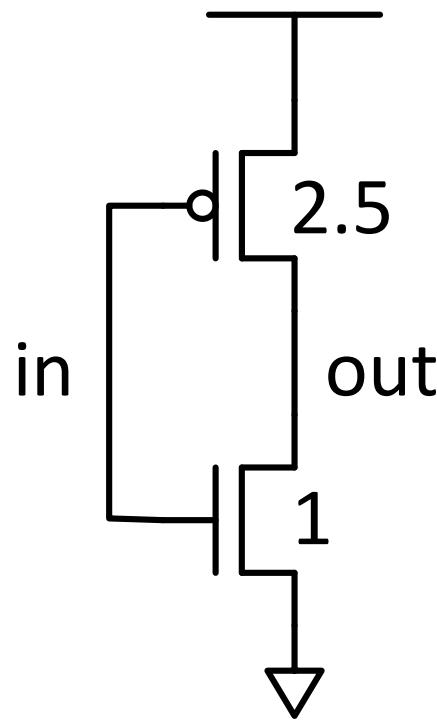
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$$\begin{aligned}R_n &= \frac{k_r}{2.0} \\C_{in} &= k'_c \times 7.0 \\R_n C_{in} &= \end{aligned}$$

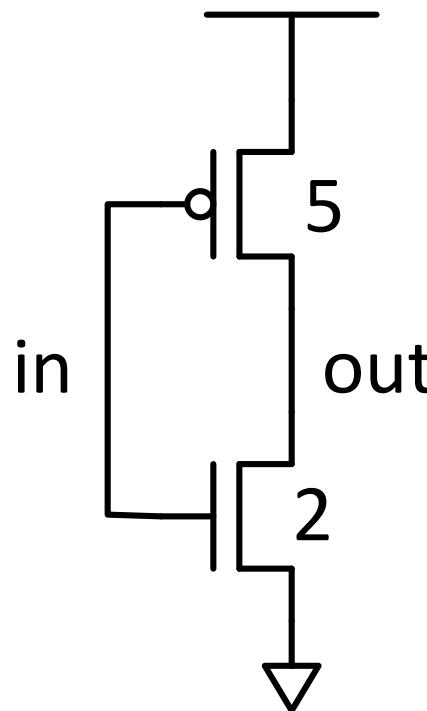
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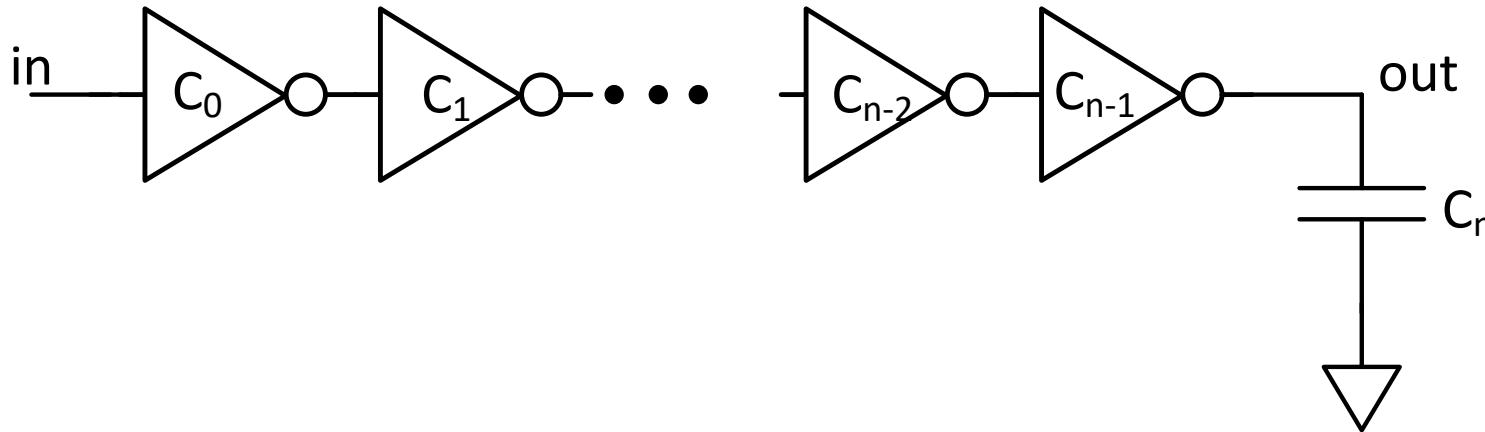
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# A Slightly More General Problem



- Solve for optimal  ~~$C_0$~~   $C_1 \dots C_{n-1}$  given  $C_n$  and  $C_0$

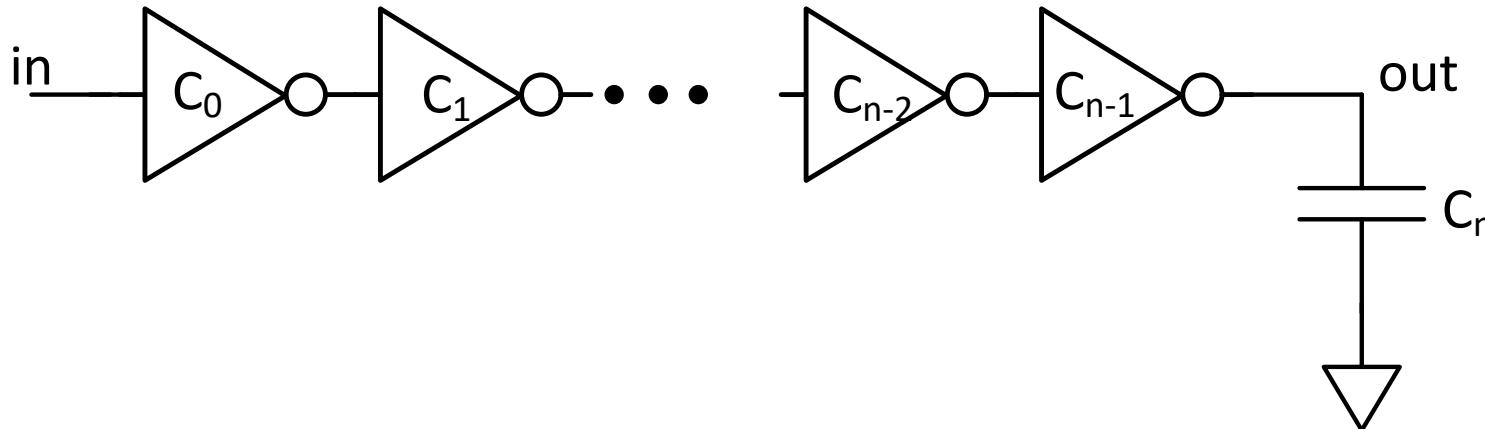
- Recall  $\tau = \sum \tau_i$

$$\tau = \sum R_i C_{i+1} = \sum \frac{k C_{i+1}}{C_i}$$

*n Pd +*      *n Pd +*

- Minimizing multivariate functions

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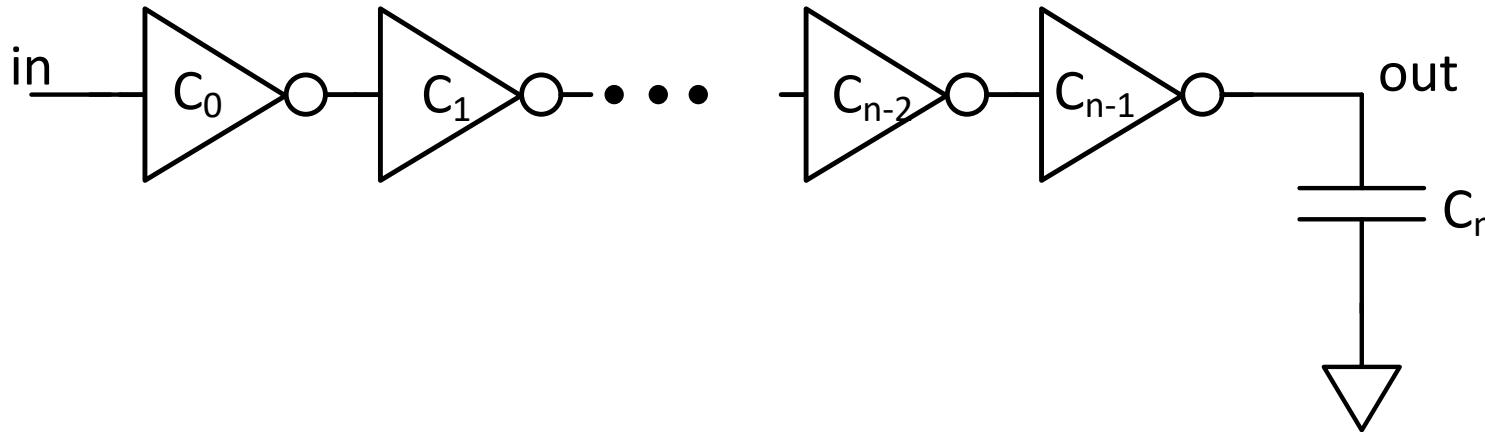
What is k again?



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# A Slightly More General Problem



- Solve for optimal  $C_0, C_1 \dots C_{n-1}$  given  $C_n$  and  $C_0$
- Recall  $\tau = \sum \tau_i$

What is k again?



$$\tau = \sum R_i C_{i+1} = \sum \frac{k C_{i+1}}{C_i} = k \left( \frac{C_1}{C_0} + \frac{C_2}{C_1} + \frac{C_3}{C_2} + \dots \right)$$

- Minimizing multivariate functions ...  $\nabla \tau = 0$

# Minimization of $\tau$

- Solving gives  $\frac{c_1}{c_0} = \frac{c_2}{c_1} = \dots = \frac{c_{n-1}}{c_{n-2}} = \frac{c_n}{c_{n-1}} = h$
- However,  $\frac{c_n}{c_0} = \text{constant} = \prod \frac{c_{i+1}}{c_i} = \prod h_i$  (Telescoping...)

$$h^n = \frac{c_1}{c_0} \cdot \frac{c_2}{c_1} \cdot \dots \cdot \frac{c_n}{c_{n-1}} = \frac{c_n}{c_0}$$

- Important assumptions
  - All of the input capacitance of the inverter scales with W
    - Wire cap ignored
    - Poly-contact cap ignored
  - Mosfet serves as the only source of resistance
- Question: How does self-loading impact the optimal solution?

$$\begin{aligned}\frac{c_1}{c_0} &= h \Rightarrow c_1 = h c_0 \\ \frac{c_2}{c_1} \cdot \frac{c_1}{c_0} &= h^2 = \frac{c_2}{c_0} \\ &\Rightarrow c_2 = h^2 c_0\end{aligned}$$

# Minimization of $\tau$

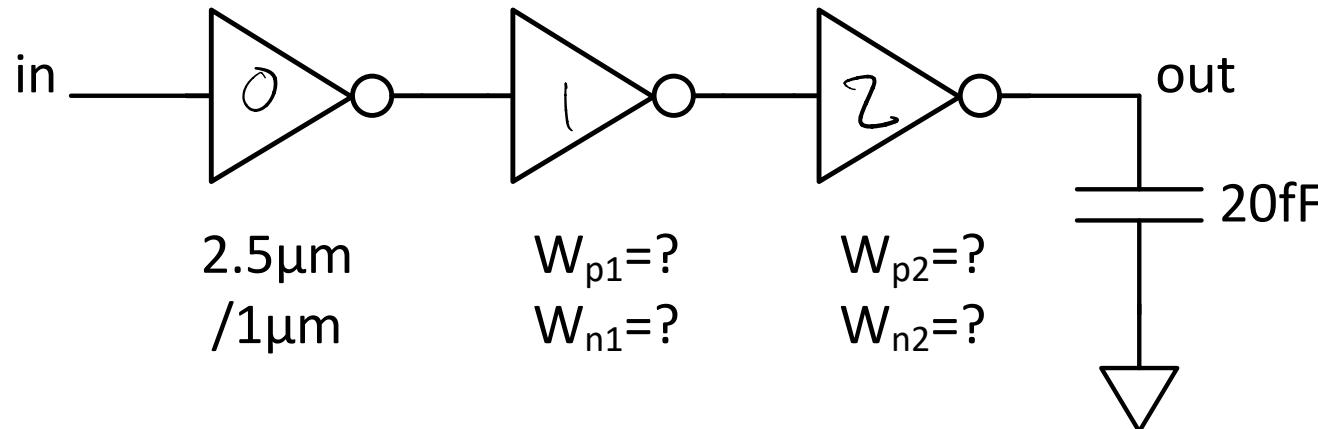
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- Solving gives  $\frac{c_1}{c_0} = \frac{c_2}{c_1} = \dots \frac{c_{n-1}}{c_{n-2}} = \frac{c_n}{c_{n-1}} = h$
- However,  $\frac{c_n}{c_0} = constant = \prod \frac{c_{i+1}}{c_i} = \prod h_i$  (Telescoping...)
- $\frac{c_n}{c_0} = h^n \Rightarrow h = \sqrt[n]{\frac{c_n}{c_0}}$
- Important assumptions
  - All of the input capacitance of the inverter scales with W
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- Question: How does self-loading impact the optimal solution?

# Sizing Example

$$38 \cdot \frac{8}{7} = \frac{8}{2} = 4 \text{ pF}$$

$1\mu\text{m} \Leftrightarrow 8/7f$



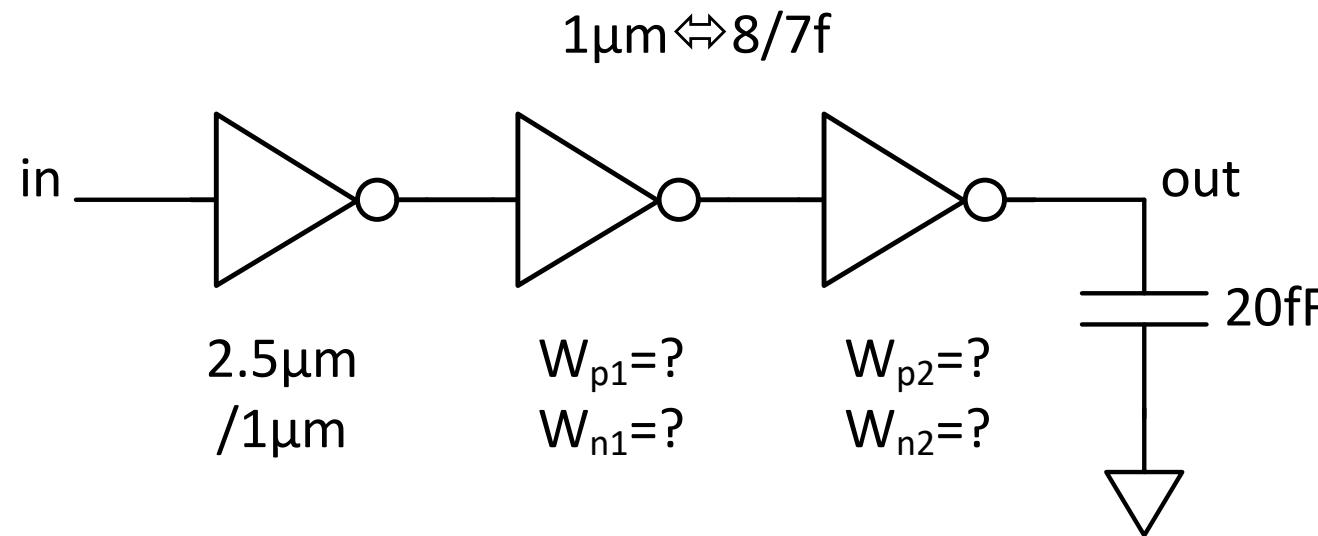
$$\frac{20\text{fF}}{C_2} \cdot \frac{C_2}{C_1} \cdot \frac{C_1}{C_0}$$

- Note:  $C_{in}$  and  $C_{out}$  units are not consistent

$$h^3 = \frac{20\text{fF}}{4\text{f}} = 5$$

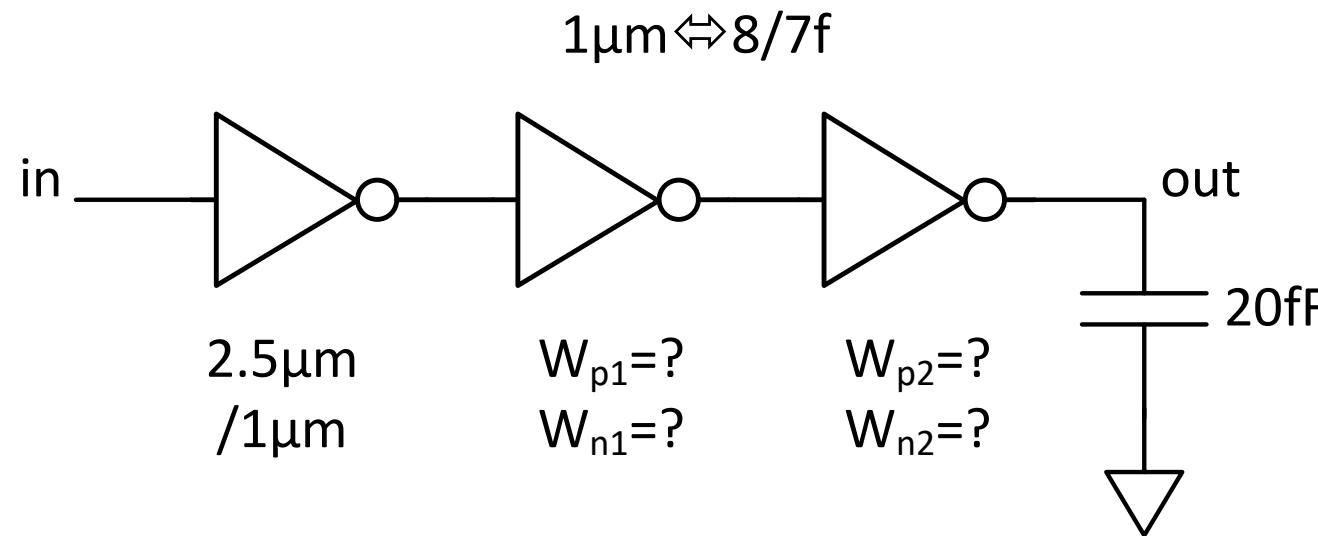
$$h = \sqrt[3]{5} \approx 1.7$$

# Sizing Example



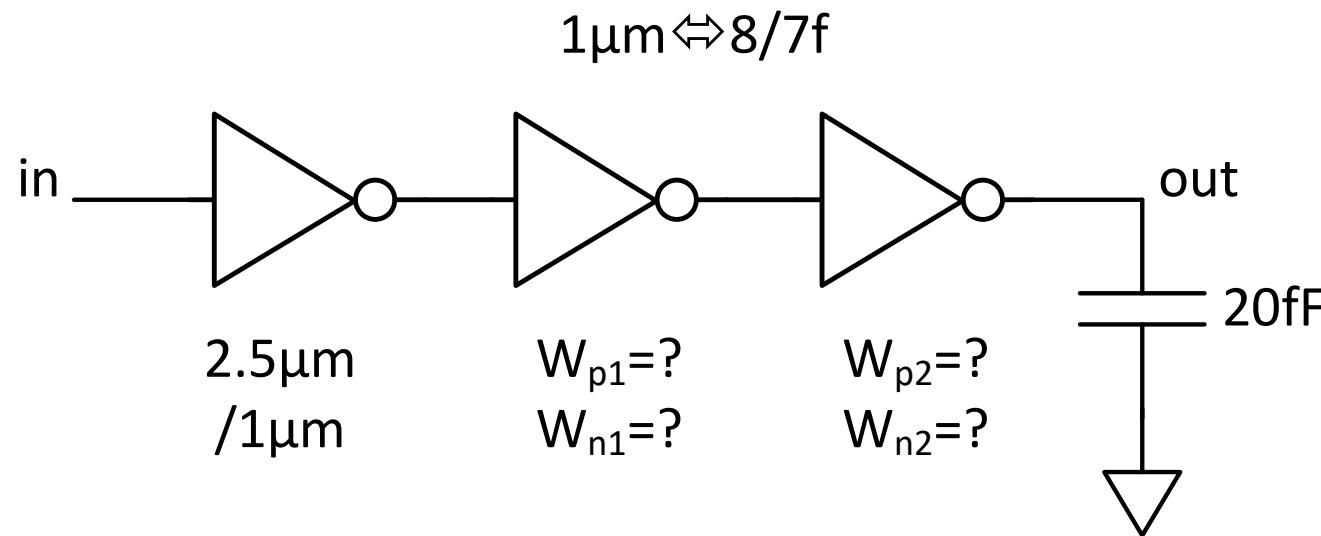
- Note:  $C_{in}$  and  $C_{out}$  units are not consistent
- $C_{in} = 3.5 * 8/7 = 4\text{f}$

# Sizing Example



- Note:  $C_{\text{in}}$  and  $C_{\text{out}}$  units are not consistent
- $C_{\text{in}} = 3.5 * 8/7 = 4\text{f}$
- $h^3 = 20/4 \Rightarrow h = \sqrt[3]{5} = 1.71$

# Sizing Example



- Note:  $C_{in}$  and  $C_{out}$  units are not consistent
- $C_{in} = 3.5 * 8/7 = 4\text{f}$
- $h^3 = 20/4 \Rightarrow h = \sqrt[3]{5} = 1.71$
- $C_1 = 4\text{f} * 1.71 = 6.84 \Rightarrow W_{p1} = 4.25 \mu\text{m}, W_{n1} = 1.71 \mu\text{m}$

## Sizing Example

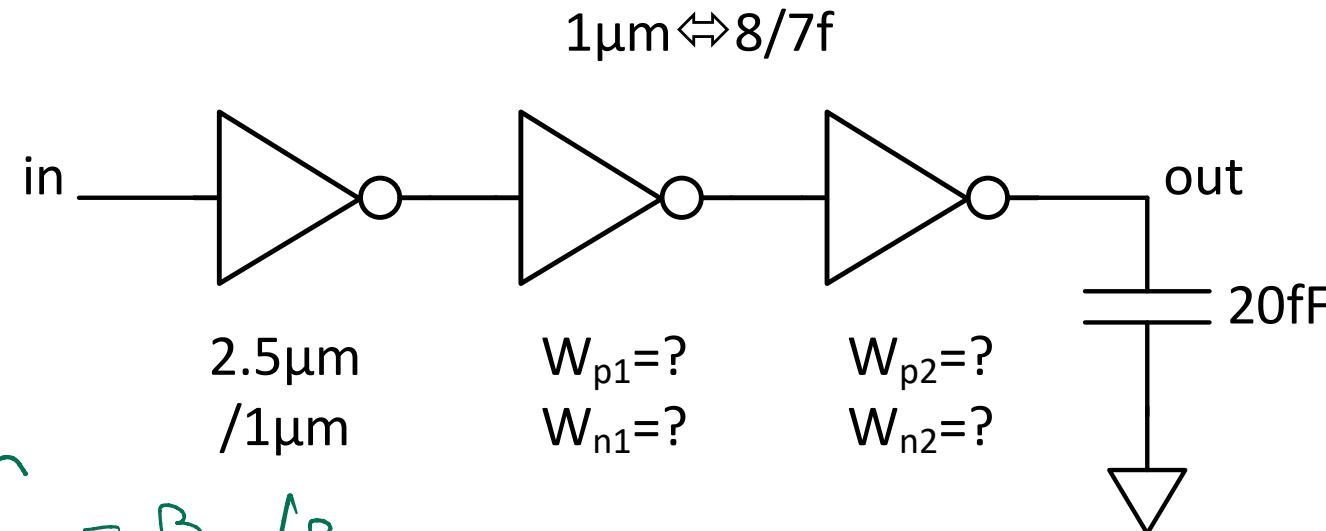
$$\frac{\beta_n}{\beta_p} \geq 2.5$$

$$\underline{\beta_p w_p}$$

$$\underline{\beta_n w_n}$$

$$\underline{\beta_p w_p = \beta_n w_n}$$

$$w_p/w_n = \beta_n/\beta_p$$



$$\frac{C_2}{C_1} \cdot \frac{C_1}{C_0} = h^2 = \frac{C_2}{C_0}$$

$$\Rightarrow C_2 = h^2 C_0$$

$$\frac{C_2}{C_1} = h$$

$$\Rightarrow C_2 = h C_1$$

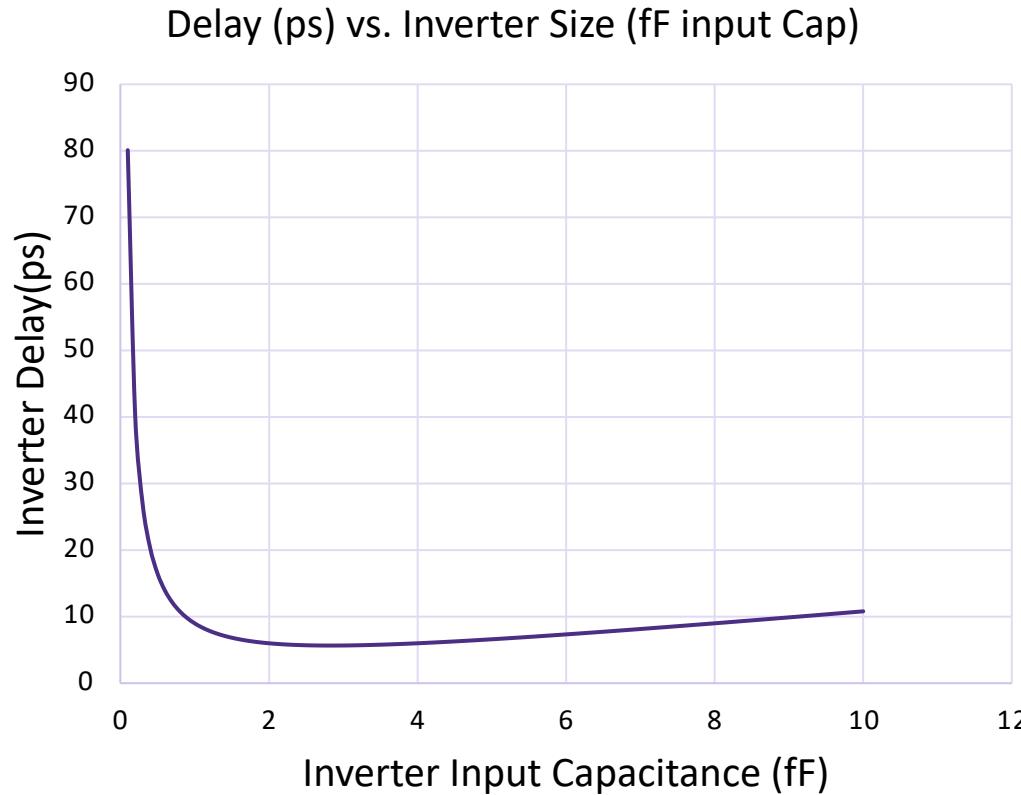
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- $C_{in} = 3.5 * 8/7 = 4\text{f}$
- $h^3 = 20/4 \Rightarrow h = \sqrt[3]{5} = 1.71$
- $C_1 = 4\text{f} * 1.71 = 6.84 \Rightarrow W_{p1} = 4.25 \mu\text{m}, W_{n1} = 1.71 \mu\text{m}$
- $C_2 = C_1 * 1.71 = 11.69 \Rightarrow W_{p1} = 7.30 \mu\text{m}, W_{n1} = 2.92 \mu\text{m}$

$$\frac{8}{7} (W_{p1} + W_{n1}) = 6.84$$

$$\frac{W_{p1}}{W_{n1}} \approx 2.5$$

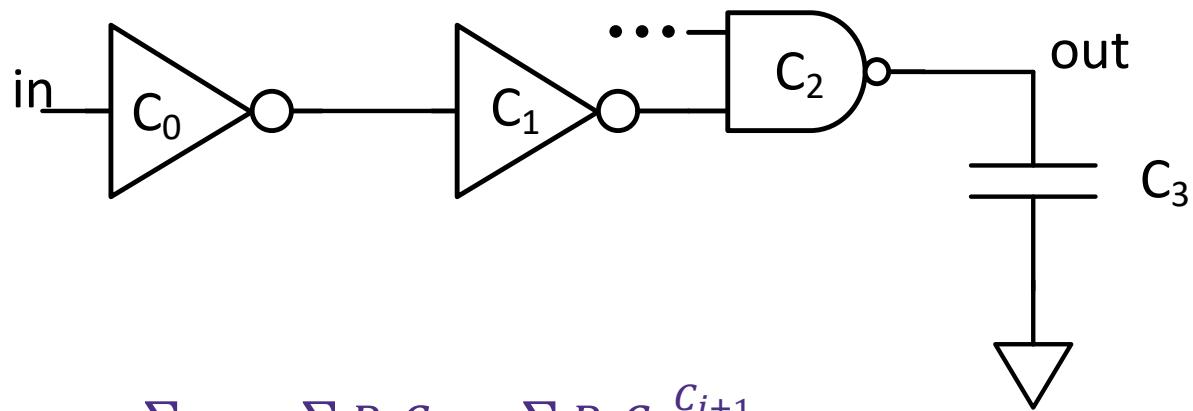
$$\frac{8}{7} W_{p1} \cdot 3.5 = 6.84$$

# Practical Sizing Considerations

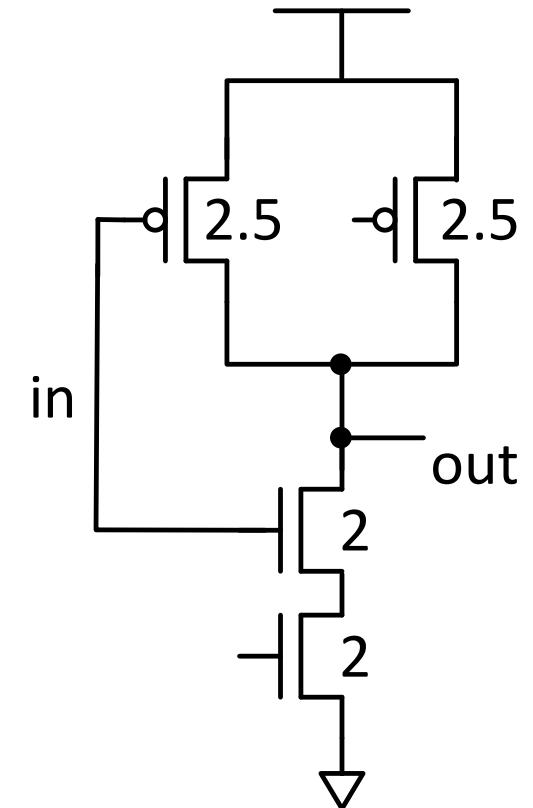


- Better to err on the side of larger drivers
- Min width issues (Allowed/Recommended for technology)
- Technique is great as an **initial starting point** for design

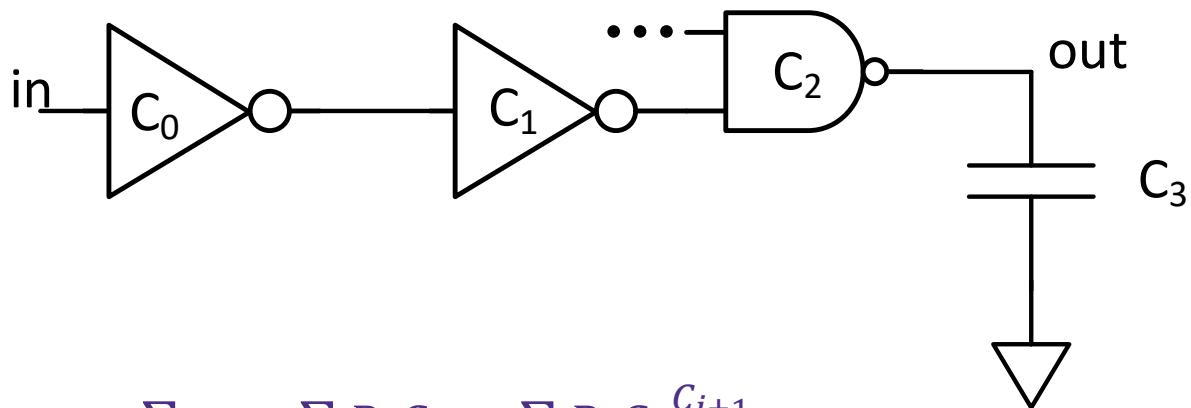
# Quick Note on General Sizing (Extra...)



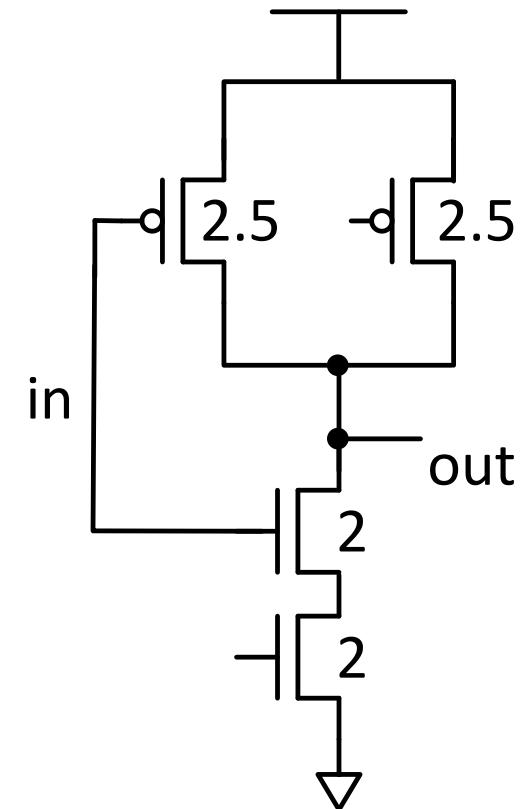
- $$\begin{aligned}\tau &= \sum \tau_i = \sum R_i C_{i+1} = \sum R_i C_i \frac{C_{i+1}}{C_i} \\ &= \sum \tau_{intrinsic} \frac{C_{i+1}}{C_i}\end{aligned}$$



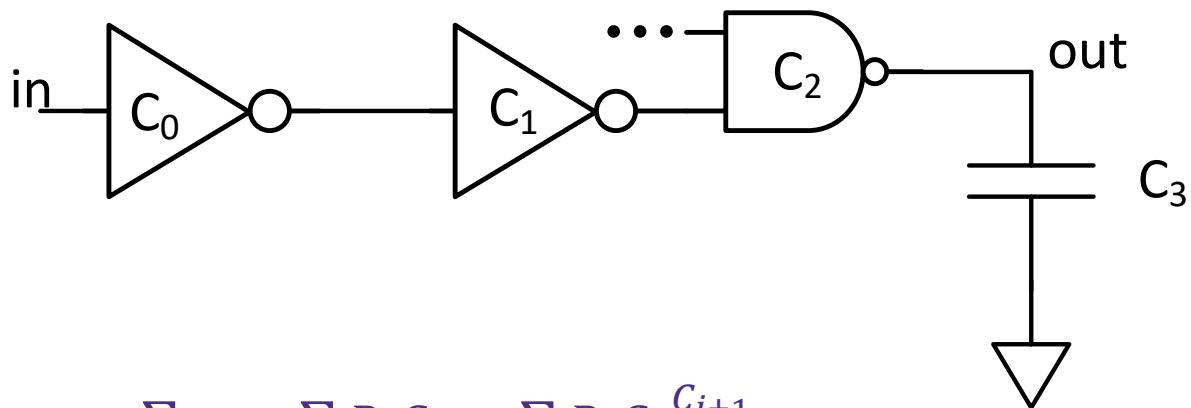
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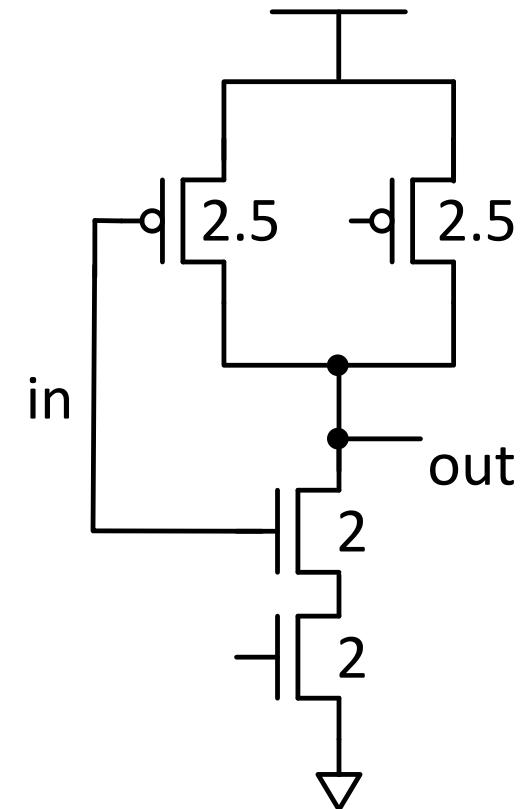
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- $RC_{intrinsic,inv} = 3.5k_r k_c$



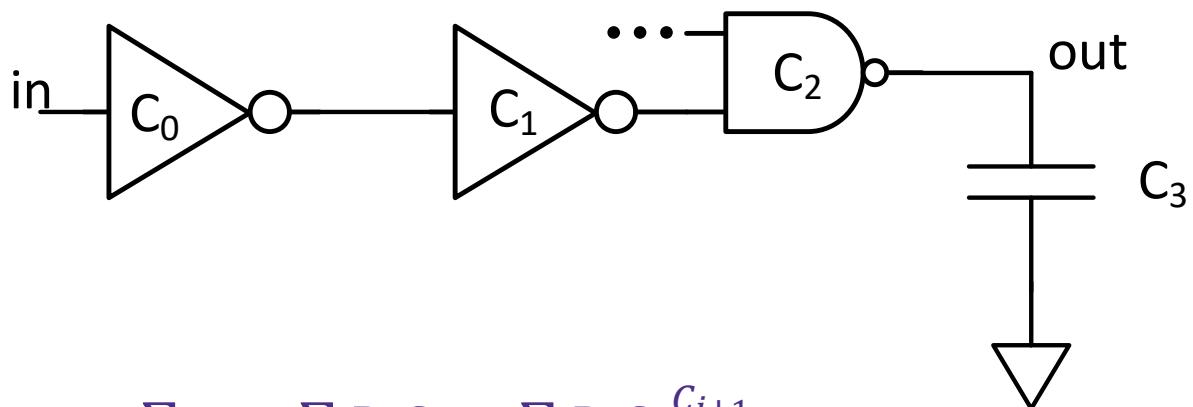
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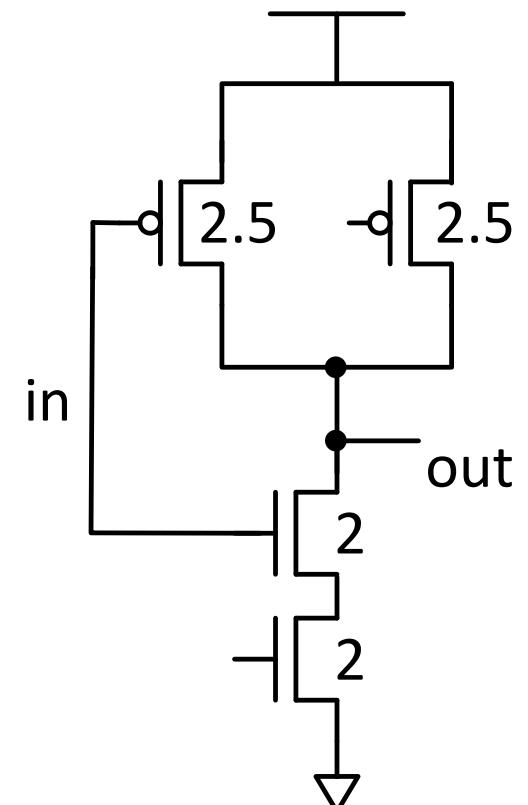
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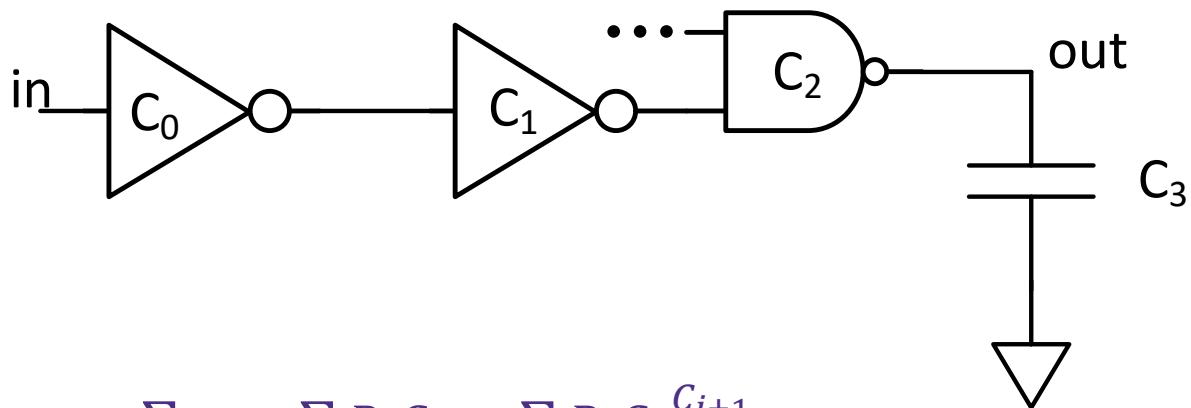
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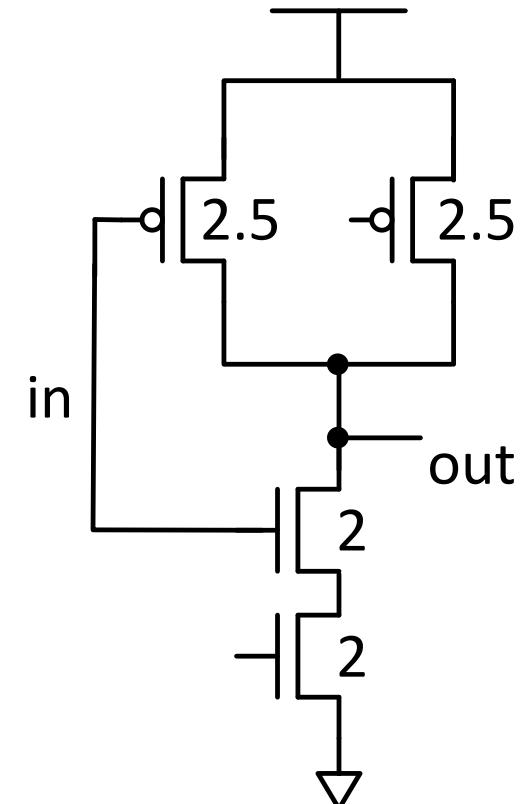
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- $\tau = 3.5k_r k_c \frac{C_1}{C_0} + 3.5k_r k_c \frac{C_2}{C_1} + 4.5k_r k_c \frac{C_3}{C_2}$   
 $\tau_{inv\_units} = \frac{C_1}{C_0} + \frac{C_2}{C_1} + \frac{4.5 C_3}{3.5 C_2}$
- Rule-of-thumb: Maintain a stage-effort of  $\approx 3.4$



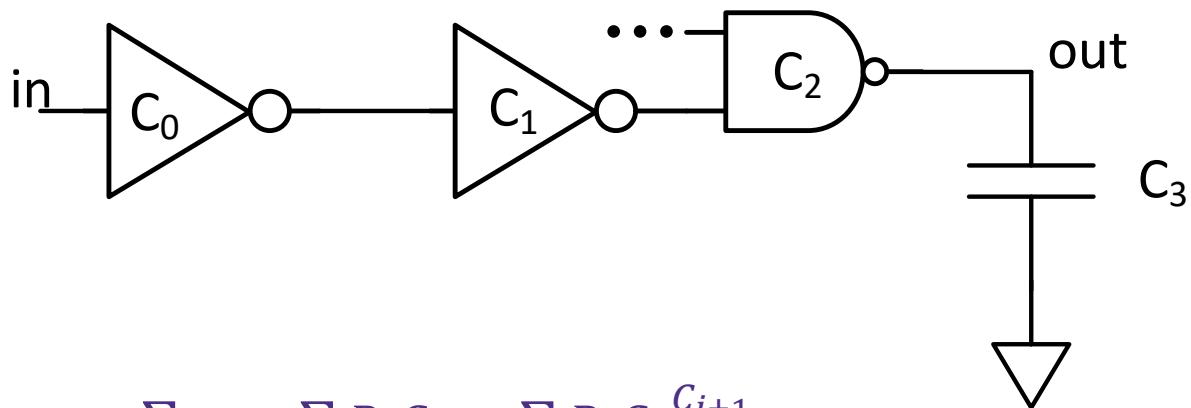
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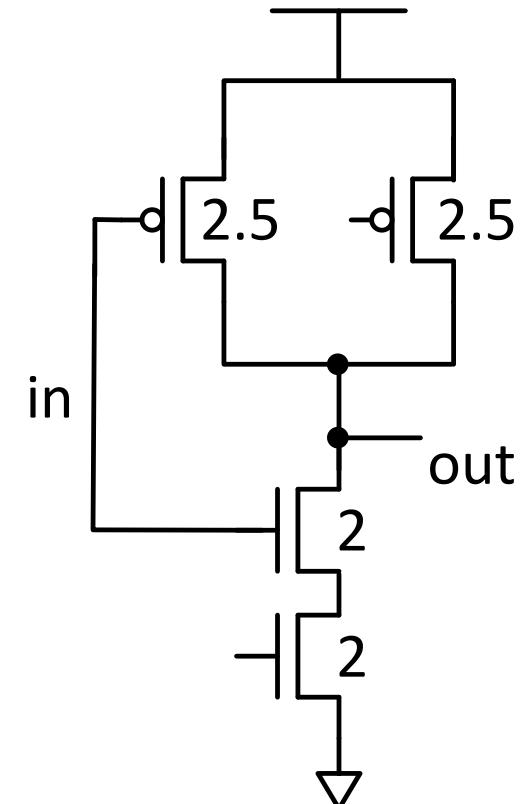
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Logical Effort
- Rule-of-thumb: Maintain a stage-effort of  $\approx 3.4$



# Quick Note on General Sizing (Extra...)



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Stage Effort
- Rule-of-thumb: Maintain a stage-effort of  $\approx 3.4$



# STATIC TIMING ANALYSIS

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