Lecture 5: The CMOS Inverter

Based on material prepared by prof. Visvesh S. Sathe

Acknowledgements

All class materials (lectures, assignments, etc.) based on material prepared by Prof. Visvesh S. Sathe, and reproduced with his permission

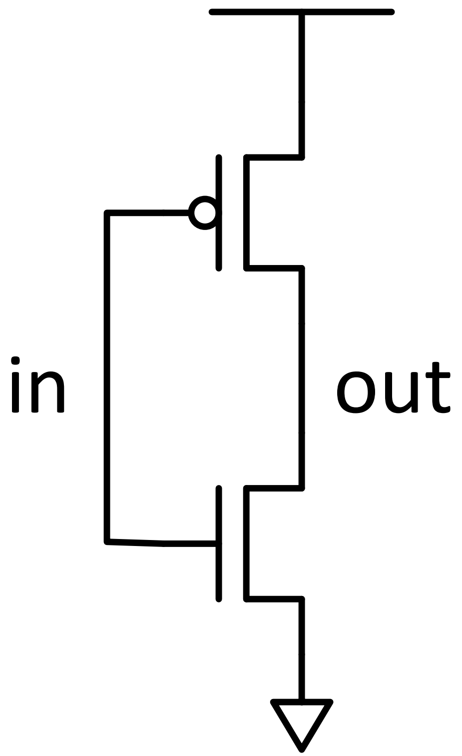
Visvesh S. Sathe
Associate Professor
Georgia Institute of Technology
https://psylab.ece.uw.edu

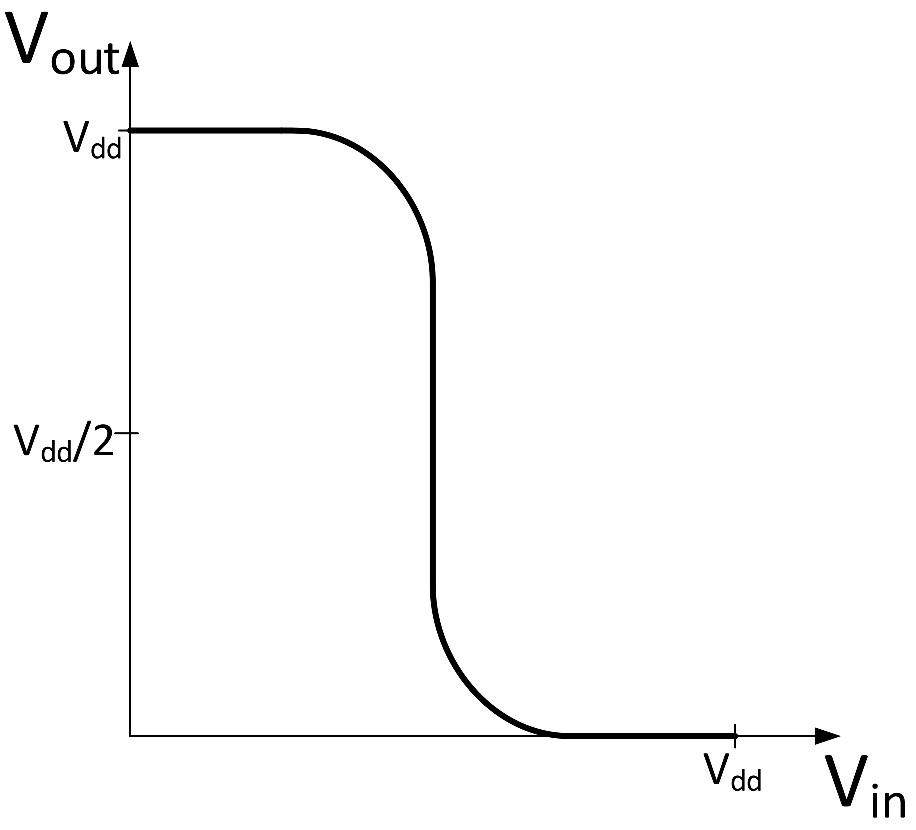
UW (2013-2022)
GaTech (2022-present)

CMOS Gate Design

- Analyze important aspects of CMOS logic
  - Static Operation (Static Noise Margin, Hold resistance)
  - Dynamic operation (Cross-over current, current-drive, delay)
  - Power dissipation
  - Gate sizing basics
  - Effect of voltage scaling
- Use inverter design to understand these various aspects

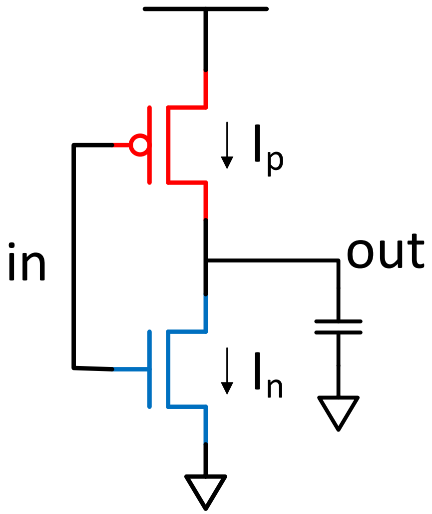
DC Response

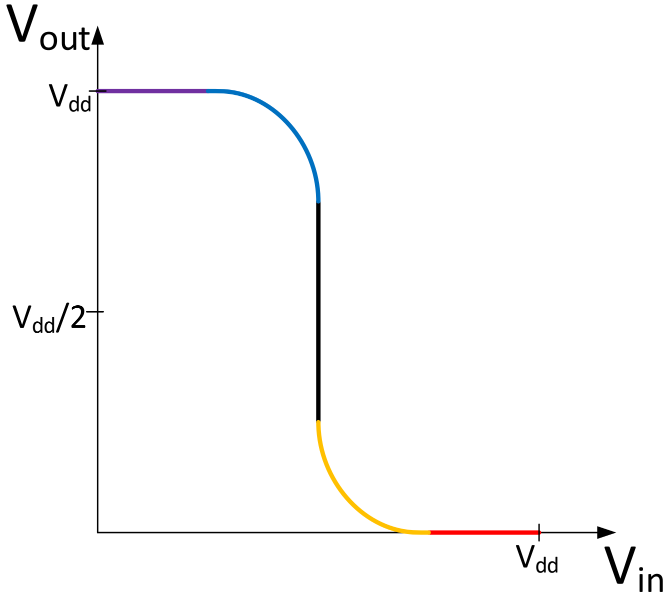




- DC transfer function of a balanced, ideal inverter
  - At each dc value of V_{in}, evaluate V_{out} and record

Understanding the DC Transfer Function

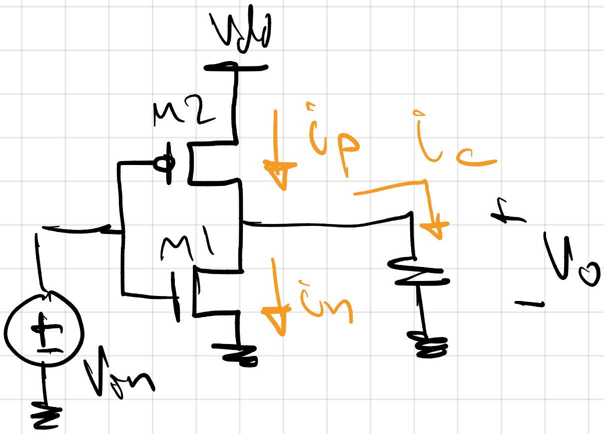


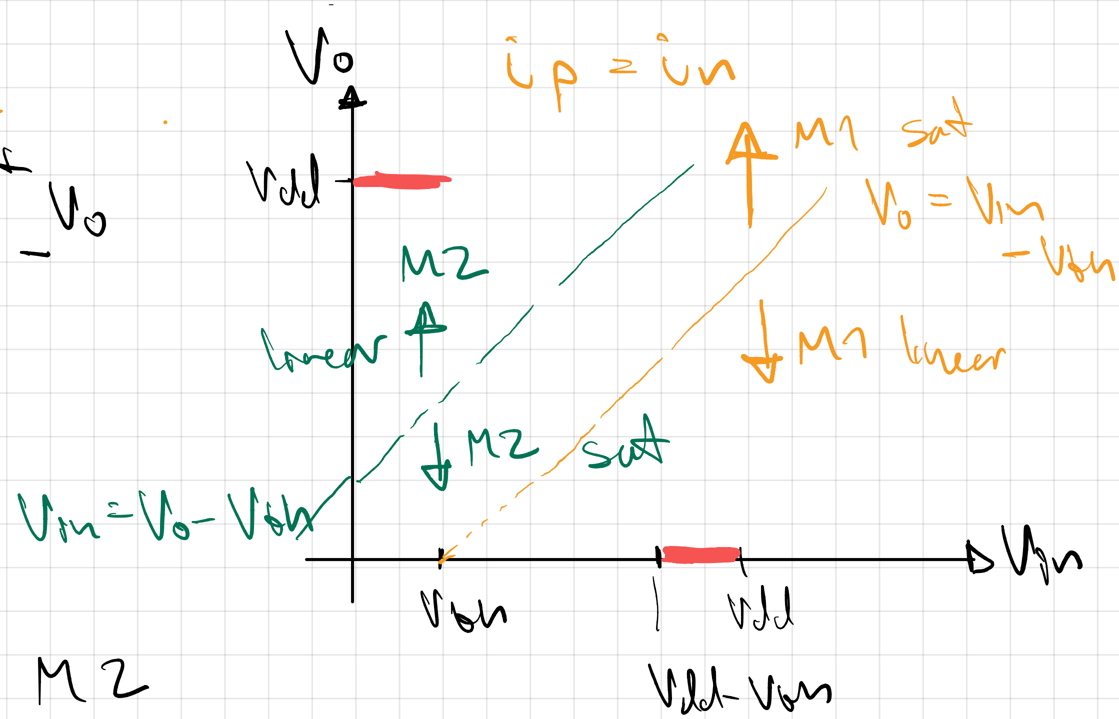


- Static analysis
  - Assumes load is capacitive (No steady-state current draw)
  - Voltages are dc (**Amount of capacitive load is irrelevant**)
- Inverter DC analysis
  - Devices operate over a variety of modes across voltage range
  - Governing equation:
  - Both, equation-based and graphical analysis is valuable
  - Useful in determining robustness to noise (Static Noise Margin/Holding Res)

$i_p = i_n + \cancel{i_c}^{\,0}$

$i_p = i_n$





M1:

cutoff

$V_{in} \le V_{th}$

saturation

$V_o \ge V_{in} - V_{th}$

M2

cutoff

$V_{in} \ge V_{dd} - V_{th}$

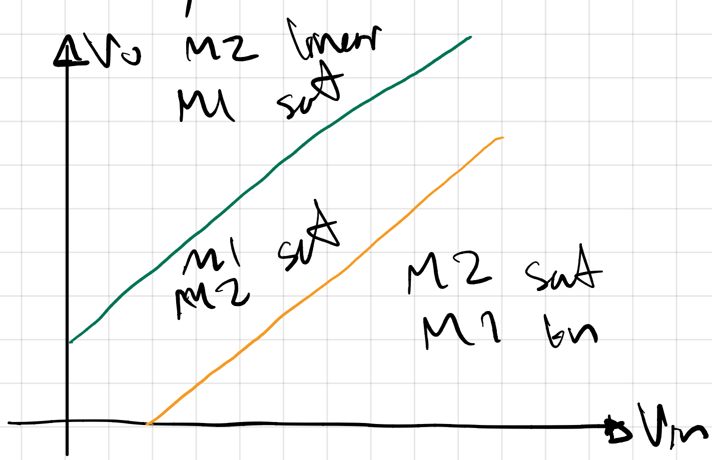
saturation

$V_{SD} \ge V_{SG} - V_{th}$

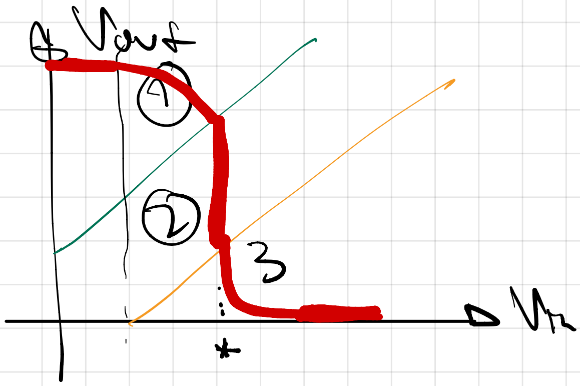
$(\cancel{V_{dd}} - V_o) \ge (\cancel{V_{dd}} - V_{in}) - V_{th}$

$V_{in} \ge V_o - V_{th}$

In summary



$i_p = i_n$



① M1 sat

M2 linear

$i_p = i_n$

$$= \beta_p\left[(V_{SG}-V_{tn})\cdot V_{SD} - \frac{V_{SD}^2}{2}\right]$$

$$= \frac{1}{2}\beta_n(V_{GS}-V_{tn})^2$$

② $\frac{1}{2}\beta_p(V_{SG}-V_{tn})^2 = \frac{1}{2}\beta_n(V_{GS}-V_{th})^2$

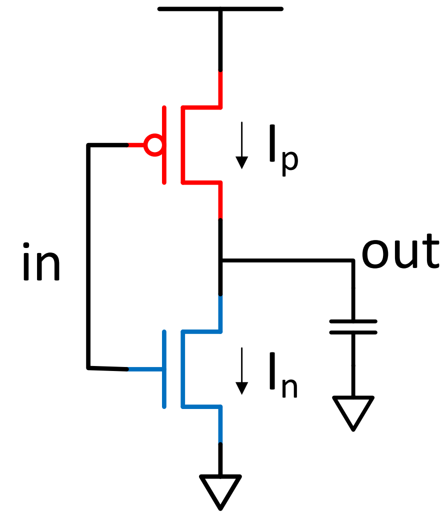
$$\cancel{\tfrac{1}{2}}\beta_p(V_{dd}-V_{in}-V_{tn})^2 = \cancel{\tfrac{1}{2}}\beta_n(V_{in}-V_{tn})^2$$

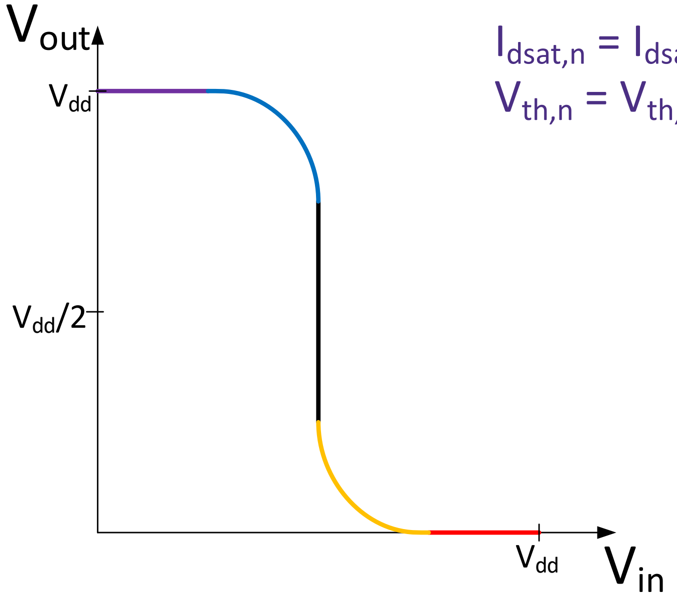
$$V_{dd}-V_{in}-V_{th} = \sqrt{\frac{\beta_n}{\beta_p}}\,(V_{in}-V_{tn})$$

$$V_{dd}-V_{tn}\left(1-\sqrt{\frac{\beta_n}{\beta_p}}\right) = V_{in}\left(1+\sqrt{\frac{\beta_n}{\beta_p}}\right)$$

$$\Rightarrow V_{in} = \frac{(L1+S)}{(R1+S)} = *$$

Understanding the DC Transfer Function

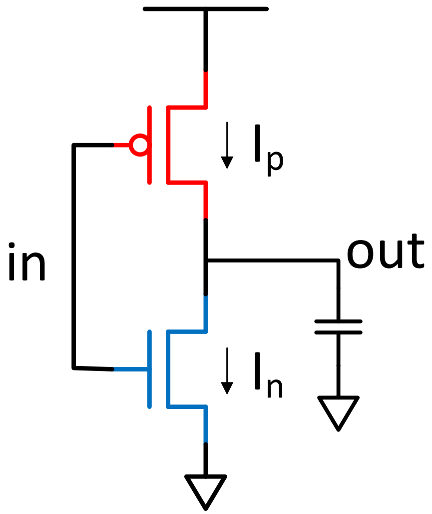


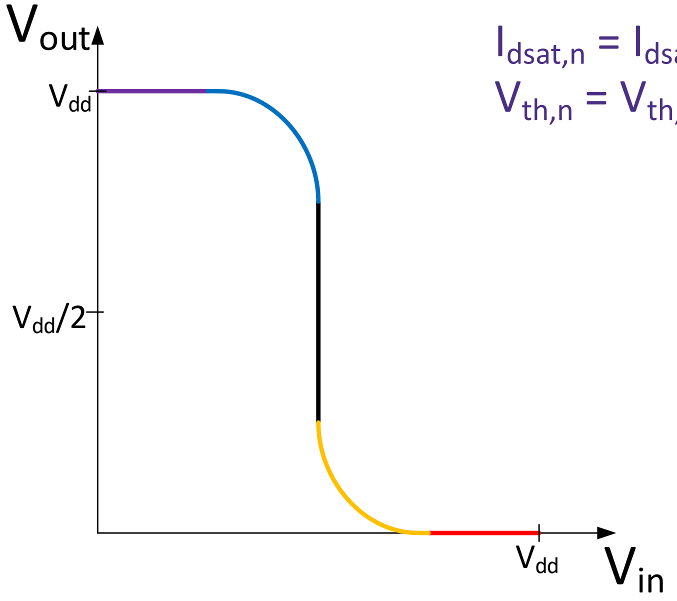


$I_{dsat,n} = I_{dsat,p}$
$V_{th,n} = V_{th,p} = 200mV$

- Static analysis
  - Assumes load is capacitive (No steady-state current draw)
  - Voltages are dc (**Amount of capacitive load is irrelevant**)
- Inverter DC analysis
  - Devices operate over a variety of modes across voltage range
  - Governing equation:
  - Both, equation-based and graphical analysis is valuable
  - Useful in determining robustness to noise (Static Noise Margin/Holding Res)

Understanding the DC Transfer Function



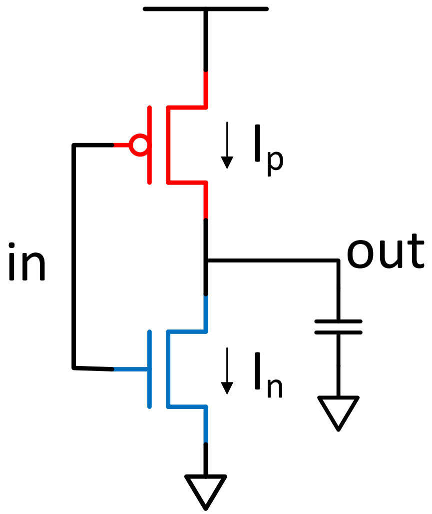


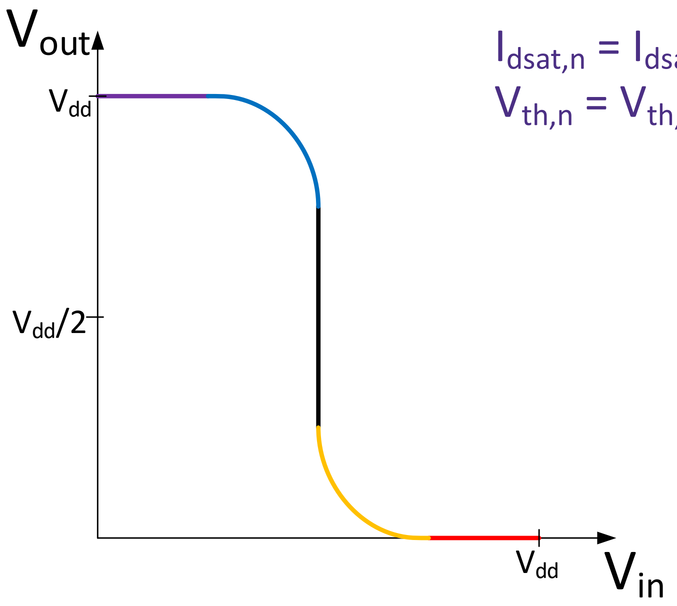
$I_{dsat,n} = I_{dsat,p}$
$V_{th,n} = V_{th,p} = 200mV$

- Static analysis
  - Assumes load is capacitive (No steady-state current draw)
  - Voltages are dc (**Amount of capacitive load is irrelevant**)
- Inverter DC analysis
  - Devices operate over a variety of modes across voltage range
  - Governing equation:
  - Both, equation-based and graphical analysis is valuable
  - Useful in determining robustness to noise (Static Noise Margin/Holding Res)

 ELECTRICAL & COMPUTER ENGINEERING

Understanding the DC Transfer Function

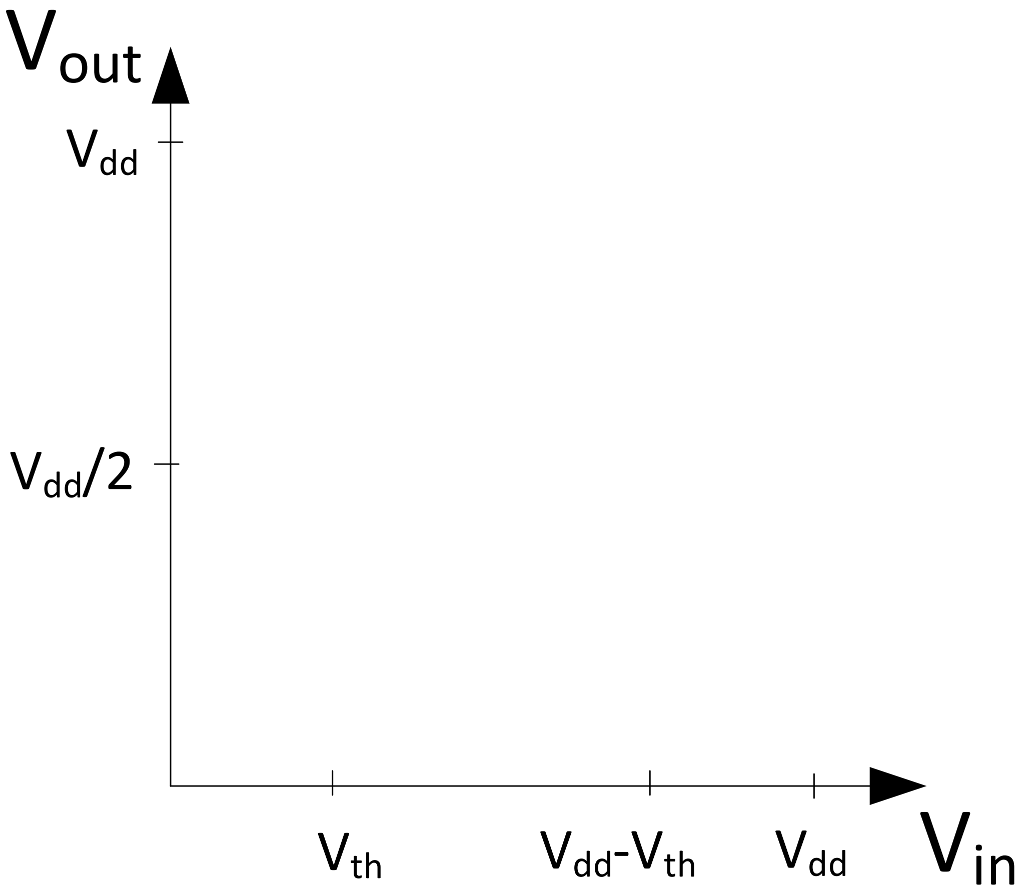




$I_{dsat,n} = I_{dsat,p}$
$V_{th,n} = V_{th,p} = 200mV$

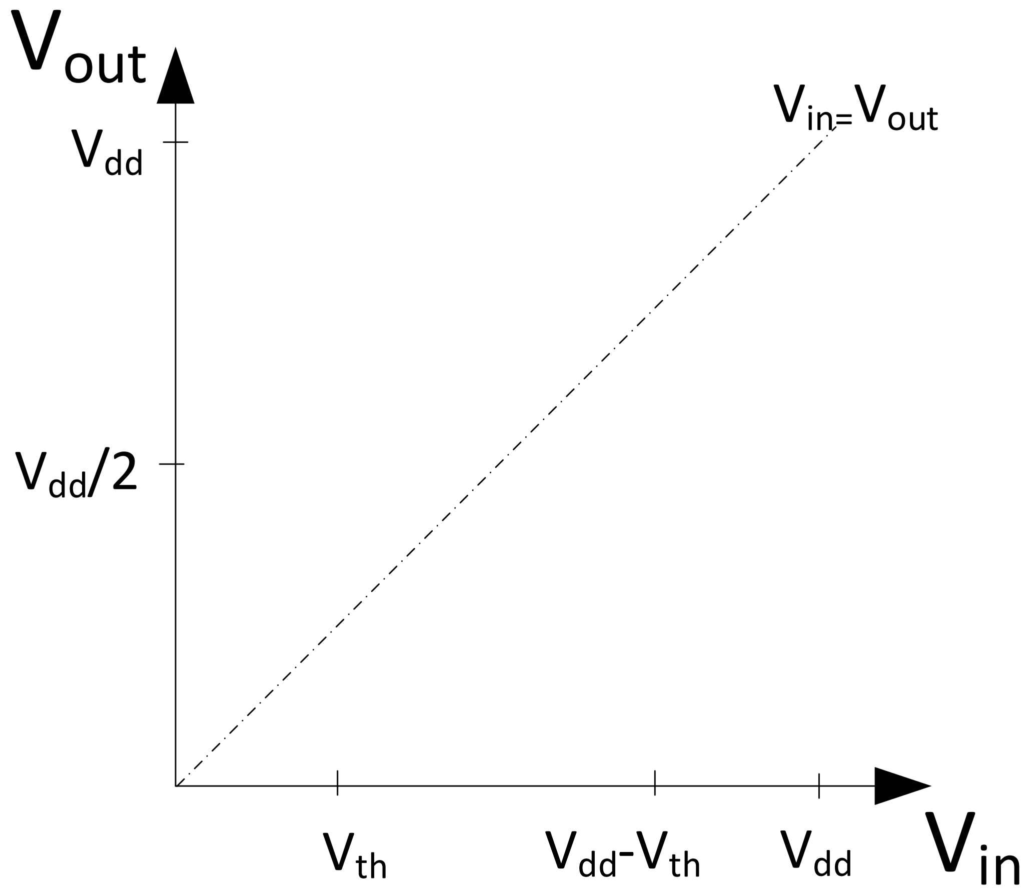
- Static analysis
  - Assumes load is capacitive (No steady-state current draw)
  - Voltages are dc (**Amount of capacitive load is irrelevant**)
- Inverter DC analysis
  - Devices operate over a variety of modes across voltage range
  - Governing equation: Pullup current == Pulldown current
  - Both, equation-based and graphical analysis is valuable
  - Useful in determining robustness to noise (Static Noise Margin/Holding Res)

Inverter DC Analysis



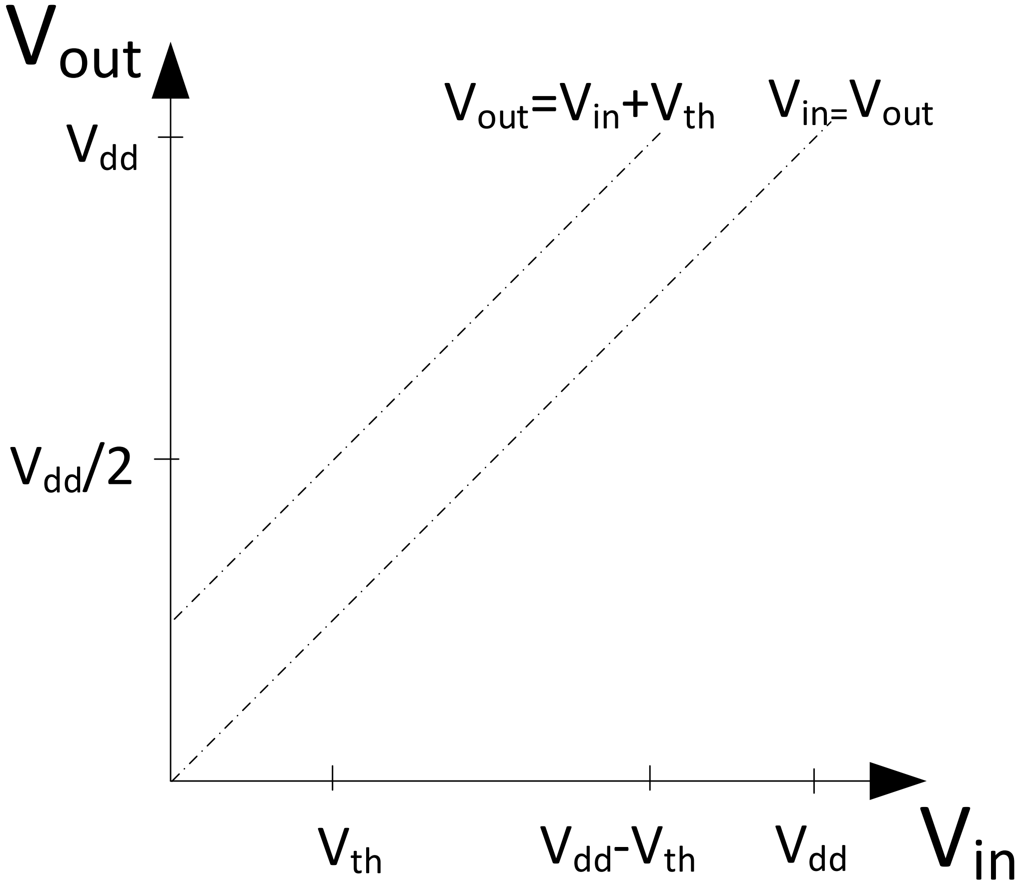
- $I_{dsat,n} = I_{dsat,p}$
- $V_{th,n} = V_{th,p} = 200mV$
- Mark out locus of operation

Inverter DC Analysis



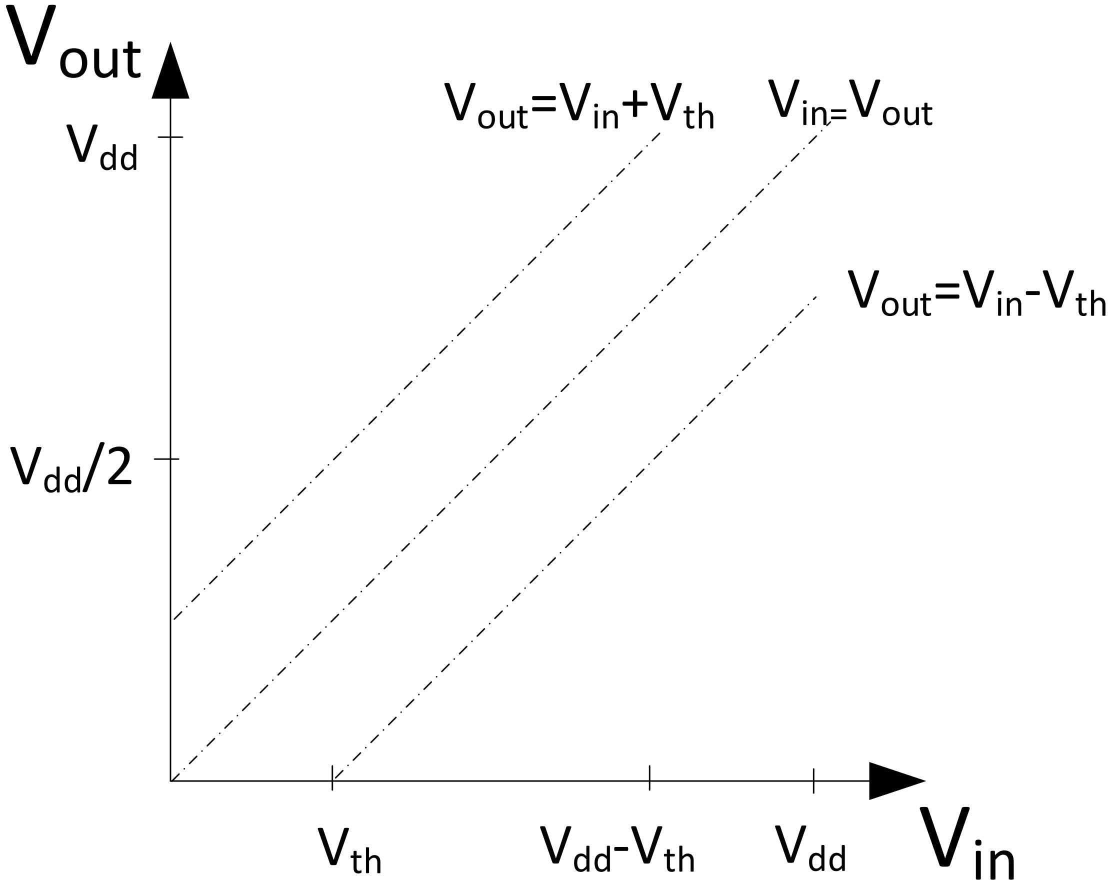
- $I_{dsat,n} = I_{dsat,p}$
- $V_{th,n} = V_{th,p} = 200mV$
- Mark out locus of operation

Inverter DC Analysis



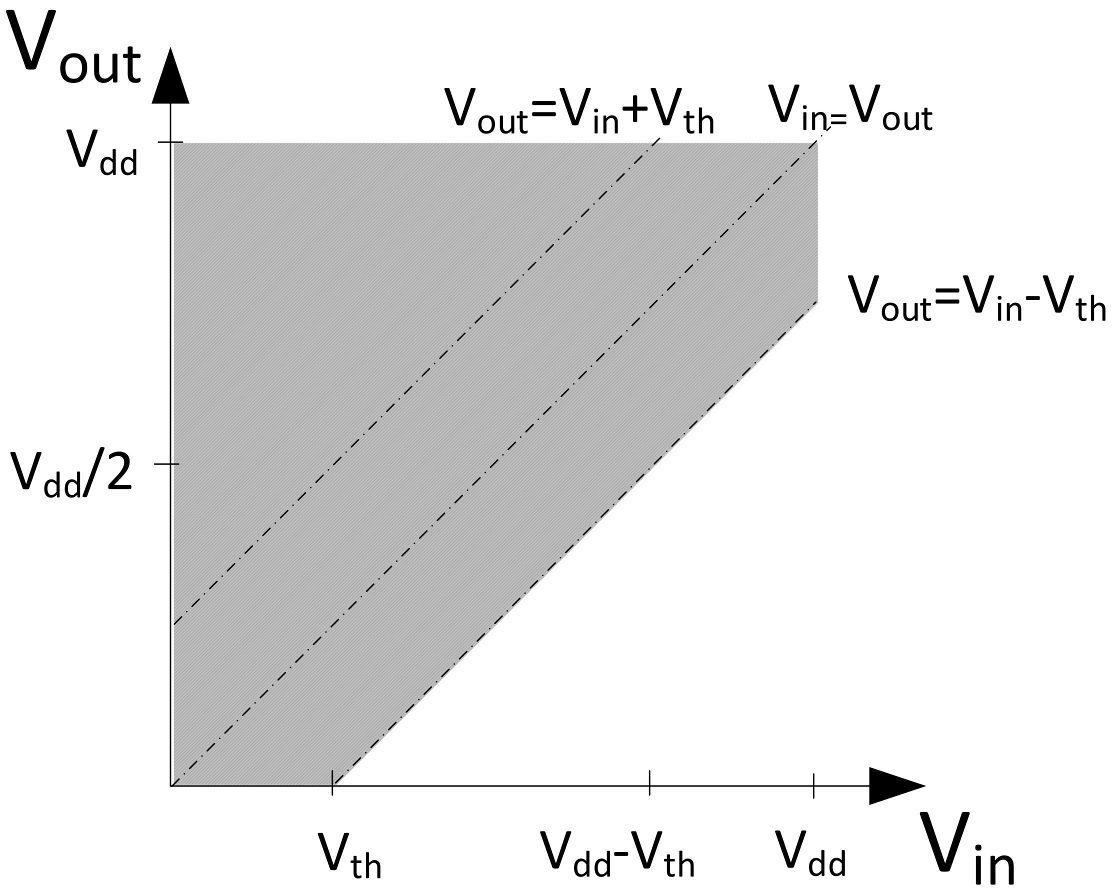
- $I_{dsat,n} = I_{dsat,p}$
- $V_{th,n} = V_{th,p} = 200mV$
- Mark out locus of operation

Inverter DC Analysis



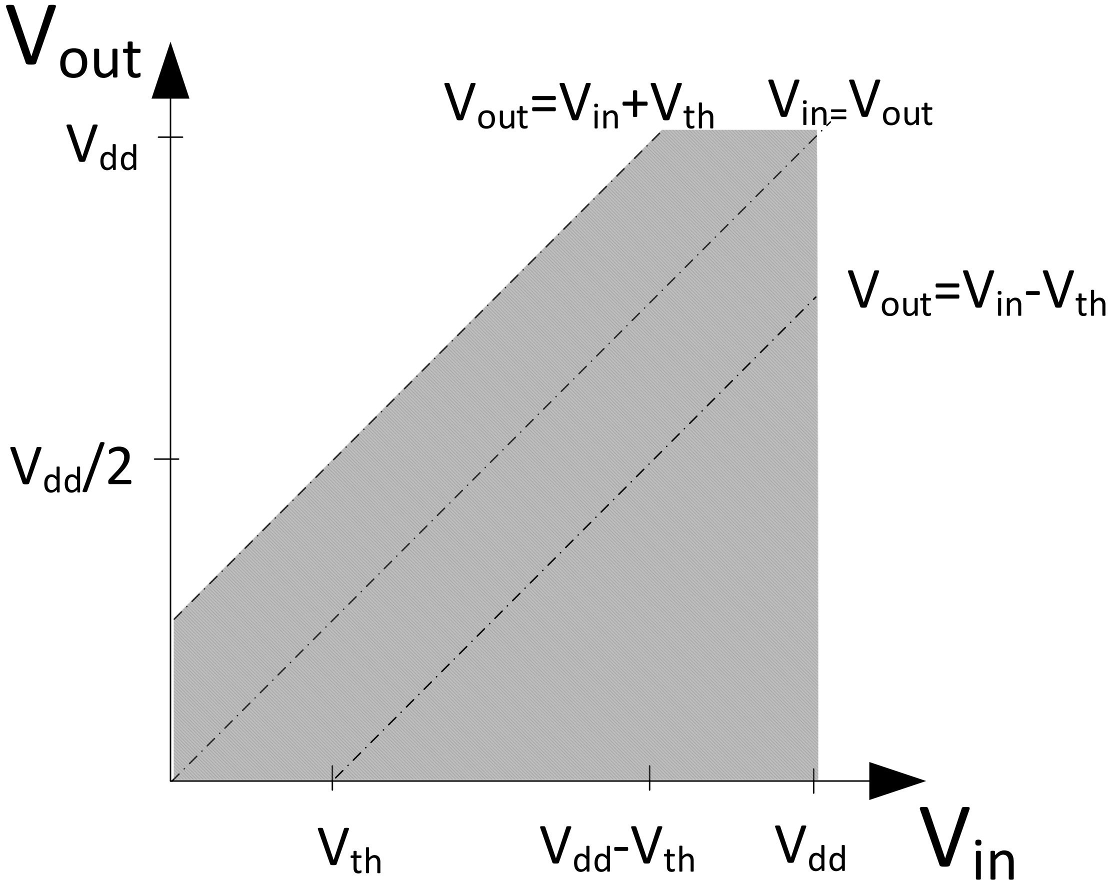
- $I_{dsat,n} = I_{dsat,p}$
- $V_{th,n} = V_{th,p} = 200mV$
- Mark out locus of operation

Inverter DC Analysis



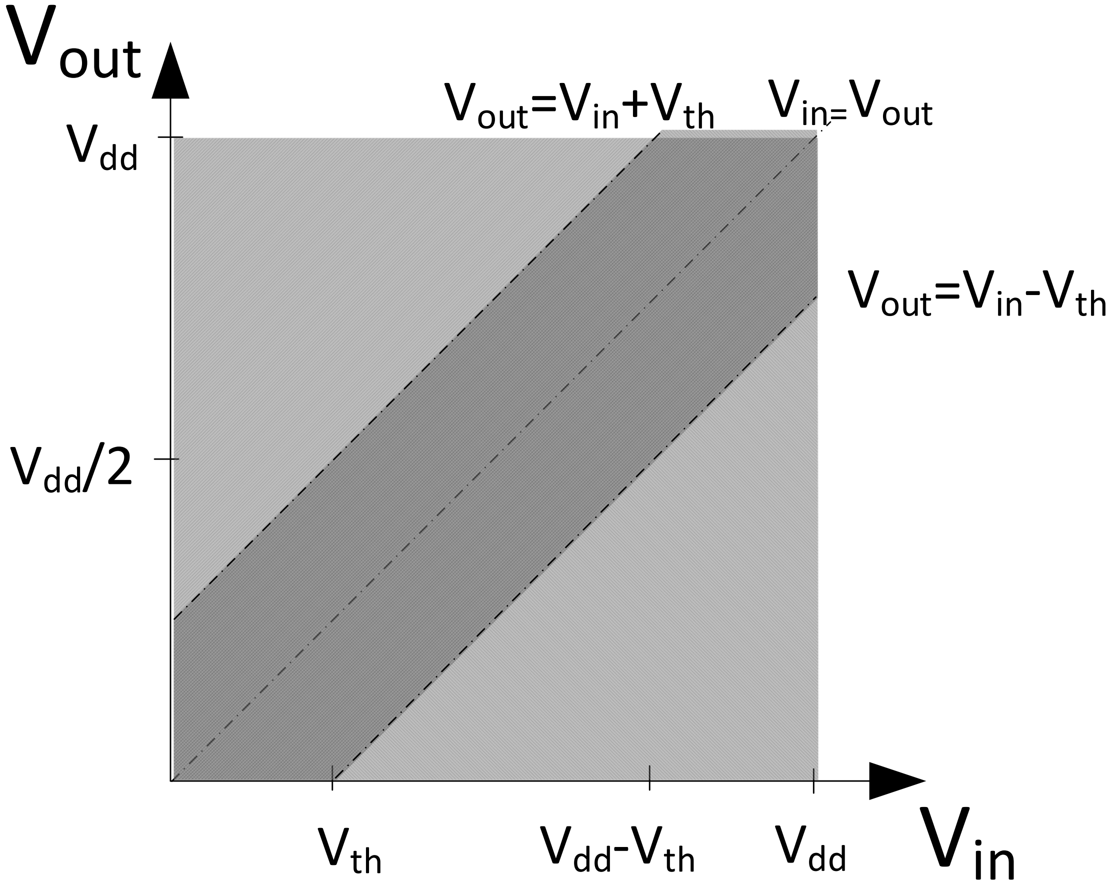
- $I_{dsat,n} = I_{dsat,p}$
- $V_{th,n} = V_{th,p} = 200mV$
- Mark out locus of operation

Inverter DC Analysis



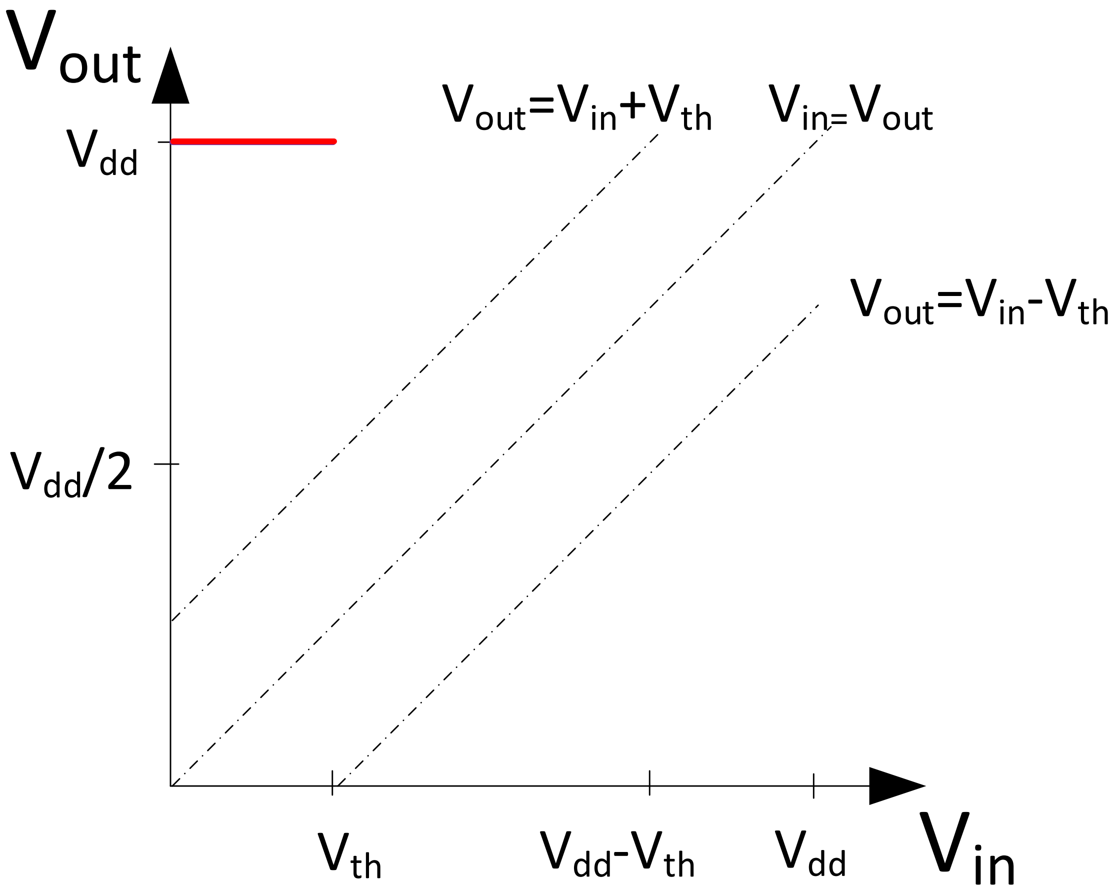
- $I_{dsat,n} = I_{dsat,p}$
- $V_{th,n} = V_{th,p} = 200mV$
- Mark out locus of operation

Inverter DC Analysis



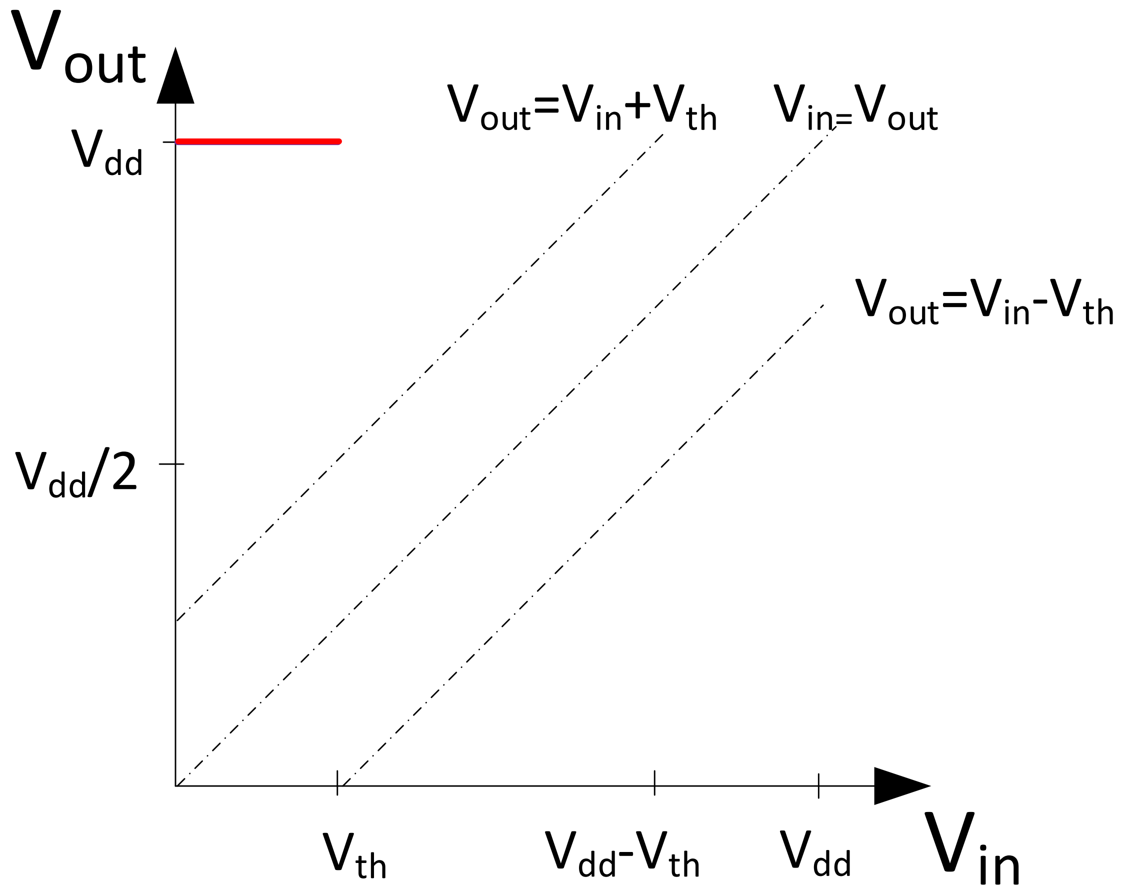
- $I_{dsat,n} = I_{dsat,p}$
- $V_{th,n} = V_{th,p} = 200mV$
- Mark out locus of operation

Inverter DC Analysis



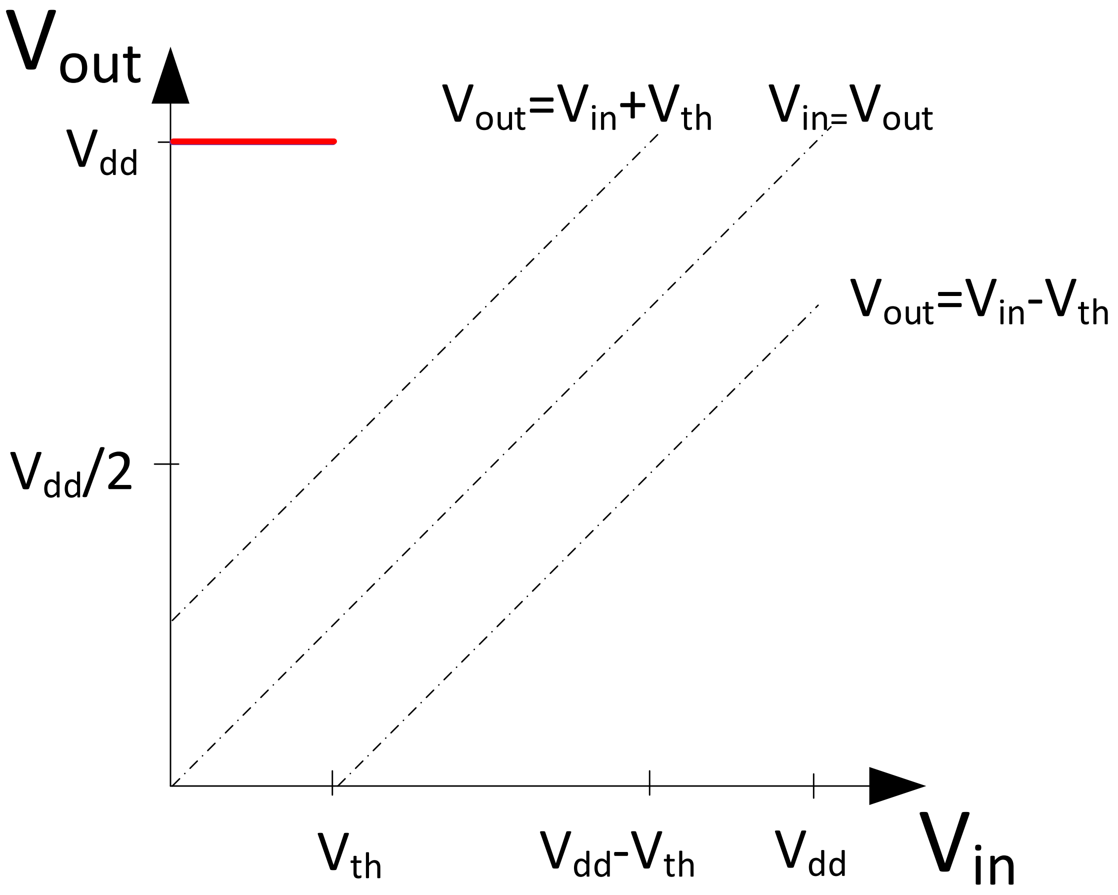
- $V_{in} = 0$

Inverter DC Analysis



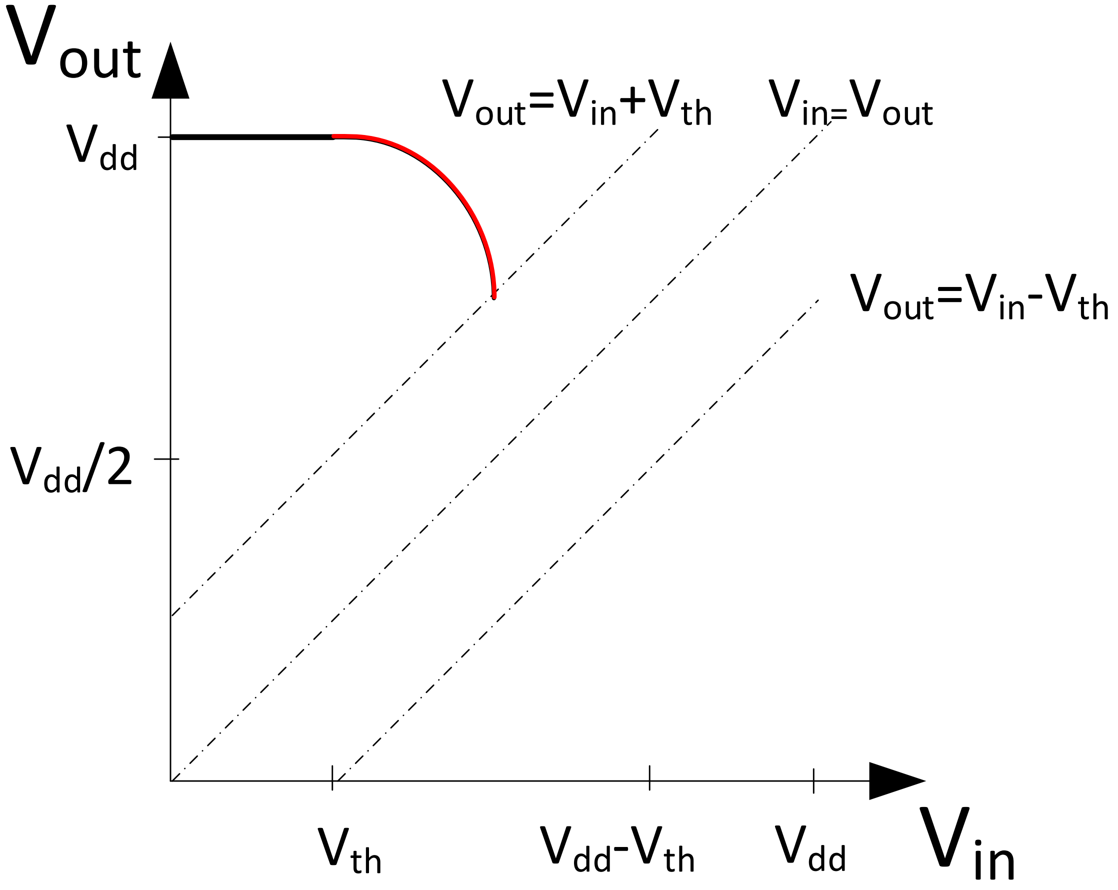
- $V_{in} = 0$ → Nmos in cutoff

Inverter DC Analysis



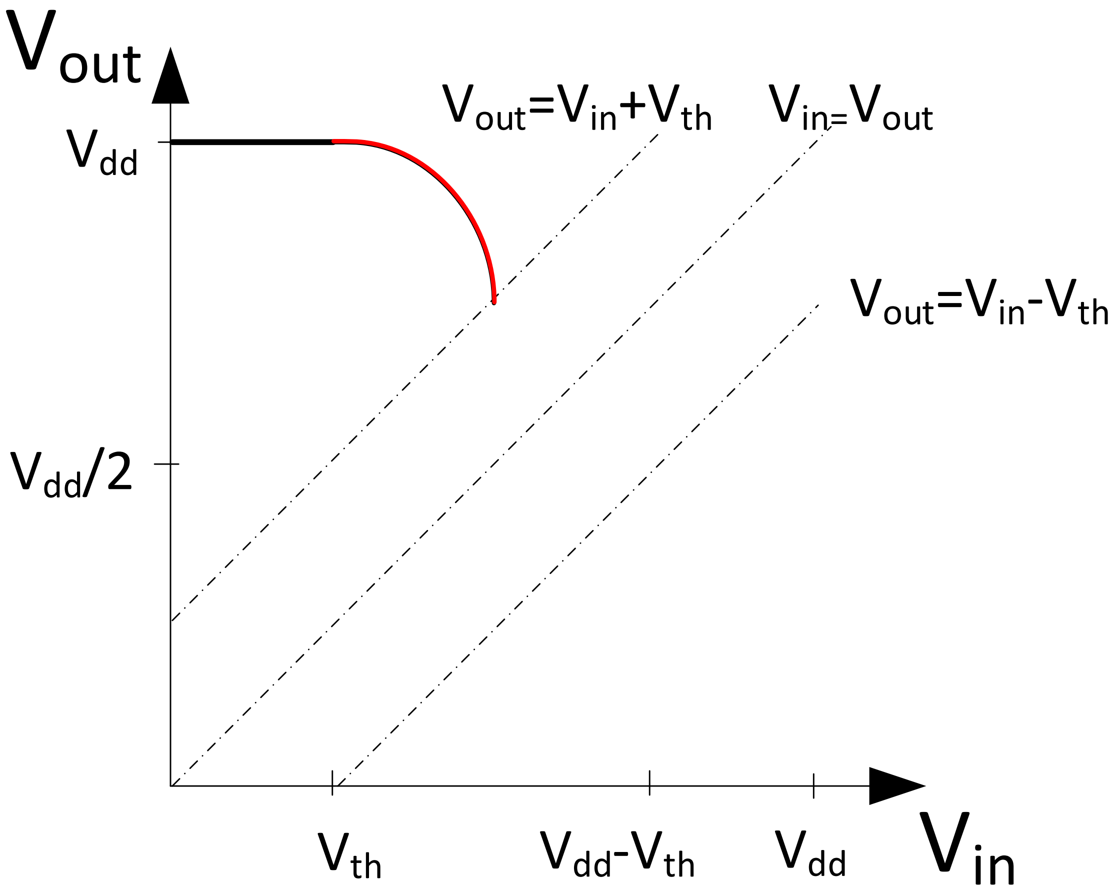
- $V_{in} = 0$ → Nmos in cutoff →Pmos in linear

Inverter DC Analysis



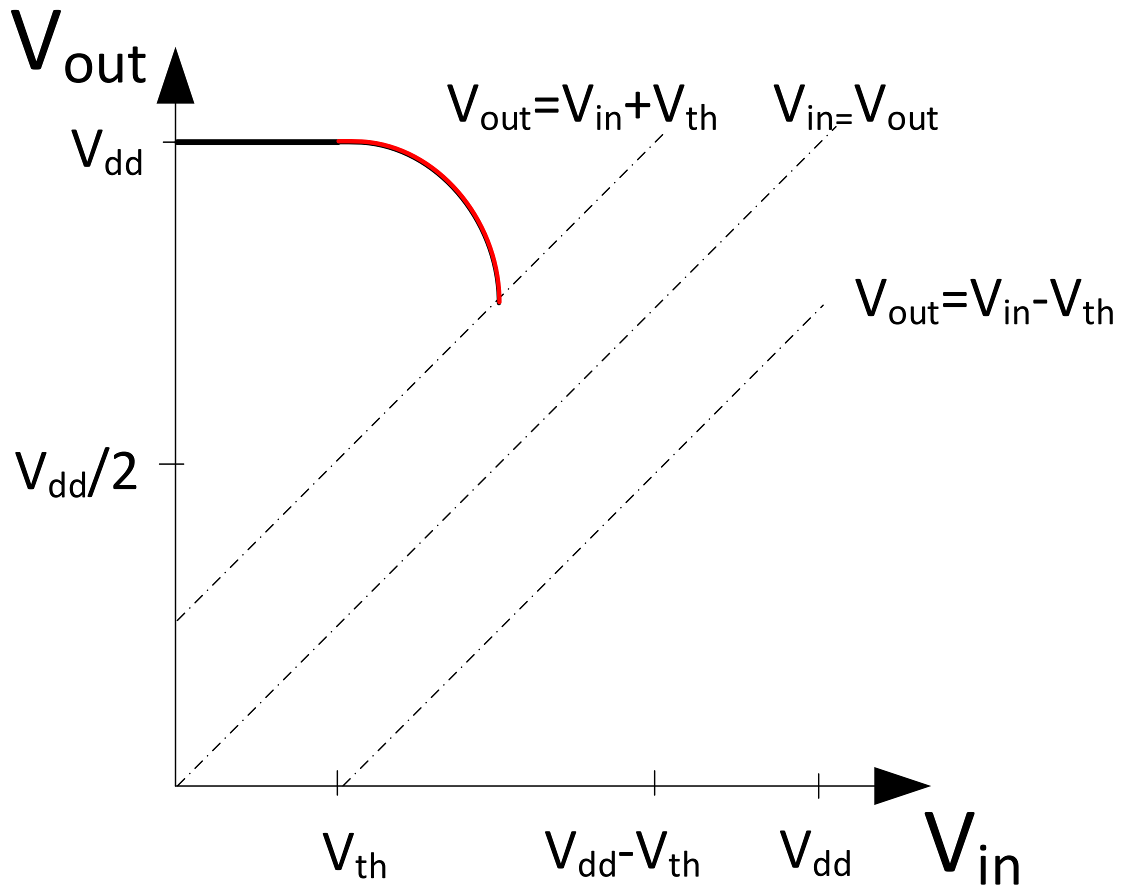
- $V_{th} < V_{in} < V_{out} - V_{th}$

Inverter DC Analysis



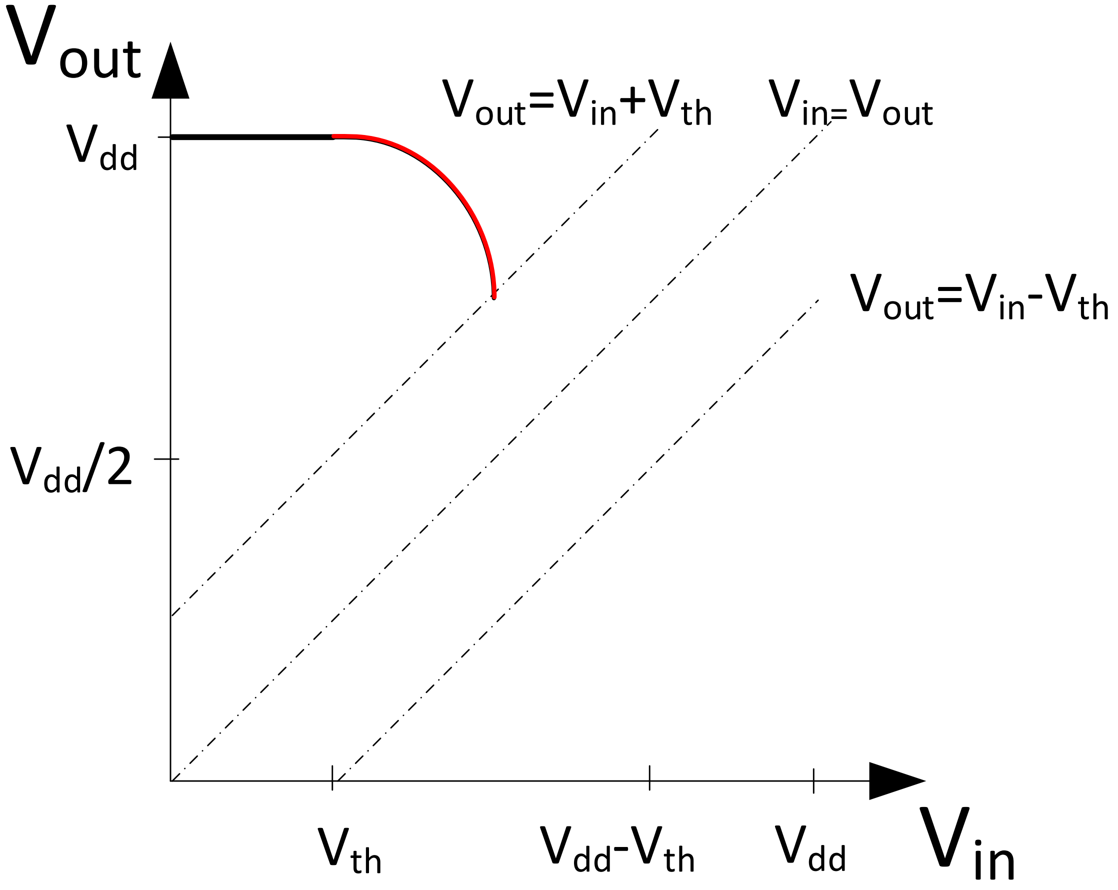
- $V_{th} < V_{in} < V_{out} - V_{th}$
  - Nmos turns on in saturation

Inverter DC Analysis



- $V_{th} < V_{in} < V_{out} - V_{th}$
  - Nmos turns on in saturation
  - Pmos in linear

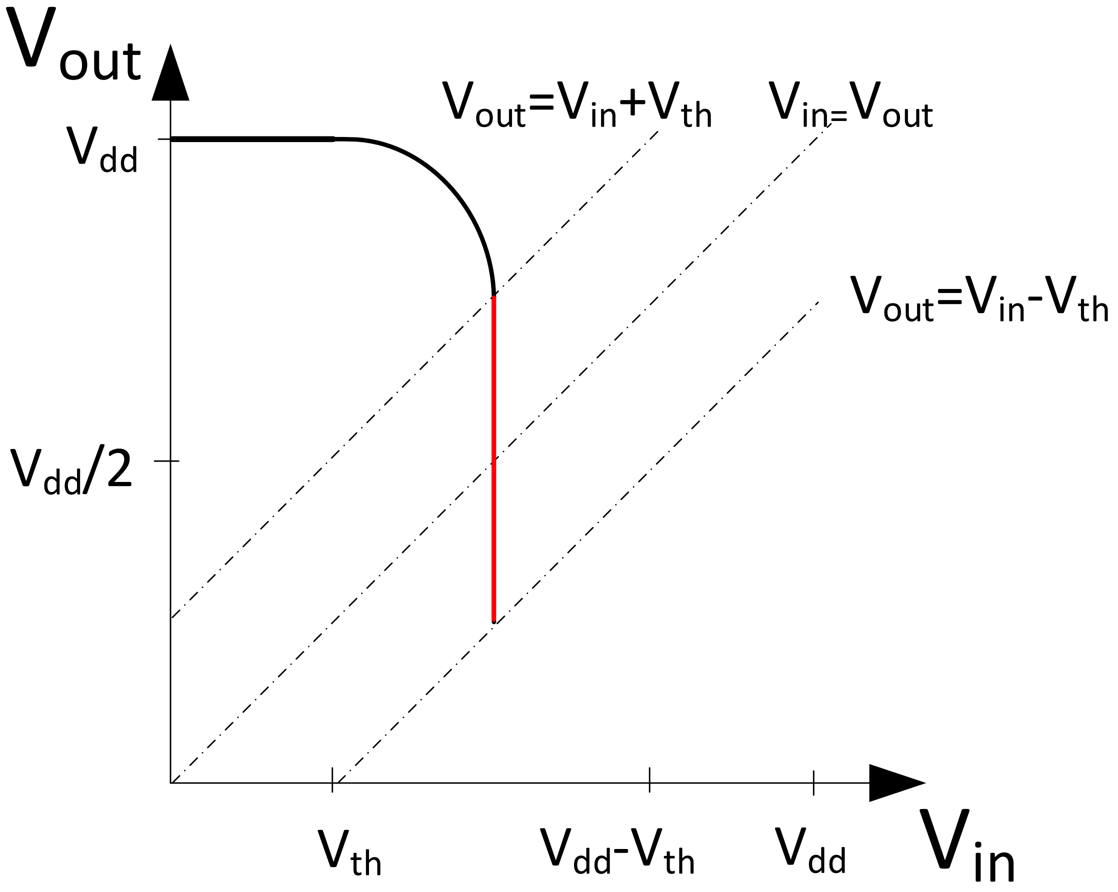
Inverter DC Analysis



- $V_{th} < V_{in} < V_{out} - V_{th}$
  - Nmos turns on in saturation
  - Pmos in linear

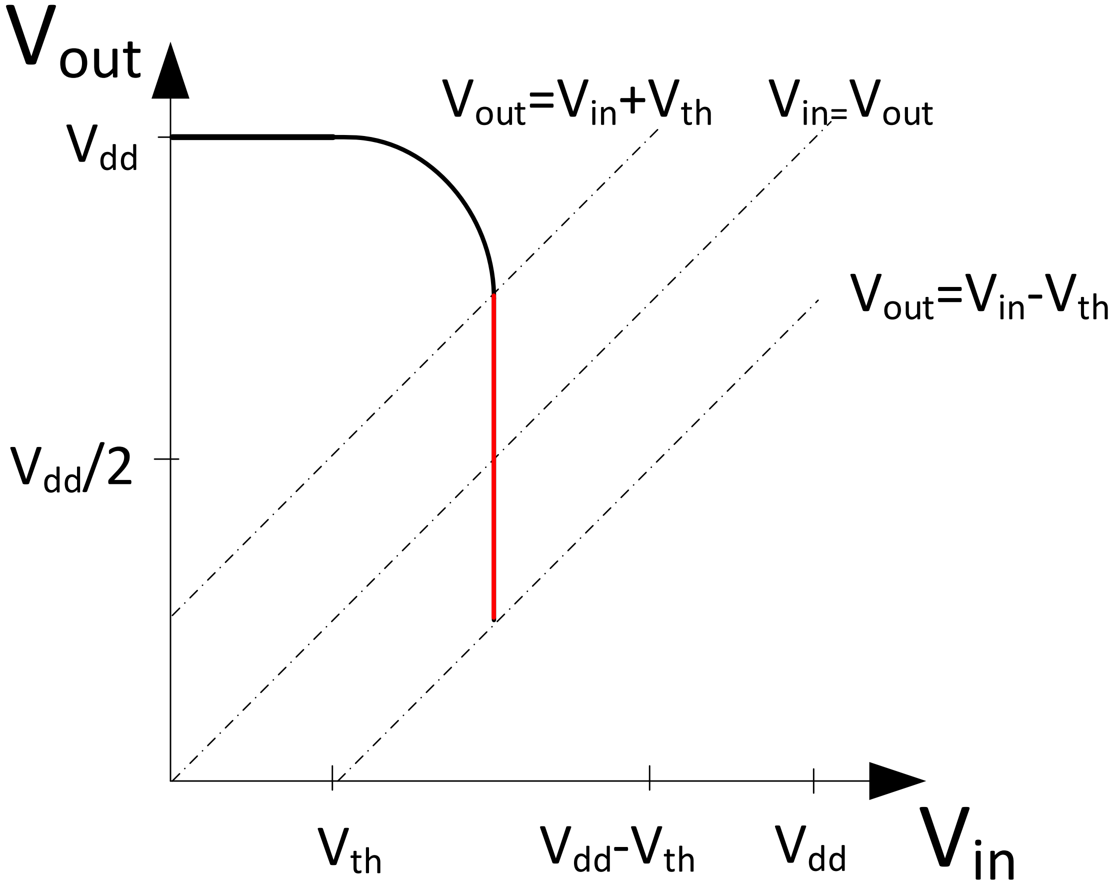
Analytically, approximate
The rate of descent of Vout.
(sub|super) (linear/quadratic/cubic)

Inverter DC Analysis



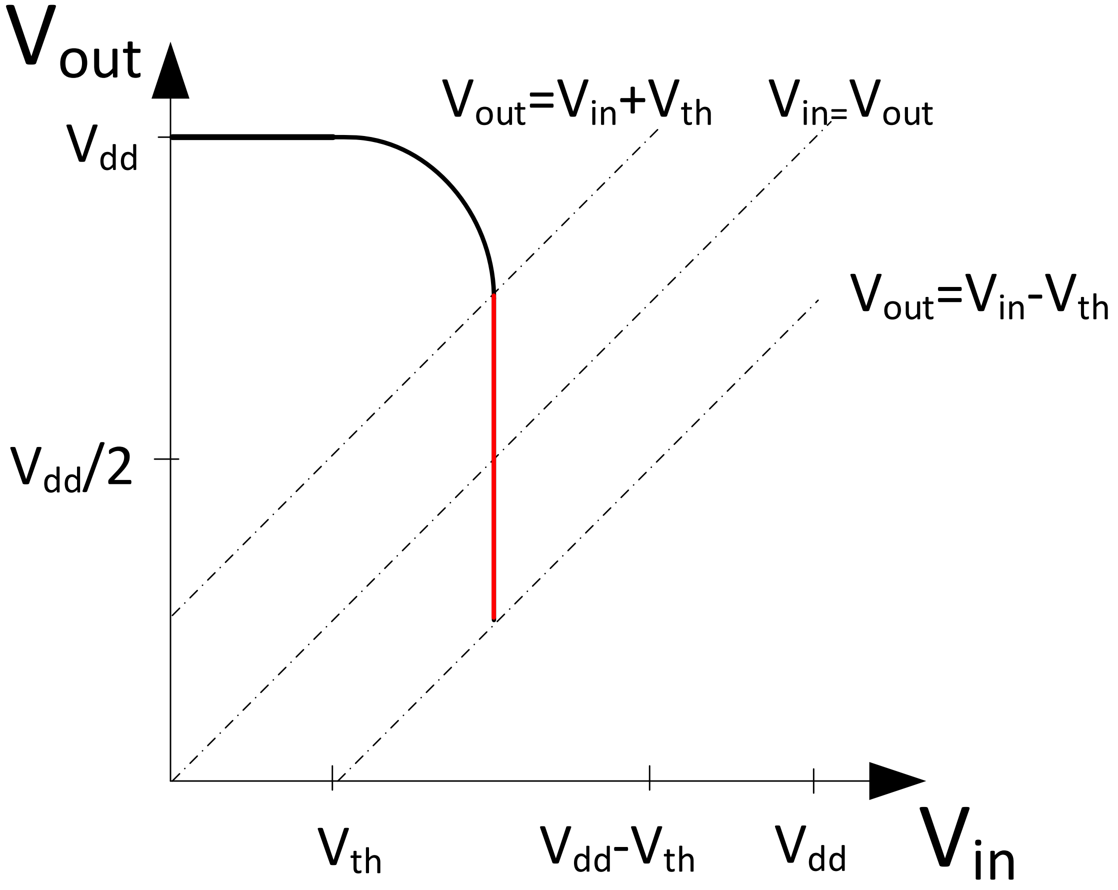
- $V_{out} - V_{th} < V_{in} < V_{out} + V_{th}$

Inverter DC Analysis



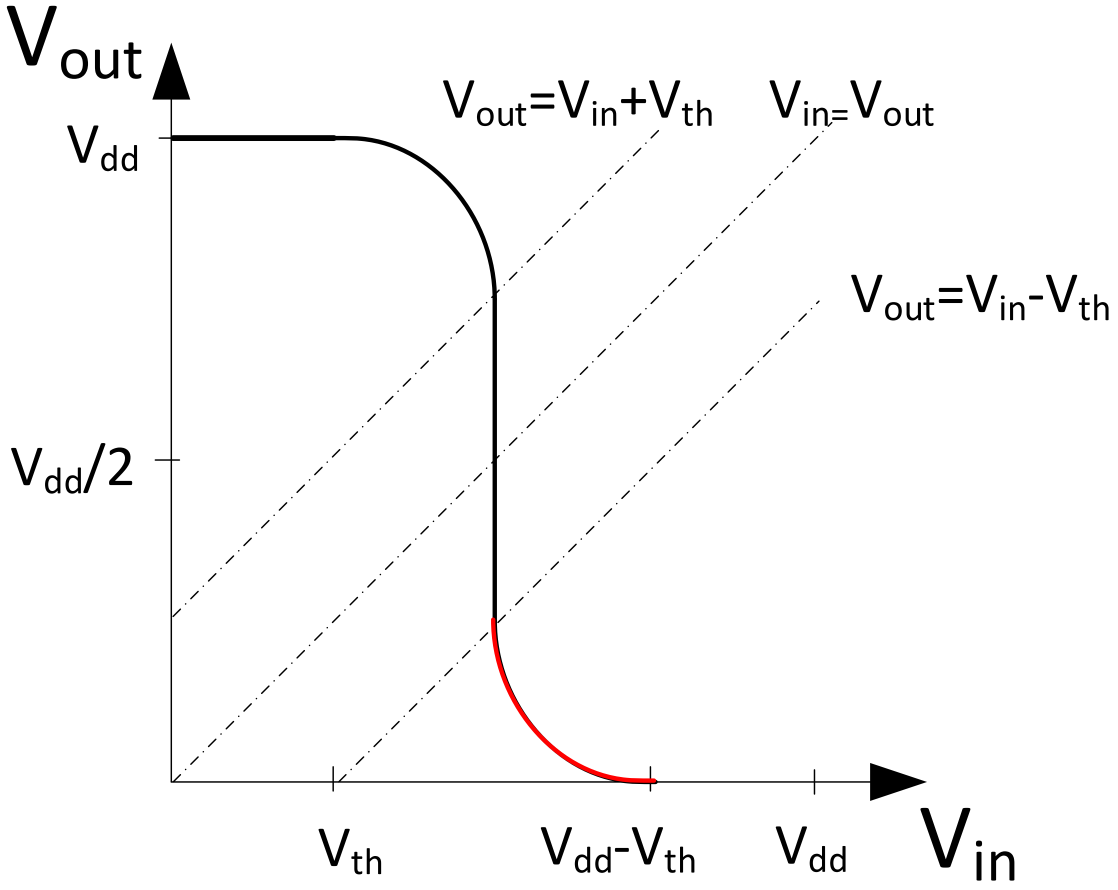
- $V_{out} - V_{th} < V_{in} < V_{out} + V_{th}$
  - Nmos remains in saturation

Inverter DC Analysis



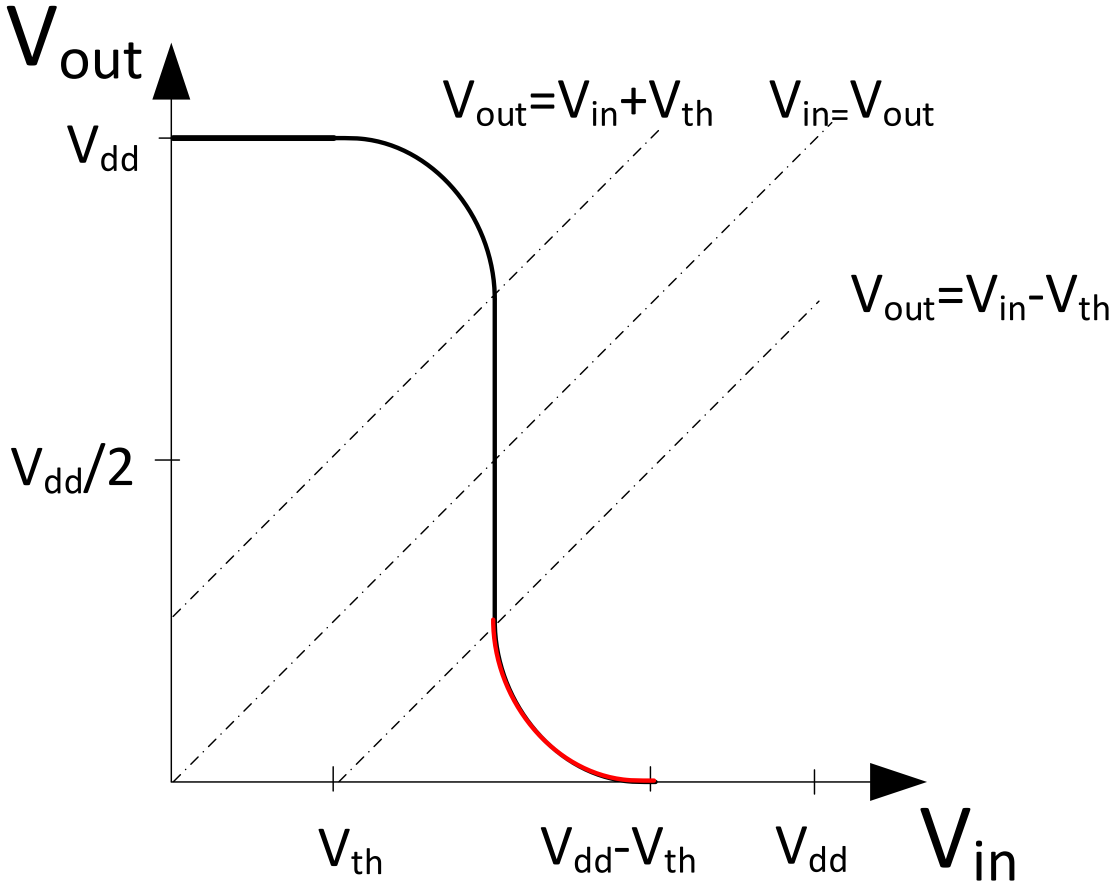
- $V_{out} - V_{th} < V_{in} < V_{out} + V_{th}$
  - Nmos remains in saturation
  - Pmos transitions to saturation

Inverter DC Analysis



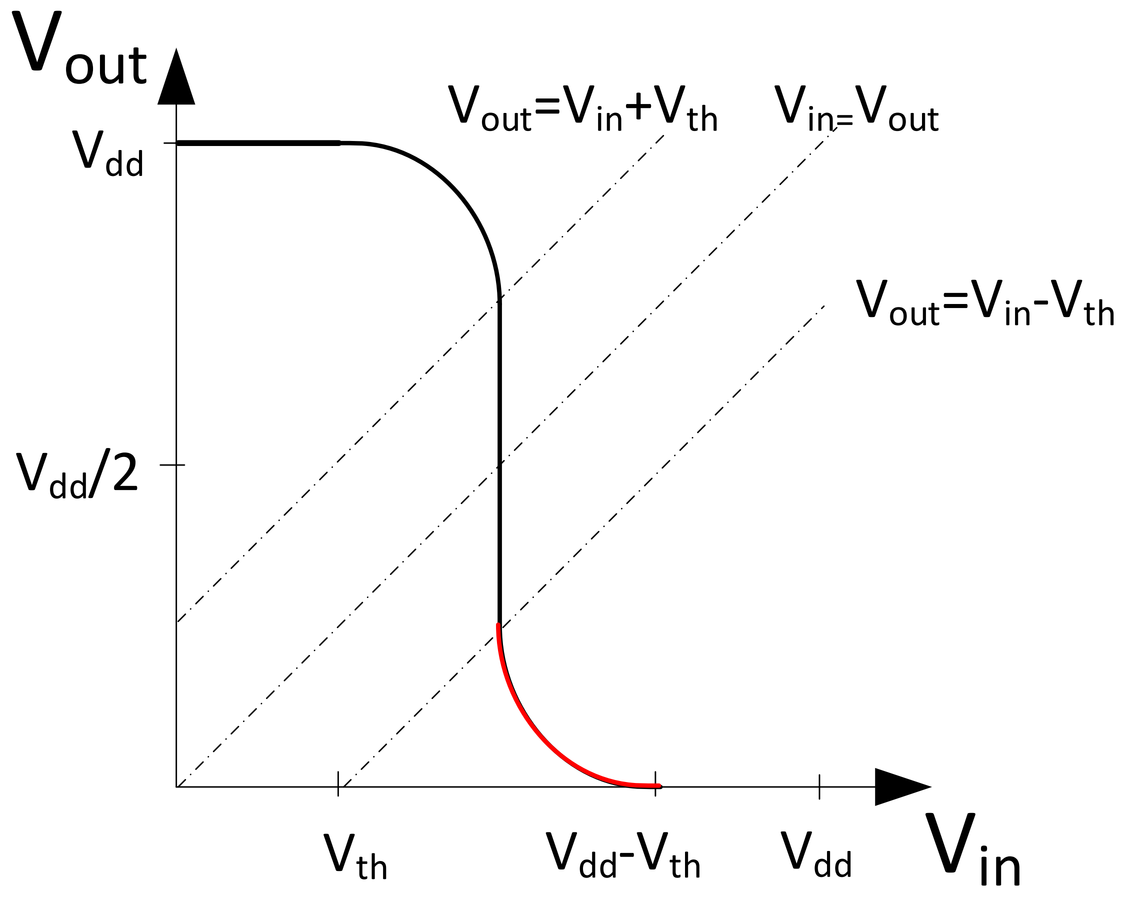
- $V_{out} + V_{th} < V_{in} < V_{dd} - V_{th}$

Inverter DC Analysis



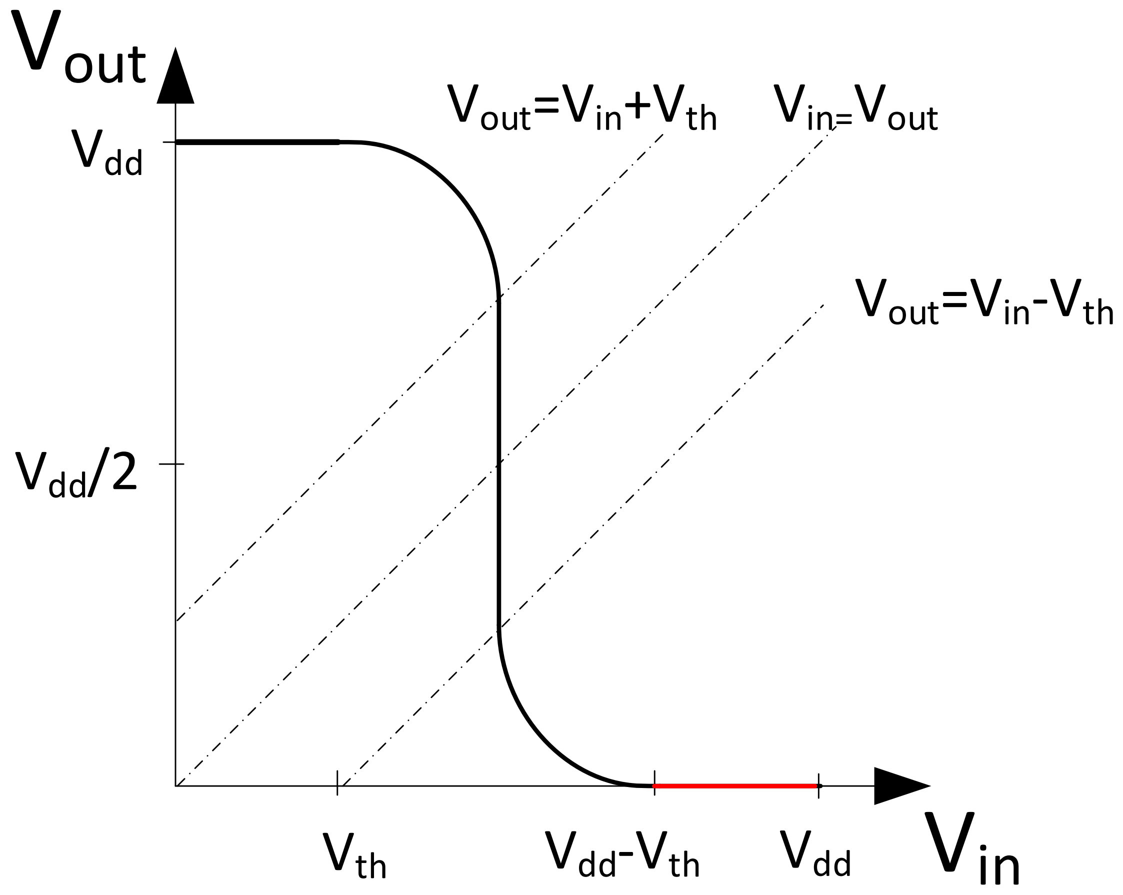
- $V_{out} + V_{th} < V_{in} < V_{dd} - V_{th}$
  - Nmos transitions to linear

Inverter DC Analysis



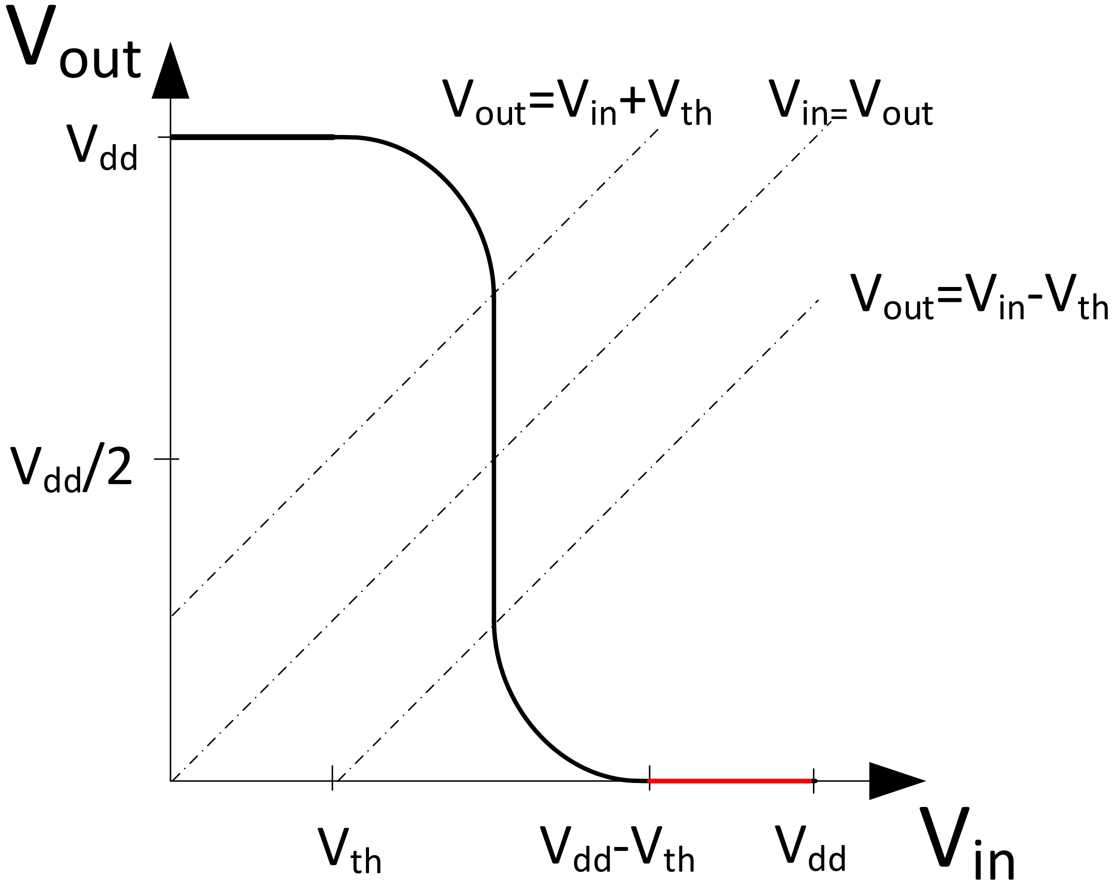
- $V_{out} + V_{th} < V_{in} < V_{dd} - V_{th}$
  - Nmos transitions to linear
  - Pmos remains in saturation

Inverter DC Analysis



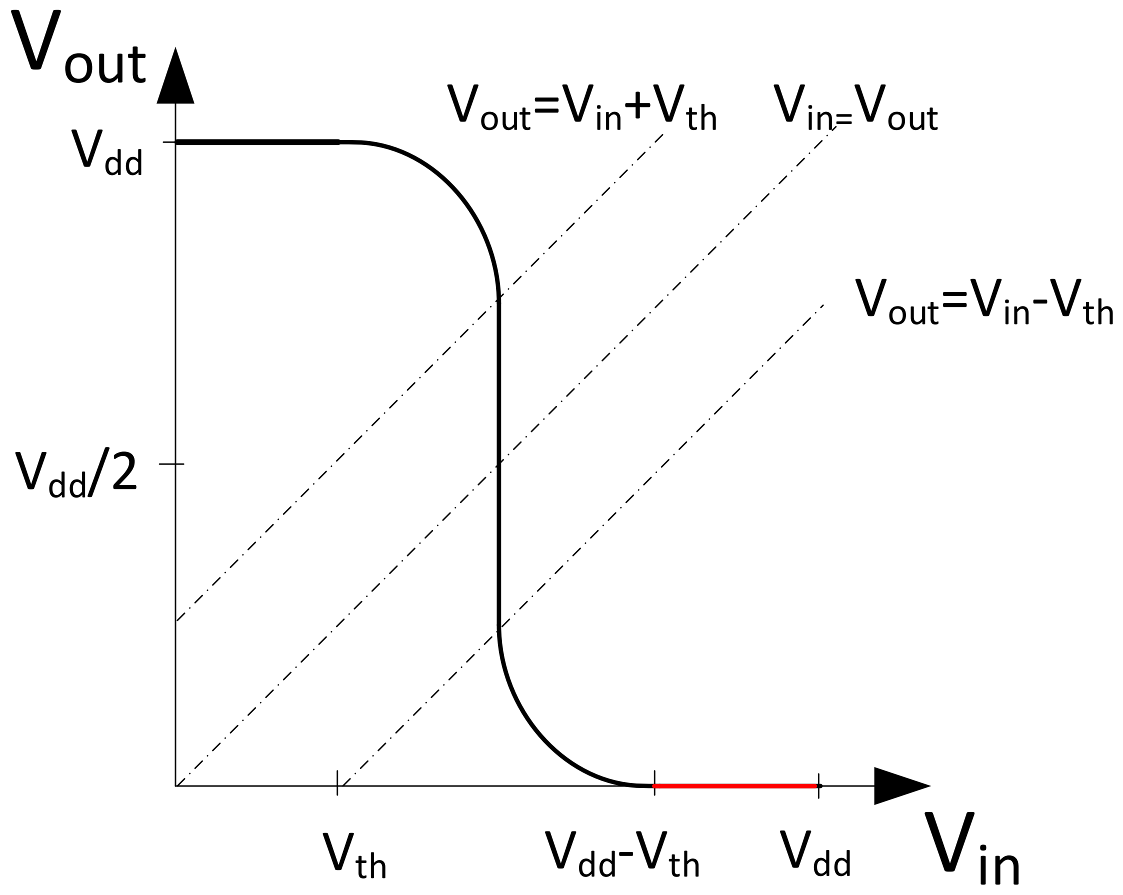
- $V_{dd} - V_{th} < V_{in} < V_{dd}$

Inverter DC Analysis



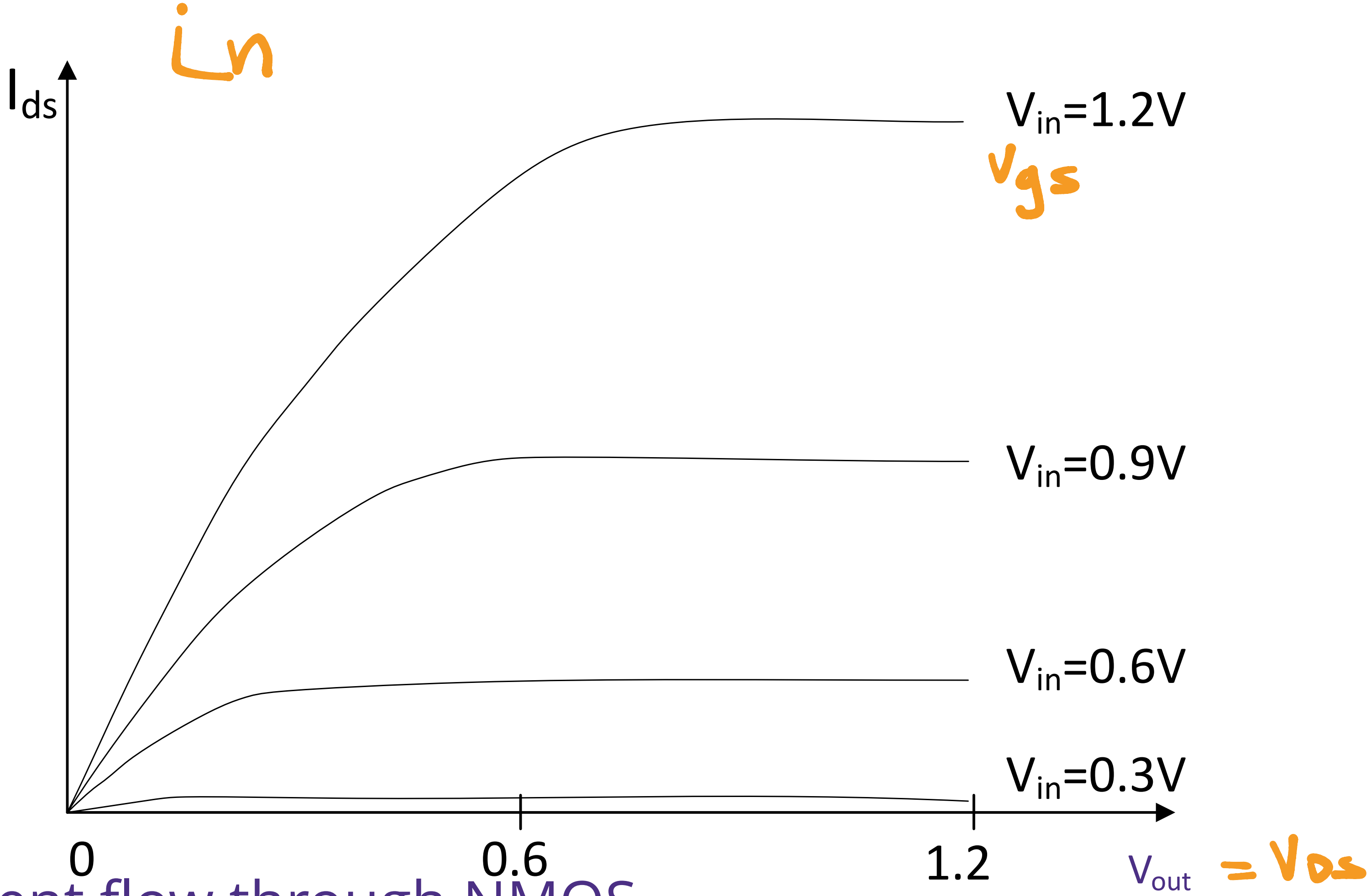
- $V_{dd} - V_{th} < V_{in} < V_{dd}$
  - Nmos remains in linear

Inverter DC Analysis



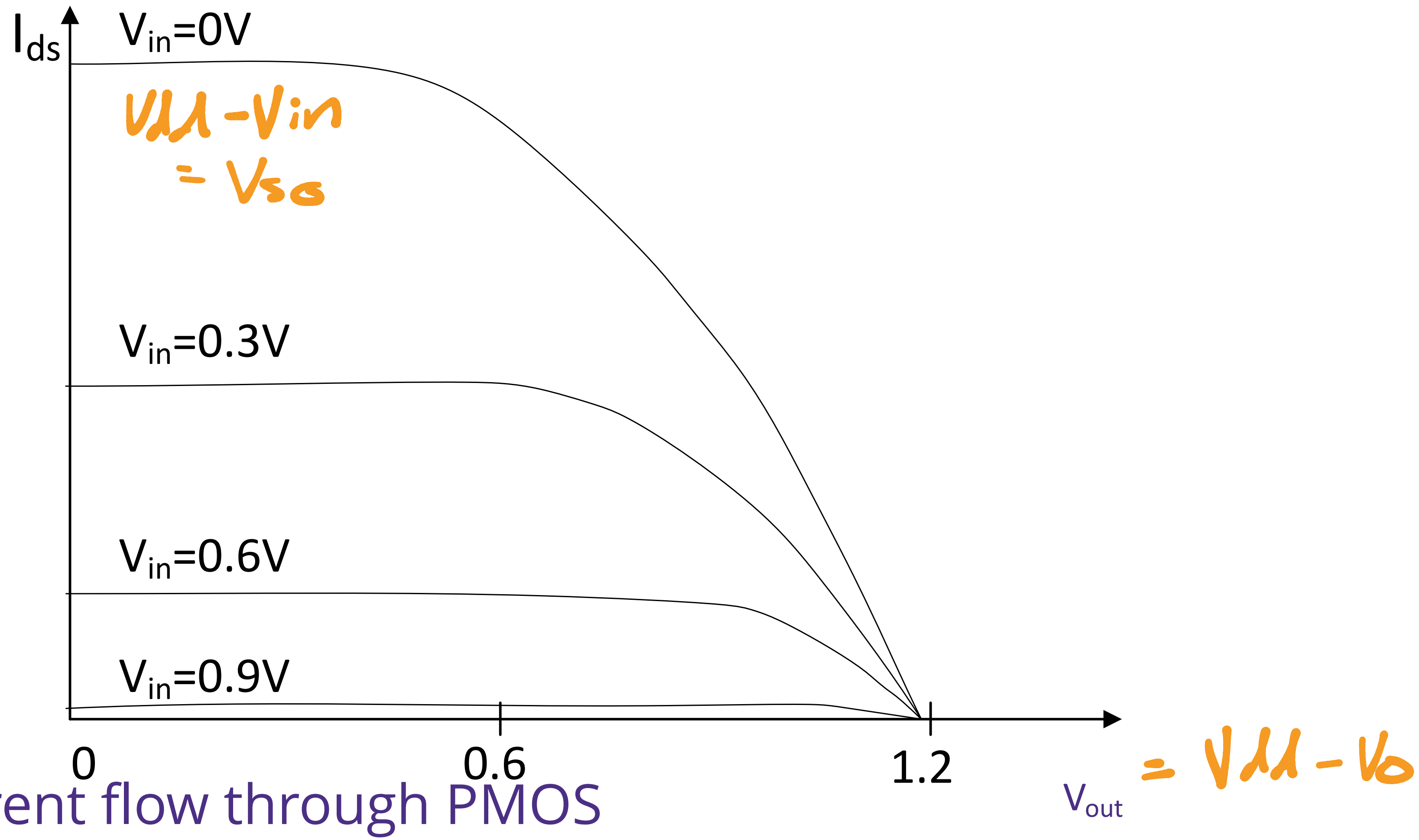
- $V_{dd} - V_{th} < V_{in} < V_{dd}$
  - Nmos remains in linear
  - Pmos transitions to cut-off

Graphical View: I_{ds} vs. V_{in}



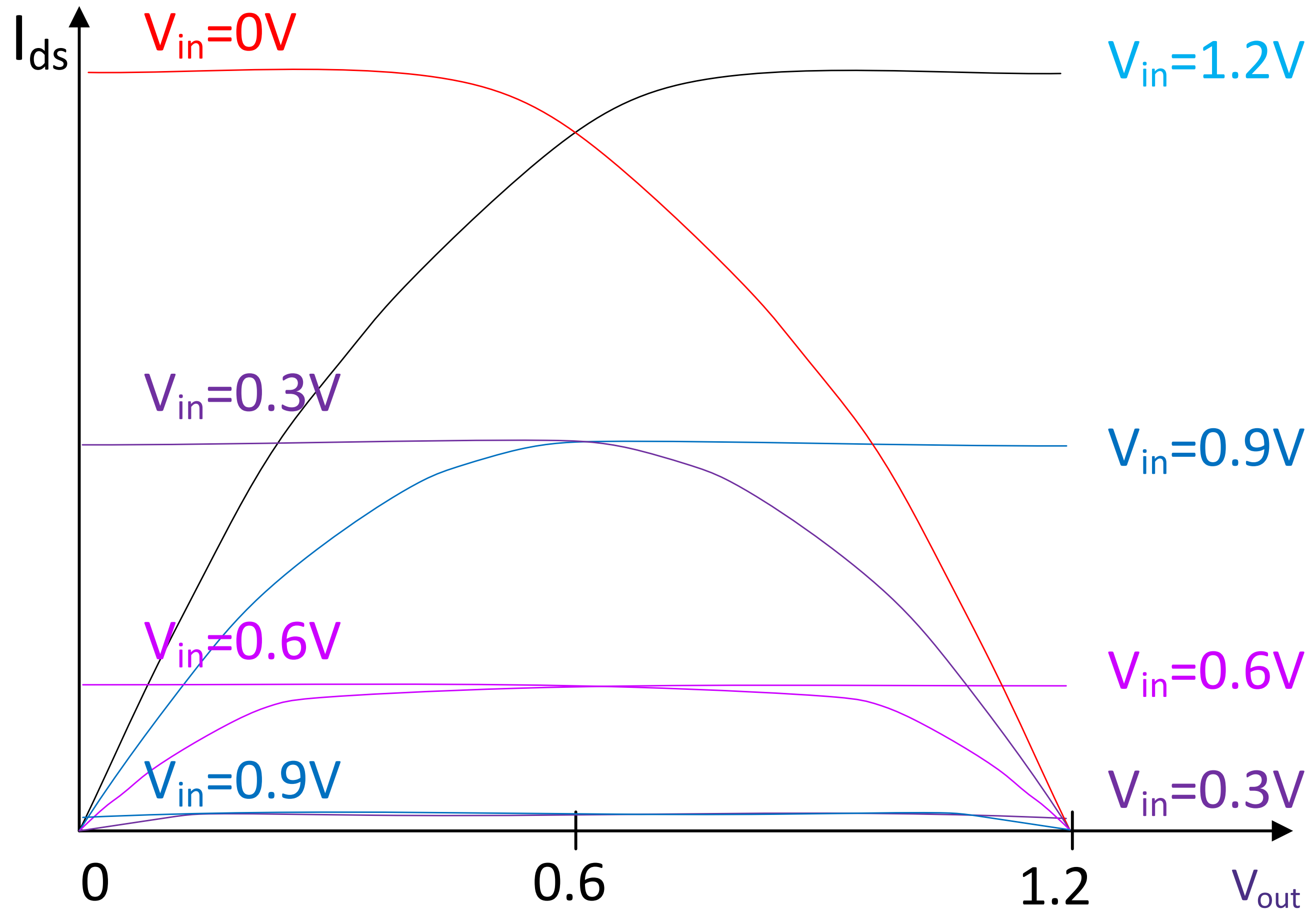
- Analyze the current flow through NMOS

Graphical View: I_{ds} vs. V_{out}

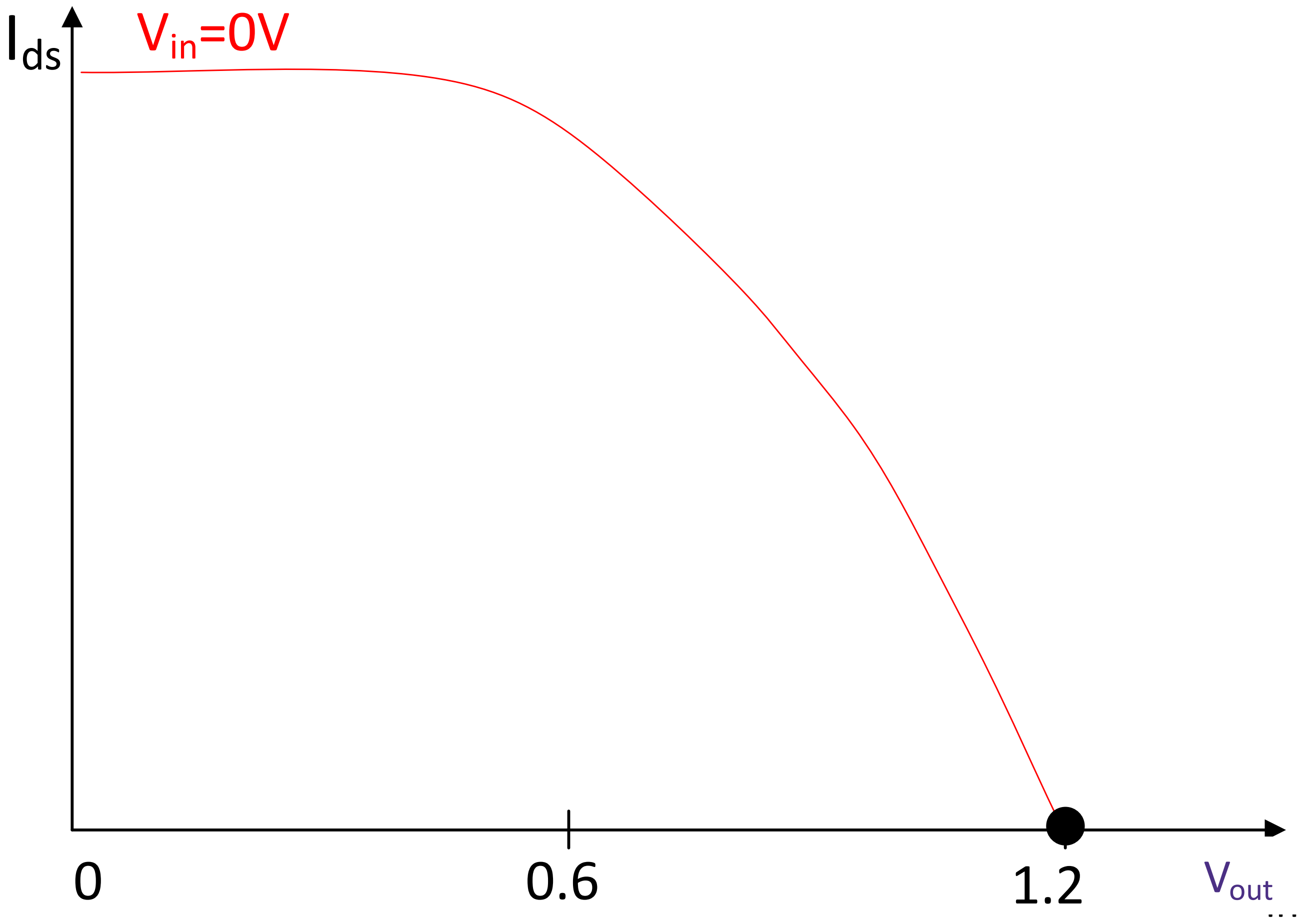


- Analyze the current flow through PMOS

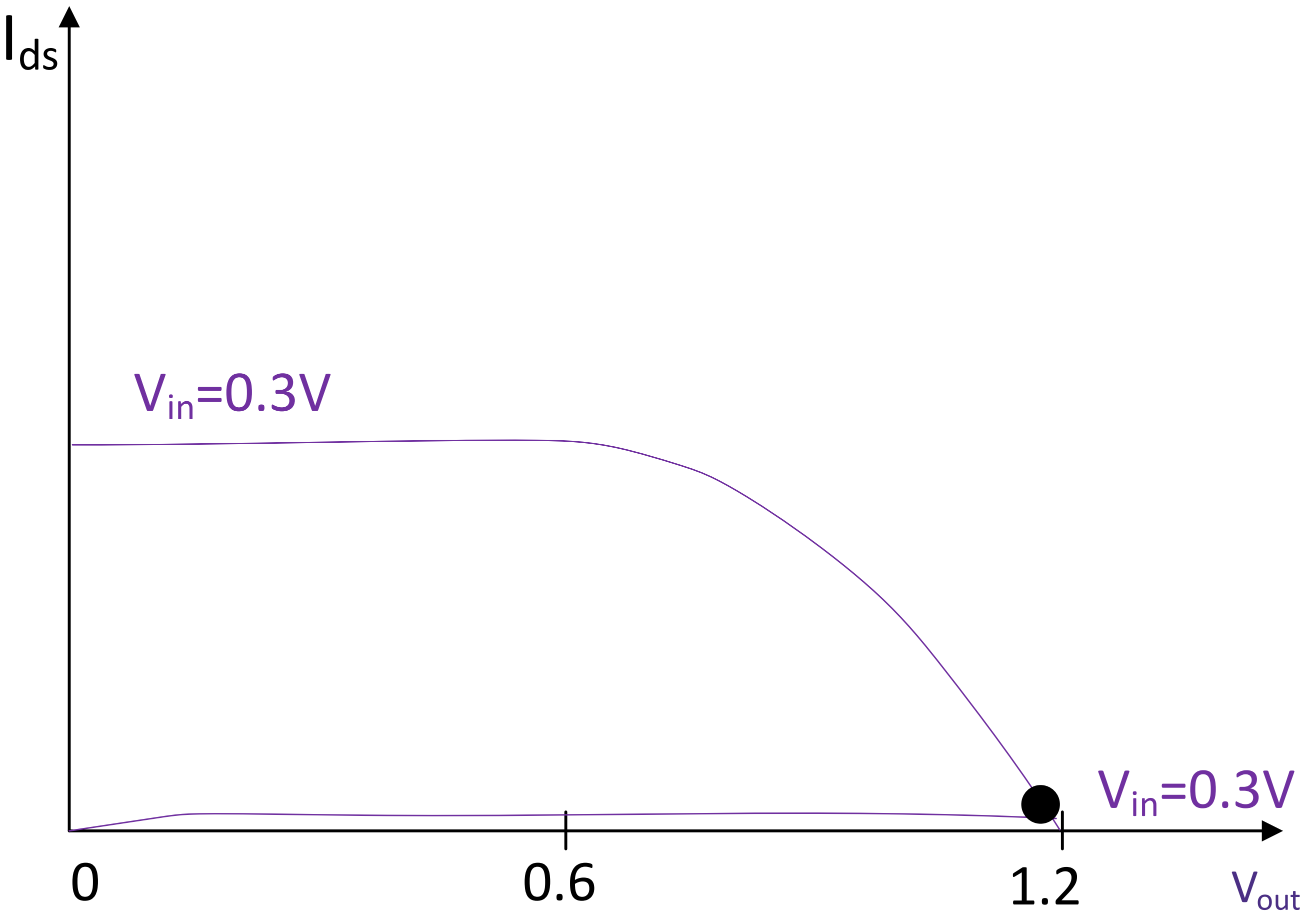
Loadline Analysis



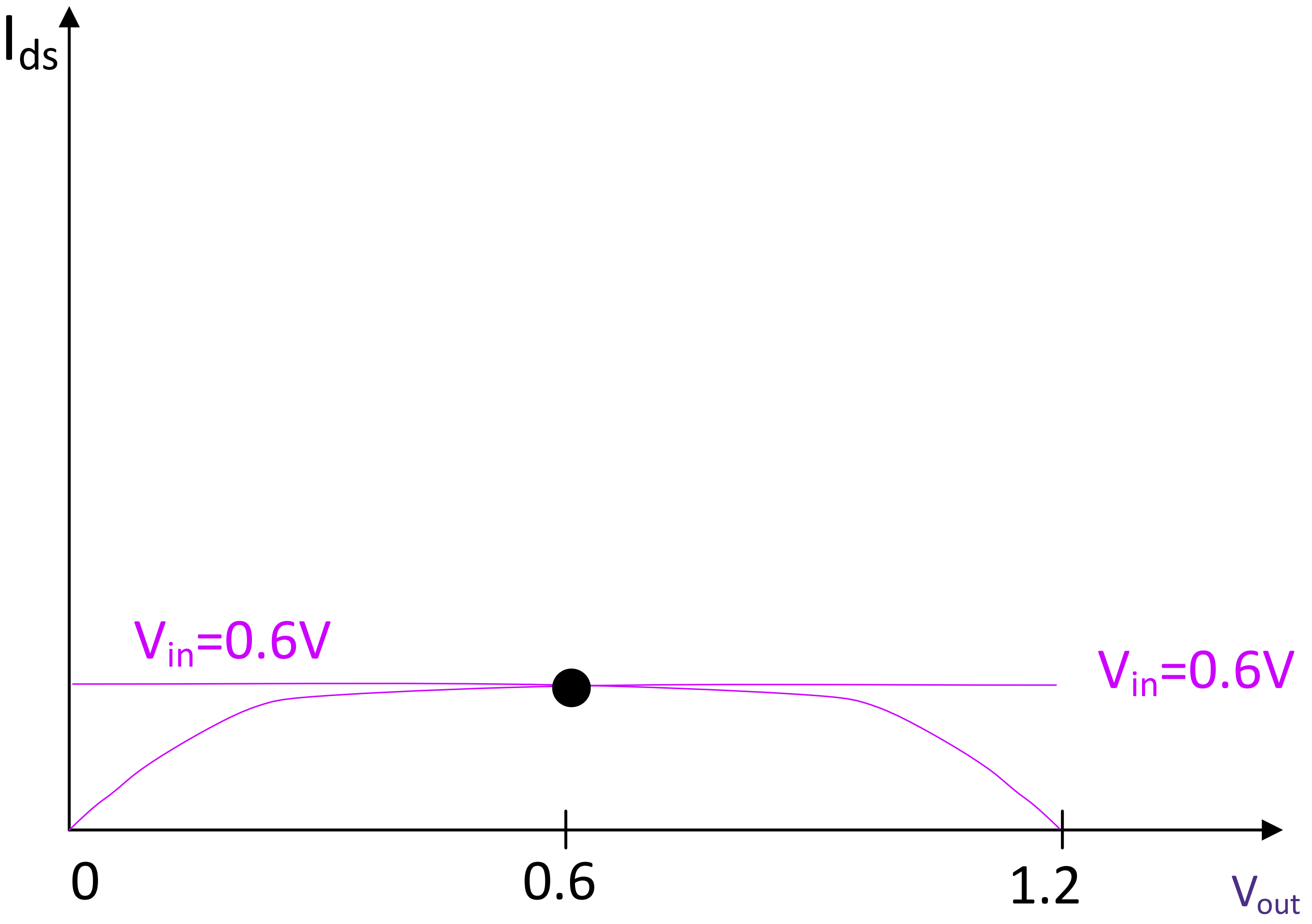
Loadline Analysis



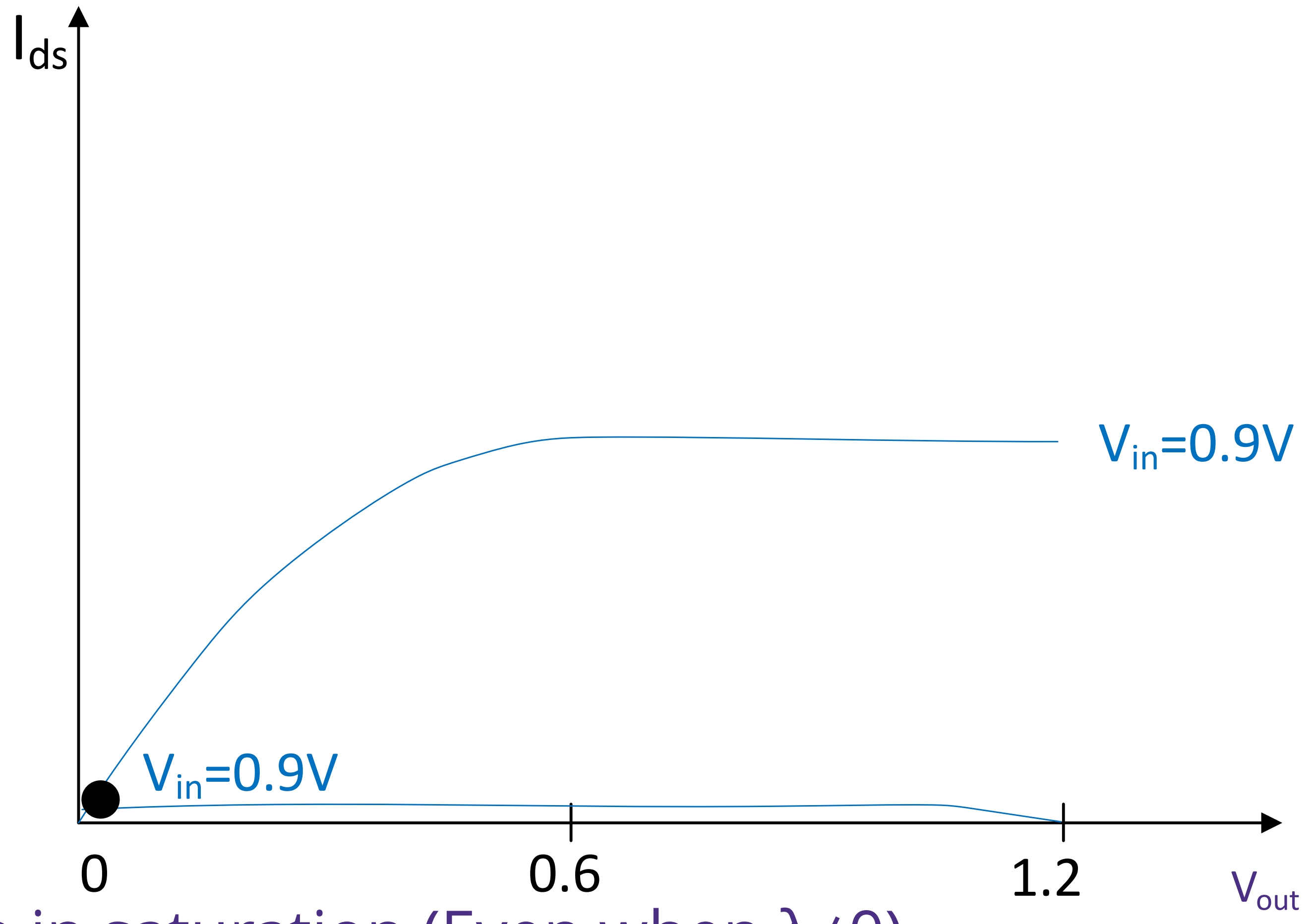
Loadline Analysis



Loadline Analysis

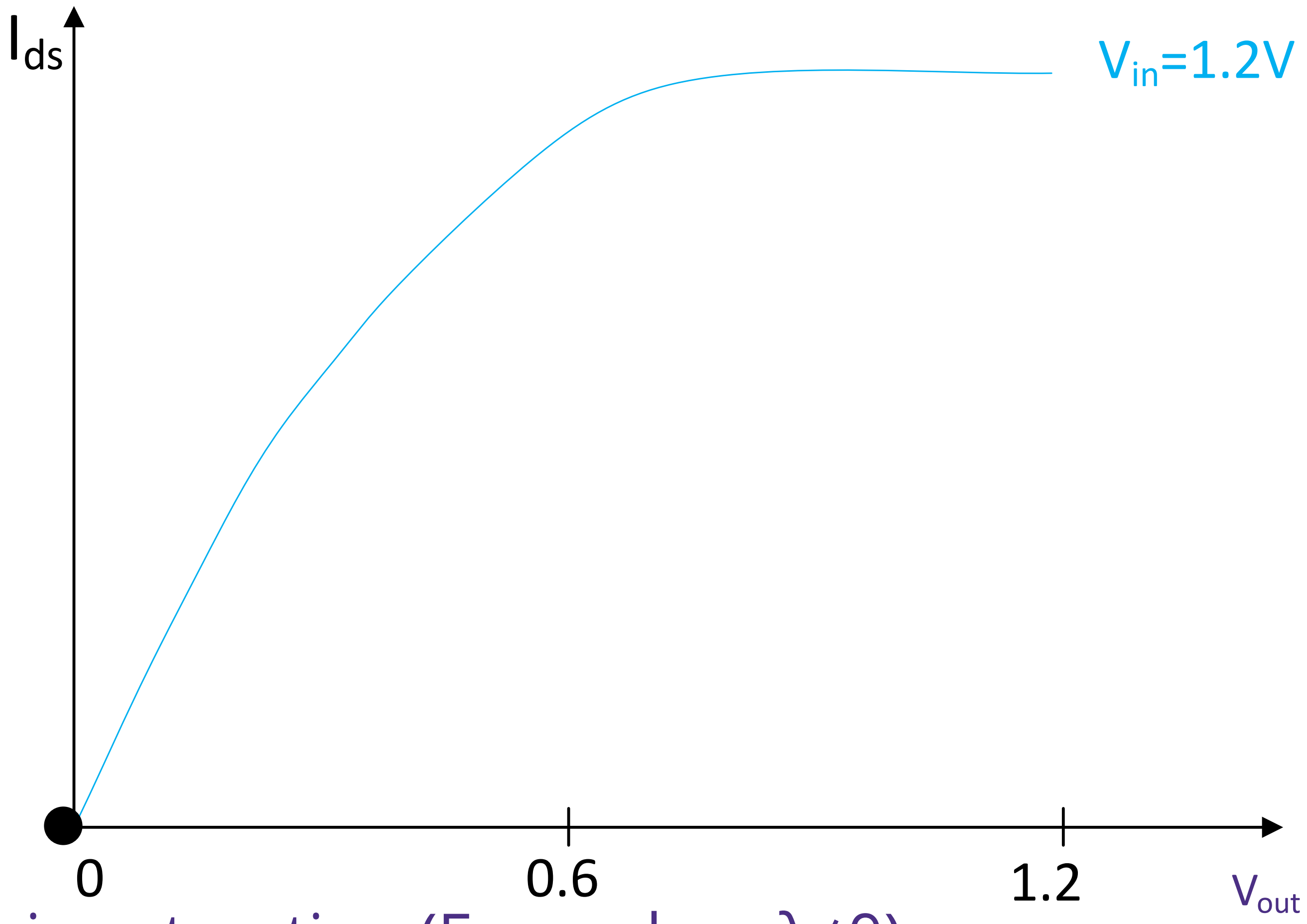


Current across the DC sweep



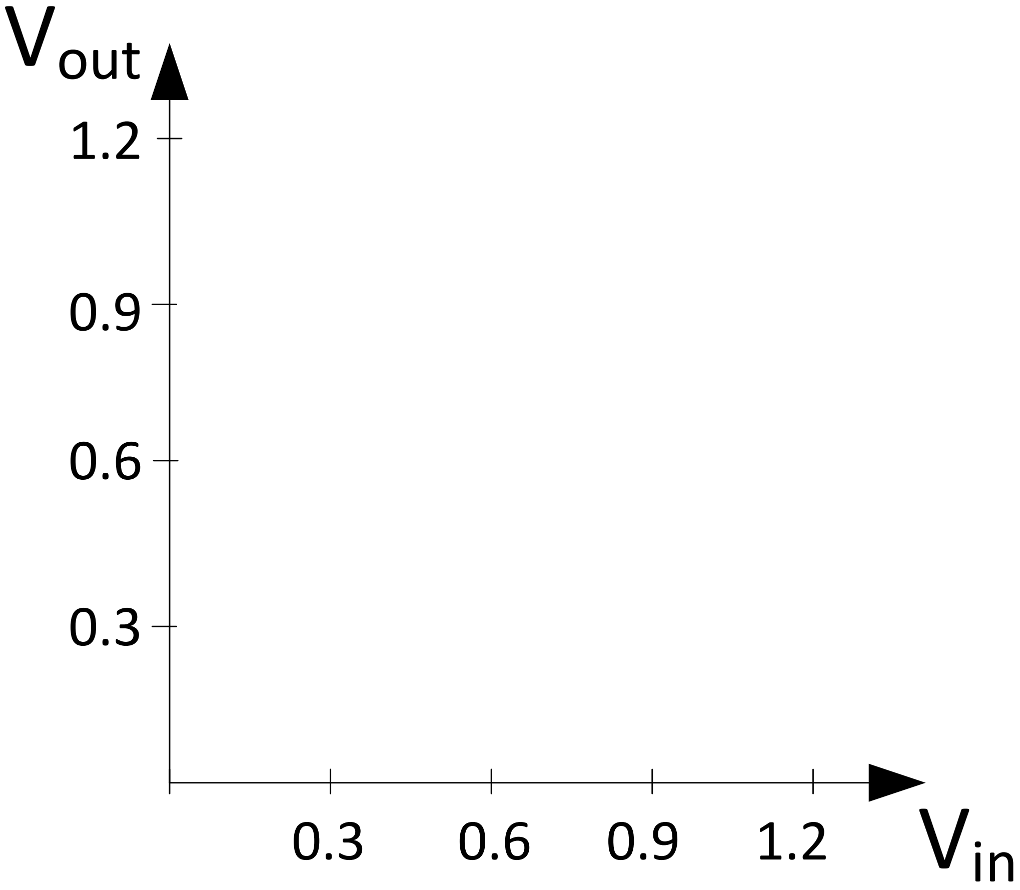
- Follow the device in saturation (Even when λ≠0)

Current across the DC sweep

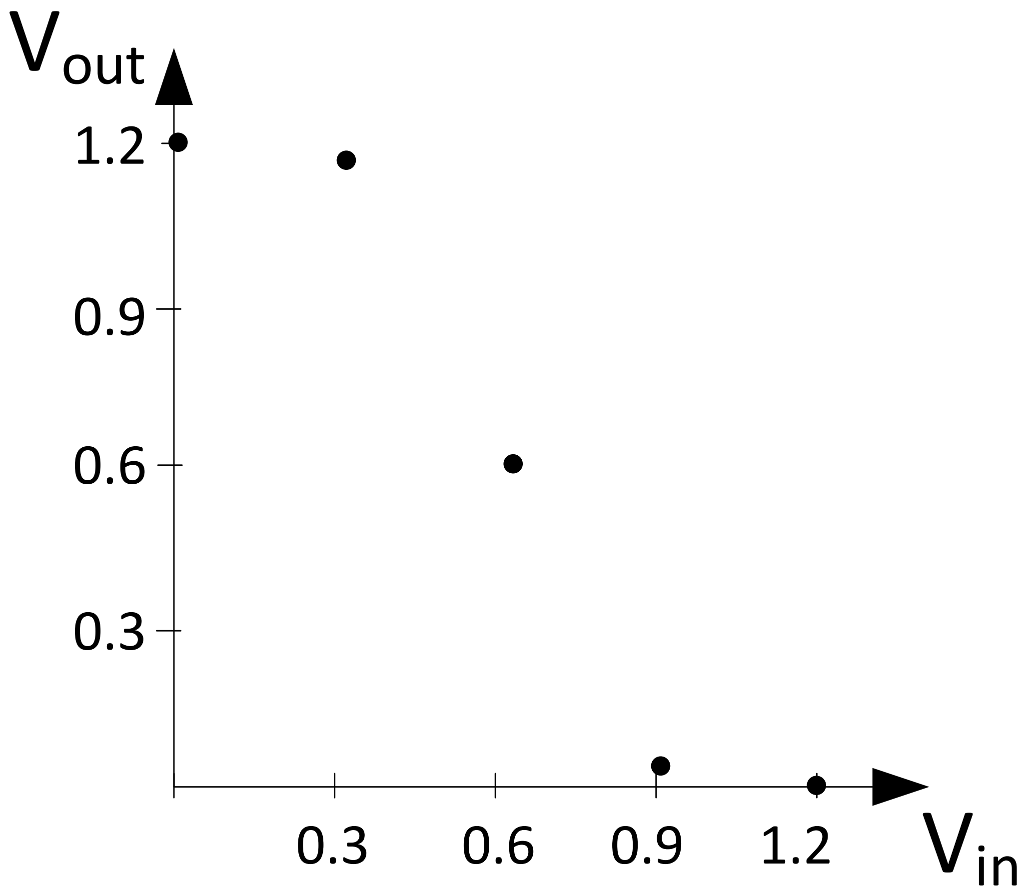


- Follow the device in saturation (Even when λ≠0)

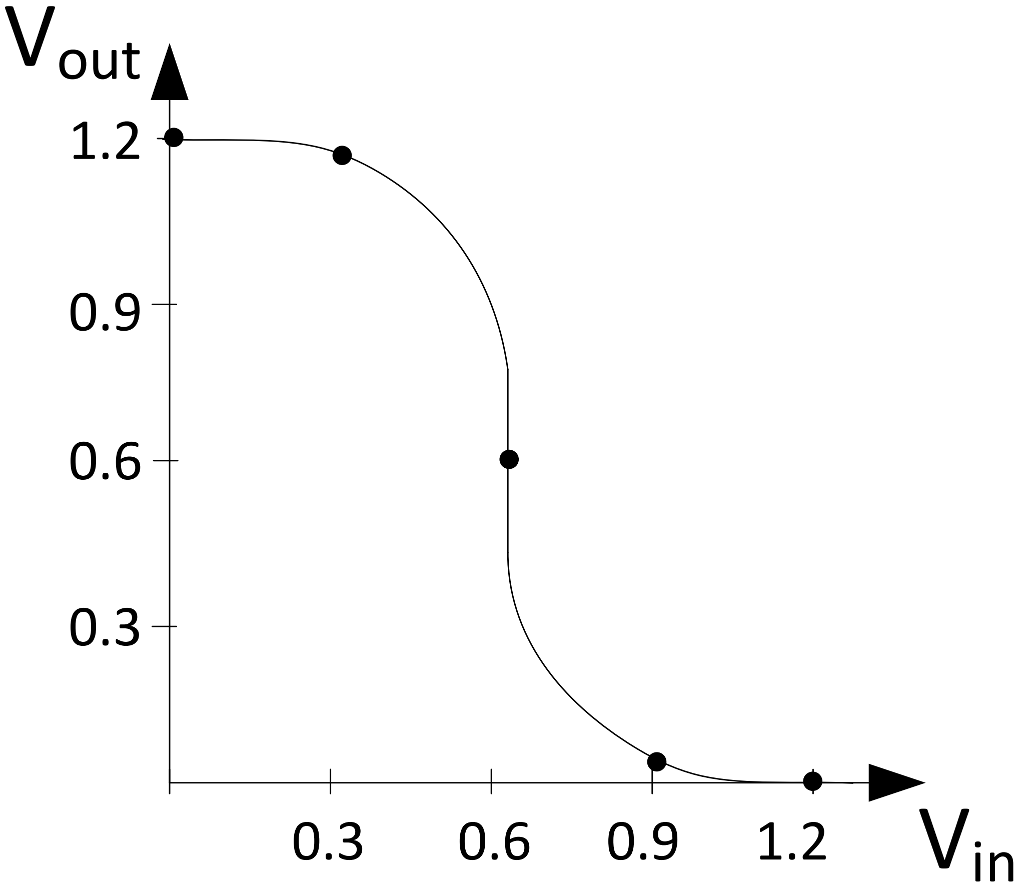
Loadline Analysis



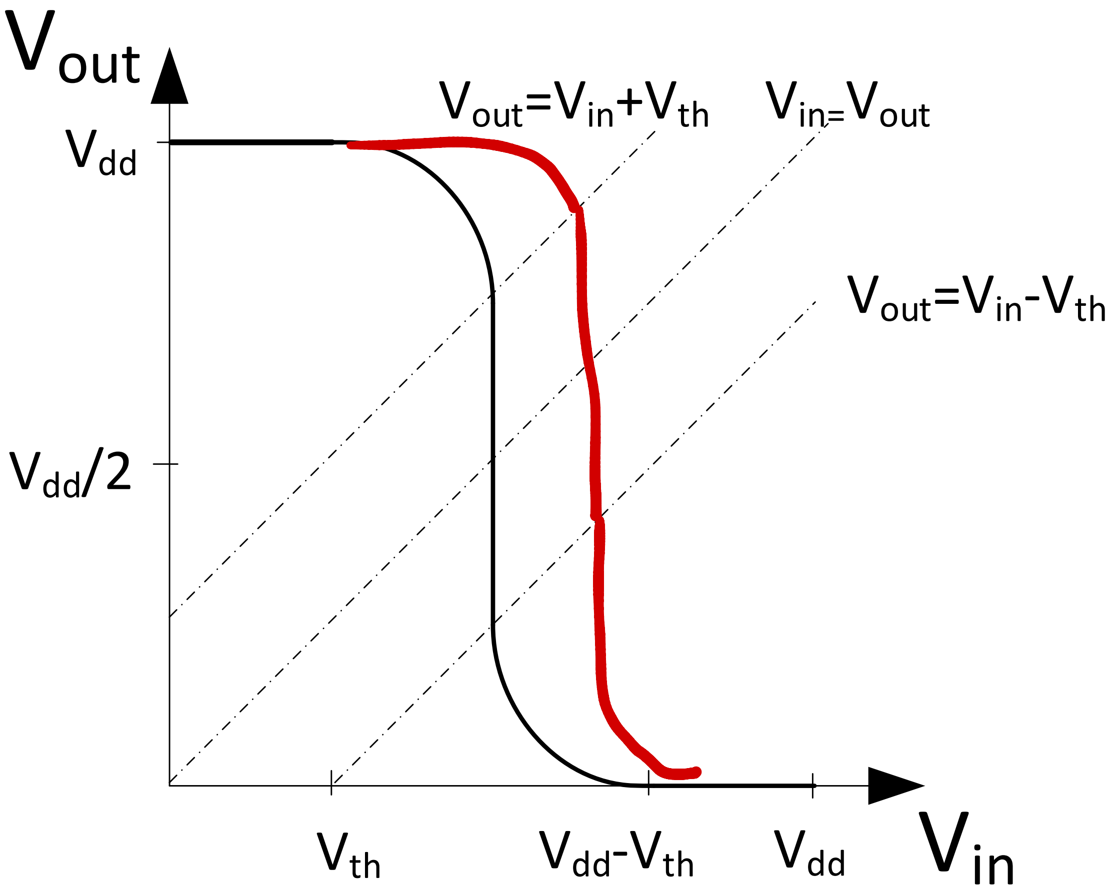
Loadline Analysis



Loadline Analysis



Breakout session



- If $I_{dsat,p}=2*I_{dsat,n}$, sketch the the DC transfer curve relative to the balanced case

$$\beta_p \frac{W_p}{L} = 2 \beta_n \frac{W_n}{L}$$

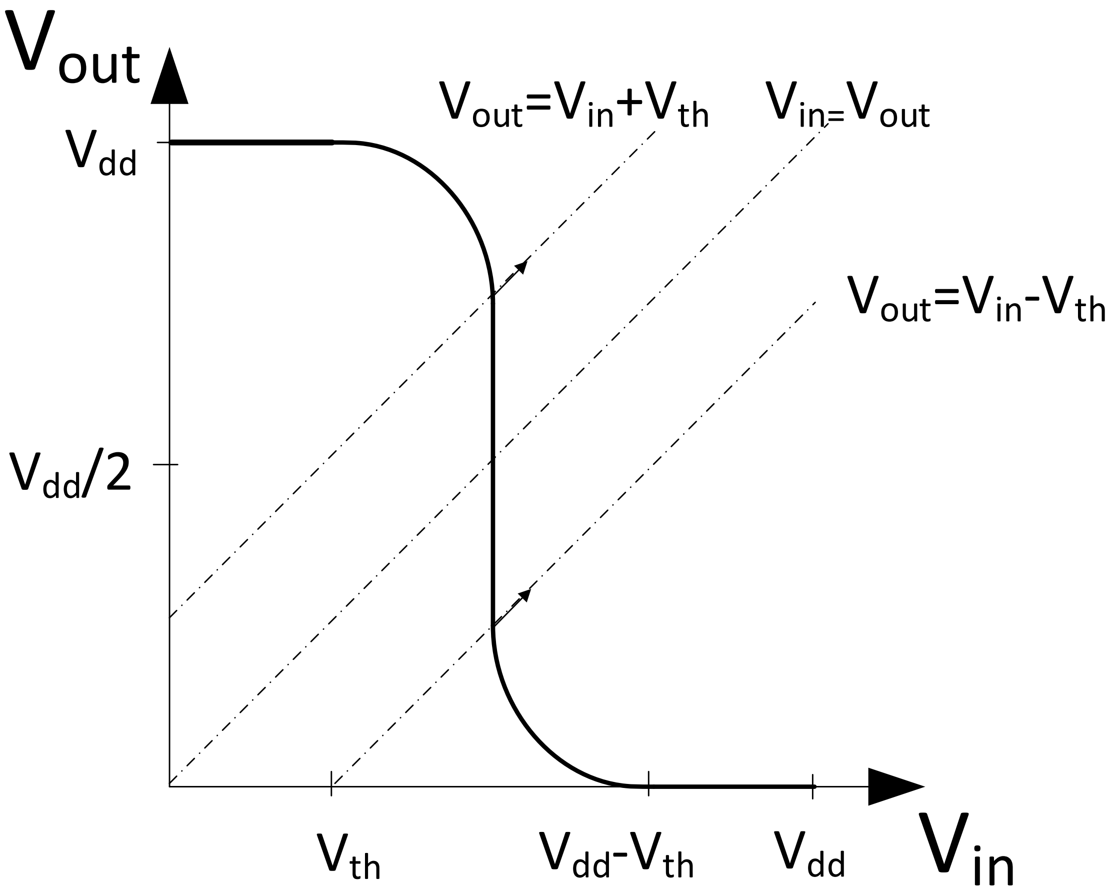
$$\frac{1}{2}\cancel{\beta_n \frac{W_n}{L}}(V_{in}-V_{tn})^2 = \frac{1}{2}\beta_p \frac{W_n}{L}(V_{dd}-V_{in}-V_{tn})^2$$

$$= \frac{1}{\cancel{2}} \cdot \cancel{2}\, \cancel{\beta_n} \cancel{\frac{W_n}{L}}(V_{dd}-V_{in}-V_{tn})^2$$

$$(V_{in}-V_{tn})^2 = 2\,(V_{dd}-V_{in}-V_{tn})^2$$

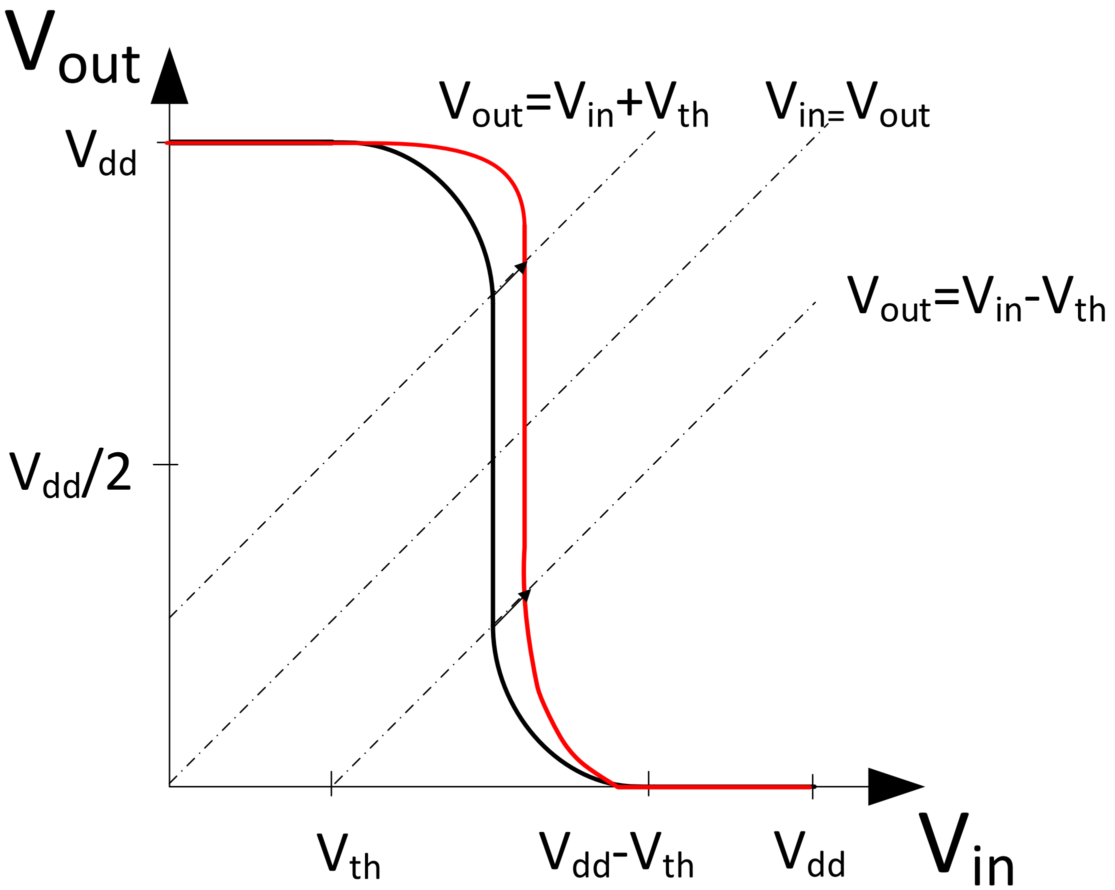
$$V_{in}-V_{tn} = \sqrt{2}\,V_{dd} - \sqrt{2}\,V_{in} - \sqrt{2}\,V_{tn}$$

Breakout session



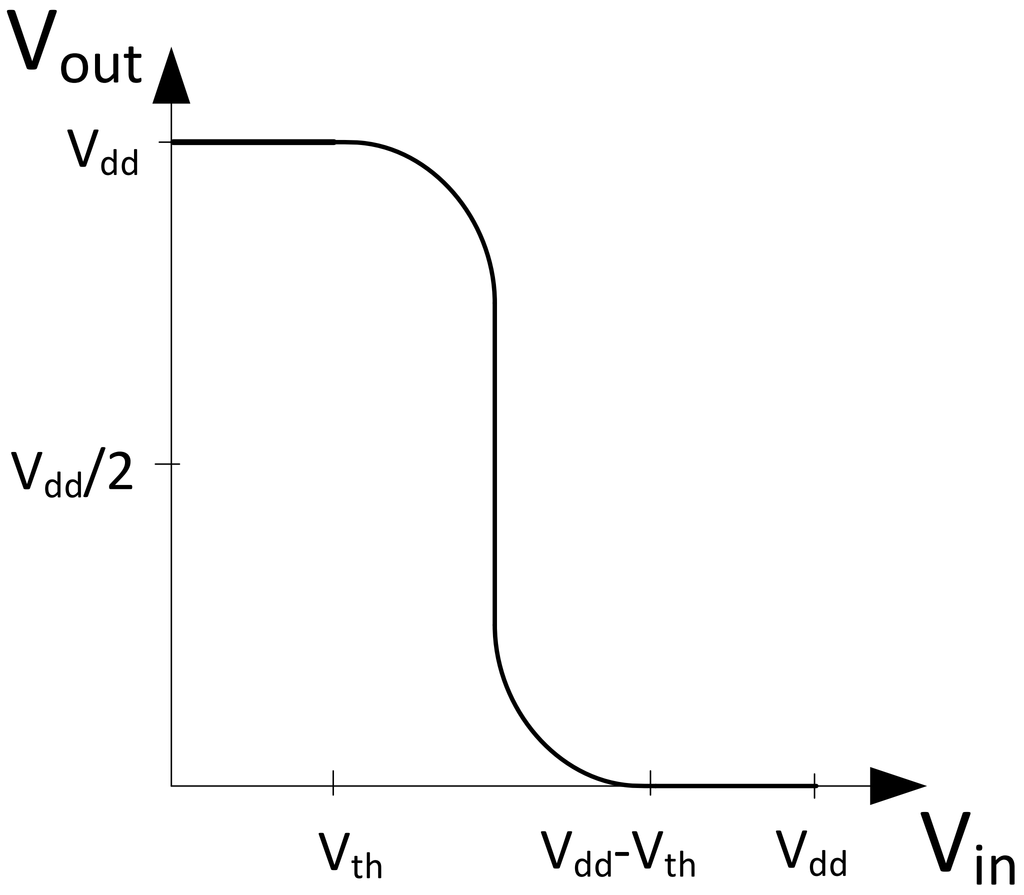
- If $I_{dsat,p}=2*I_{dsat,n}$, sketch the the DC transfer curve relative to the balanced case

Breakout session



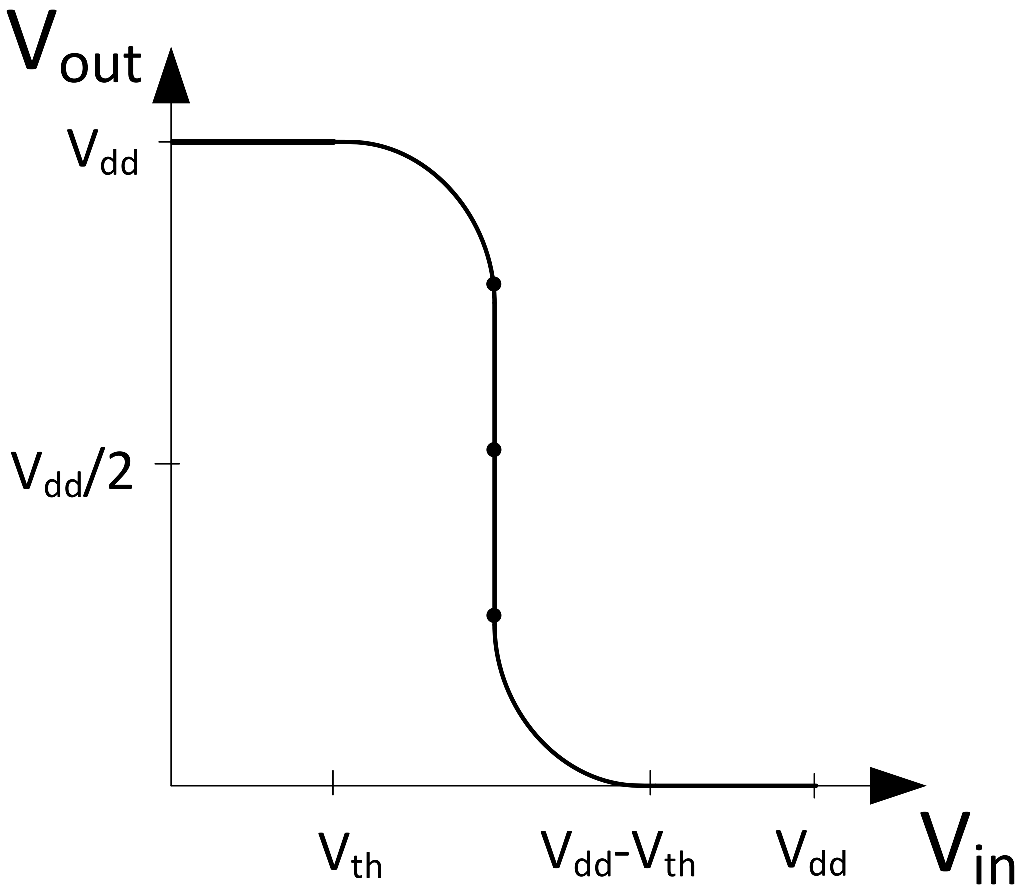
- If $I_{dsat,p}=2*I_{dsat,n}$, sketch the the DC transfer curve relative to the balanced case

Channel length modulation



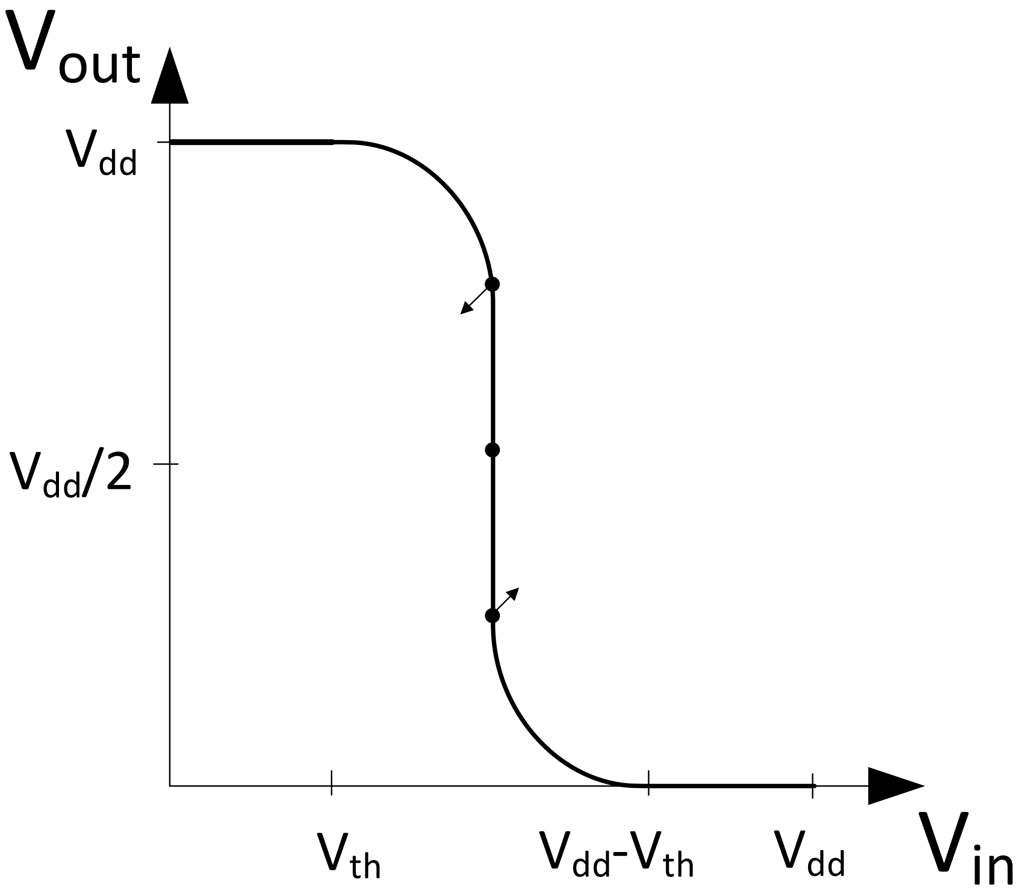
- Channel length modulation ➔ Less abrupt DC transfer curve in “transition region” region where both devices are in saturation 50

Channel length modulation



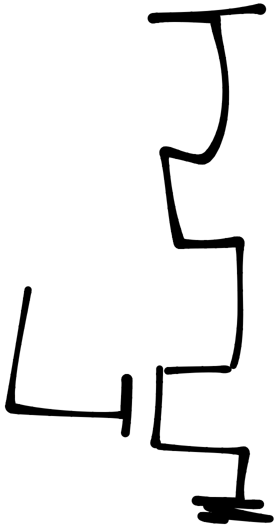
- Channel length modulation ➔ Less abrupt DC transfer curve in "transition region" region where both devices are in saturation

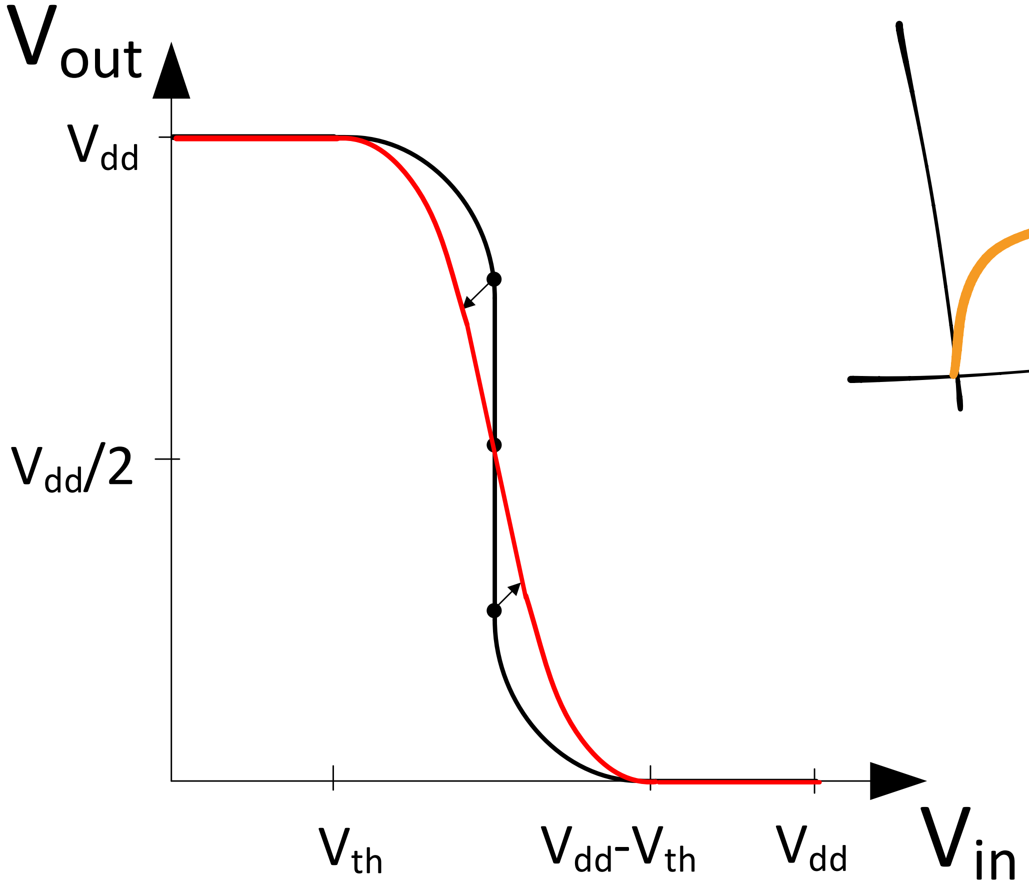
Channel length modulation

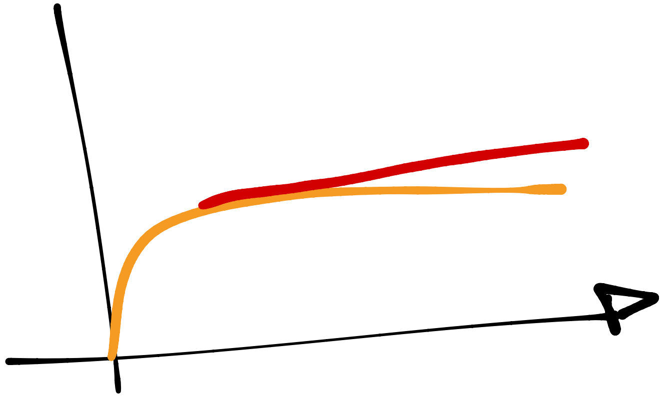


- Channel length modulation ➔ Less abrupt DC transfer curve in "transition region" region where both devices are in saturation

Channel length modulation

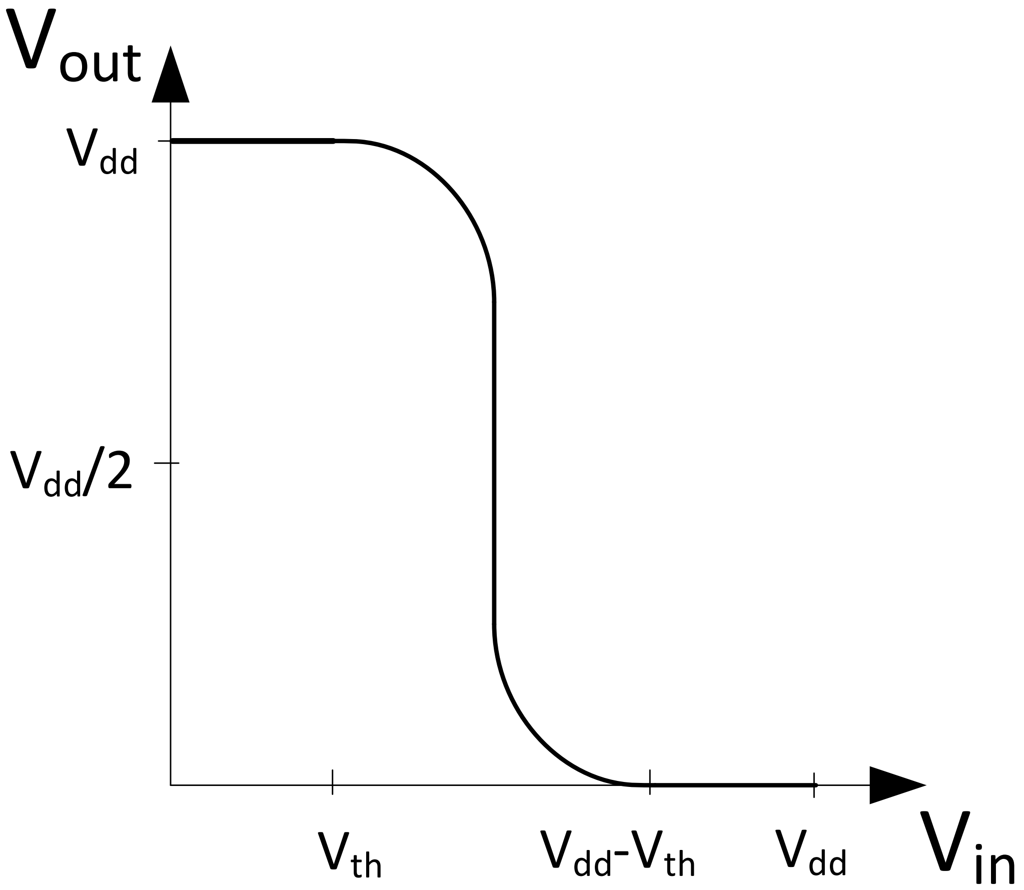






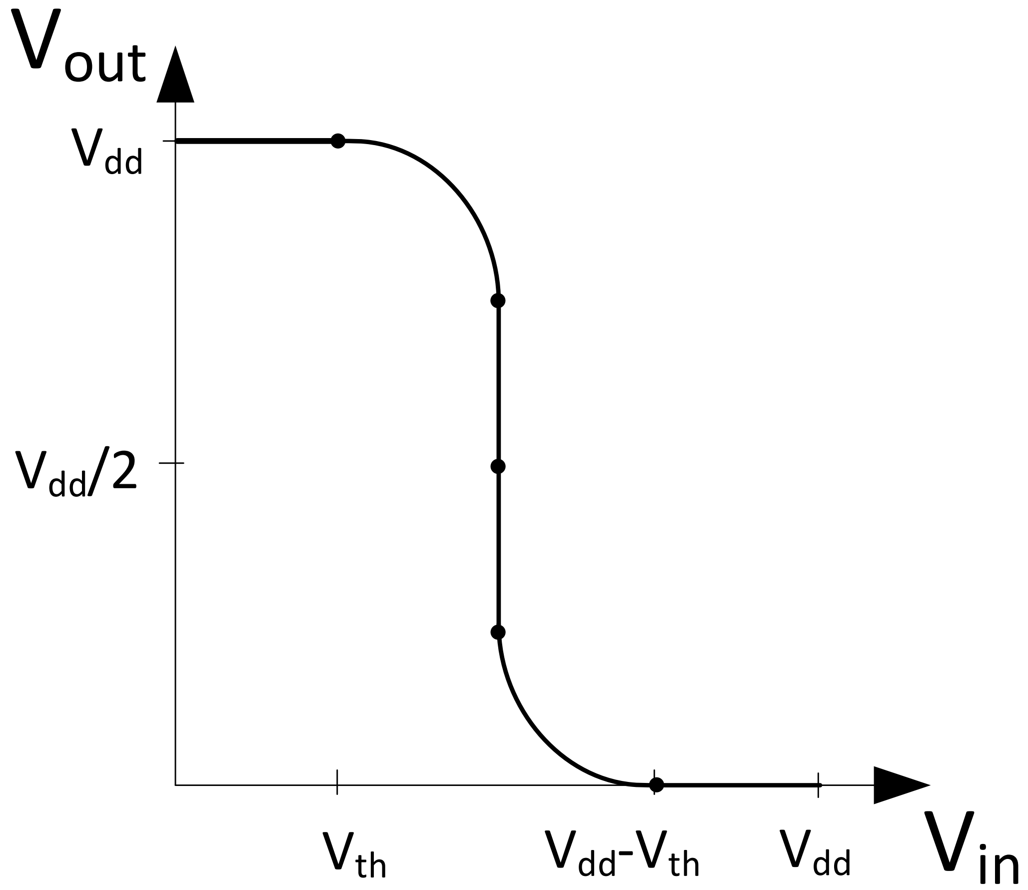
- Channel length modulation ➔ Less abrupt DC transfer curve in “transition region” region where both devices are in saturation

V_{th} Impact on DC Transfer Curve



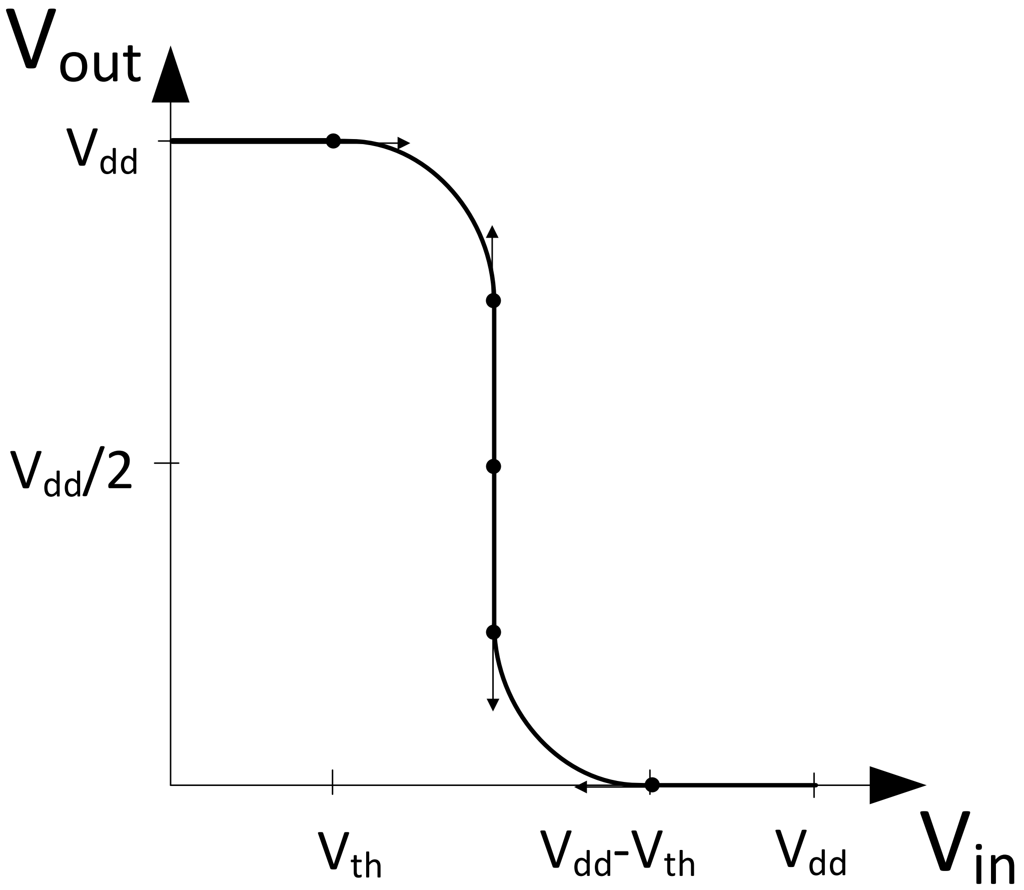
- V_{th}, determines vertical window size of transition region

V_{th} Impact on DC Transfer Curve



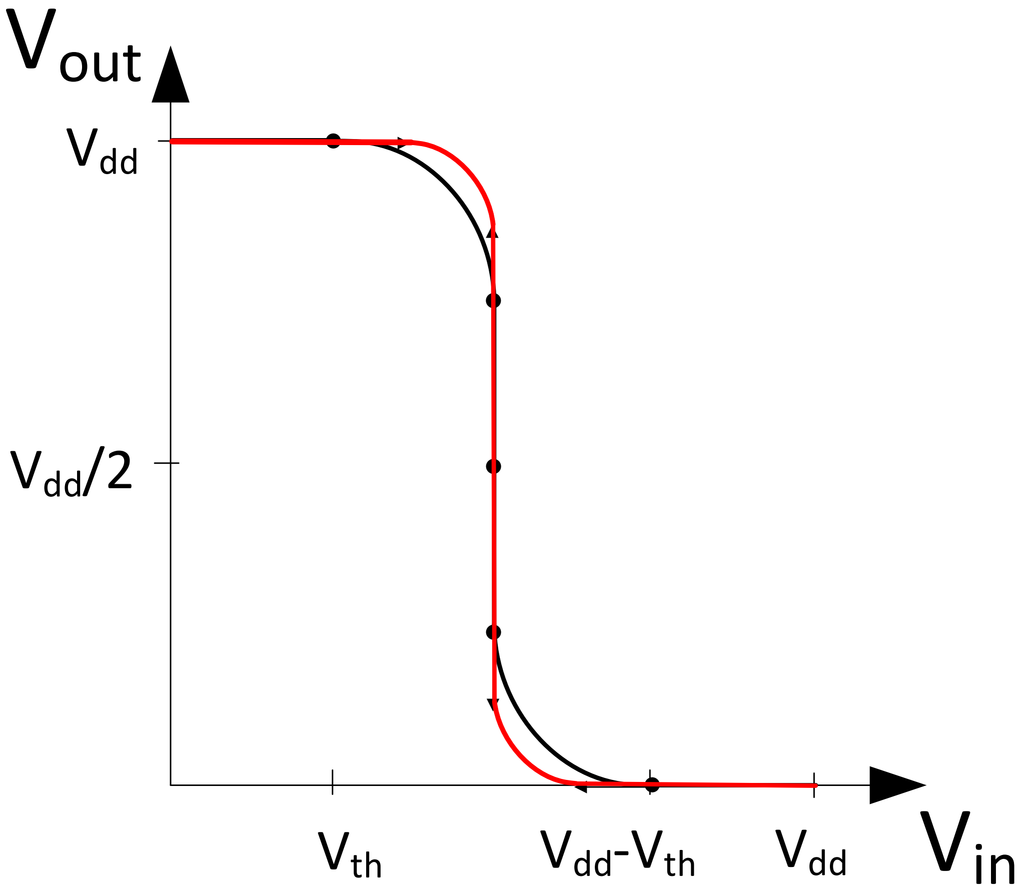
- V_{th}, determines vertical window size of transition region

V_{th} Impact on DC Transfer Curve



- V_{th}, determines vertical window size of transition region

V_{th} Impact on DC Transfer Curve

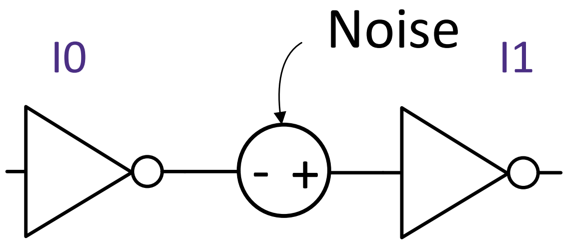


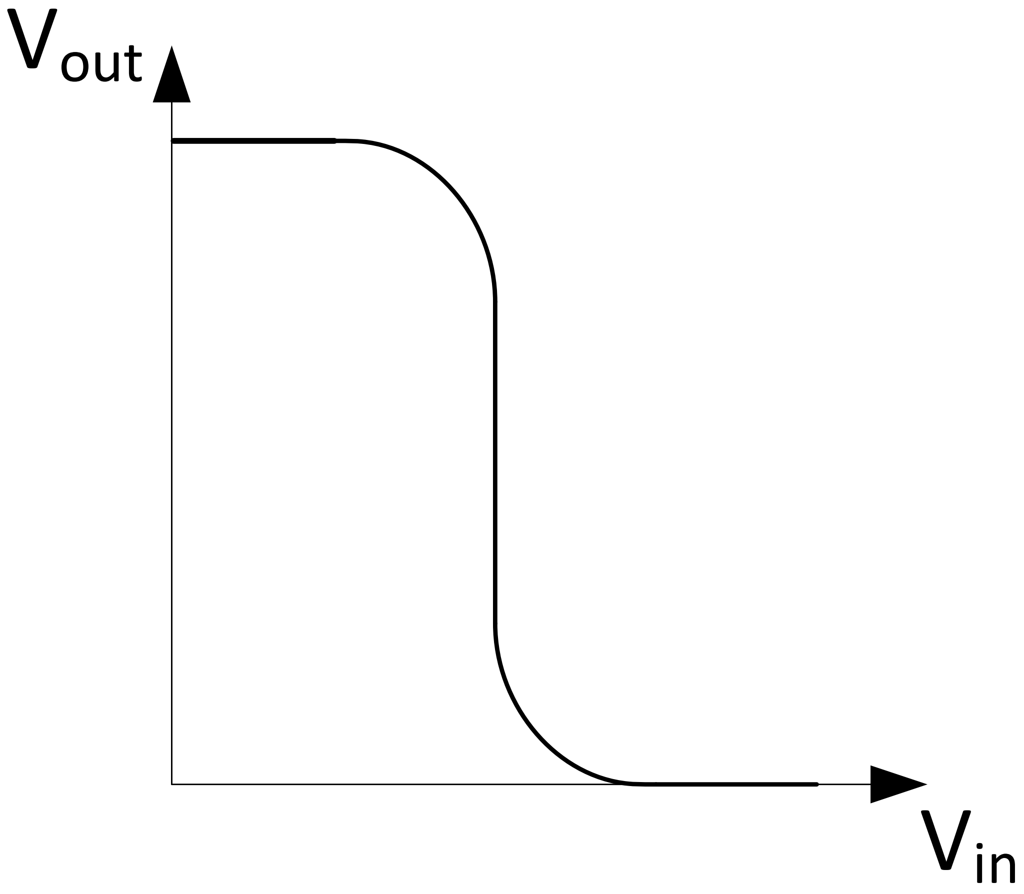
- V_{th}, determines vertical window size of transition region

V_{th} Impact on DC Transfer Curve

- What if $V_{th} = 0.6V_{dd}$?

Importance of DC Transfer Function

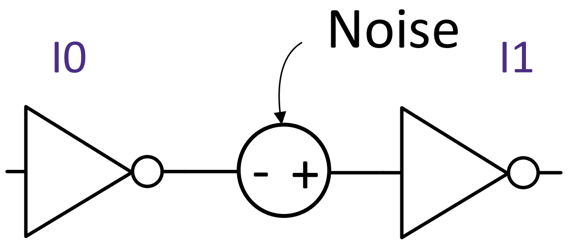


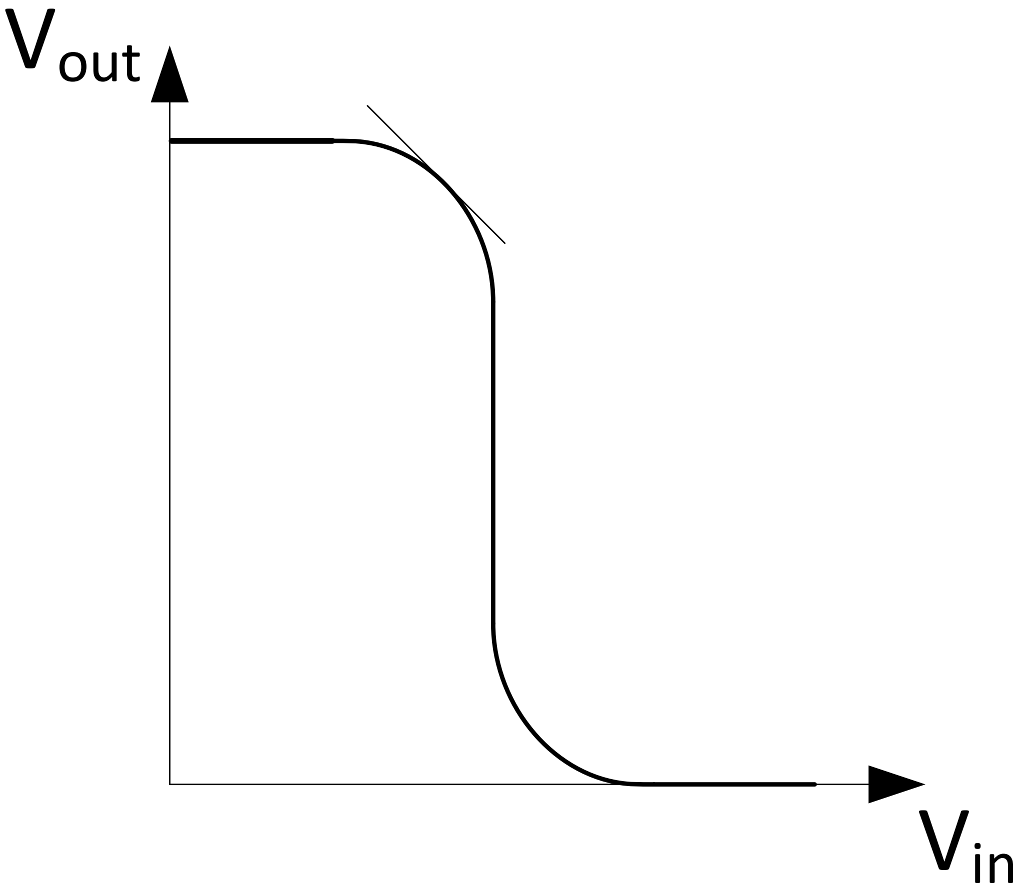


- Static Noise Margin (NM)

ELECTRICAL & COMPUTER ENGINEERING

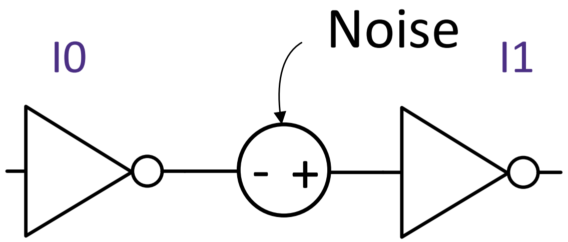
Importance of DC Transfer Function

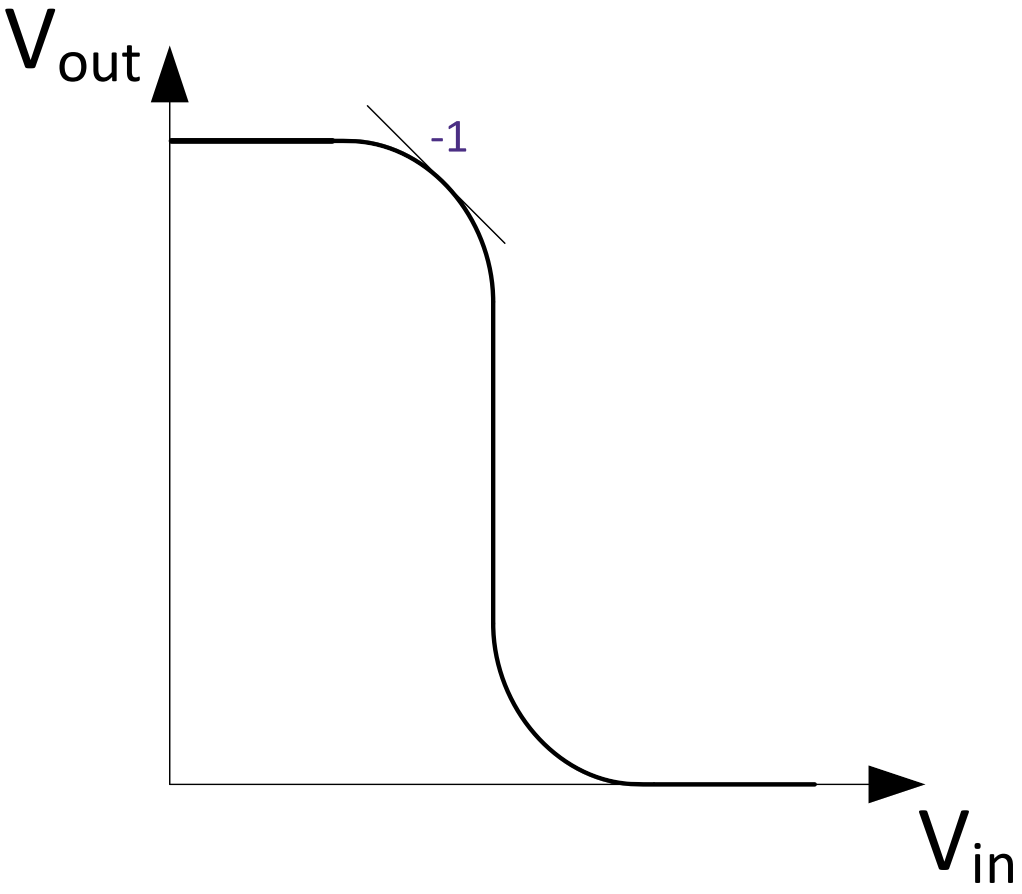




- Static Noise Margin (NM)

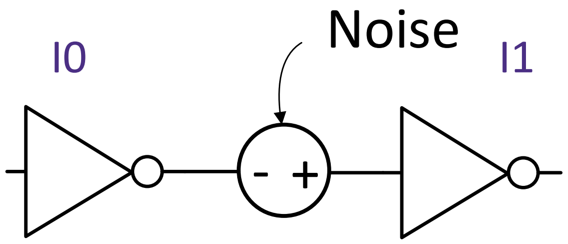
Importance of DC Transfer Function

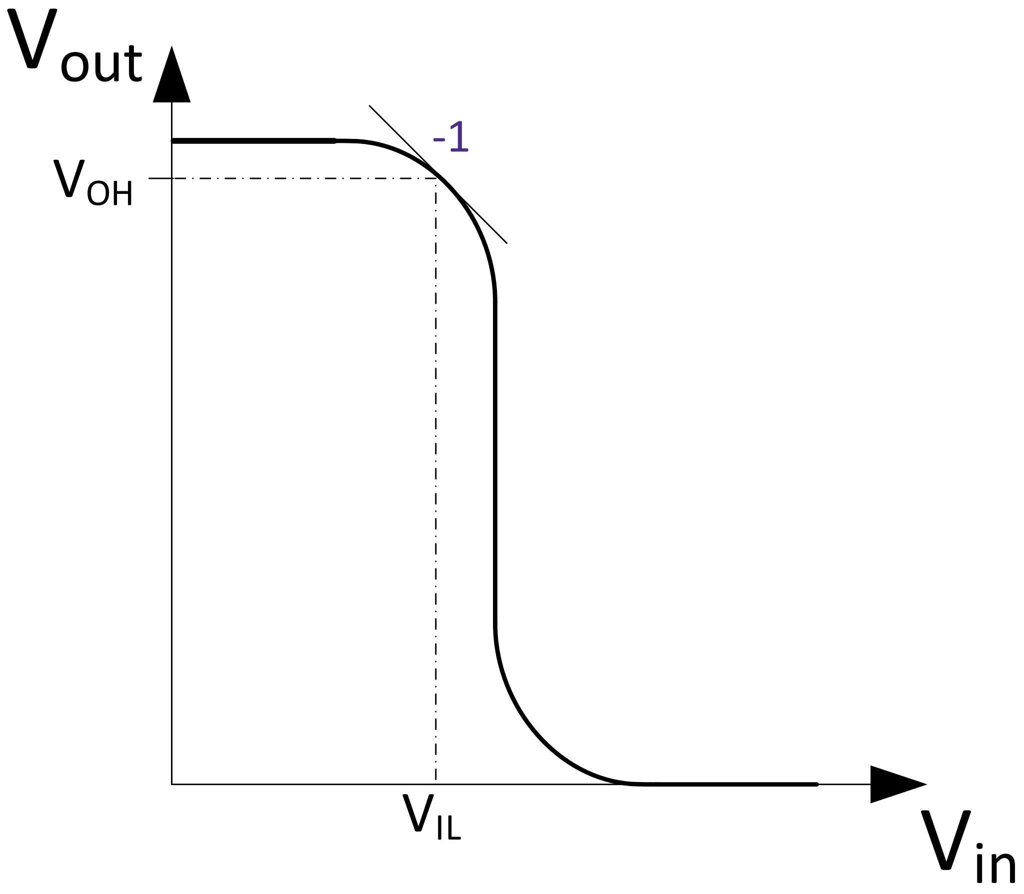




- Static Noise Margin (NM)

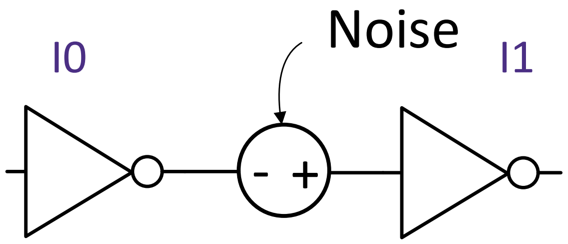
Importance of DC Transfer Function

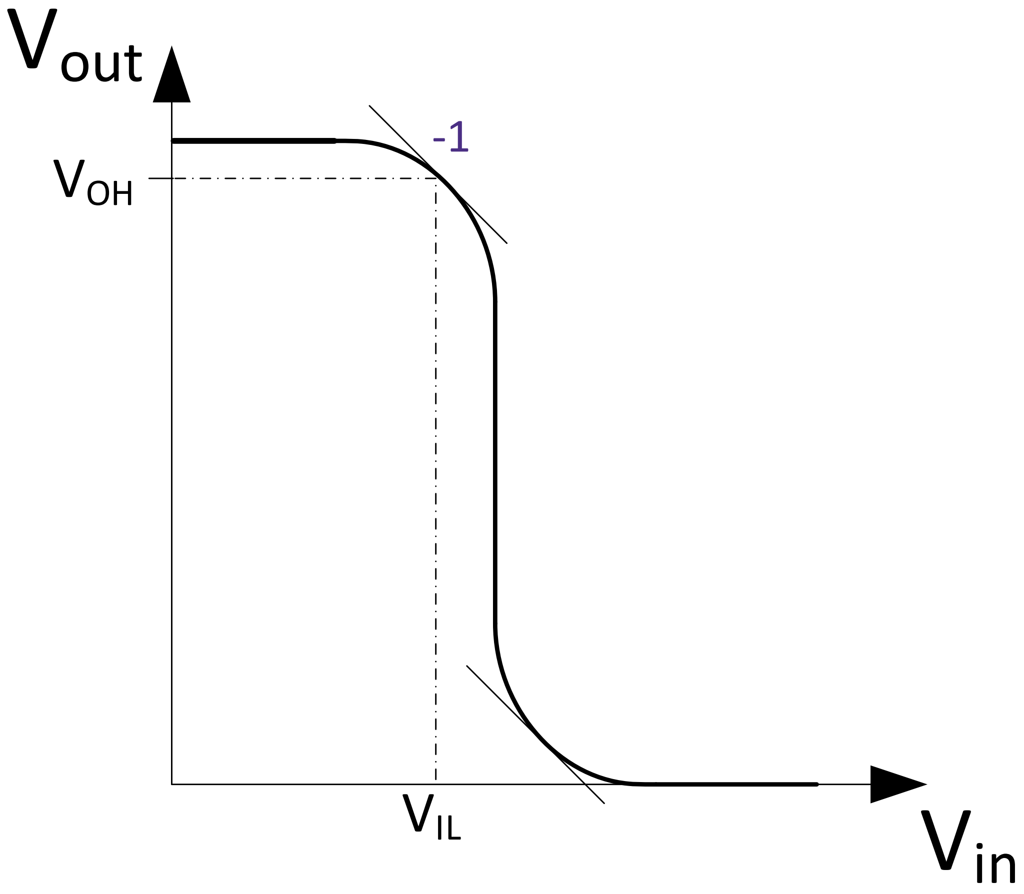




- Static Noise Margin (NM)

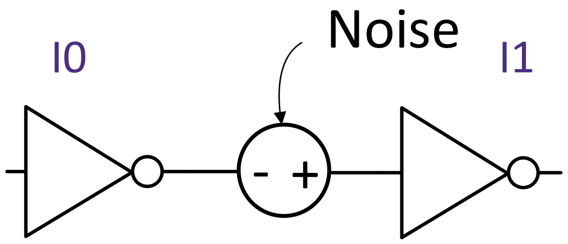
Importance of DC Transfer Function

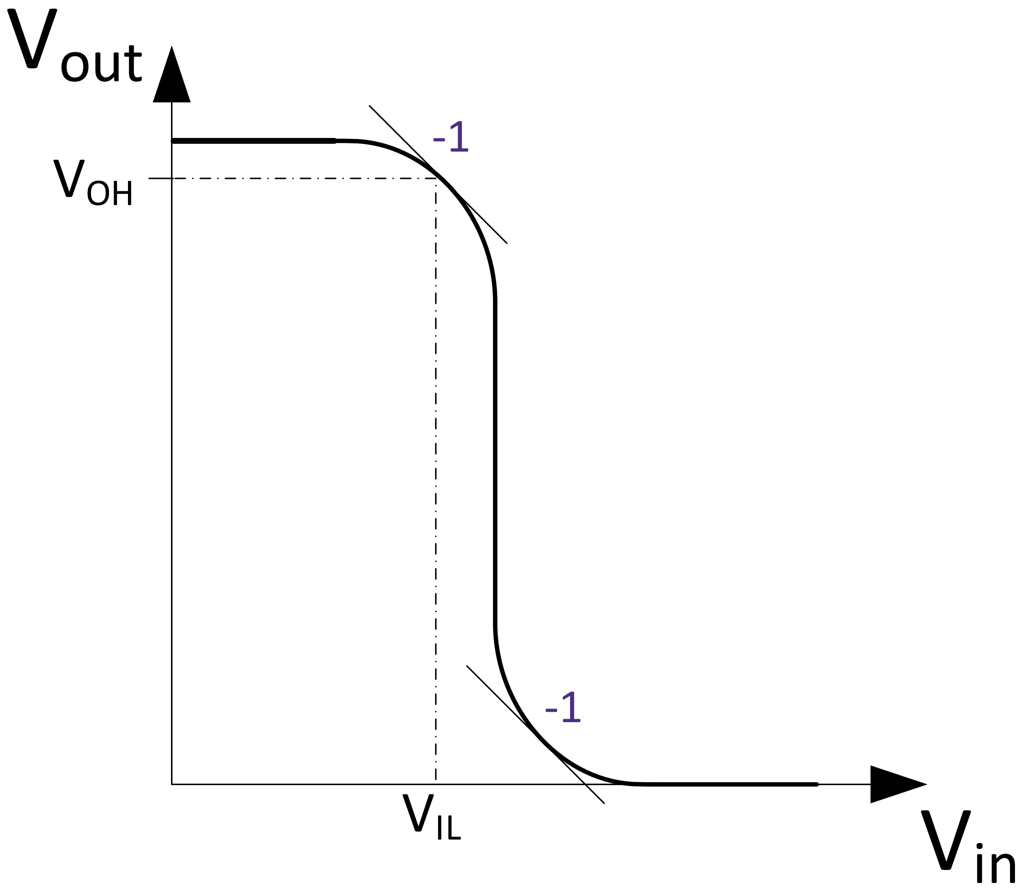




- Static Noise Margin (NM)

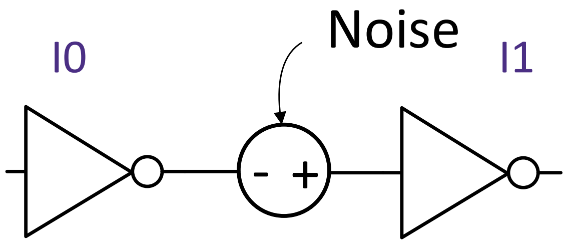
Importance of DC Transfer Function

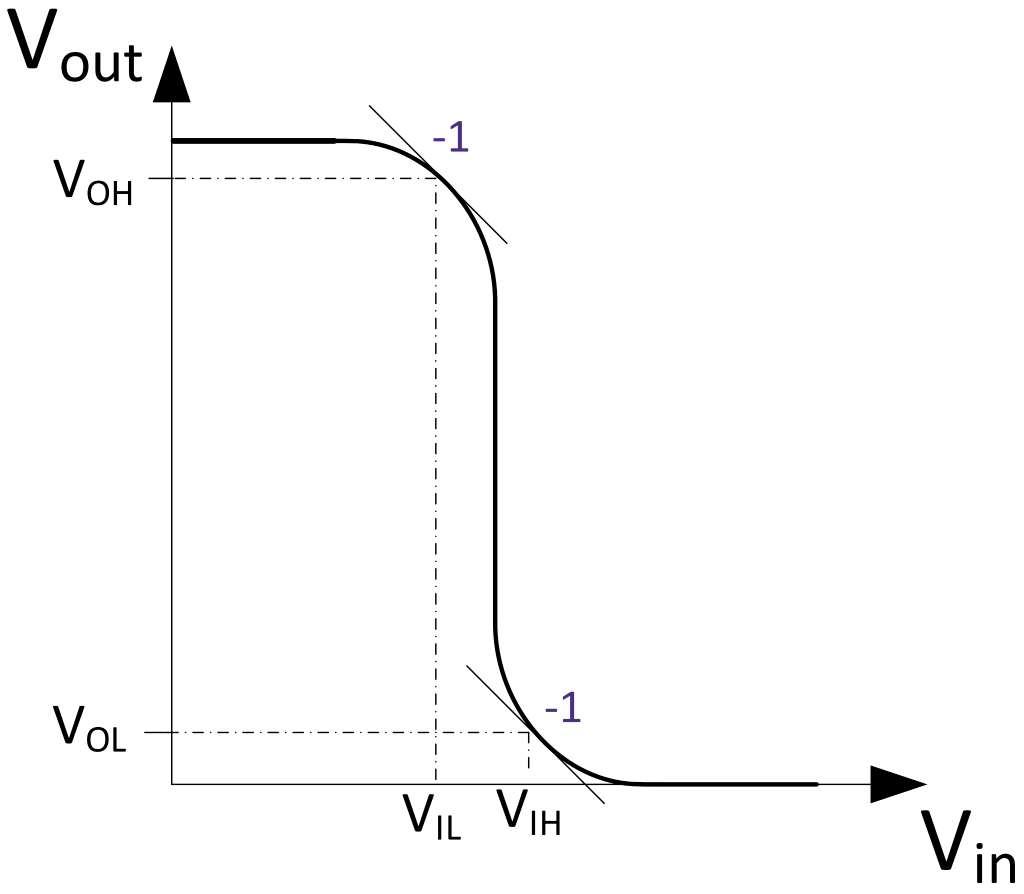




- Static Noise Margin (NM)

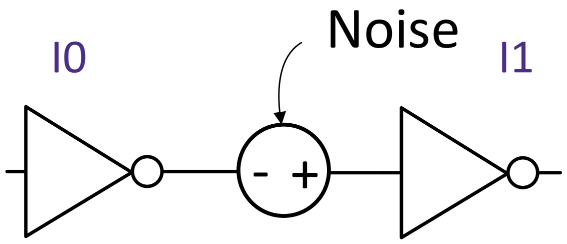
Importance of DC Transfer Function

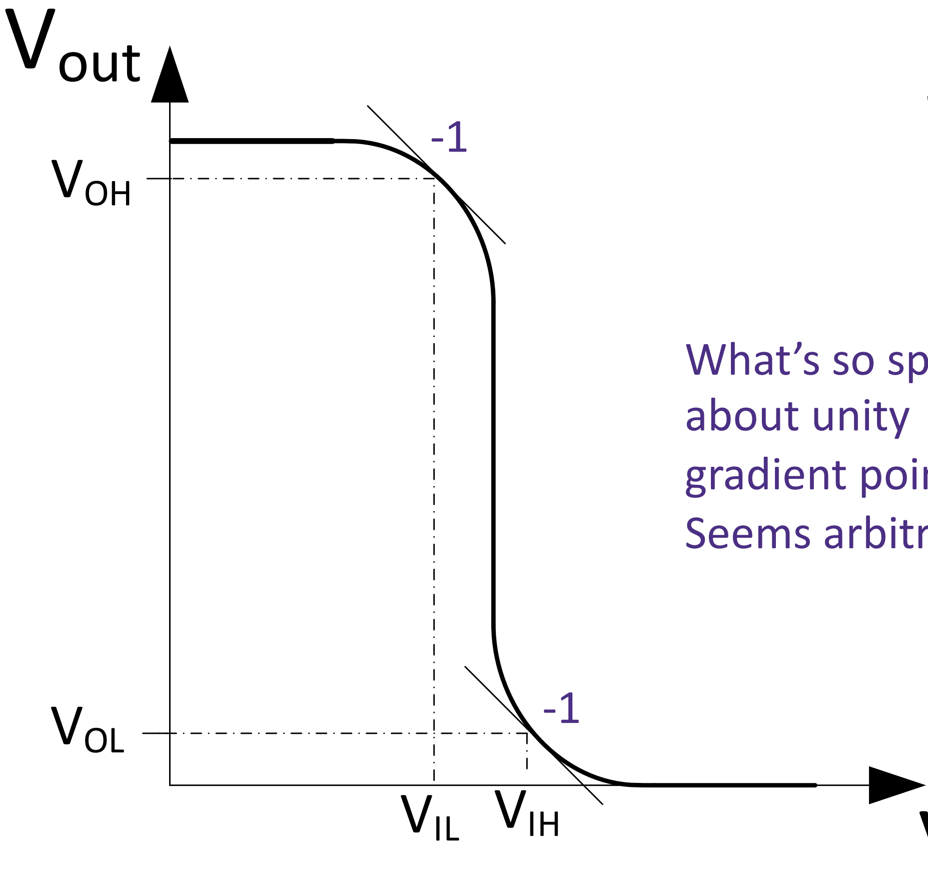




- Static Noise Margin (NM)

Importance of DC Transfer Function

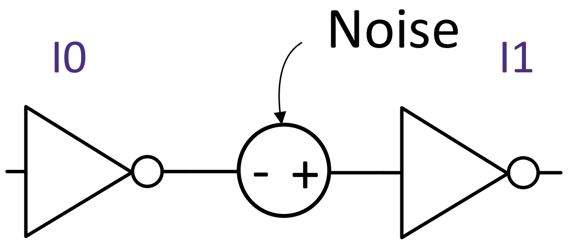


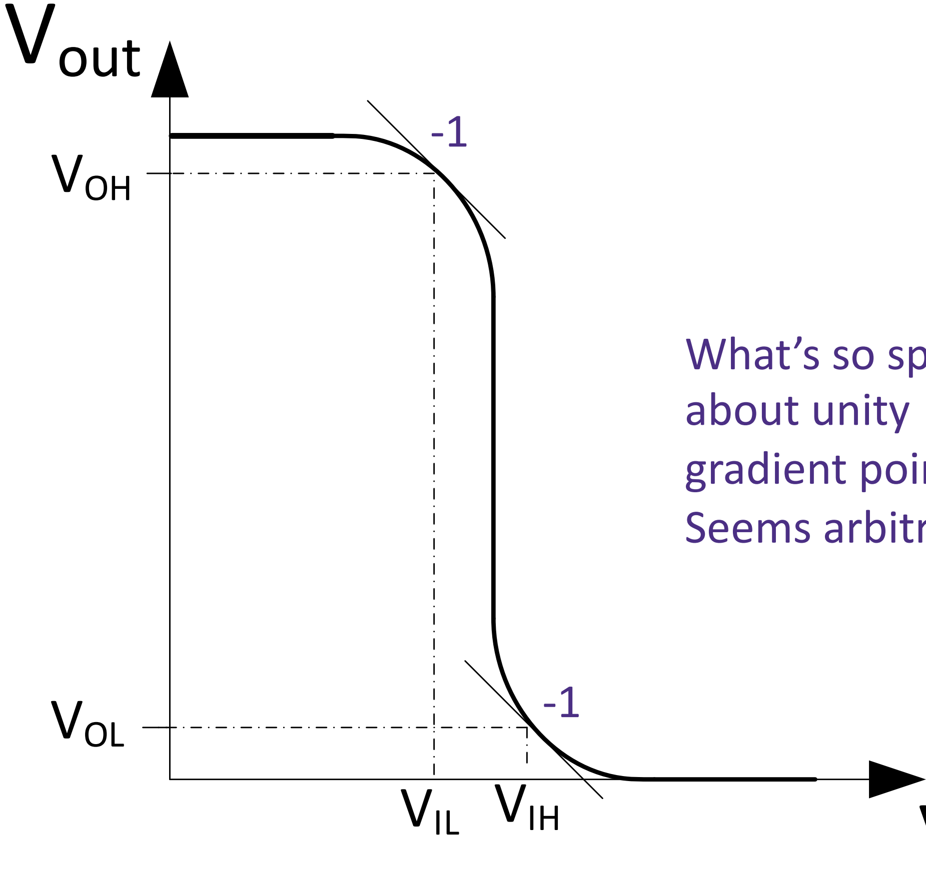


What's so special about unity gradient points?? Seems arbitrary…

- Static Noise Margin (NM)

Importance of DC Transfer Function

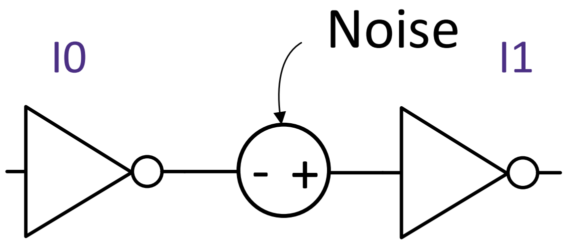


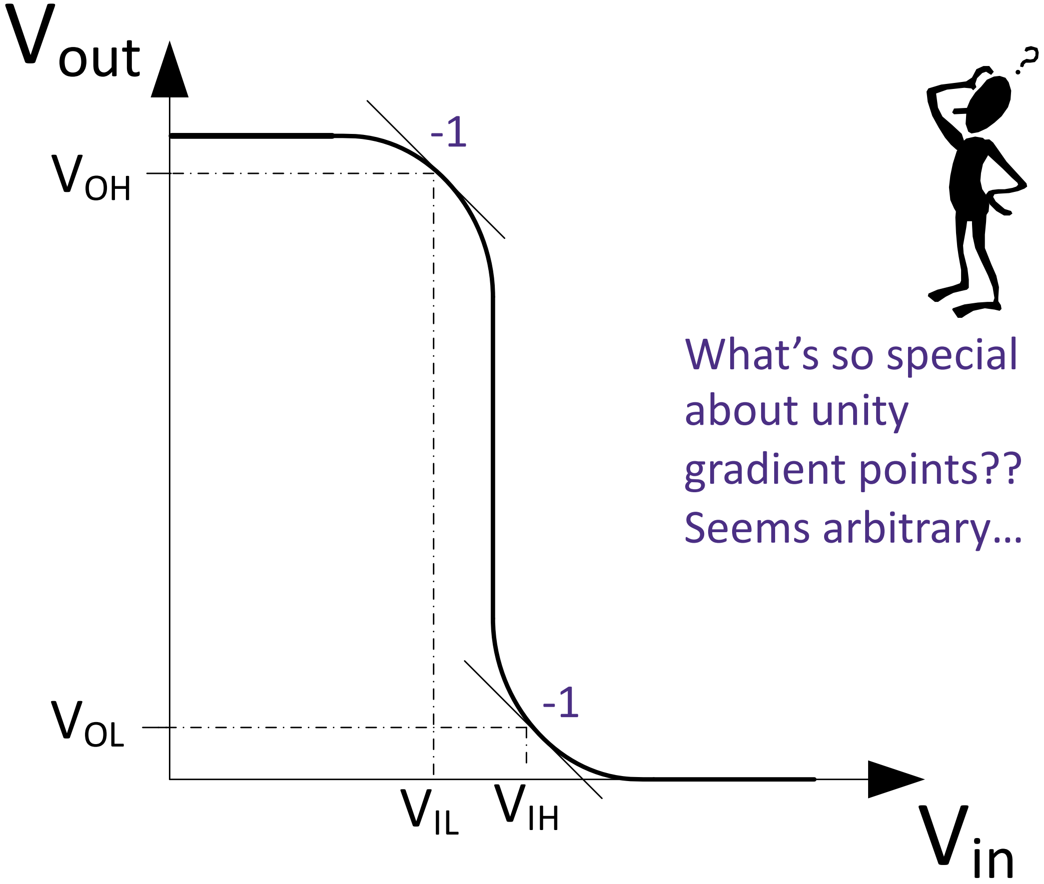


What’s so special about unity gradient points?? Seems arbitrary…

- Static Noise Margin (NM)
- $NM_0 = V_{il} - V_{ol}$
- $NM_1 = V_{oh} - V_{ih}$

Importance of DC Transfer Function

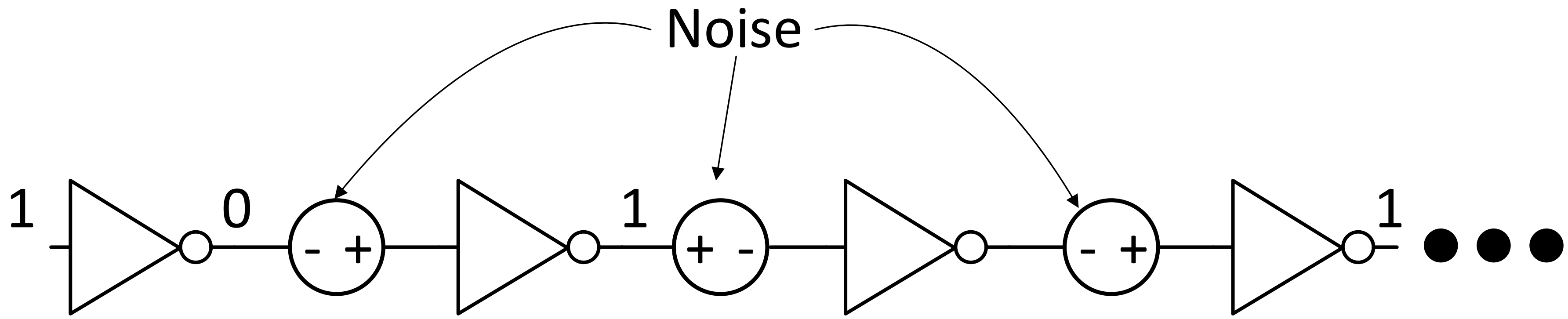




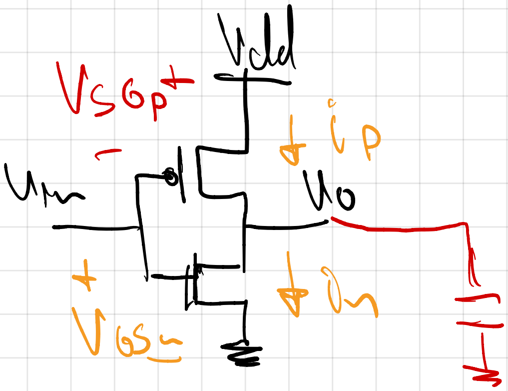
What’s so special about unity gradient points?? Seems arbitrary…

- Static Noise Margin (NM)
- $NM_0 = V_{il} – V_{ol}$
- $NM_1 = V_{oh} – V_{ih}$
- What is the best possible NM for an inverter? What would it take?

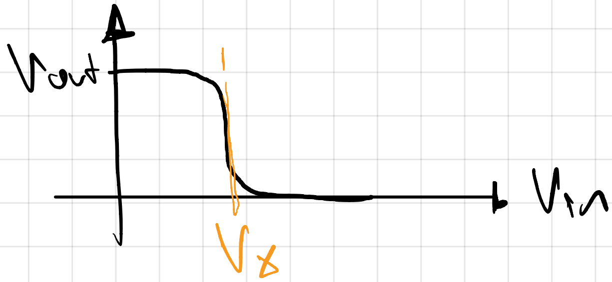
Some More Thoughts on Noise Margins



- Importance of unity-gain points (Cascade of inverters)
- What happens if noise voltage exceeds noise margin?
- Noise margin vs. V_{dd}



$i_p = i_n$



$$\beta_p \frac{W_p}{L}(V_{SG_p}-V_{th})^2 = \beta_n \frac{W_n}{L}(V_{GS_n}-V_{th})^2$$

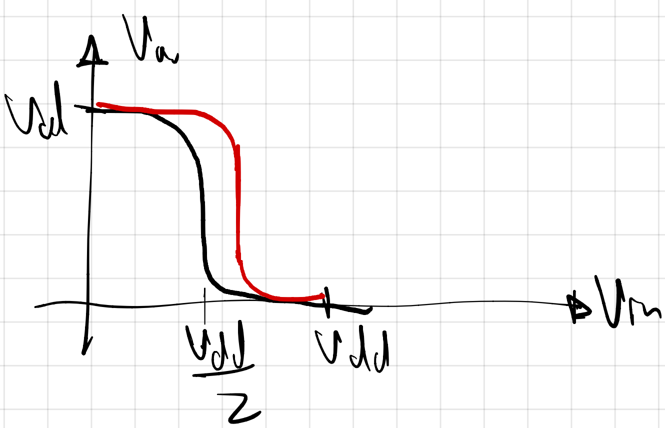
I_p $\quad \beta_p \frac{W_p}{L} > \beta_n \frac{W_n}{L}$

$$\Rightarrow V_{SG_p}-\cancel{V_{th}} < V_{GS_n}-\cancel{V_{th}}$$

$$V_{dd}-V_{in} < V_{in}$$

$$V_{dd} < 2V_{in}$$

$$\frac{V_{dd}}{2} < V_{in}$$



Logic values Voltage

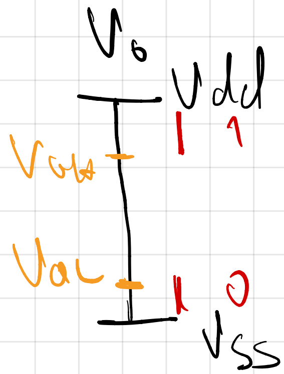
1 High V_{dd} 1V

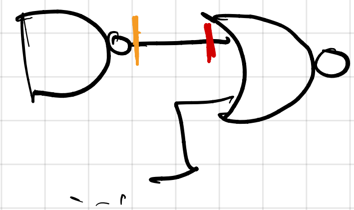
0.99V

0.7V

0 Low V_{ss} 0V

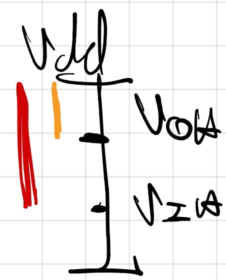
0.5V ?



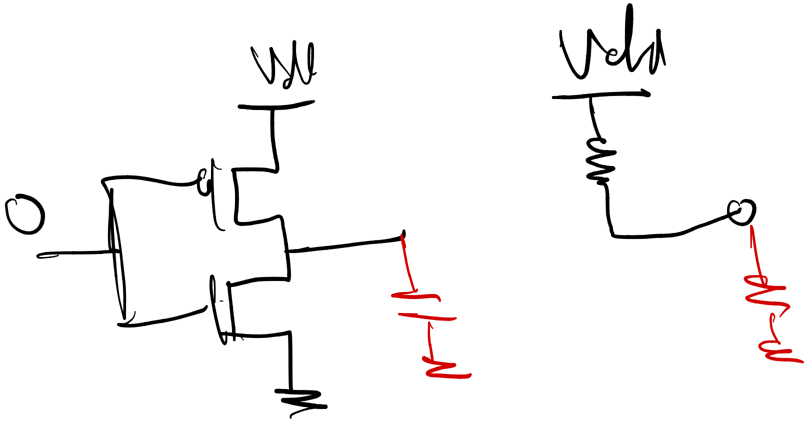


out1 V_{OH} + noise > V_{IH}

$NM_H = V_{OH} - V_{IH}$

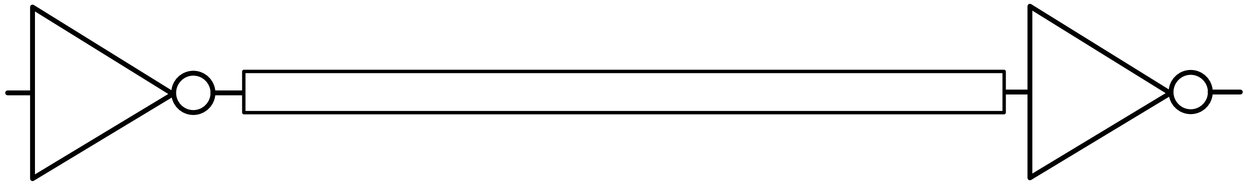


Holding Resistance



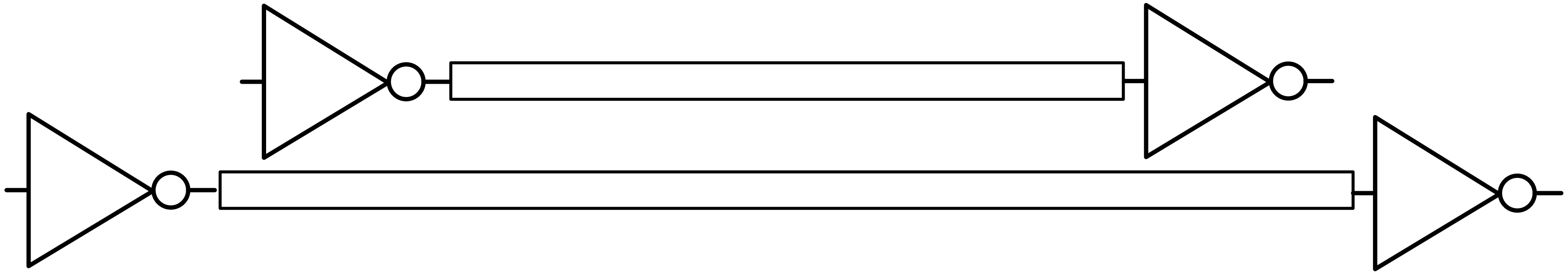
- Static inverter analysis also important for holding resistance analysis

Holding Resistance



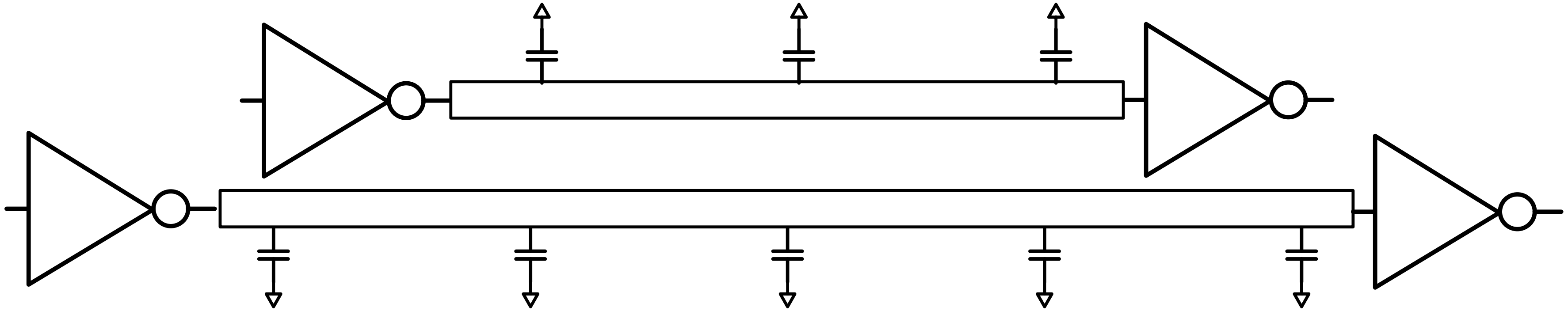
- Static inverter analysis also important for holding resistance analysis

Holding Resistance



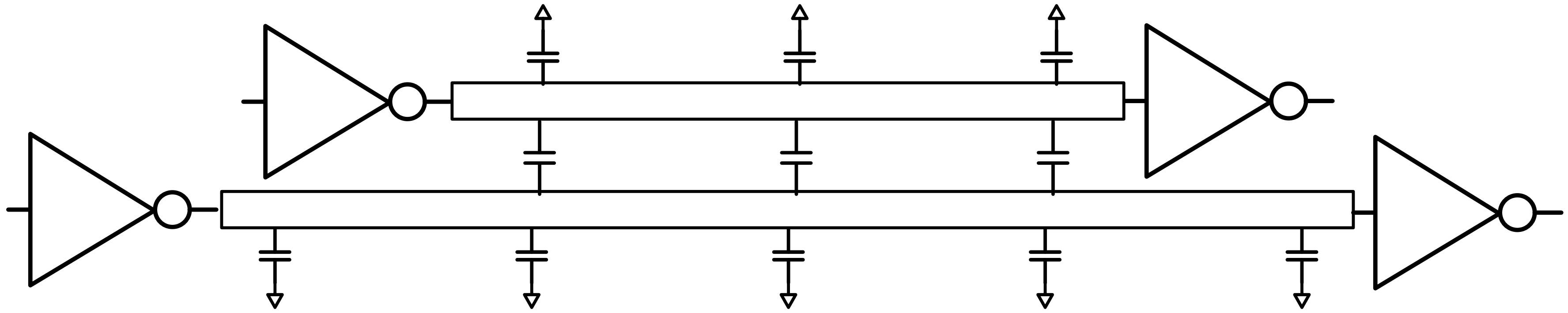
- Static inverter analysis also important for holding resistance analysis

Holding Resistance



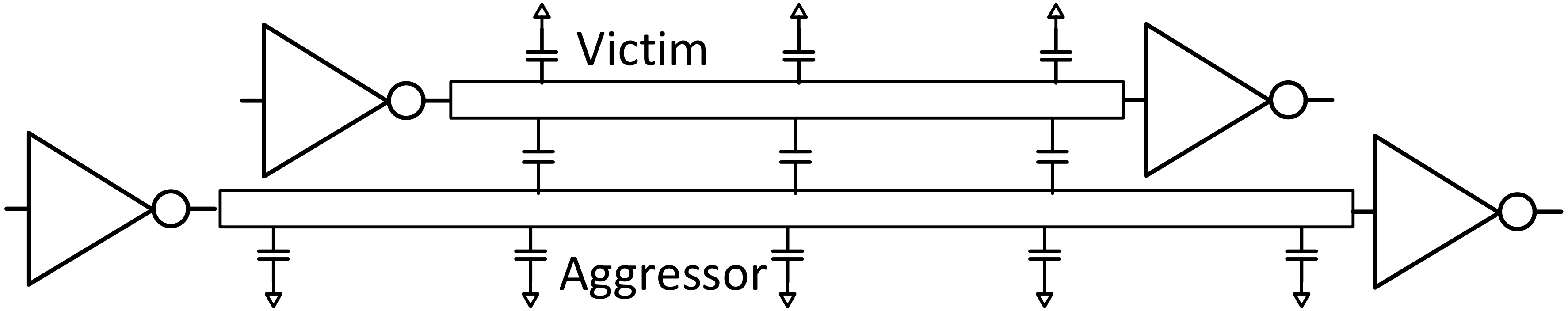
- Static inverter analysis also important for holding resistance analysis

Holding Resistance



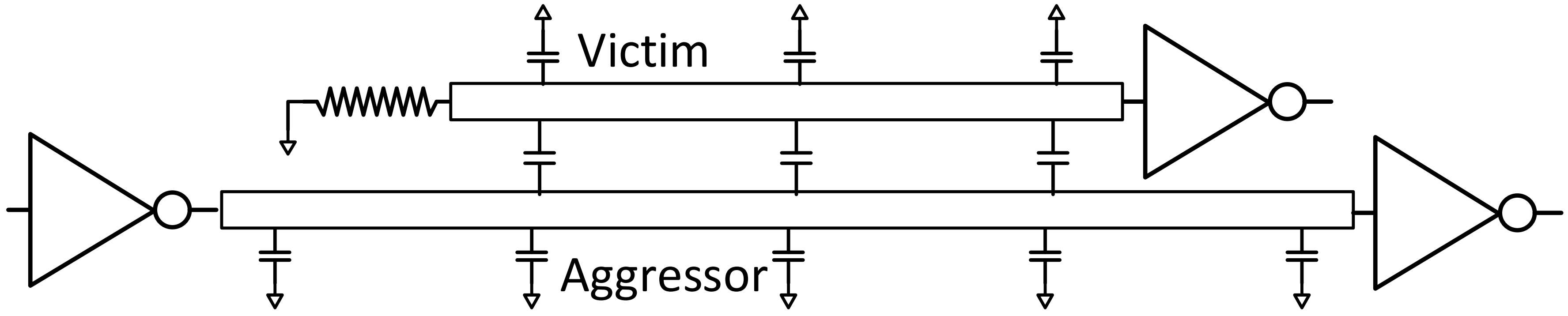
- Static inverter analysis also important for holding resistance analysis

Holding Resistance



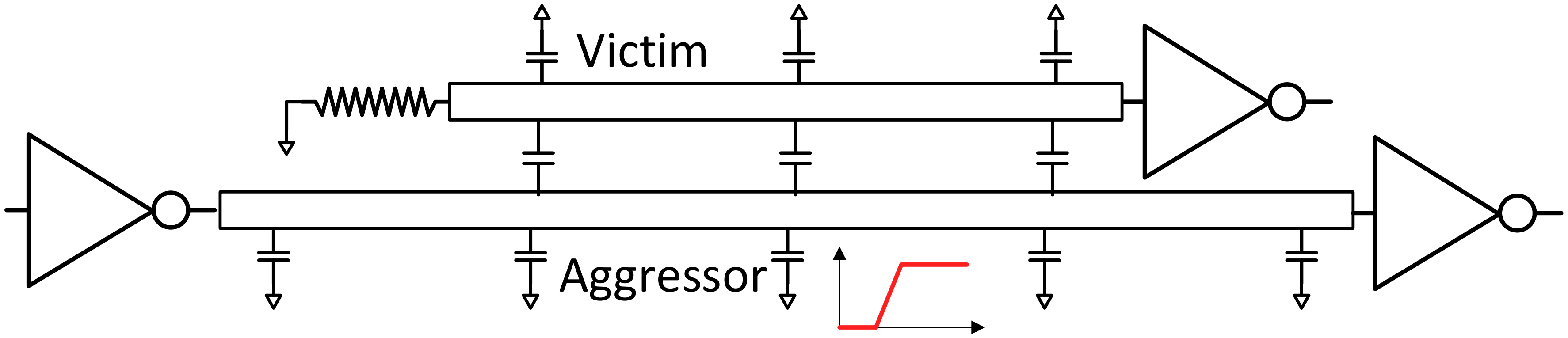
- Static inverter analysis also important for holding resistance analysis

Holding Resistance



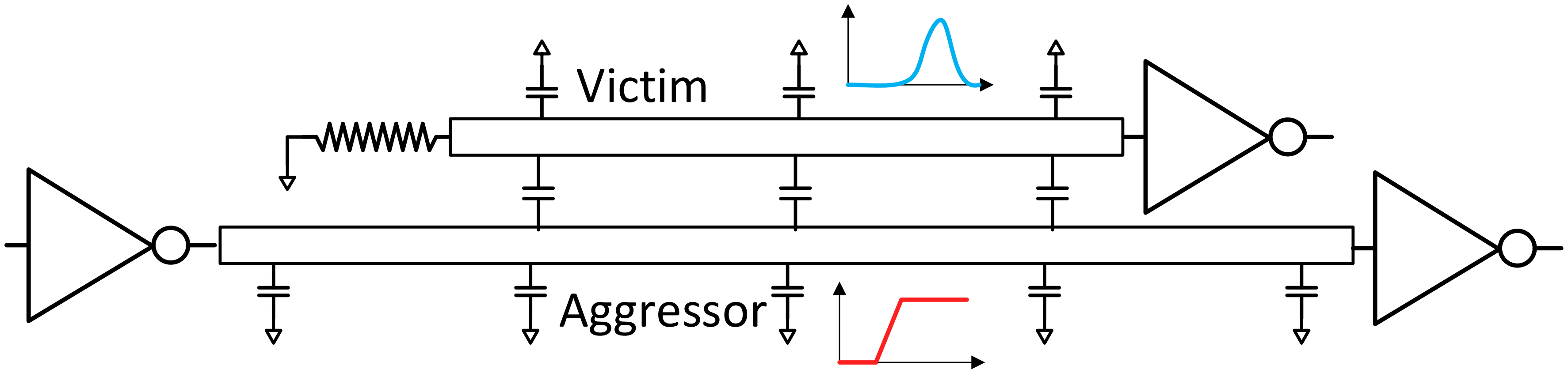
- Static inverter analysis also important for holding resistance analysis

Holding Resistance



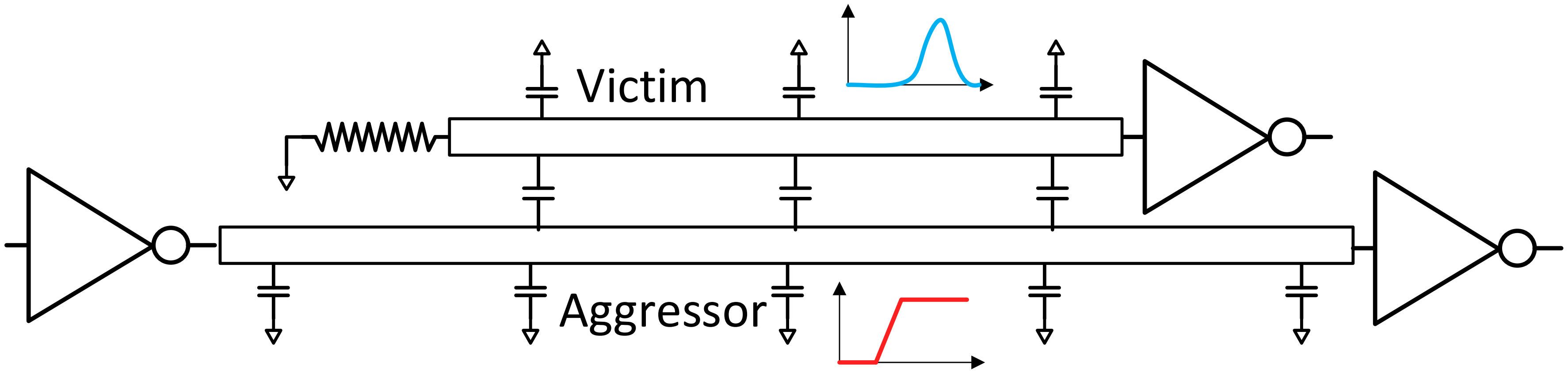
- Static inverter analysis also important for holding resistance analysis

Holding Resistance



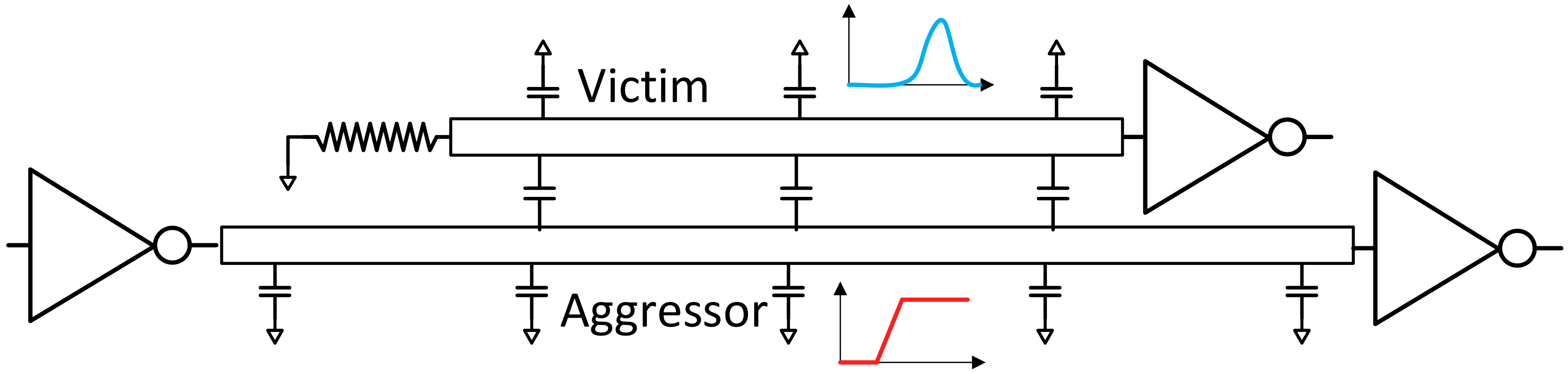
- Static inverter analysis also important for holding resistance analysis

Holding Resistance



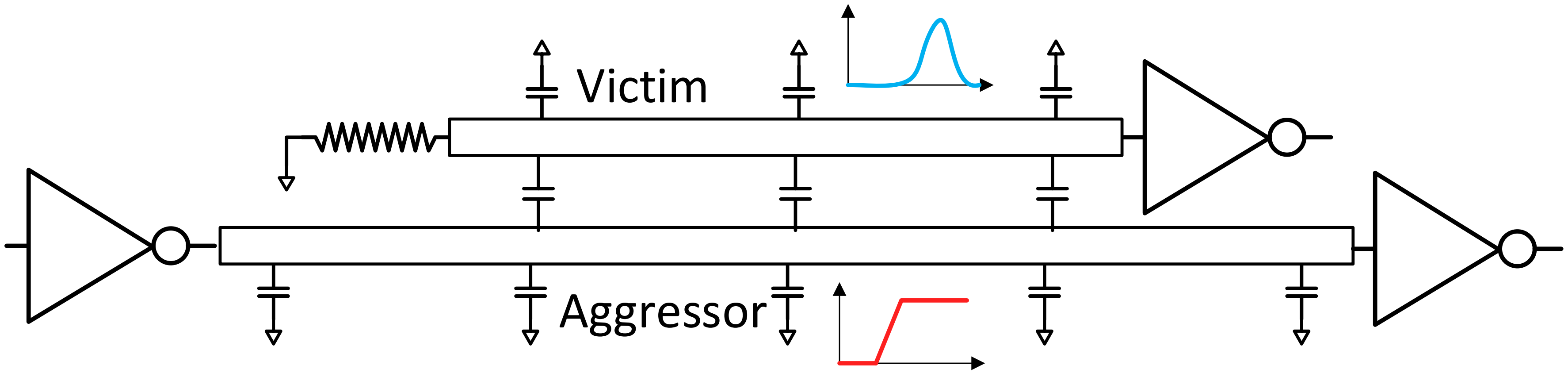
- Static inverter analysis also important for holding resistance analysis
  - Crosstalk analysis

Holding Resistance



- Static inverter analysis also important for holding resistance analysis
  - Crosstalk analysis
  - Holding resistance impacts peak noise glitch

Holding Resistance



Why does the glitch matter?
What are the key glitch parameters
What are the relevant glitch-determining parameters

- Static inverter analysis also important for holding resistance analysis
  - Crosstalk analysis
  - Holding resistance impacts peak noise glitch

$\frac{W}{L}$

Question

- What happens if a 1V inverter sees a 2V step (common ground)
- What happens if a 2V inverter sees a 1V step (0V->1V)

Reading assignment