EE 476
Layout Class Convention

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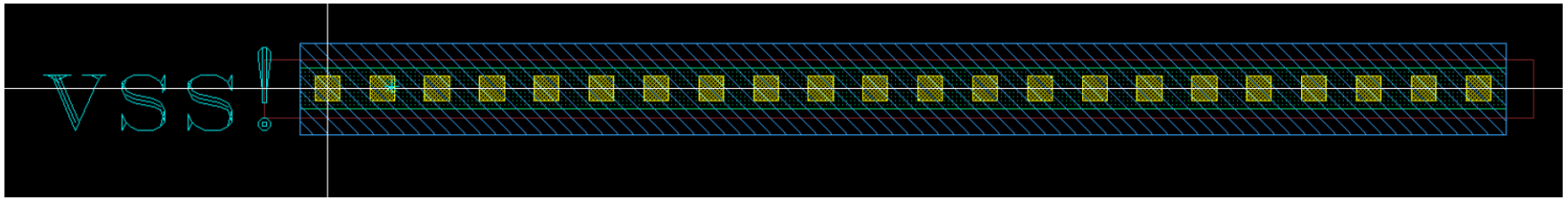
Purpose

- Details layout rules (class conventions) not included in DRC/LVS as well as metrics used to determine layout quality
- Parts to this presentation:
  - Class Layout Rules: power rails, metal grid, PR boundary
    - design quality metrics: area, metal usage, delay, energy/power
  - Bad layout examples
  - Wrap-Up

Class Layout Conventions

Power Rails

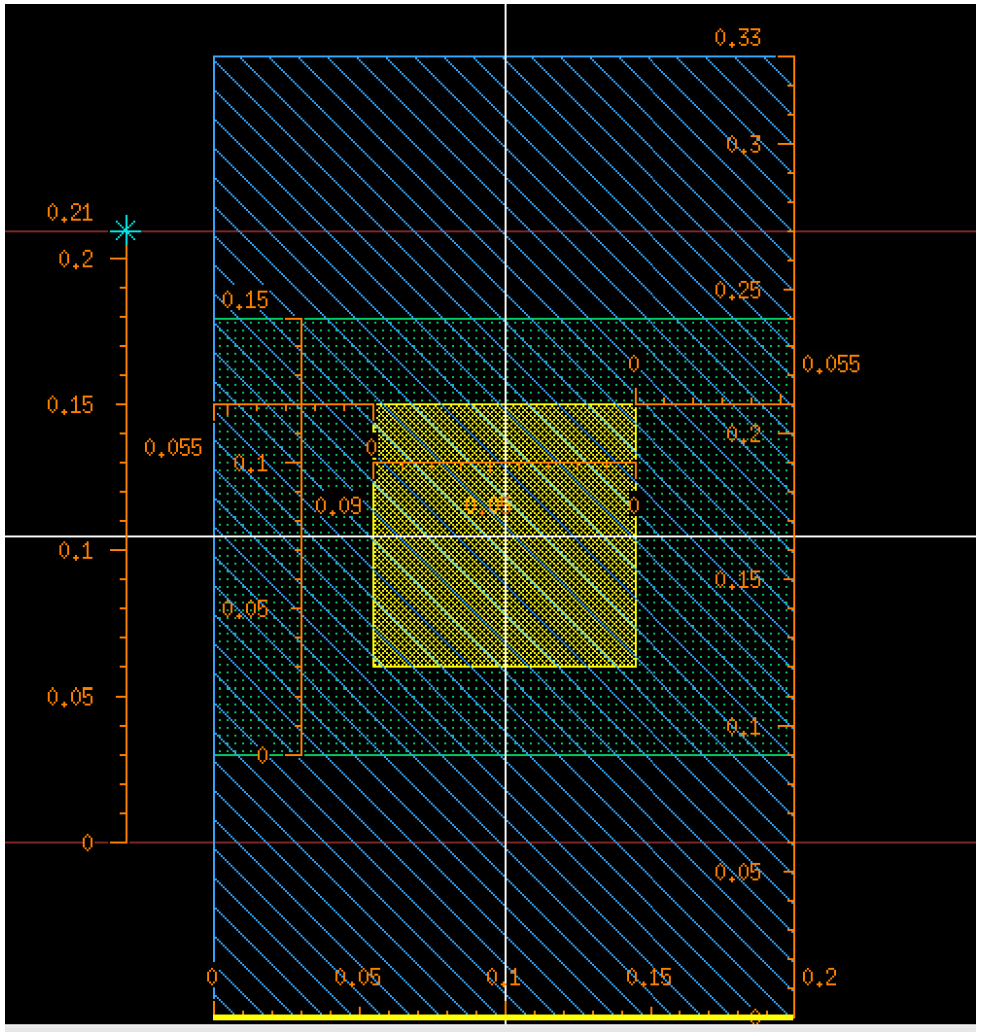
- Power rails run horizontally across your whole design – no breaks allowed
- Power rails consist of the following layers: OD, CO, PP or NP, M1, (and M2 later)
  - Example power rail below



- When stacking cells, the power rails of the top and bottom cell should overlap exactly. Example later.

Power Rails – determining the length

- The power rail of your design should be sized so that multiple power rails can be butted next to each other without any inconsistency in the power rail. In practice, this means your power rail will have a length that is a multiple of 0.2um
- Figure shows the minimum length power rail for your design. Rails for all your designs should look like many of these minimum rails placed adjacent to each other in 1 long continuous rail.

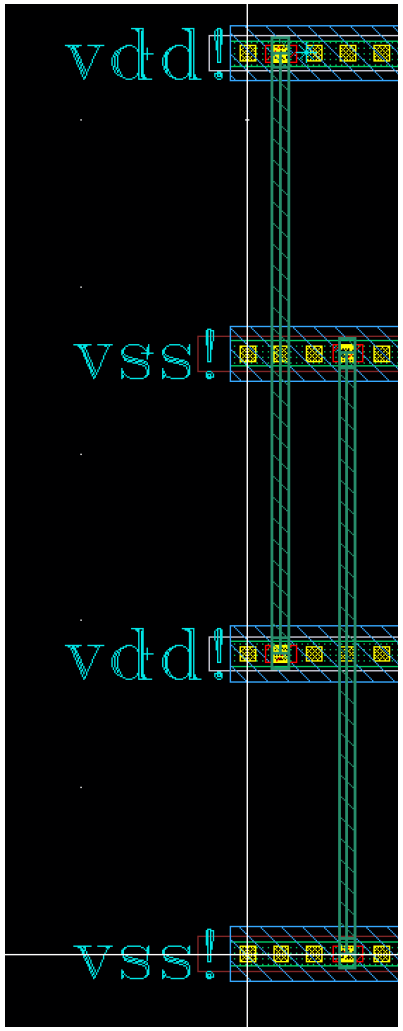


Power Rails – m2+ note

- Later in the presentation you are restricted to using m2 tracks which do not overlap with the power rails.
- This is because normally we would put an equally wide m2 power rail over the m1 power rail and connect them together.
- *For class 2022 and beyond there will be metals from all layers (M1-M9) over the power rail both horizontally and vertically that will cause you to lose 3 tracks out of every cell height worth of metal tracks in both the horizontal and vertical direction.*

Power rails – Connecting multiple rails

- If your design is taller than 1 cell height, then in later CADs you are required to physically connect the rails together
- Connect your VDD/VSS rails together using two m3 rails.
  - Example on the right to give you an idea, but you'll have to make some modifications to pass DRC.
- *This does not apply to class 2022 and after*

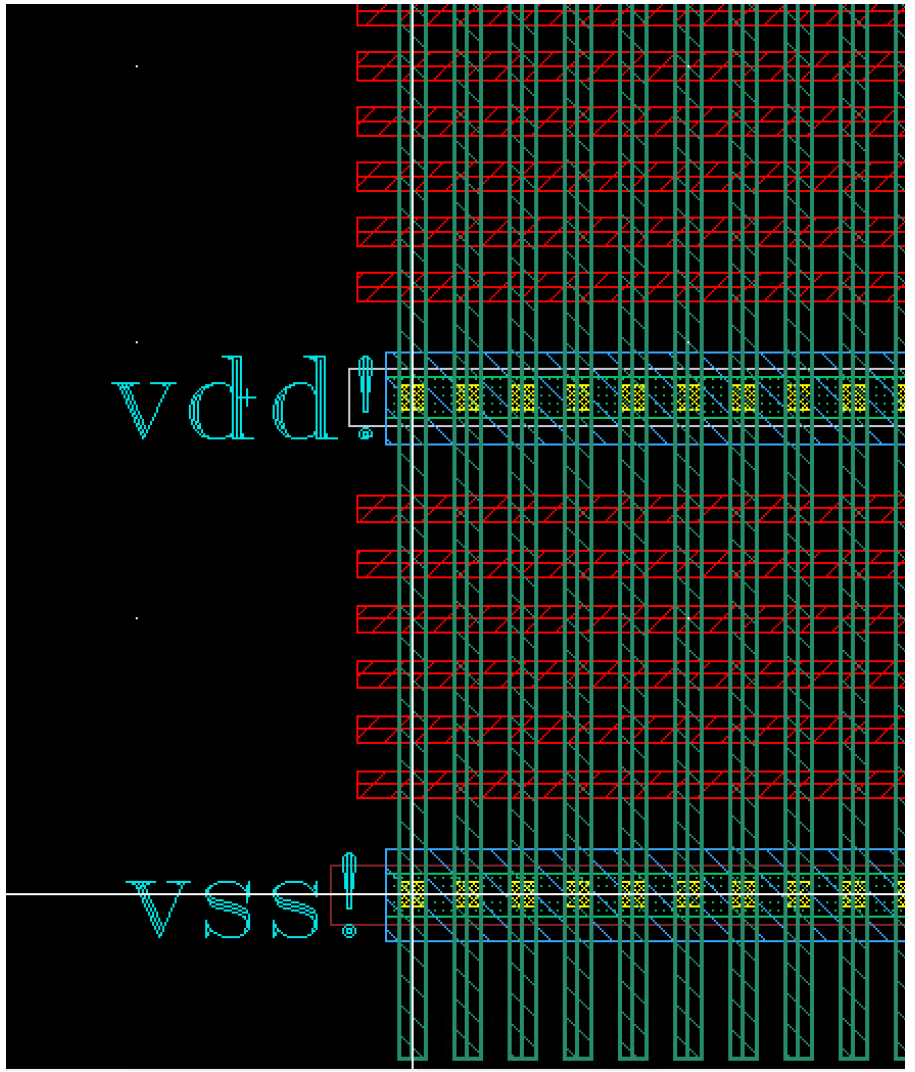


Metal Grid

- All routing metals must be on a 0.2um/0.2um grid centered on one of the contacts on your VDD/VSS rail.
- Even numbered metals m2 and above are horizontal only
- Odd numbered metals m3 and above are vertical only
- m1 is free of directional restrictions
- Metal must all be routed within the bounds of your power rails, If you run out of tracks for your design, then you may increase the size of your design by lengthening or vertically stacking more power rails.

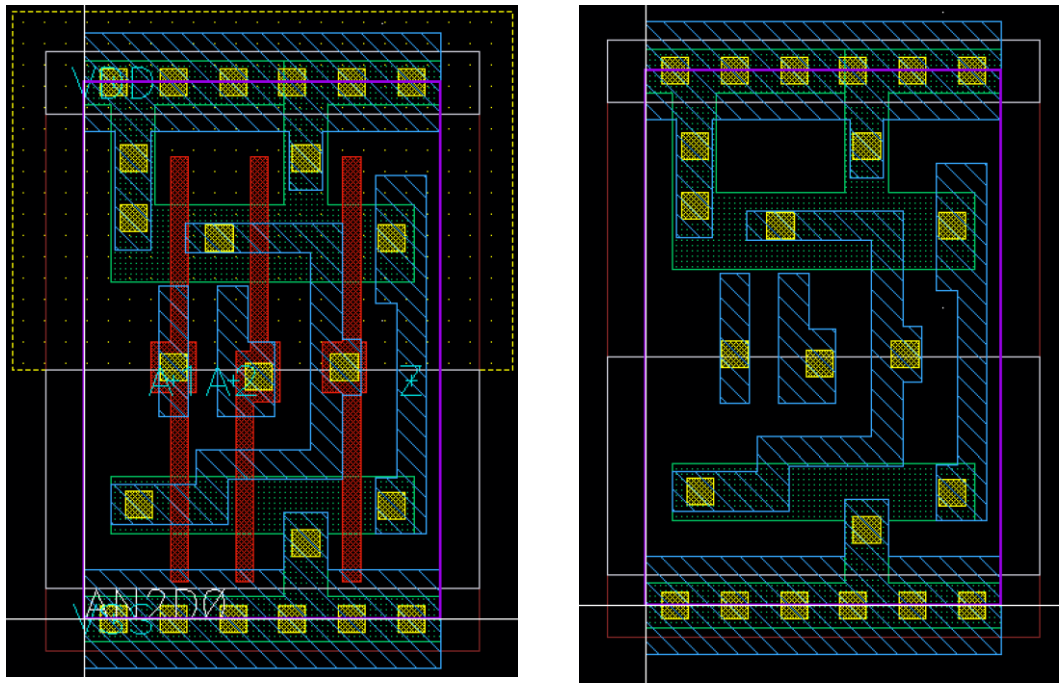
Metal Grid – the grid visualized

- The figure shows how your grid will look over your power rails with your rail contact properly centered.
- No m2 tracks directly over or adjacent to the power rail. (i.e. you lose 3 tracks per cell height)
- For higher even metals it is ok to route over power rails, *but this will not apply to class 2022 and later*.



PR boundary

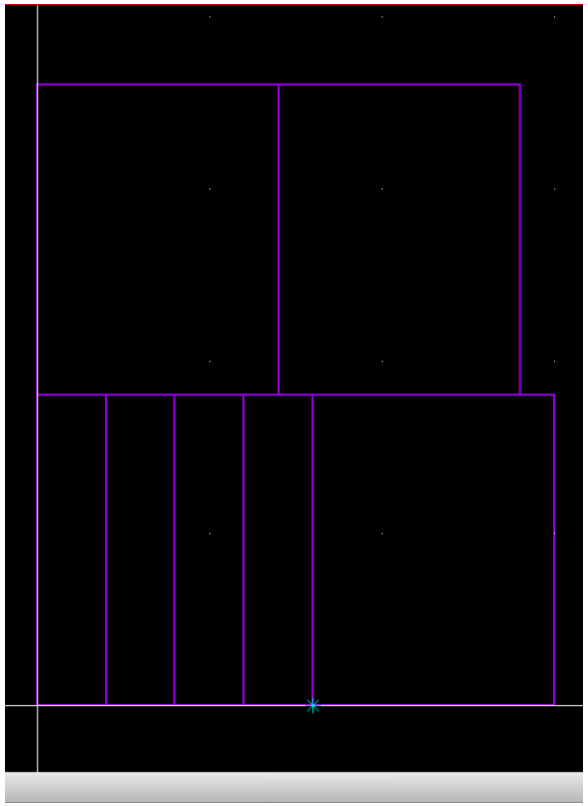
- The P&R boundary defines edge of your design.,
- It should be drawn such that by abutting the PR boundaries of multiple cells, you get a resulting design which is DRC clean and meeting the class convention.

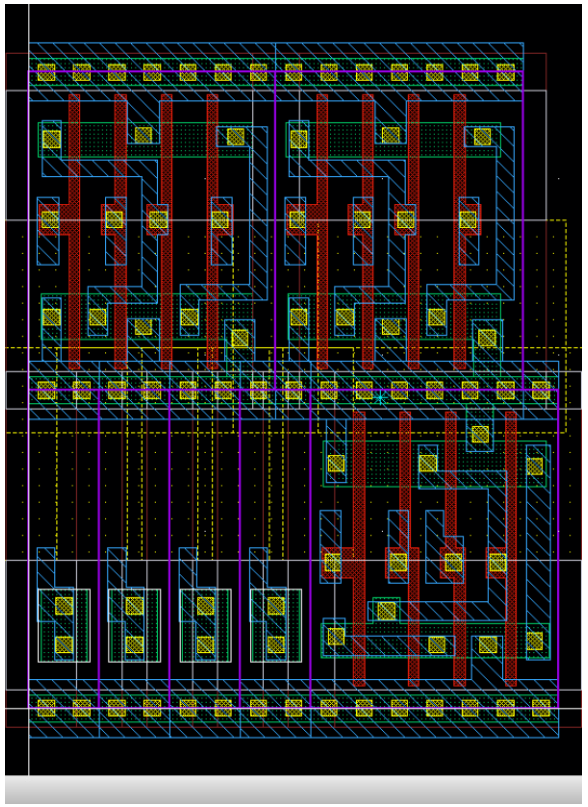


Left: AN2D0 layout
Right: AN2D0 layout with less layers visible
The PR boundary is the purple box bisecting the power rail contacts and overlapping with the x and y axis.

PR boundary – abutting cells example

- The left and right are the same design, but in the left you can only see the PR boundary, and on the right you can see the layers revealed
  - Make note of how the middle rails perfectly overlap to create a single rail - contact spacing throughout the rails remains consistent. There are also no DRC spacing conflicts between cells. This is the benefit of a properly drawn PR boundary





Class Conventions – big picture

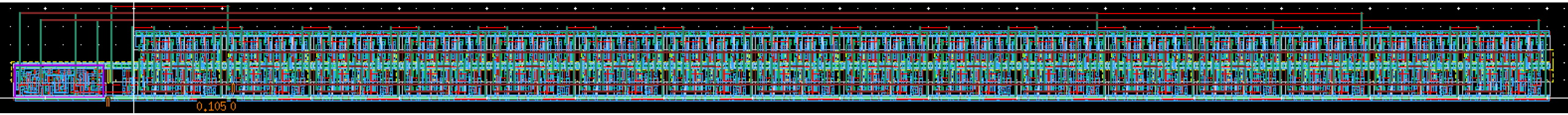
- The result of following class conventions about power rails, metal grid, and PR boundaries enables us to create designs which can easily be used as building blocks for larger designs with minimal modification, just as the standard cells can be used by us to build our designs.
- BIG PICTURE – To some extent you can consider your designs to be huge standard cells, which are themselves created out of smaller standard cells.
  - In case you are using your own custom cells, they should follow class convention so that they have the same benefits of a standard cell.

Design quality metrics

- These are metrics that may be used to evaluate the quality of your design.
  - **Area –** smaller is better
  - **Metal length –** less/shorter metal connections is better.
  - **Metal layer usage –** use as few metal layers as possible, starting from m1 and moving up (m2, m3, m4, etc.) as you run out of tracks/routing area in lower layers.
  - **Delay –** Lower delay (i.e. faster design) is better
  - **Energy/Power –** Lower average energy/power consumption is better
- These are the main metrics we use in this class. However, these are not all the metrics that can be used to evaluate the quality of a design. That will depend on your specific project goals.

Design fault #1 – metal outside power rails

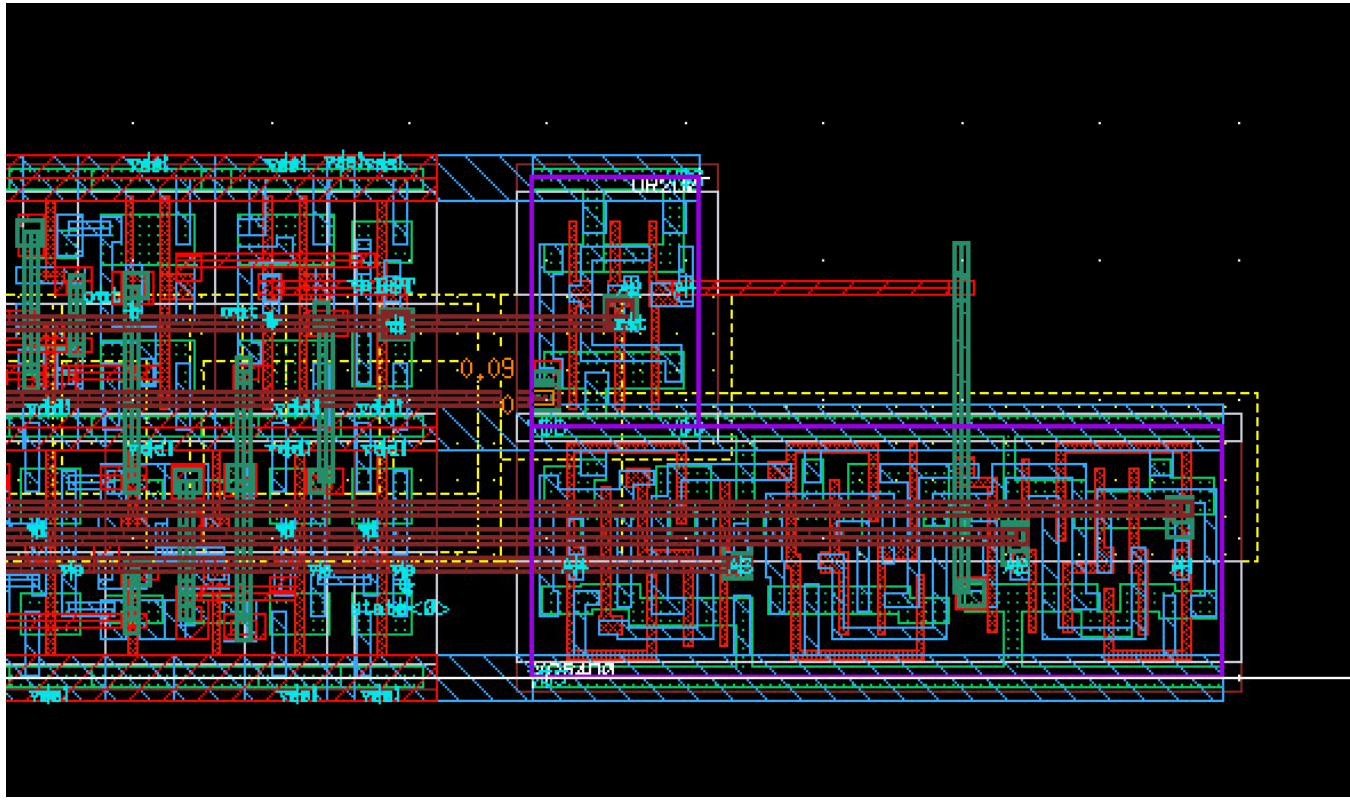
- Your entire design, including routing metals, should be done within the space enclosed by your power rails



- Above design has m3 and m4 above power rails, for this design there should be a 3rd power rail to encompass all routing metals.
- Better: Metals should be routed within the confines of the existing rails without adding extra space just for routing.

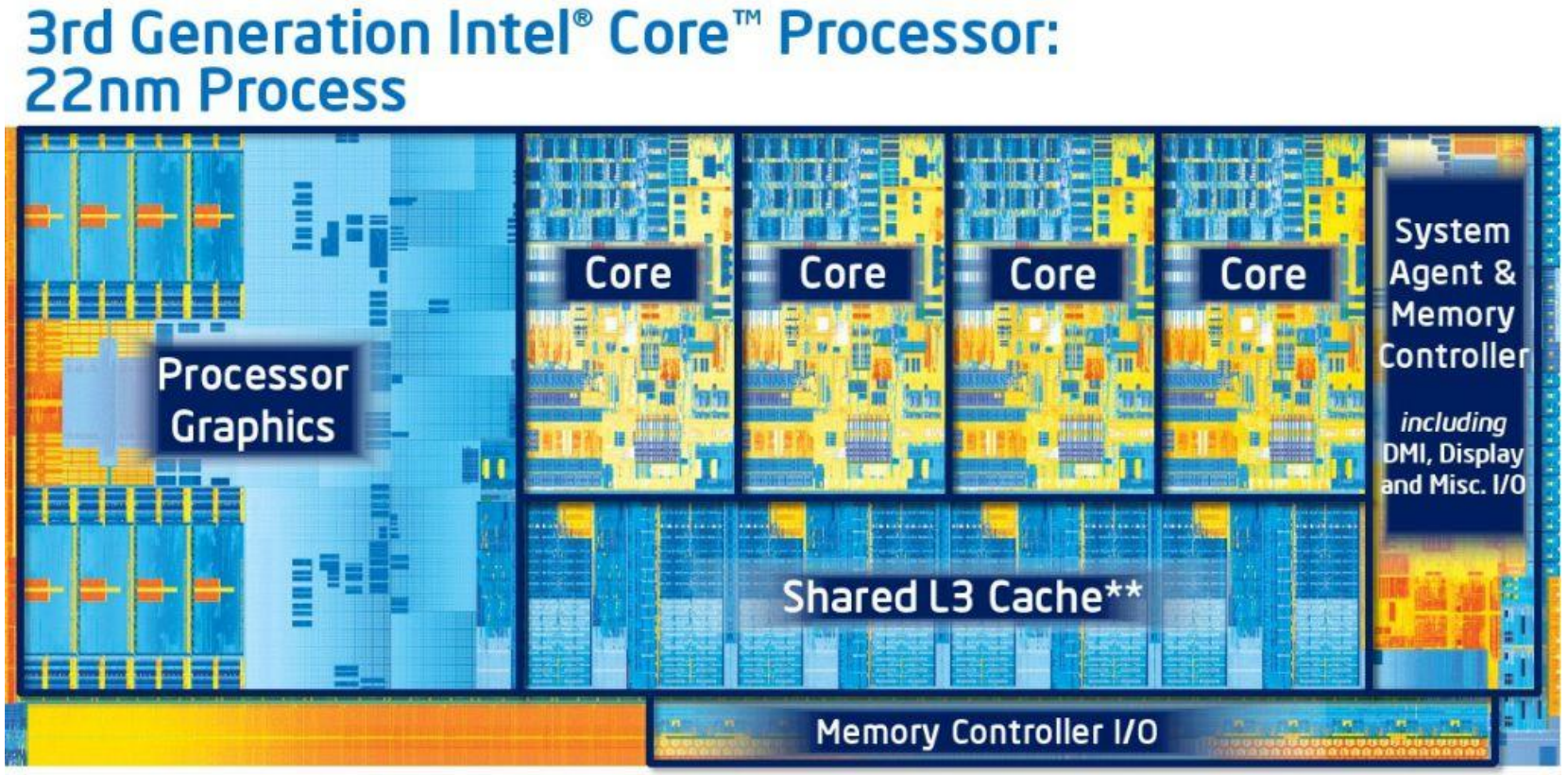
Design fault #1 - caveat

- In this design, you see an m2 track and m3 track in the top right which is not enclosed in the rails
- This is technically a violation, however it is unimportant because the true boundary of your design is essentially rectangular (i.e. You would not tile another cell in this space anyways), so the overall effect is negligible.
- However, this person should still extend the top rail fully to the right of their design with the other 2 power rails



Design fault #1 – real floorplans/die shots 1

- To reinforce the idea of rectangular design boundary, this and some following slides are floorplans/die shots of real circuits.
- Notice how almost all subblocks are rectangular. Top level blocks are also roughly rectangular shaped (exactly rectangular for this shot)



Design fault #1 – real floorplans/die shots 2

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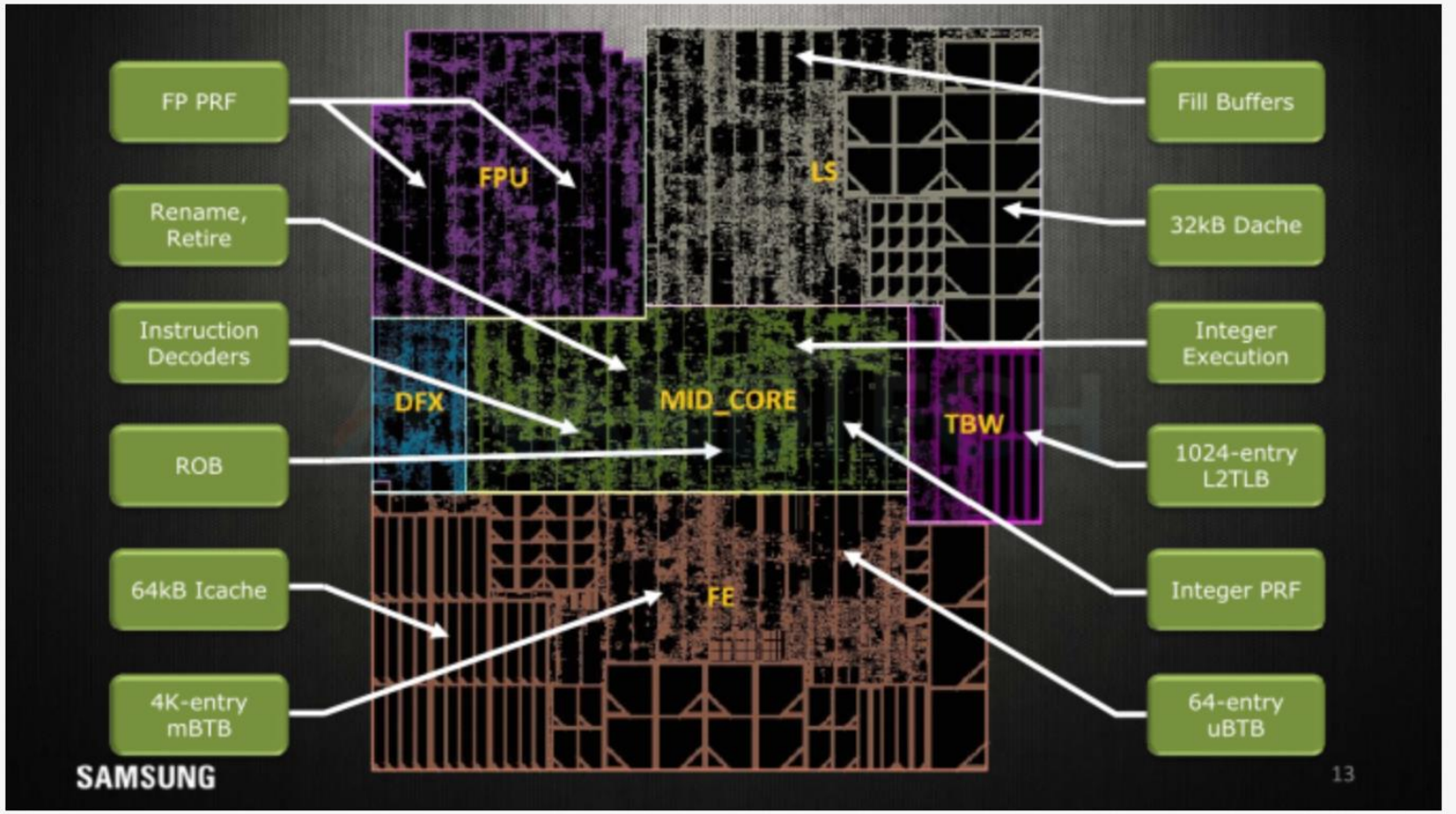
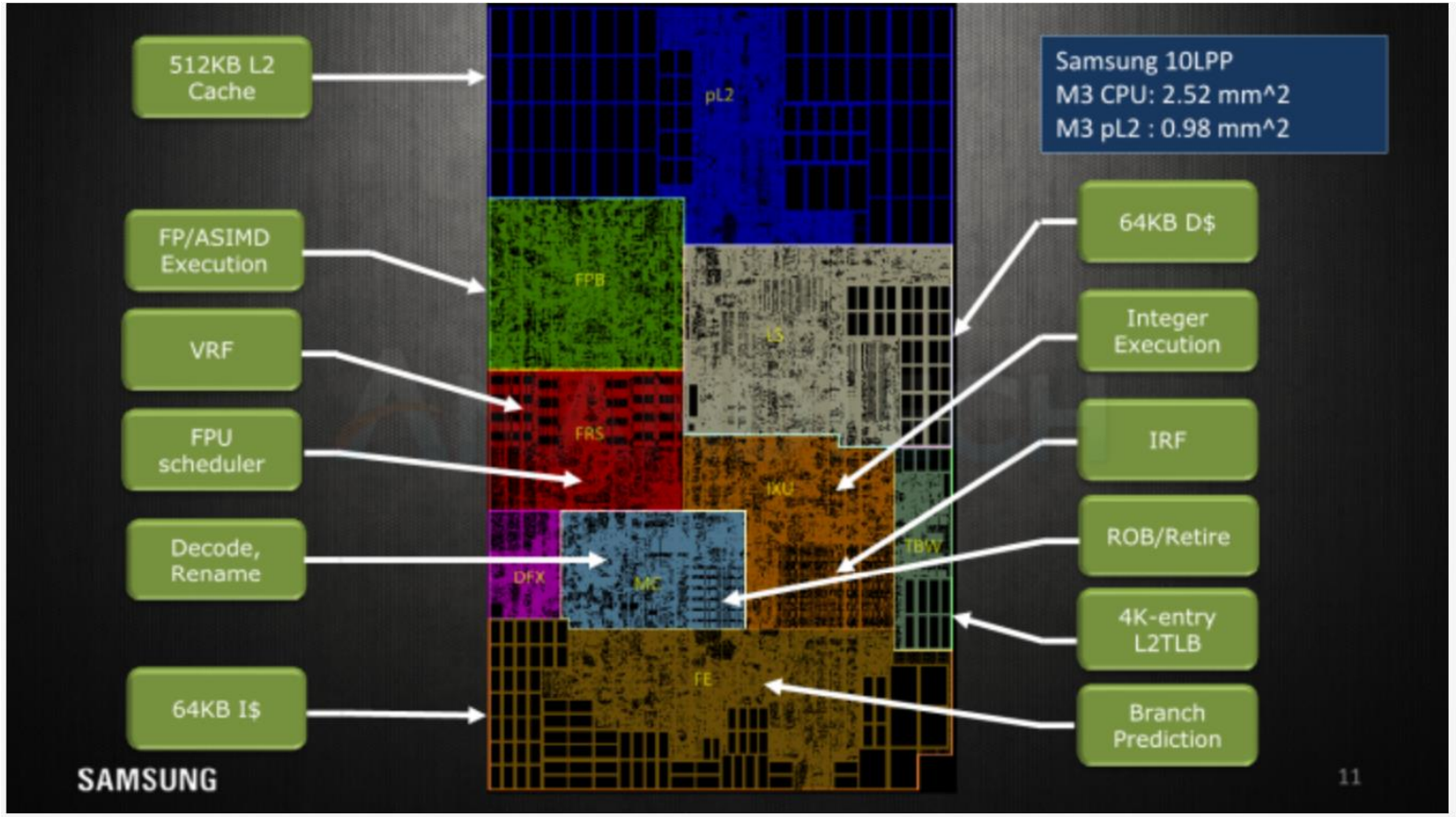


Exynos M1 Core Layout

Design fault #1 – real floorplans/die shots 3

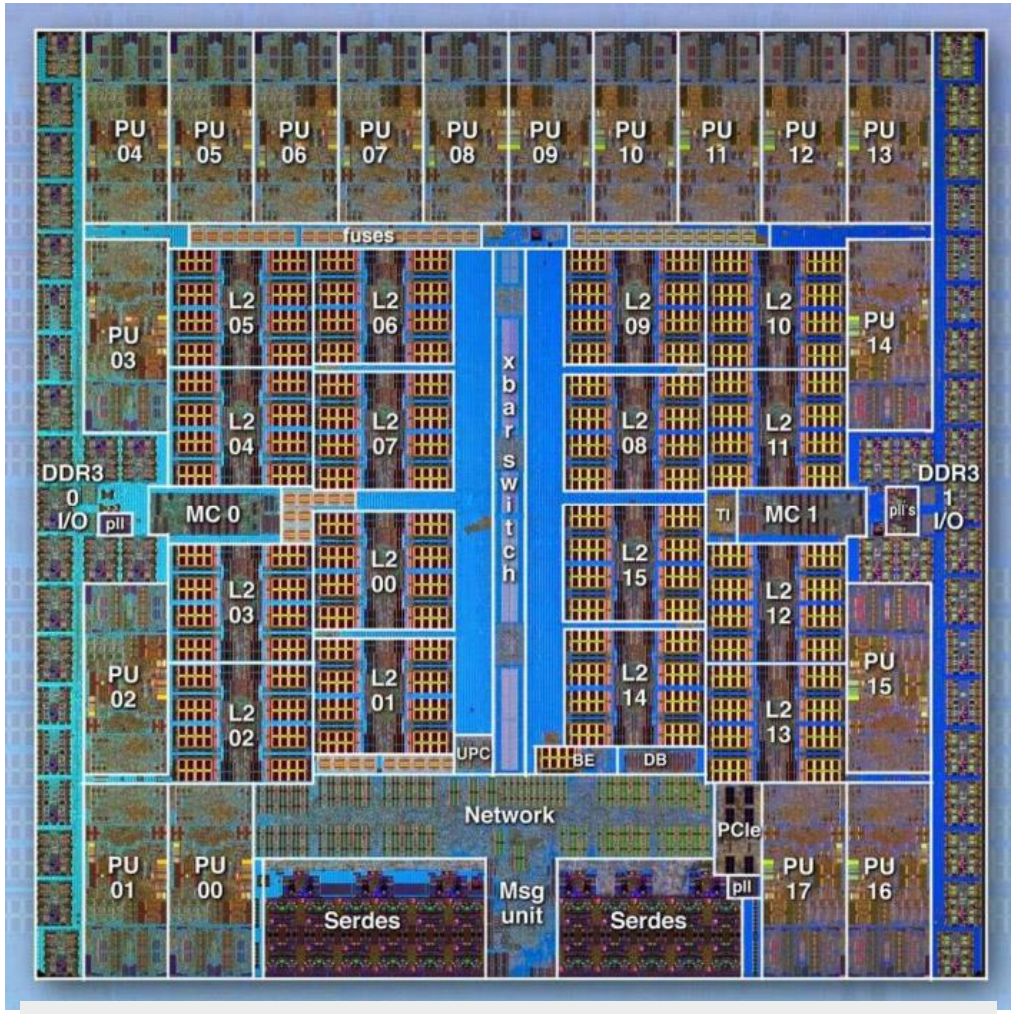
- To reinforce the idea of rectangular design boundary, this and some following slides are floorplans/die shots of real circuits.
- Notice how almost all subblocks are rectangular. Top level blocks are also roughly rectangular shaped



Exynos M3 Core Layout

Design fault #1 – real floorplans/die shots 4

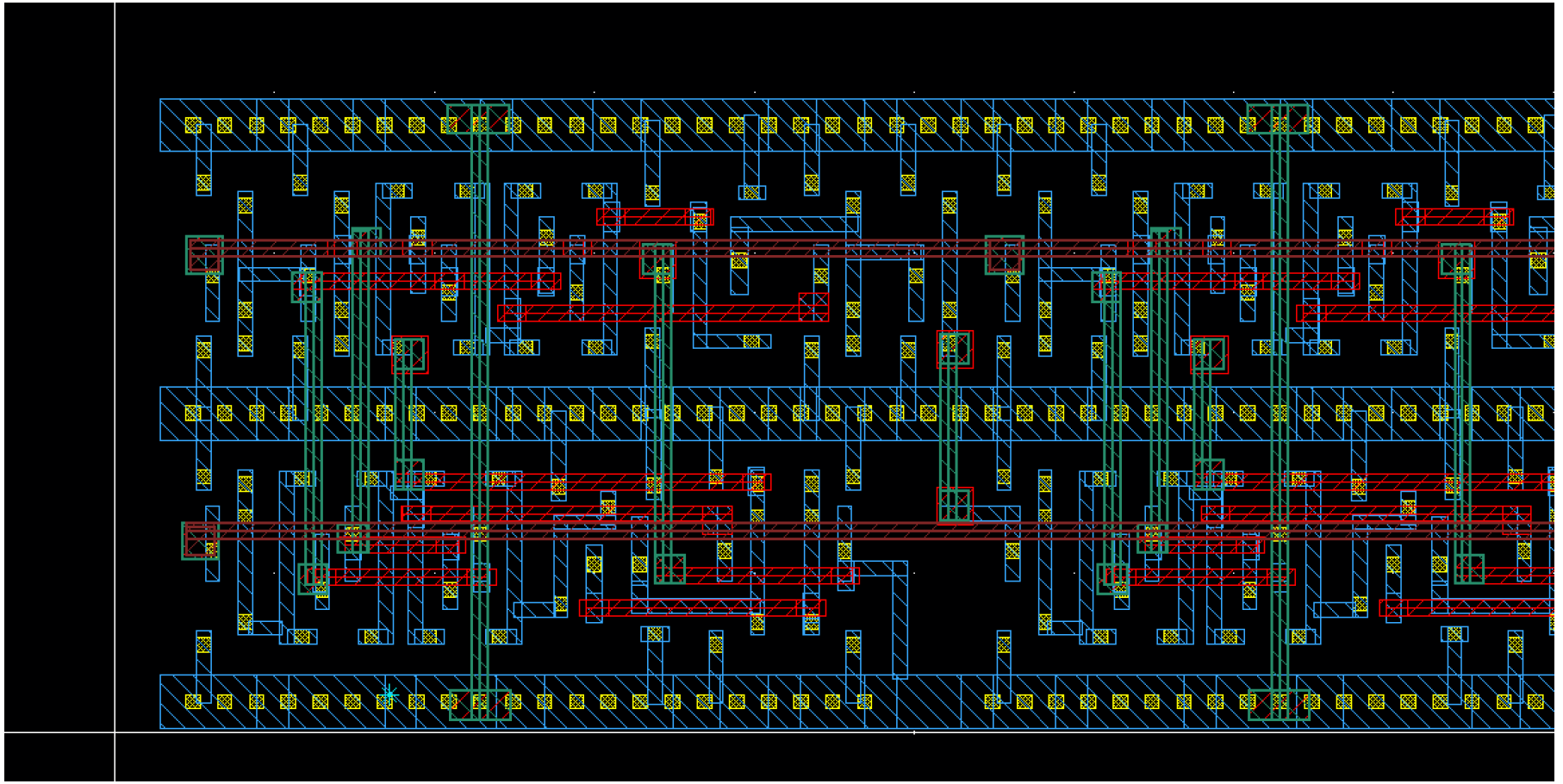
- To reinforce the idea of rectangular design boundary, this and some following slides are floorplans/die shots of real circuits.
- Notice how almost all subblocks are rectangular. Top level blocks are also roughly rectangular shaped



BlueGeneQ ASIC die shot

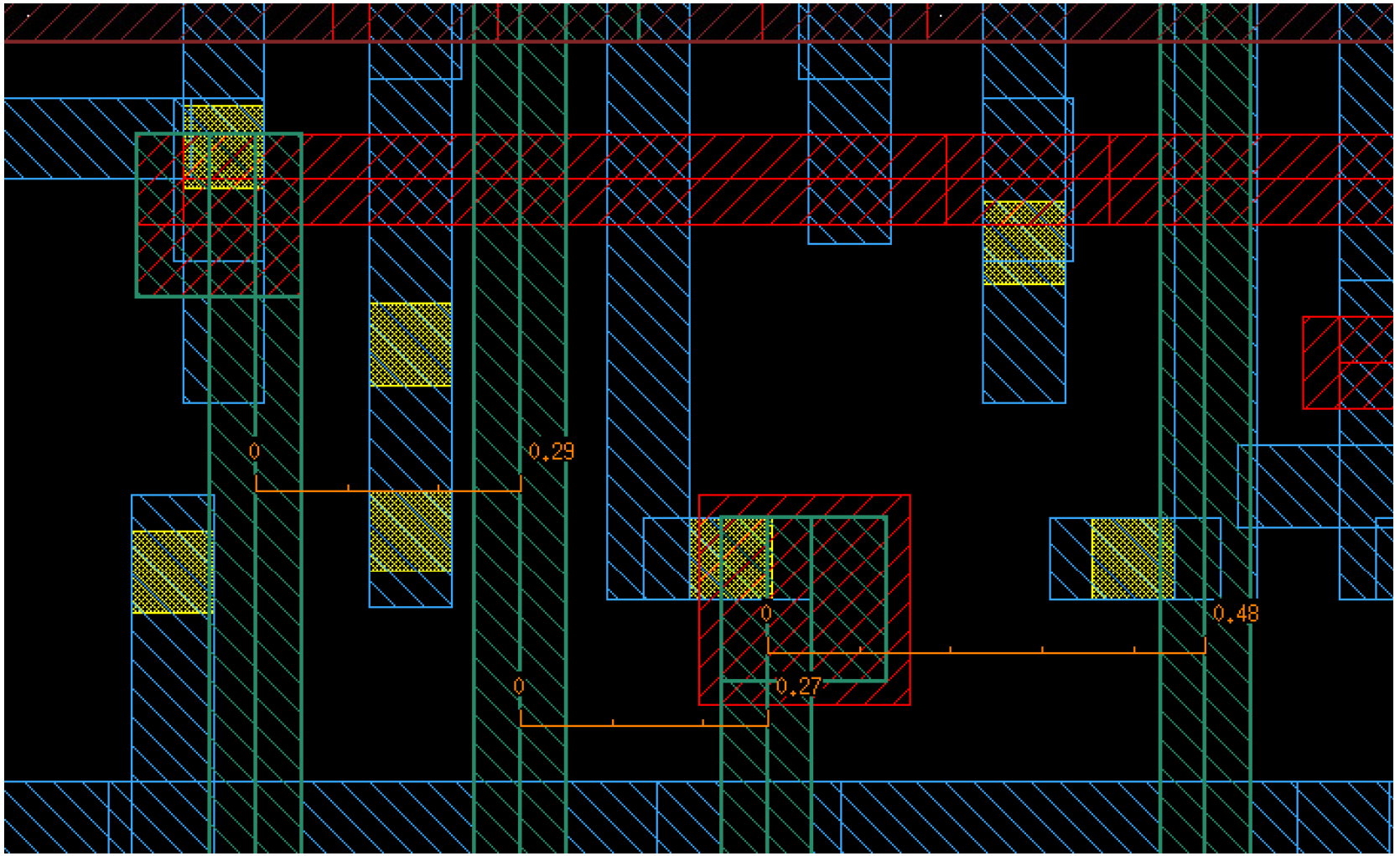
Design fault #2 – off-grid metal

- This shows only the metal and contacts of a design.
- At first glance, it looks good. However, after measuring the metal spacing, it can be shown that the metal routes are off grid



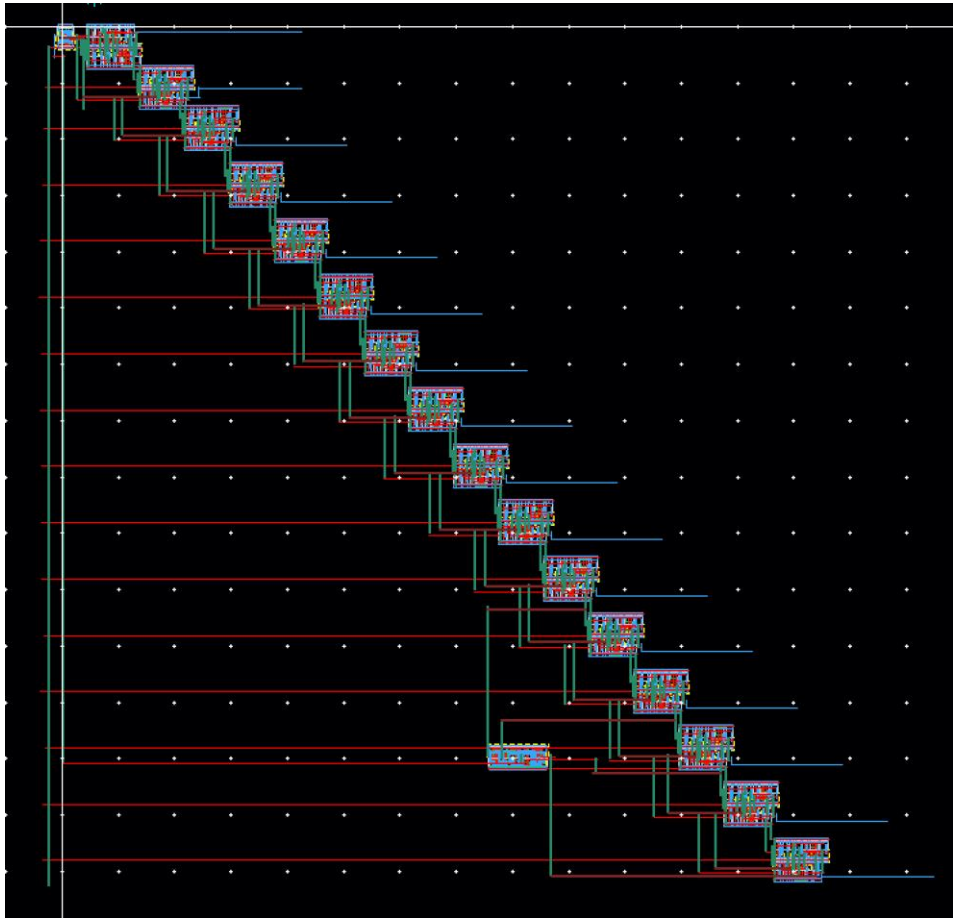
Design fault #2 – off-grid metal

- This shows only the metal and contacts of a design.
- At first glance, it looks good. However, after measuring the metal spacing, it can be shown that the metal routes are off grid
- Metals should have a center-to-center pitch which is a multiple of 0.2um



Design Fault #3 – Can you count them all?

- This is a big box. But it is very sparse.
- Please be more conservative with the addition of new cell heights. Generally it is best to get a design that is pointing either in the x or y direction, not along y = -x.
- This design will be very hard to fit into a larger project without wasting a lot of space.



Design Fault #4 – TBD

Wrap-up

- That’s all for now, I may update this with more examples of bad designs later.
- Hopefully this will help clear up misunderstandings about how you should design your layouts.