

Lecture 3: Basic MOSFET Theory

Based on material prepared by prof. Visvesh S. Sathe

Acknowledgements

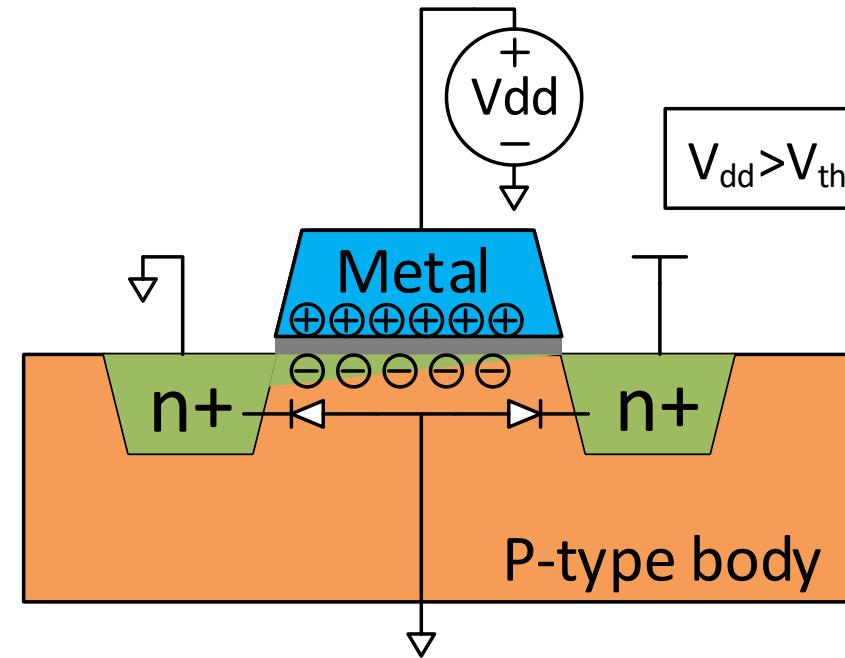
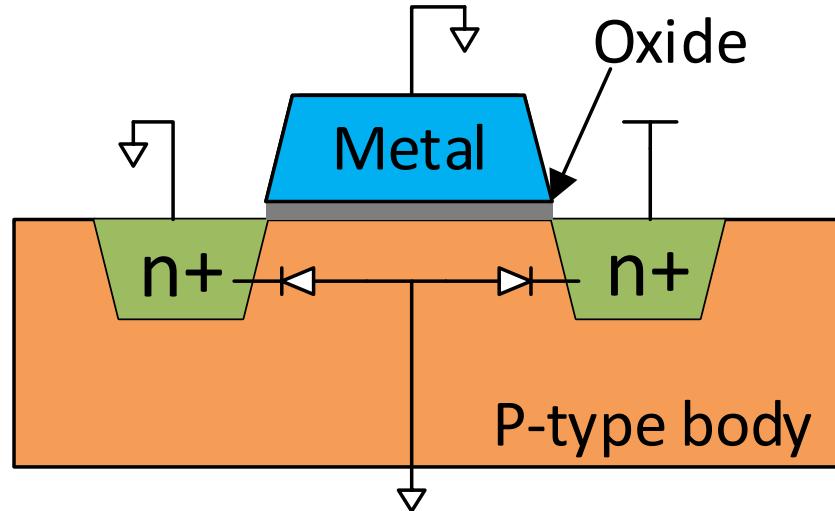
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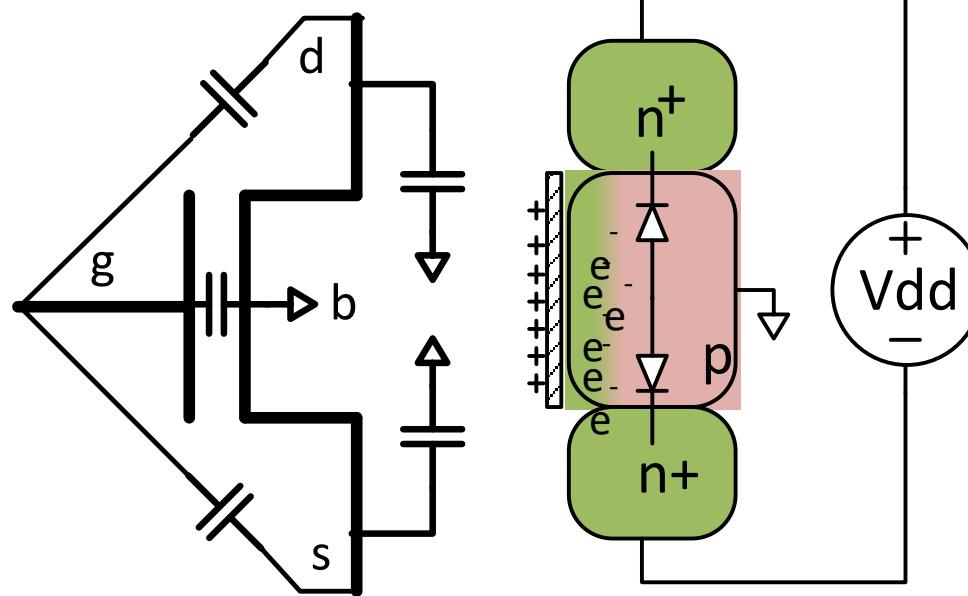
UW (2013-2022)
GaTech (2022-present)

The MOS Structure



- Metal Oxide Semiconductor
 - “Metal” implemented as poly-crystalline silicon (polysilicon) till recently
 - Conductor-insulator-semiconductor “sandwich”
 - Changing the voltage across Metal-Semiconductor varies the properties of the semiconductor

Quick Detour: Parasitic Capacitance



- What is capacitance exactly?
 - So what's so bad about it?
 - V-driven, not Q-driven
 - Low C → Lower Q, faster, lower energy
 - Smaller is faster (Dennard's law)
 - Major Parasitic contributors
 - MOSFET gates, MOSFET source/drains, wire

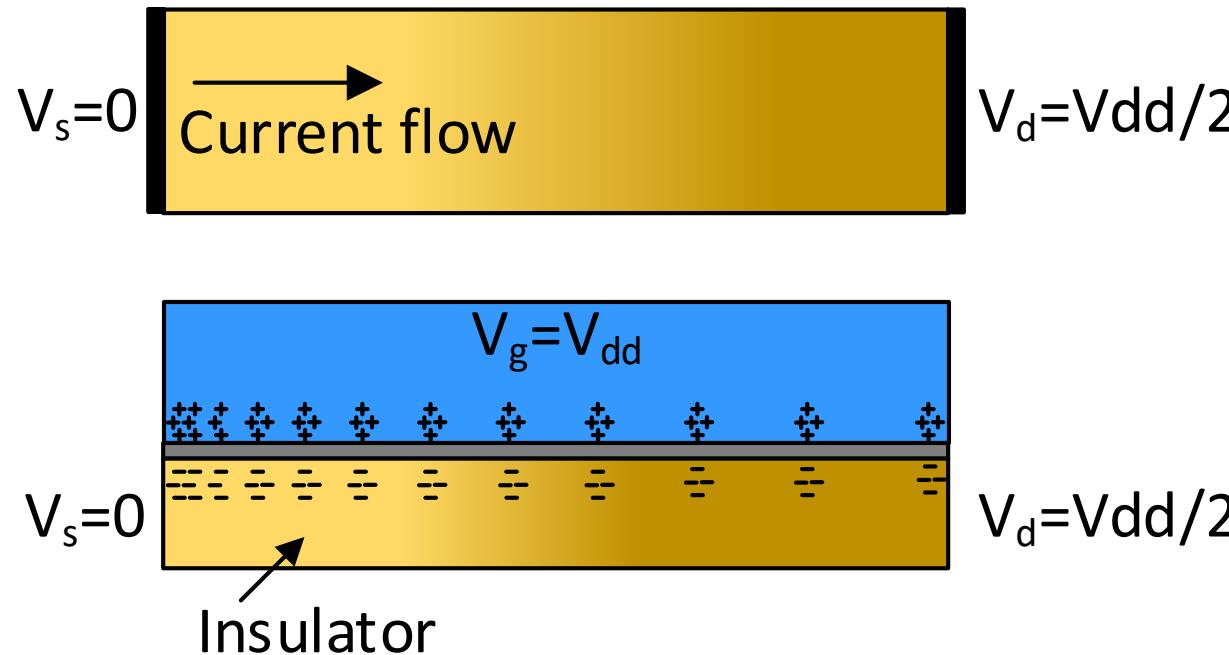
Impact

- Circuit Speed (Digital)
- Power (Digital)
- Bandwidth (Analog)
- Stability (Digital, Analog)

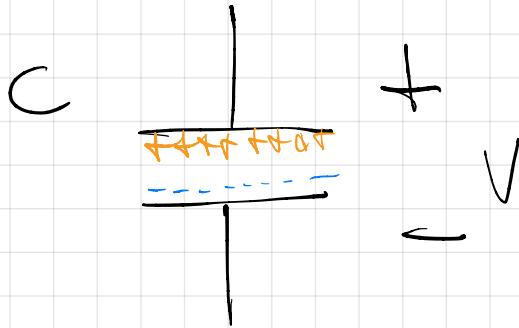
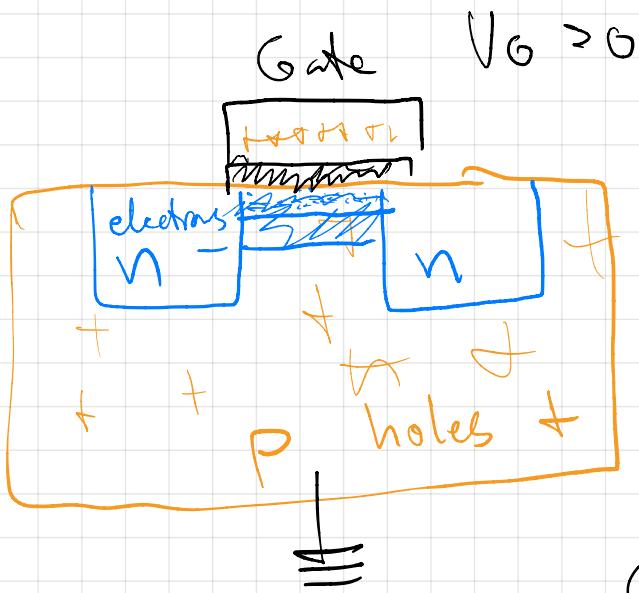
Calculate the per-unit length capacitance of an infinitely long cylindrical wire, diameter d in free space



MOS Transistor – A 10K foot view

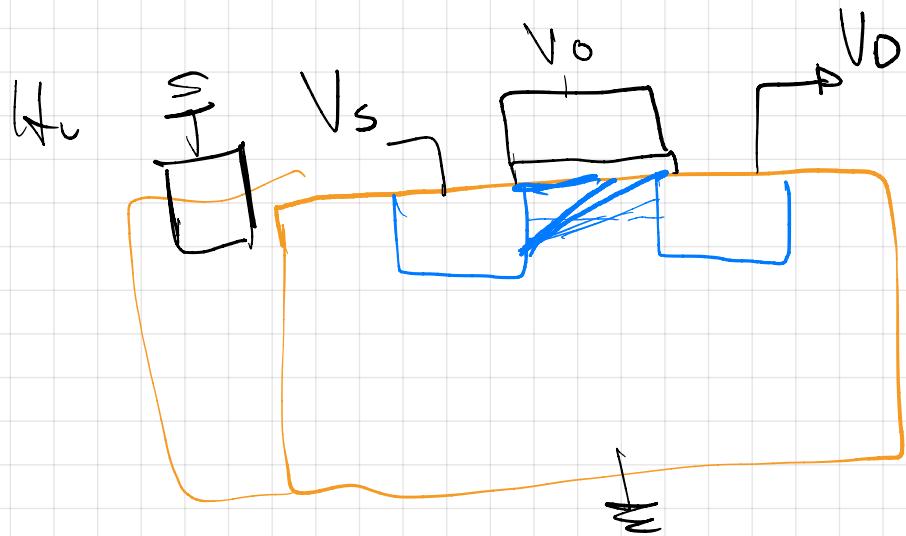


- Capacitor charge buildup allows for a “channel” to form
- Charge density not uniform → ? Impact on R. ? Impact on $V(x)$
- How can I reduce the resistance of this device further?

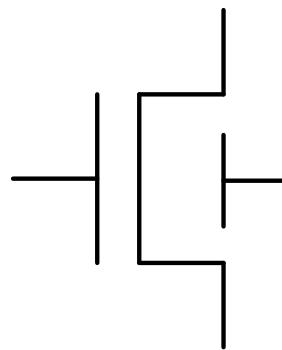


$$Q = CV$$

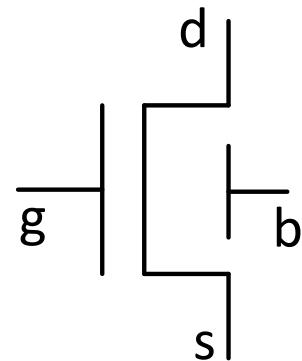
Charging
Neumann



MOS Transistor – A Strictly Intuitive View

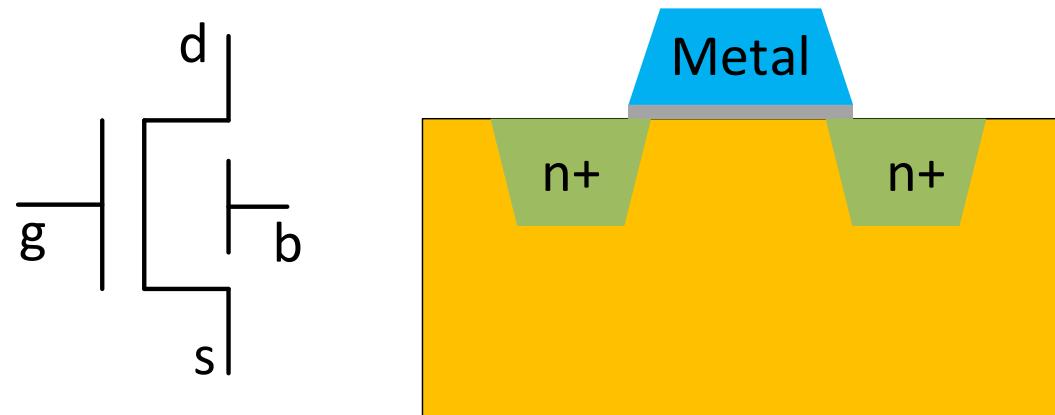


MOS Transistor – A Strictly Intuitive View

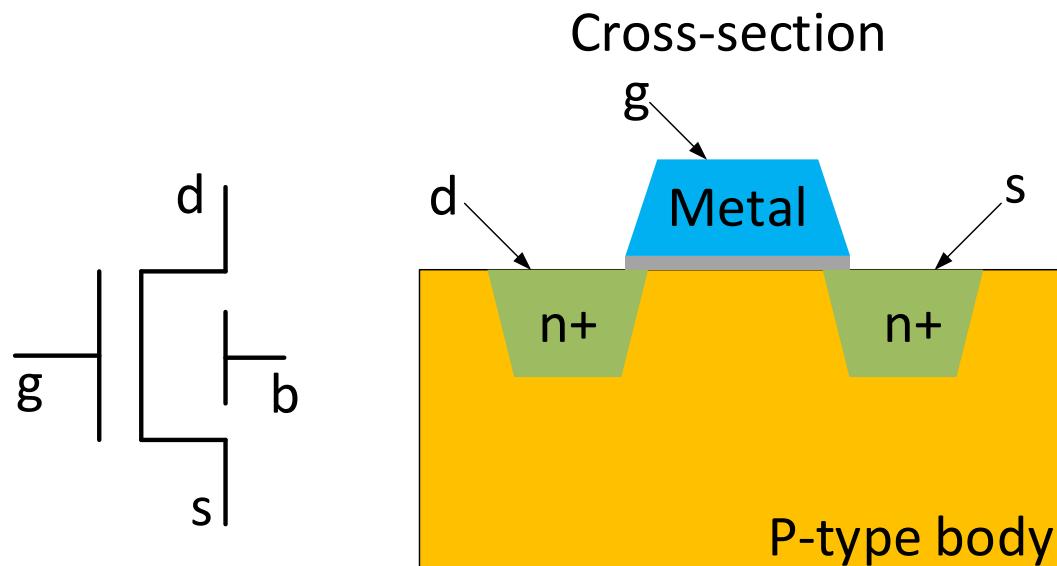


MOS Transistor – A Strictly Intuitive View

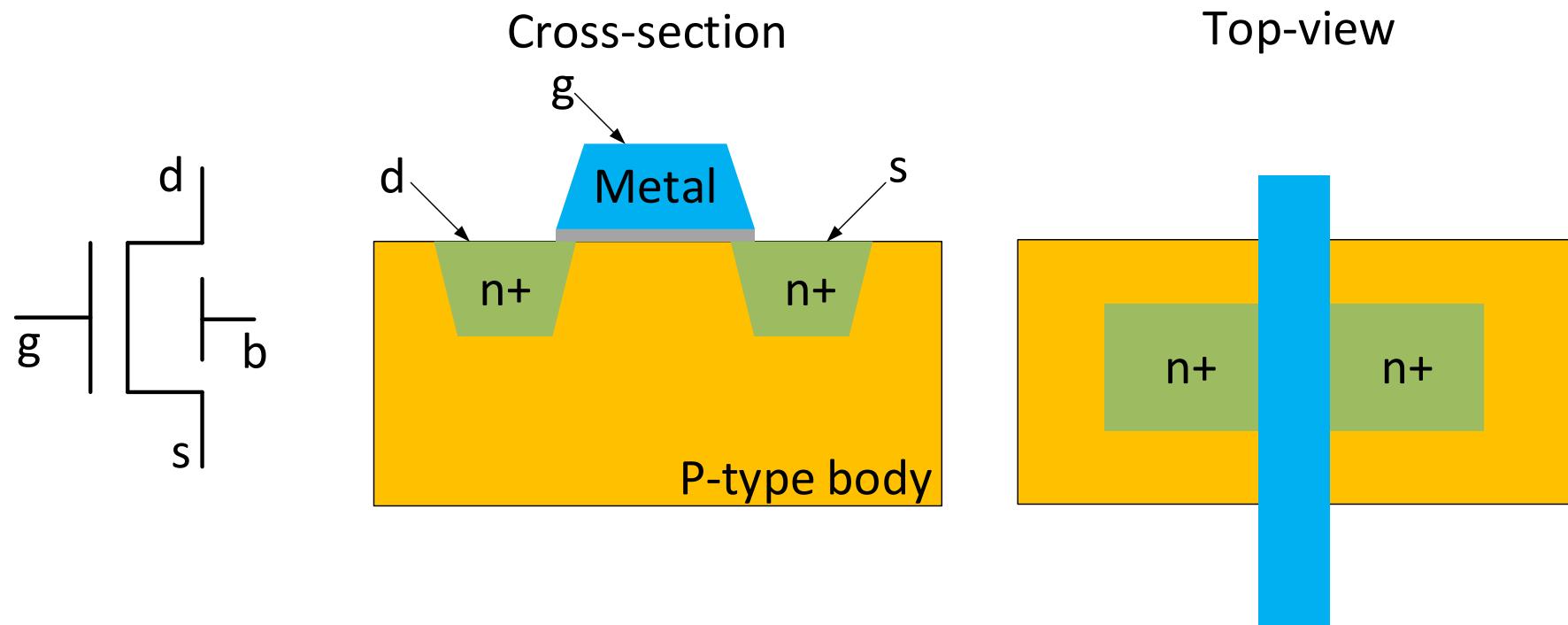
Cross-section



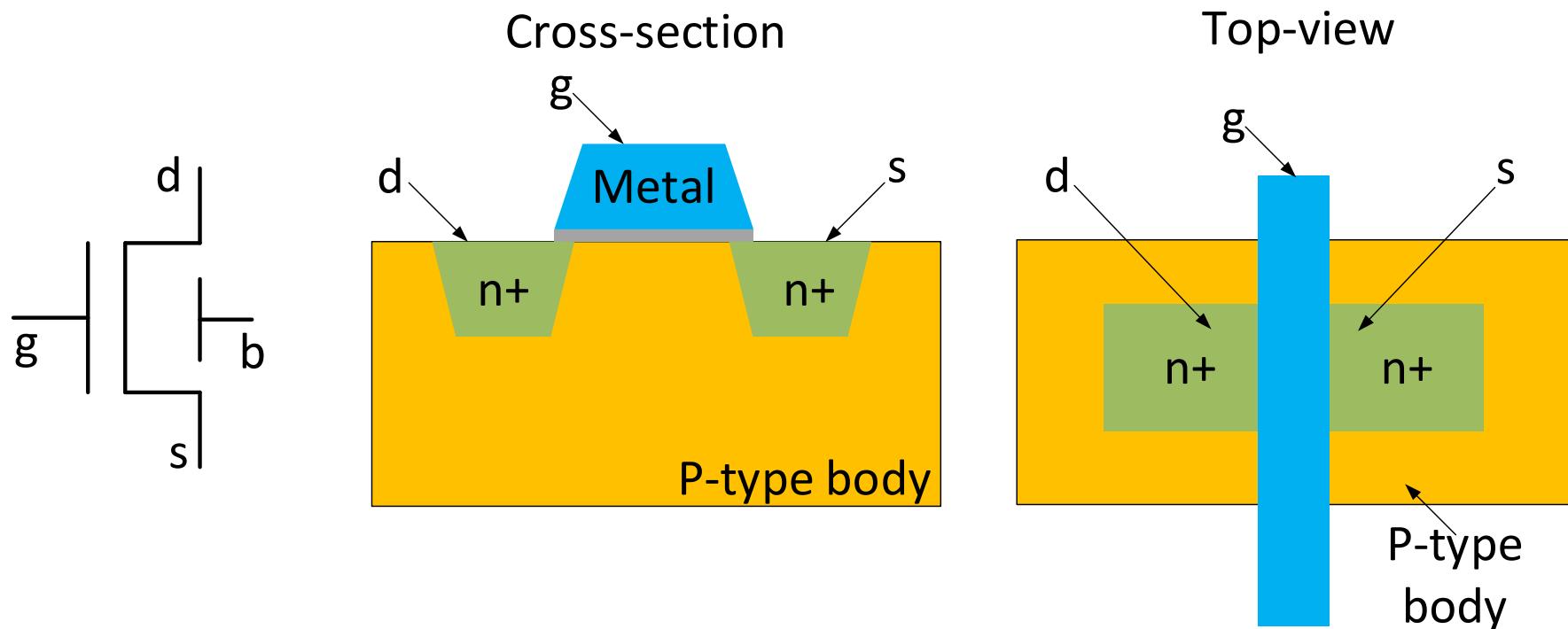
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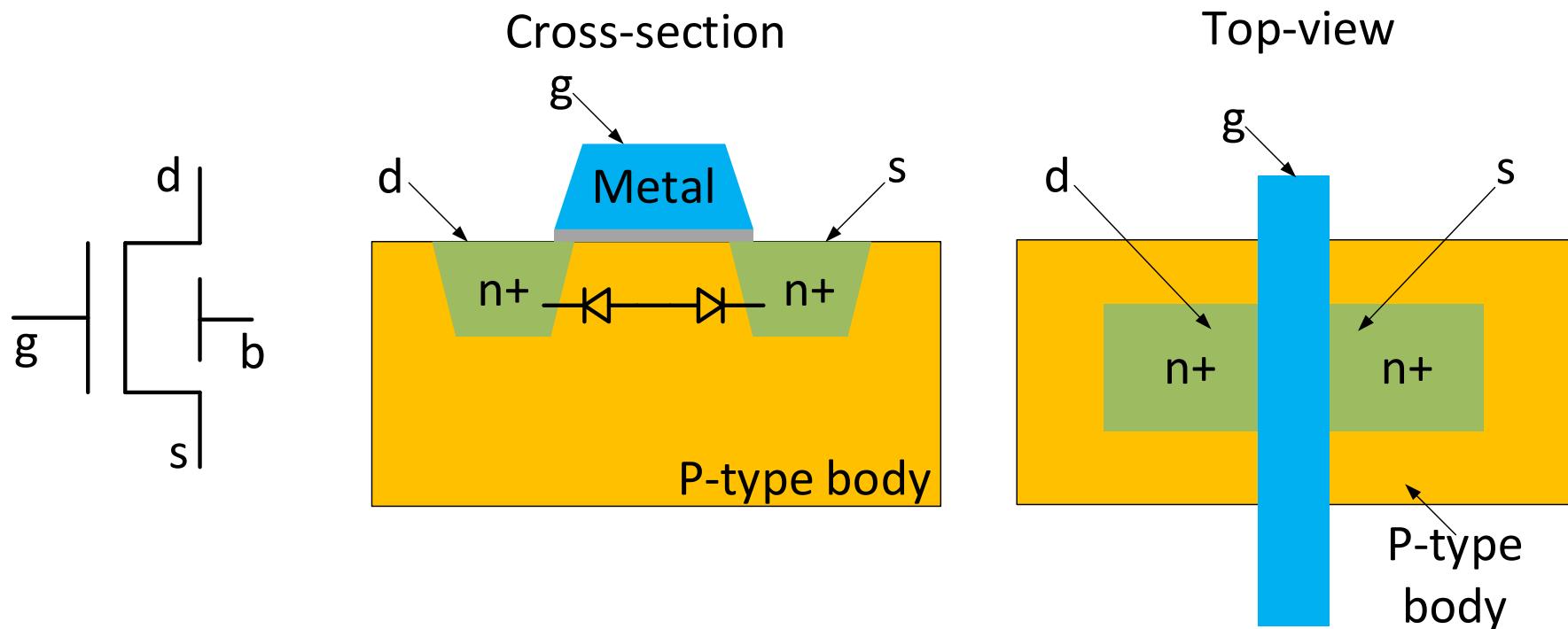
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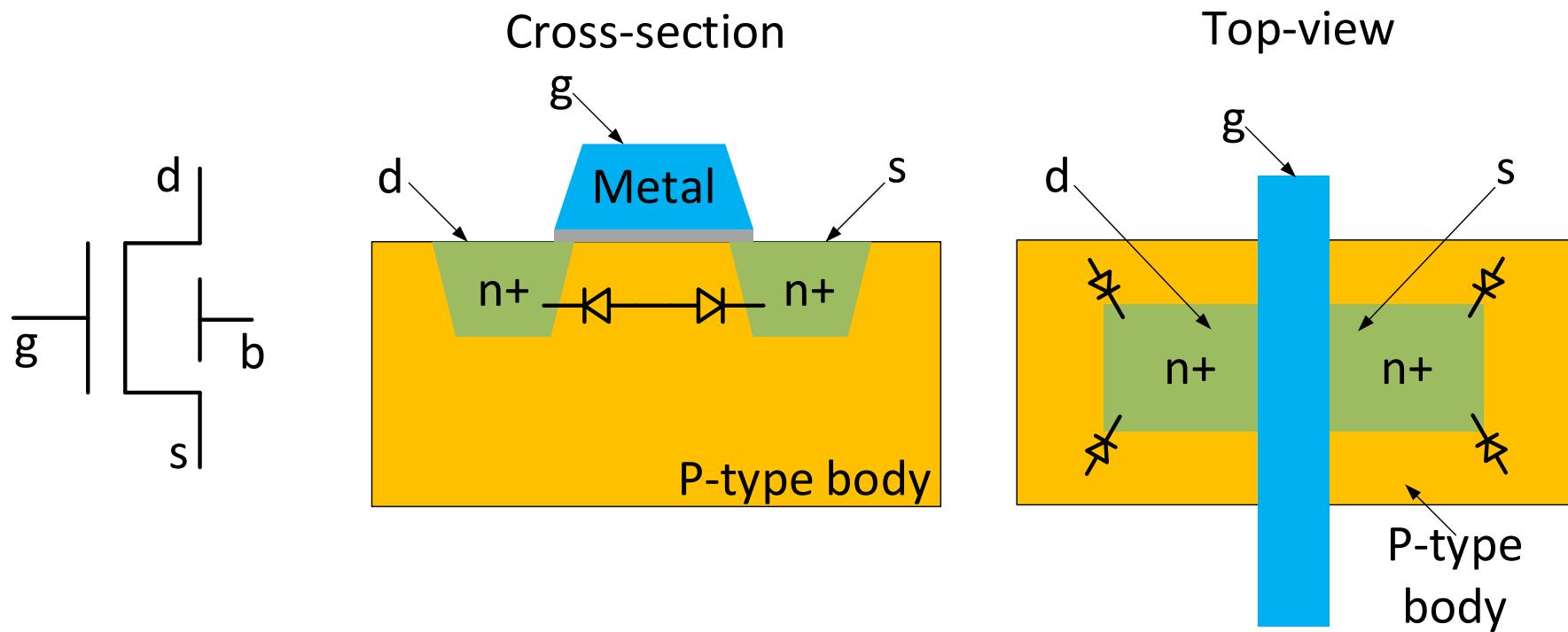
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MOS Transistor – A Strictly Intuitive View

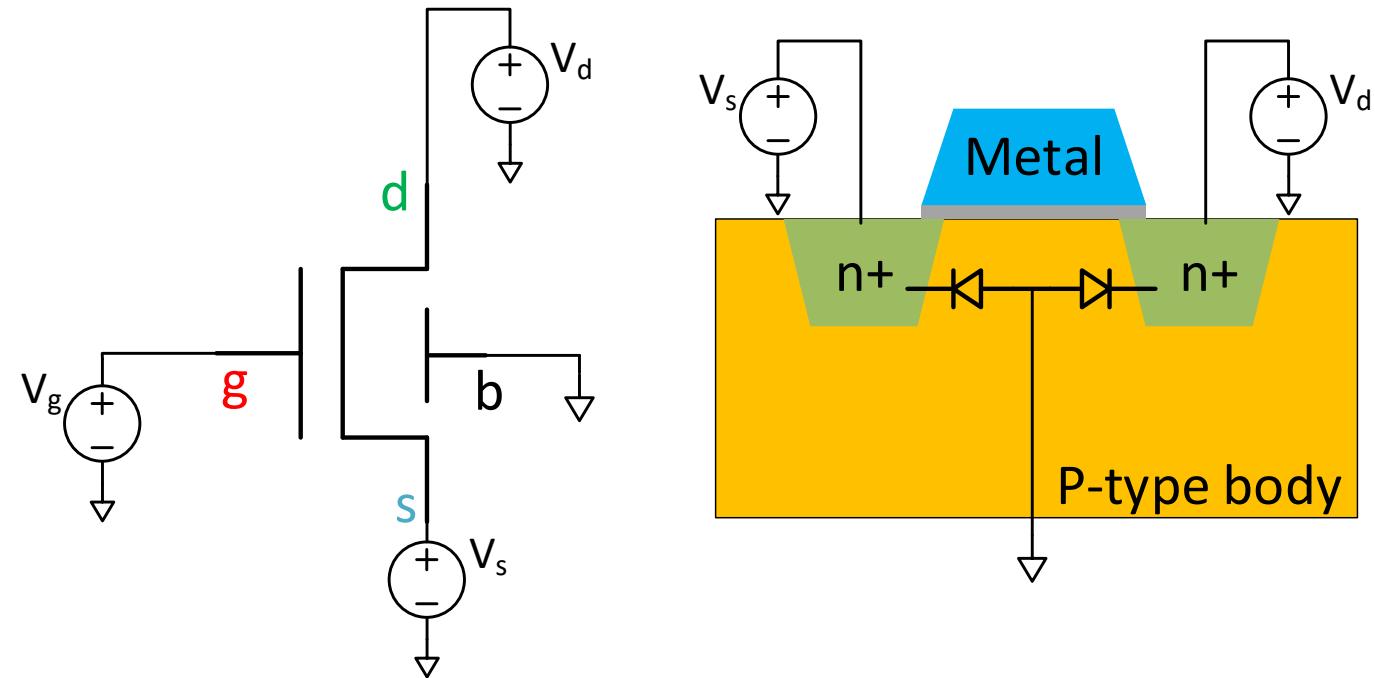


MOS Transistor – A Strictly Intuitive View

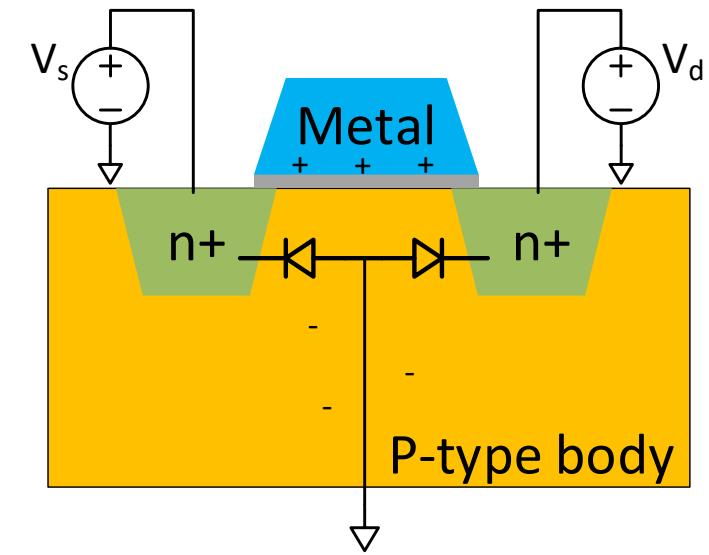
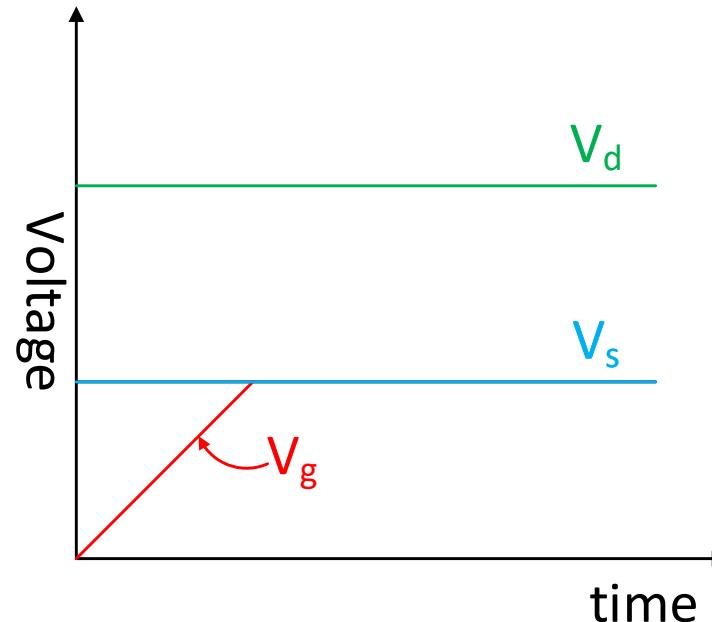
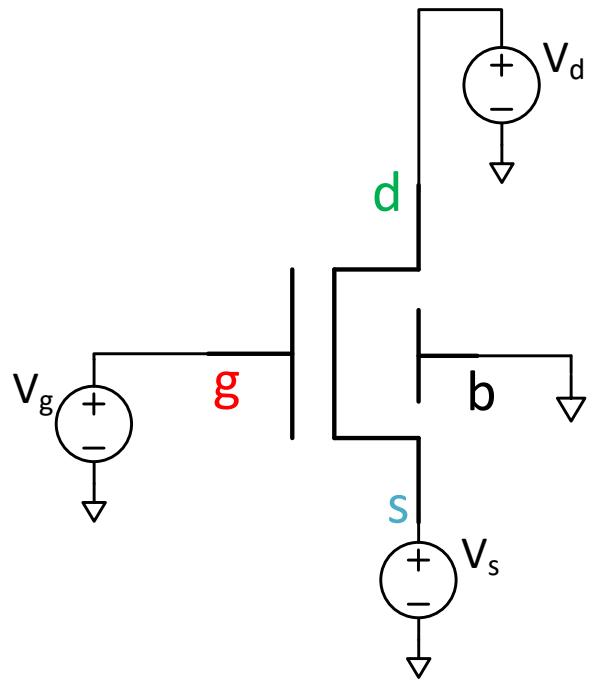


MOS Transistor – A Strictly Intuitive View

- For this course
 - Body of an **nmos** device is always tied to **ground**
 - Body of a **pmos** device is always tied to **Vdd**

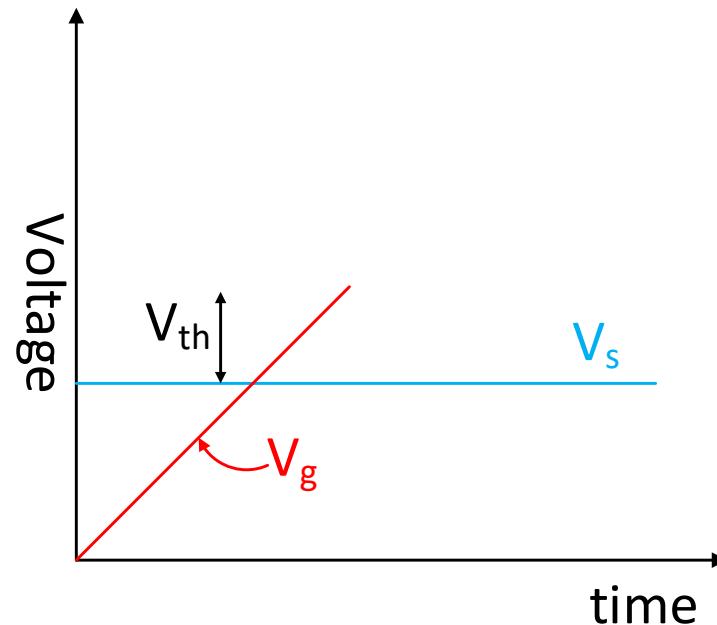
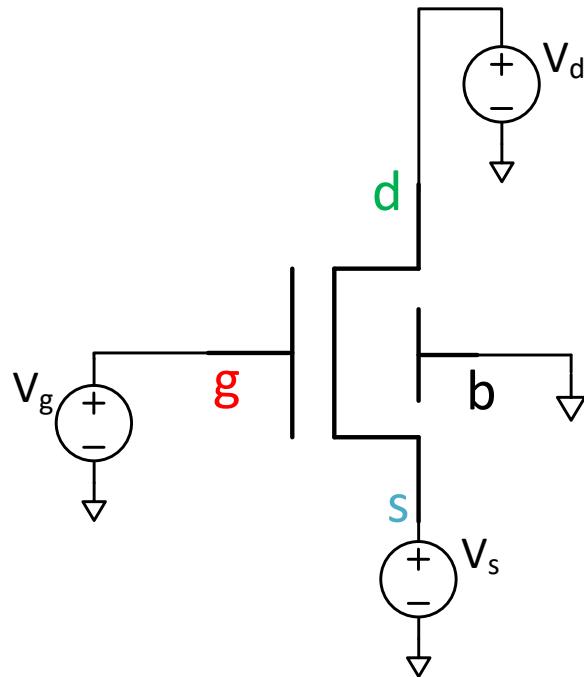


MOS Transistor – A Strictly Intuitive View

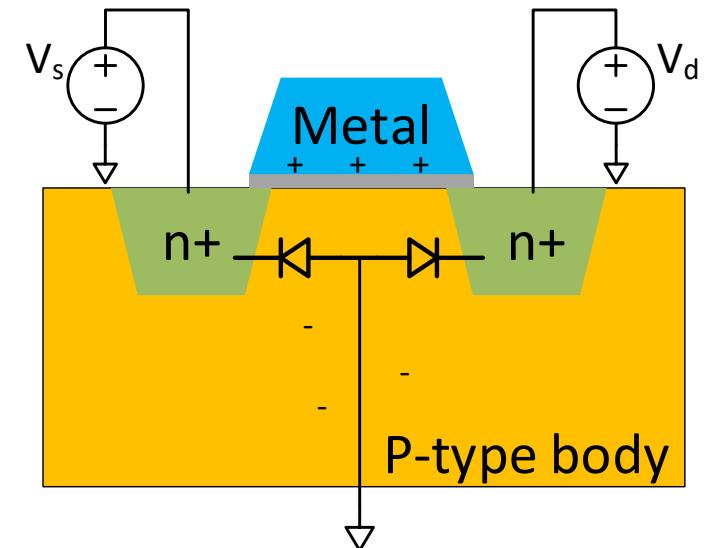


- Initially $V_g < V_s$
- No channel formed

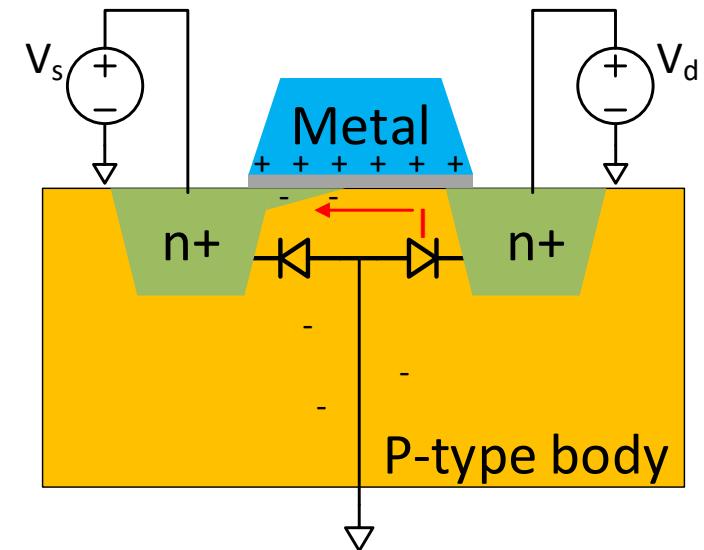
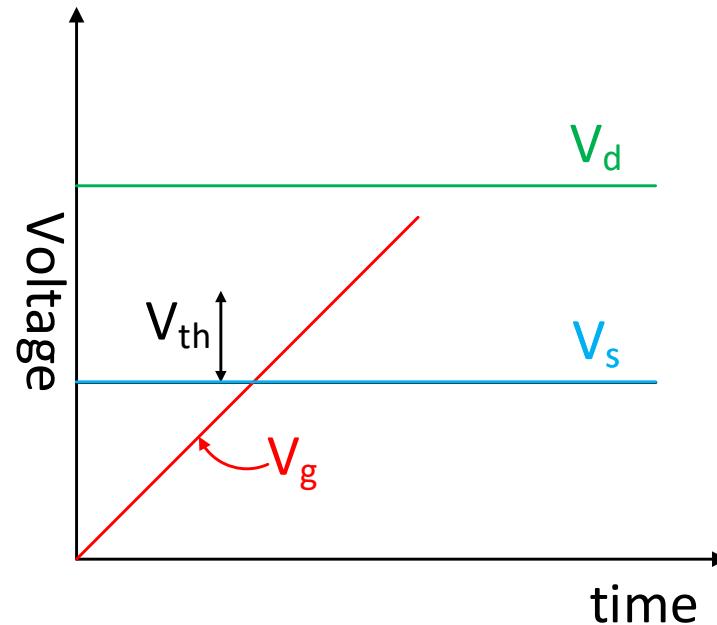
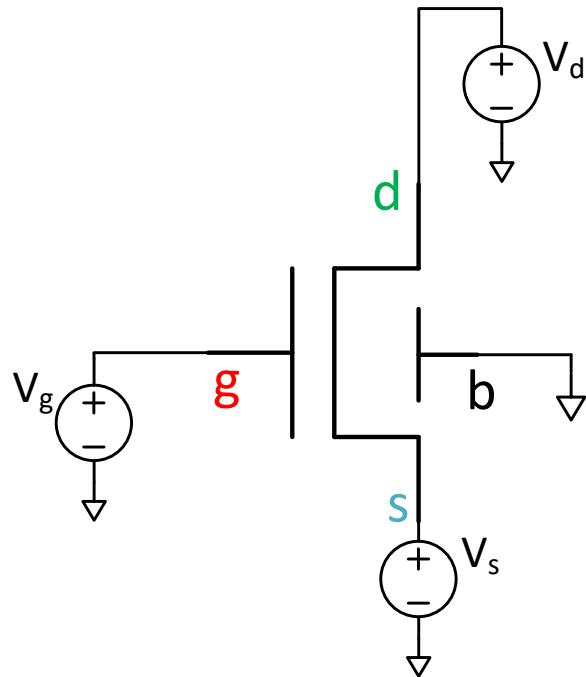
MOS Transistor – A Strictly Intuitive View



- Initially $V_g > V_s$
- But $V_g - V_s < V_{th} \rightarrow$ No channel formed
- $V_g - V_s \rightarrow V_{gs}$
- $V_{gs} - V_{th} = V_{gs}'$ (Also called gate overdrive)

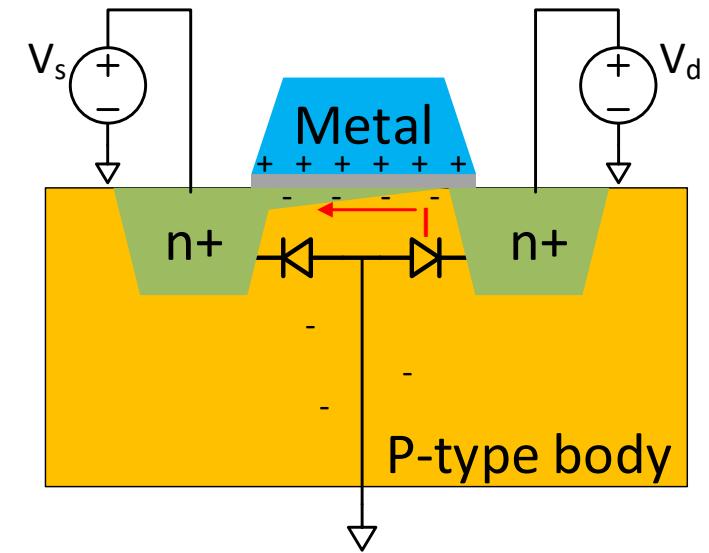
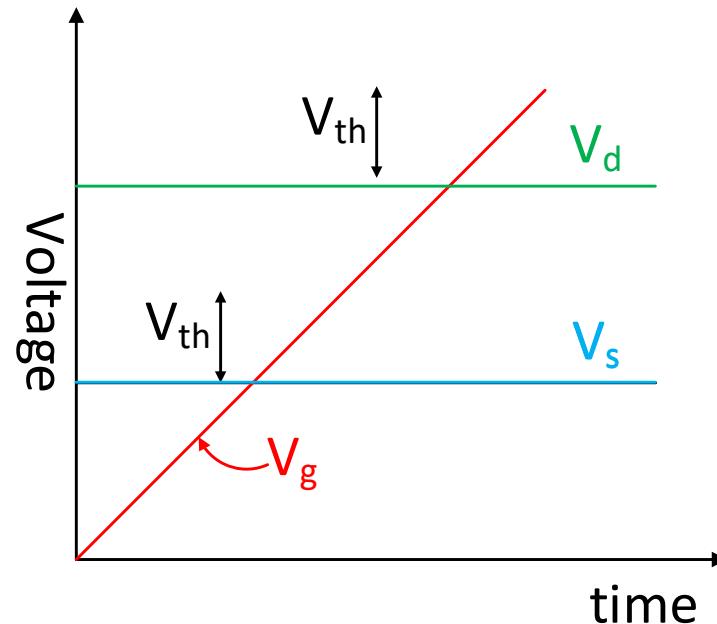
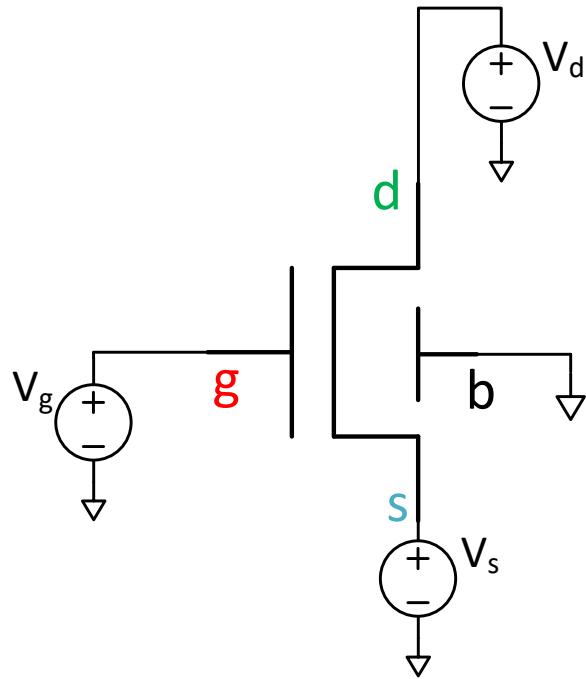


MOS Transistor – A Strictly Intuitive View



- Channel begins forming as $V_g - V_s > V_{th} \equiv V'_{gs} > 0$ (+gate overdrive)
- Channel still does not extend to L
- Channel not very thick

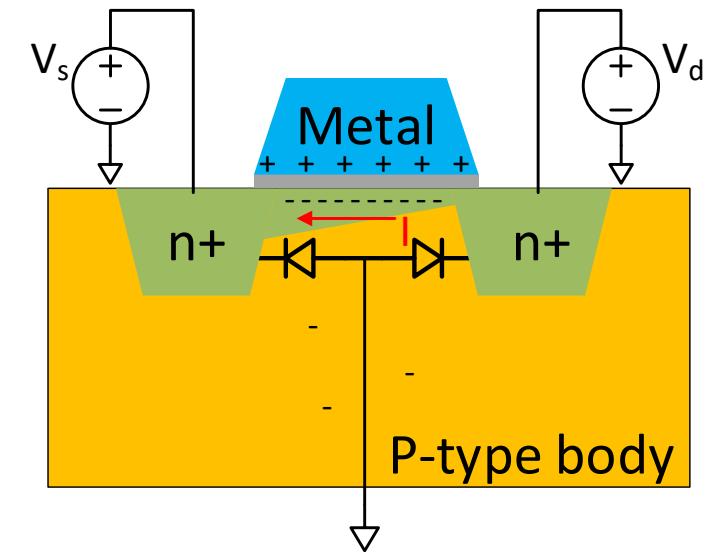
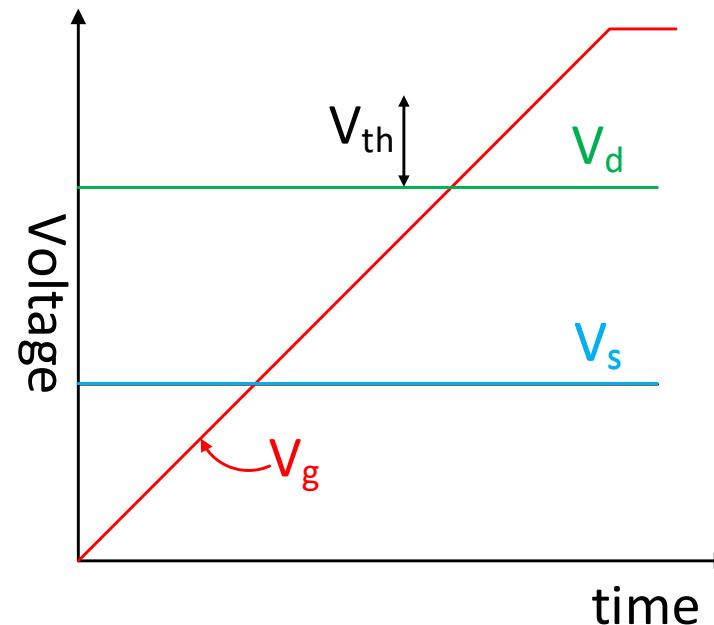
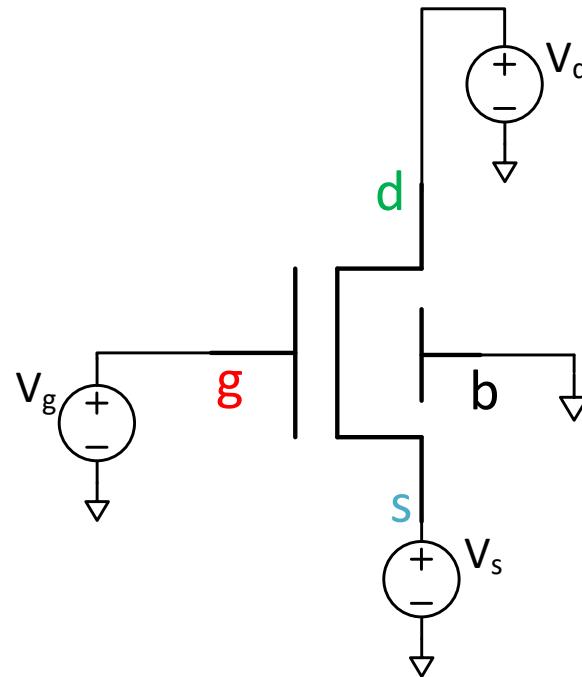
MOS Transistor – A Strictly Intuitive View



- Channel begins to form as $V_g - V_s > V_{th}$
- Channel still does not extend to L
- Channel thickness increasing

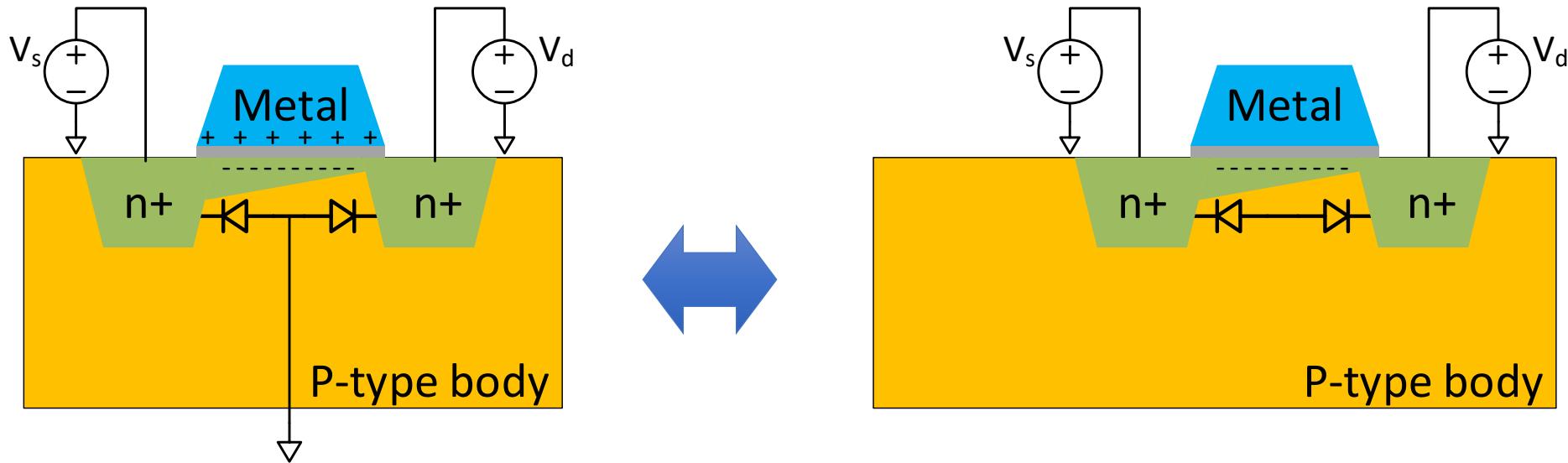
HERE

MOS Transistor – A Strictly Intuitive View

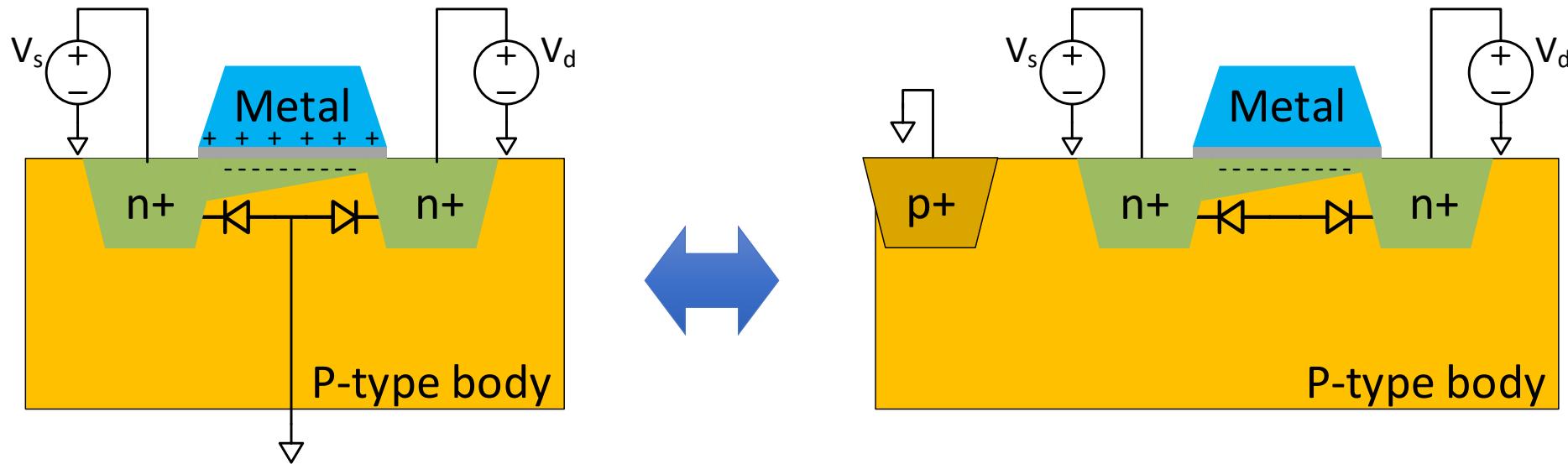


- Channel extends to L as $V_g - V_d > V_{th}$
- Channel thicker now $\rightarrow \downarrow$ resistance
- Thickness varies along channel!

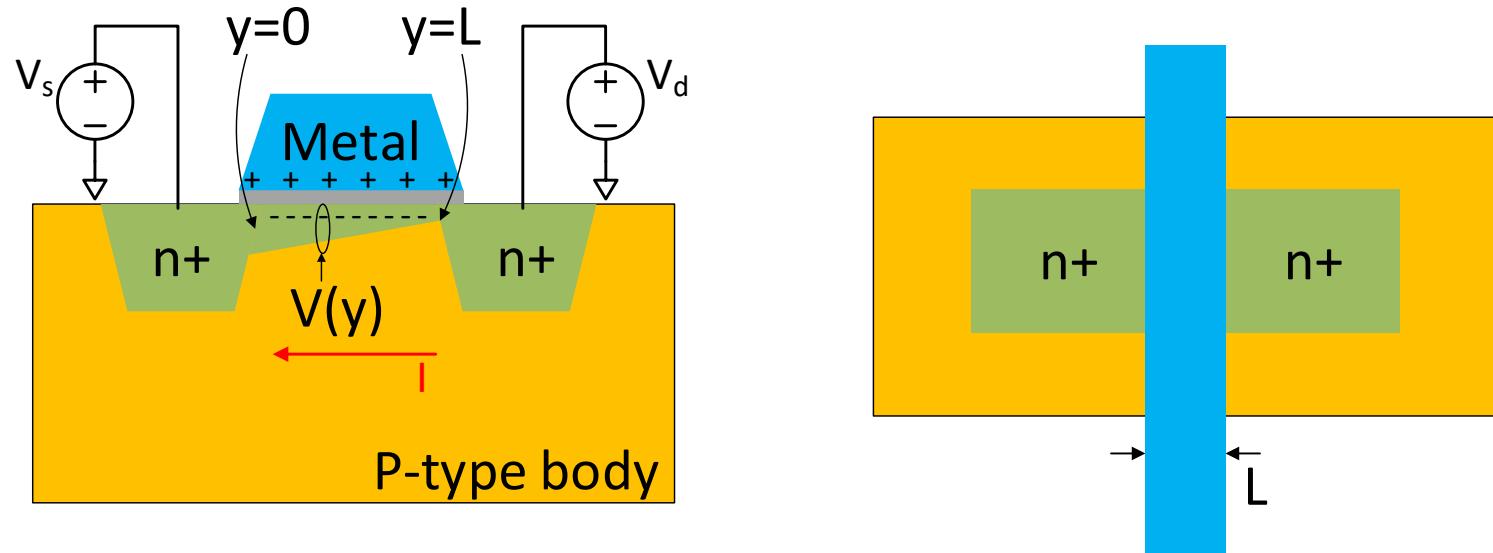
The Substrate Contact



The Substrate Contact



The Ideal Shockley MOSFET model



- Analyze the MOS device in the linear region: $V_{gs} - V_{th} = V_{gs}' > V_{ds}$
- Recall that channel is fully formed
- Steady-state → Current is the same at any point y along the channel

MOSFET Current Flow

$I =$

MOSFET Current Flow

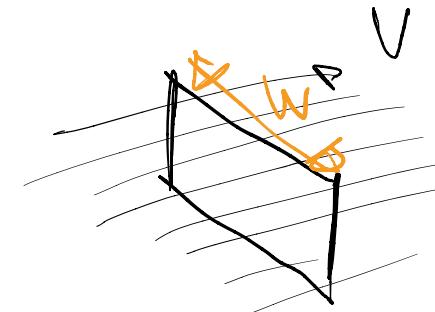
$$I = W$$

MOSFET Current Flow

$$I = W \cdot Q_d$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$



MOSFET Current Flow

$$\begin{aligned}I &= W \cdot Q_d \cdot v \\&= W \cdot C_{ox}\end{aligned}$$

MOSFET Current Flow

$$\begin{aligned}I &= W \cdot Q_d \cdot v \\&= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right)\end{aligned}$$

$$Q = C V$$

MOSFET Current Flow

$$\begin{aligned}I &= W \cdot Q_d \cdot v \\&= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y\end{aligned}$$

MOSFET Current Flow

$$\begin{aligned}I &= W \cdot Q_d \cdot v \\&= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y \\&= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu \frac{\partial V}{\partial y}\end{aligned}$$

MOSFET Current Flow

$$\begin{aligned}I &= W \cdot Q_d \cdot v \\&= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y \\&= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu \frac{\partial V}{\partial y} \\I dy &= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu dV\end{aligned}$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$

$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y$$

$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu \frac{\partial V}{\partial y}$$

$$I dy = W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu dV$$

Integrating both sides gives ...

$$\int_0^L I dy =$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$

$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y$$

$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu \frac{\partial V}{\partial y}$$

$$I dy = W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu dV$$

Integrating both sides gives ...

$$\int_0^L I dy = \int_0^{V_{ds}} W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu dV$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$

$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y$$

$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu \frac{\partial V}{\partial y}$$

$$I dy = W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu dV$$

Integrating both sides gives ...

$$\int_0^L I dy = \int_0^{V_{ds}} W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu dV$$

$$IL = \mu C_{ox} W \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$

$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y$$

$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu \frac{\partial V}{\partial y}$$

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$$IL = \mu C_{ox} W \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

$$I = \mu C_{ox} \frac{W}{L} \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$

$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y$$

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Integrating both sides gives ...

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$$IL = \mu C_{ox} W \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

$$I = \mu C_{ox} \frac{W}{L} \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right], \quad \text{Letting } \beta = \mu C_{ox} \frac{W}{L}$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$

$$= W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu E_y$$

$$= W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu \frac{\partial V}{\partial y}$$

$$I dy = W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu dV$$

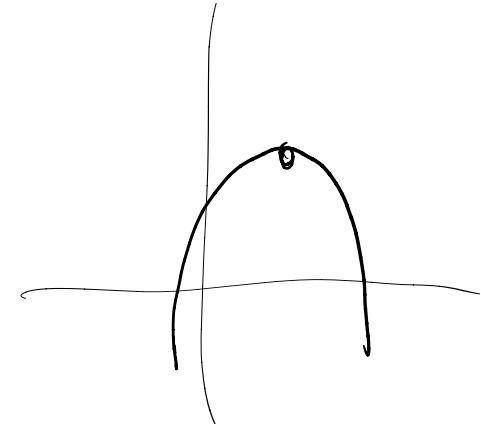
Integrating both sides gives ...

$$\int_0^L I dy = \int_0^{V_{ds}} W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu dV$$

$$IL = \mu C_{ox} W \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

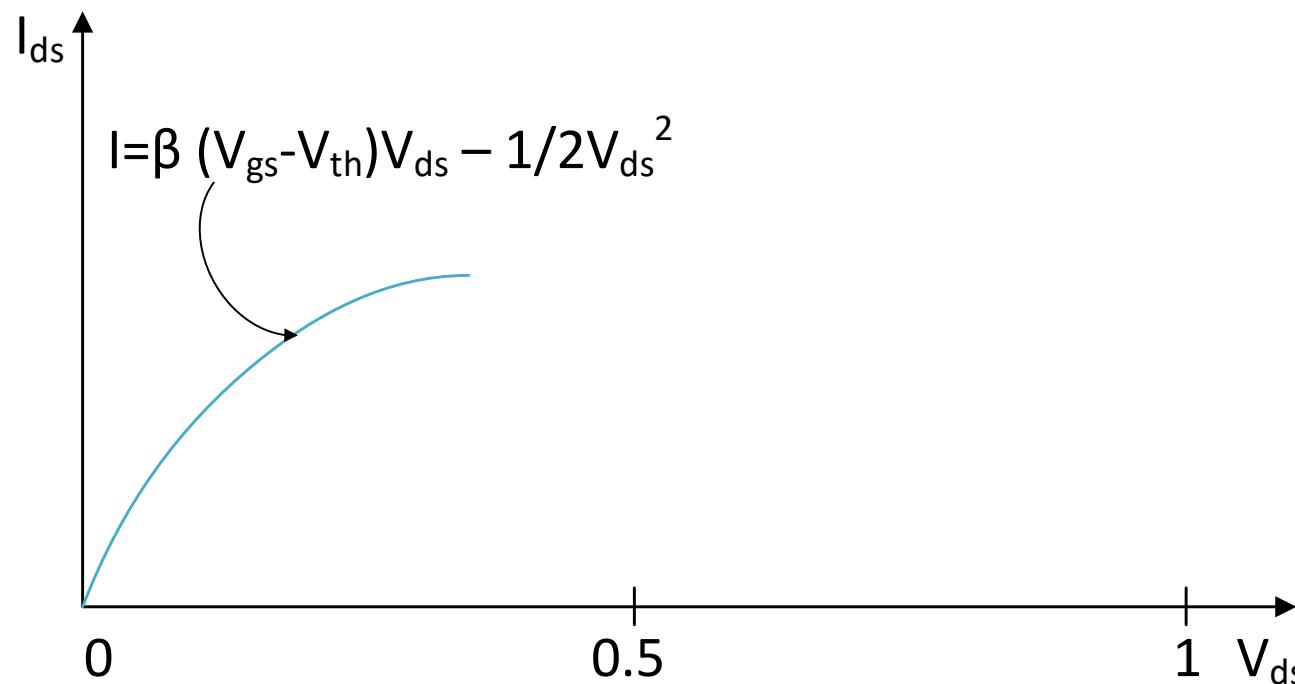
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$$I = \beta \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$



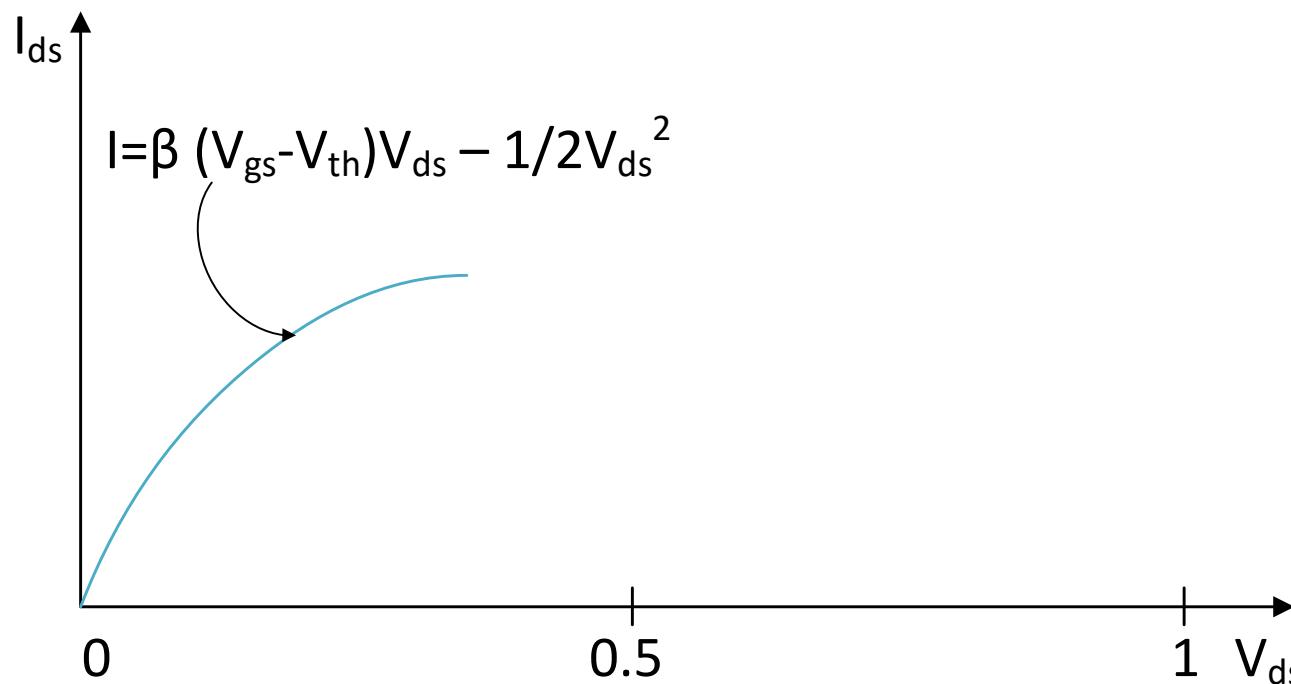
MOSFET Operation: Triode region

- Equation corresponds to device in Linear (or Triode) region
 - Channel is continuous from source to drain
- Question: Plot I_{ds} vs. V_{ds} for a fixed V_{gs}



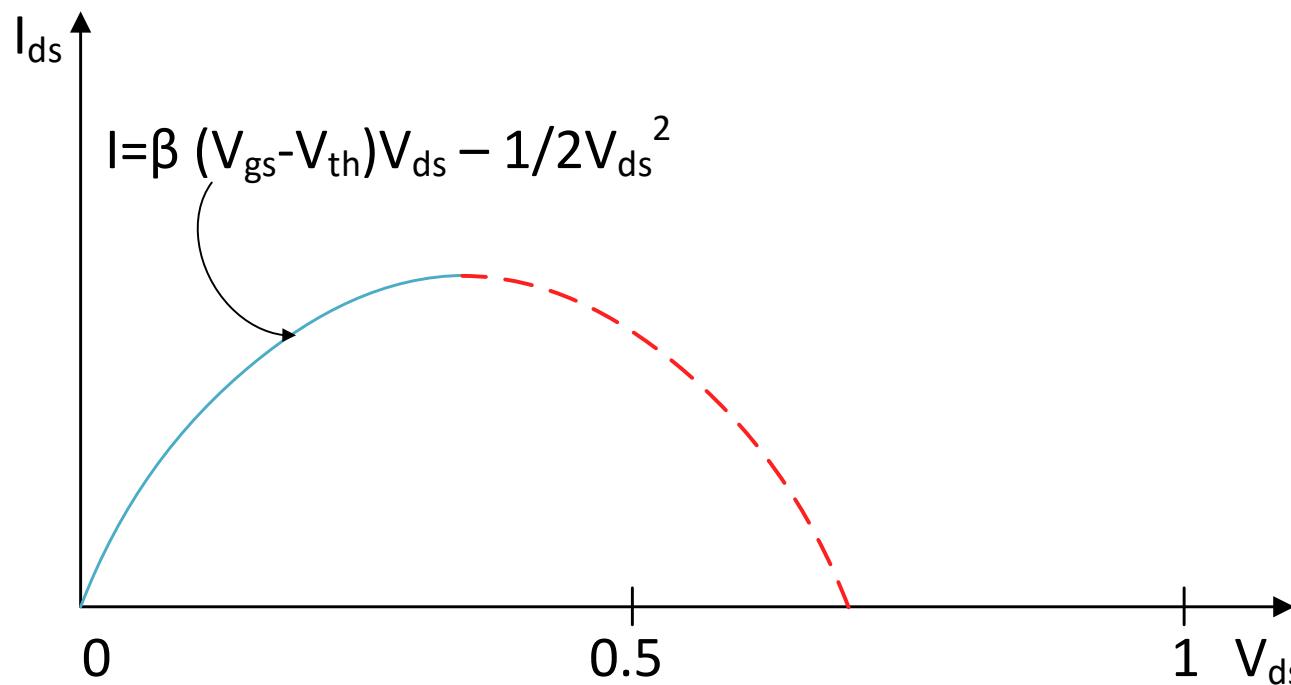
MOSFET Operation: Triode region

- Equation corresponds to device in Linear (or Triode) region
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- Question: Plot I_{ds} vs. V_{ds} for a fixed V_{gs}
- What happens for $V_{ds} > V_{gs} - V_{th}$?



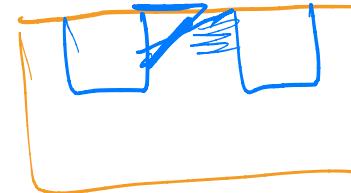
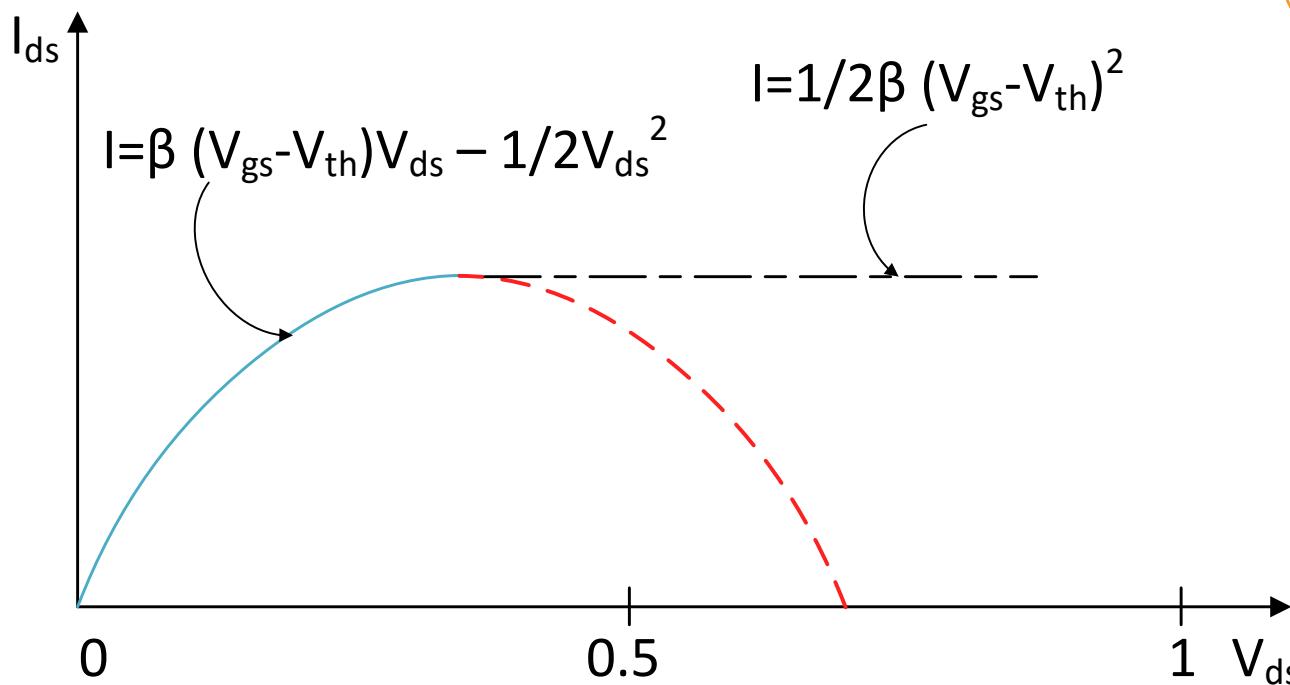
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MOSFET Operation: Triode region

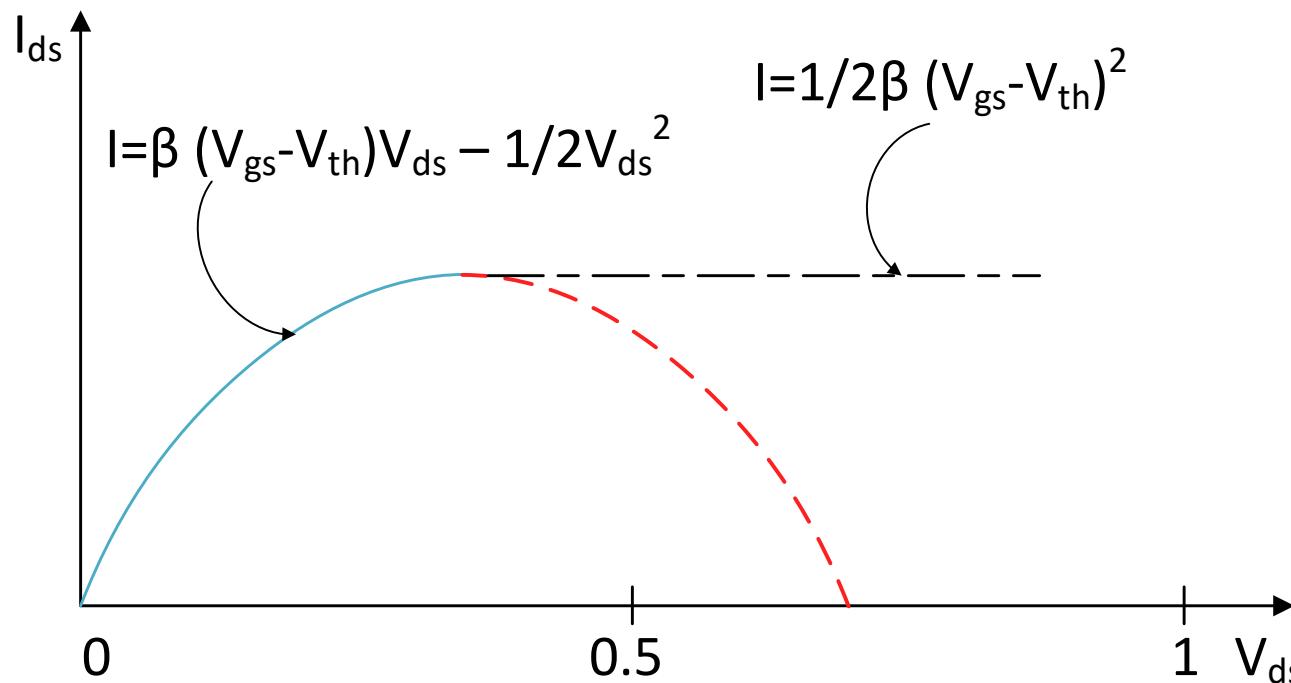
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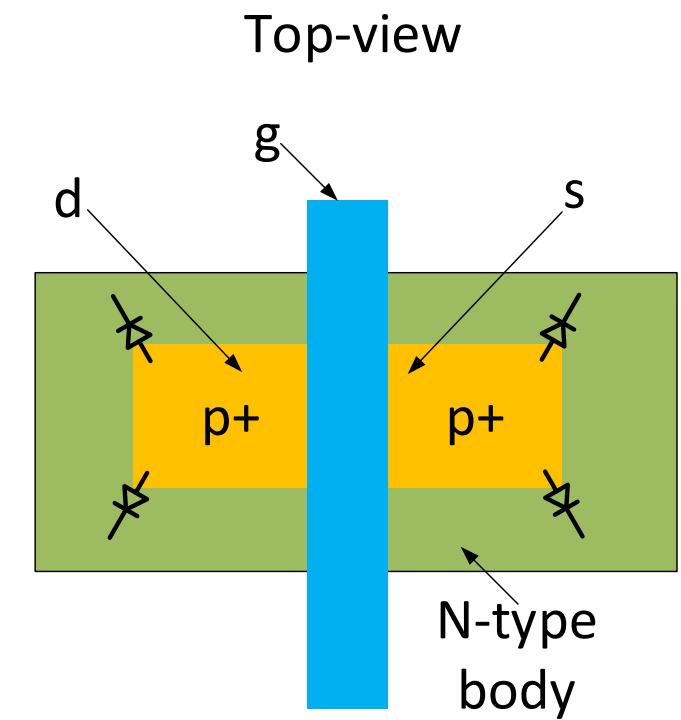
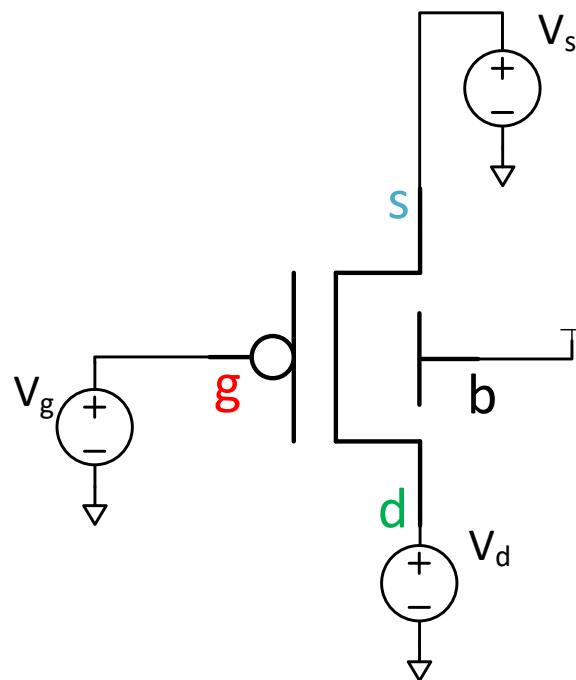
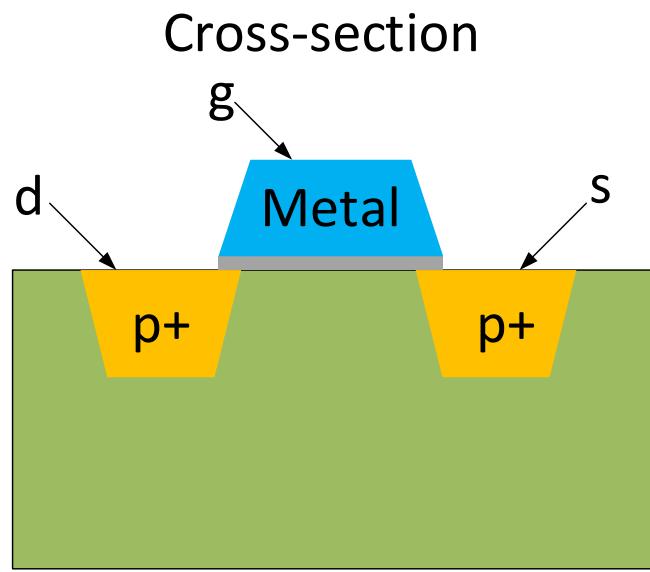
$V_{gs} < V_{th}$
cutoff
 $V_{gs} > V_{th}$
 $V_{ds} < V_{gs} - V_{th}$
Linear
Triode
 $V_{ds} \geq V_{gs} - V_{th}$
Saturation

MOSFET Operation: Triode region

- Equation corresponds to device in Linear (or Triode) region
 - Channel is continuous from source to drain
- Question: Plot I_{ds} vs. V_{ds} for a fixed V_{gs}
- What happens for $V_{ds} > V_{gs} - V_{th}$?
 - Device enters saturation
 - The channel “pinches-off” (More on this shortly)

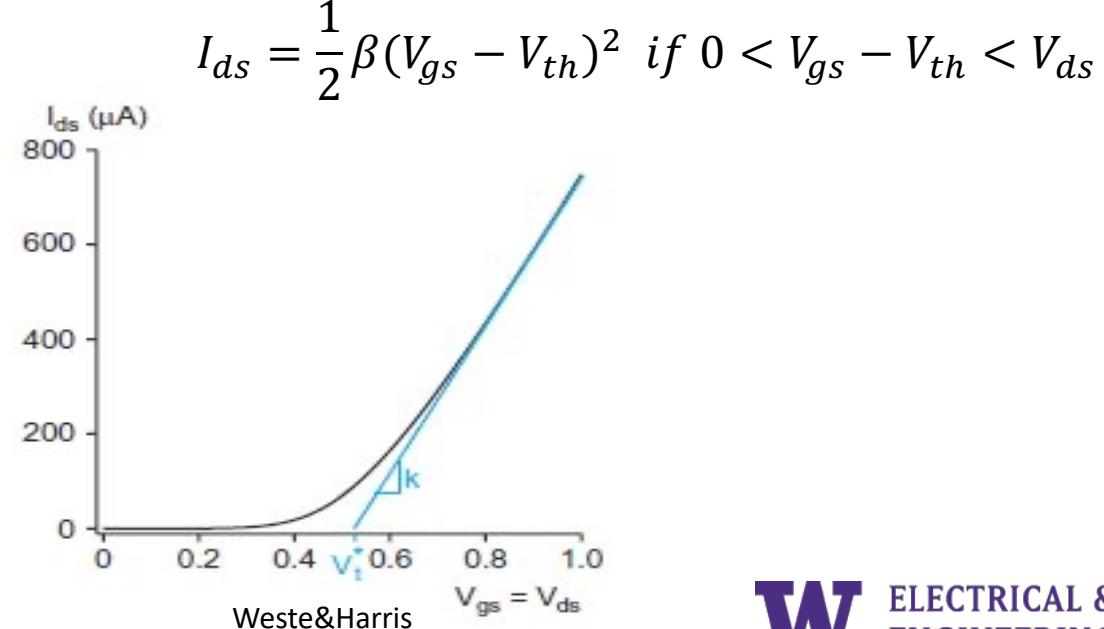
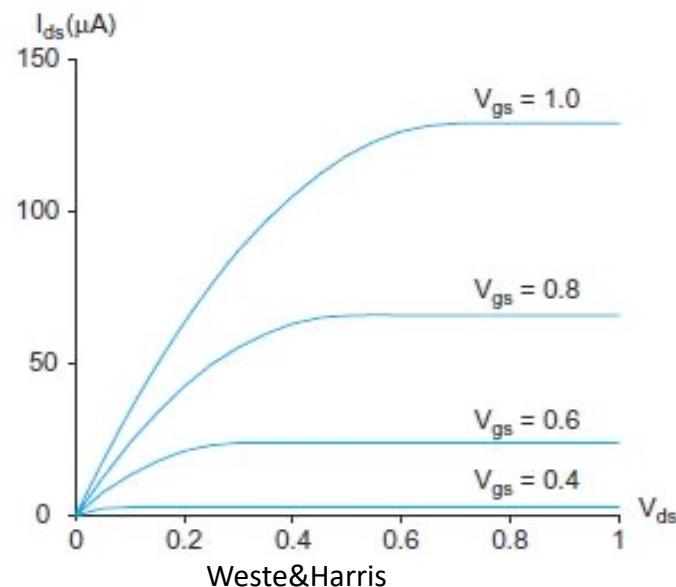


Break-out session: Figure out the PMOS...

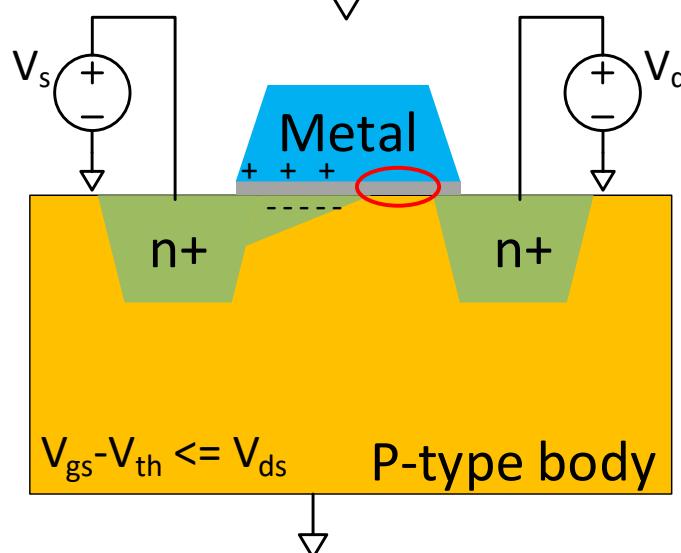
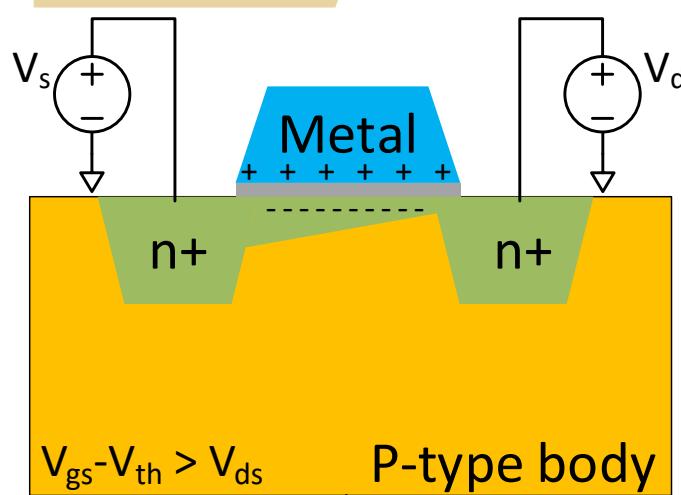


MOSFET Operation: Saturation

- Saturation condition: $V_{gs} - V_{th} \leq V_{ds}$
 - $V_{gs} - V_{th}$ (also denoted as V_{gs}') , the gate overdrive is less than the on-voltage
- Current “levels-off”
 - I_d no longer a function of V_{ds} (to the first order. More on this later)
 - Depends only on V_{gs} and V_{th}

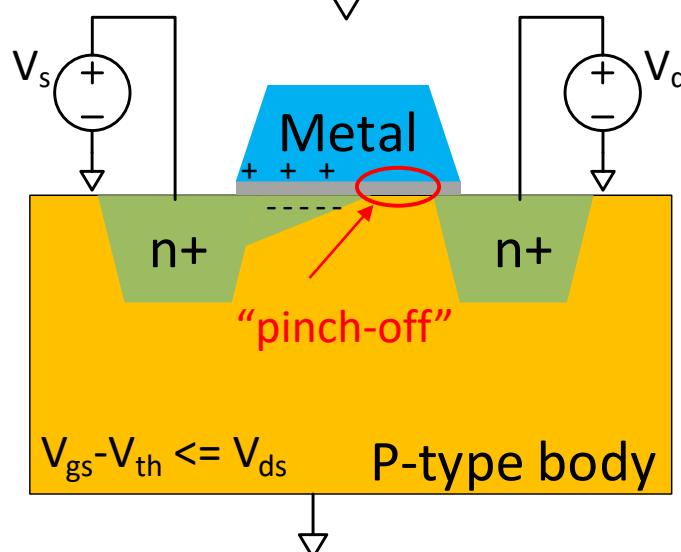
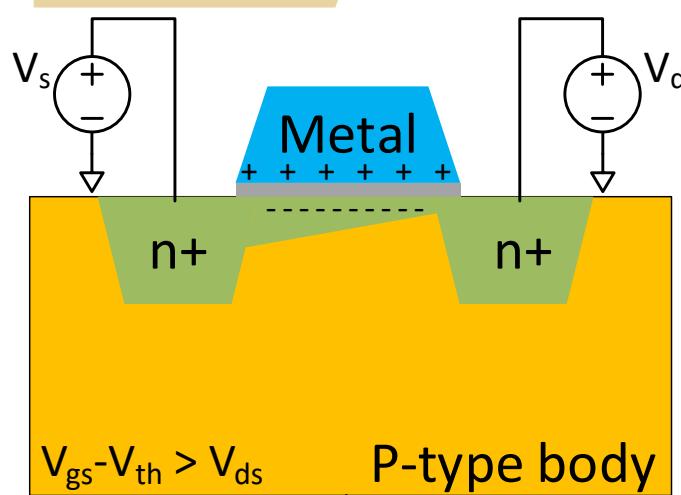


Channel Length Modulation



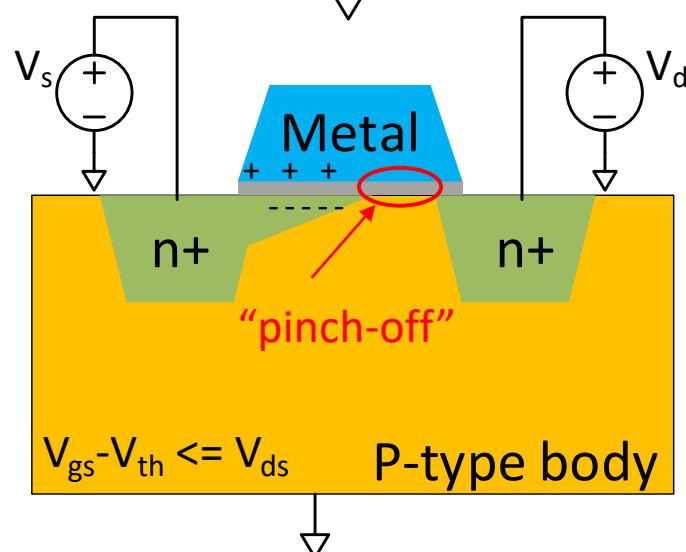
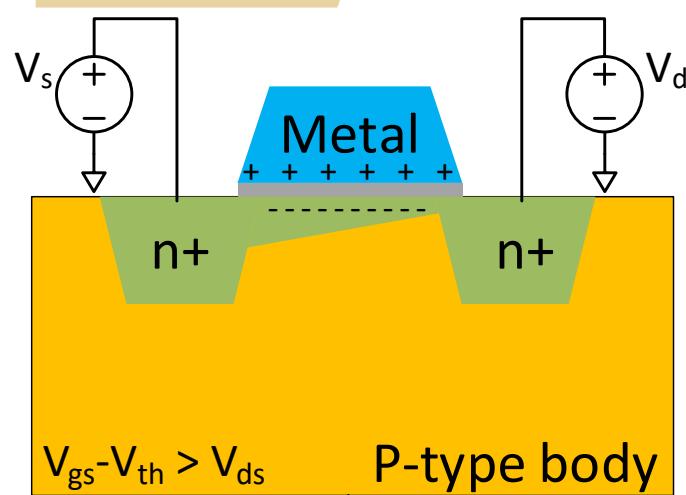
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Channel Length Modulation



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Channel Length Modulation

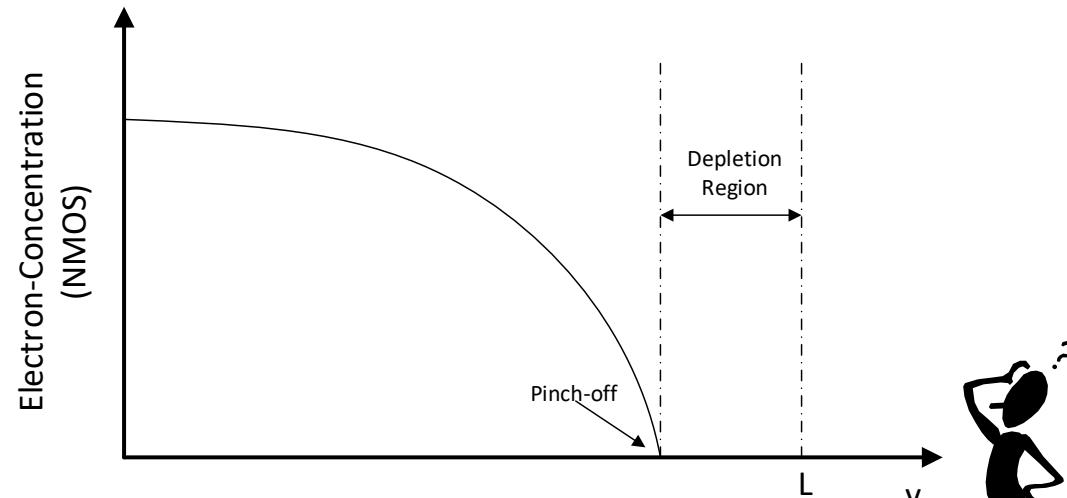
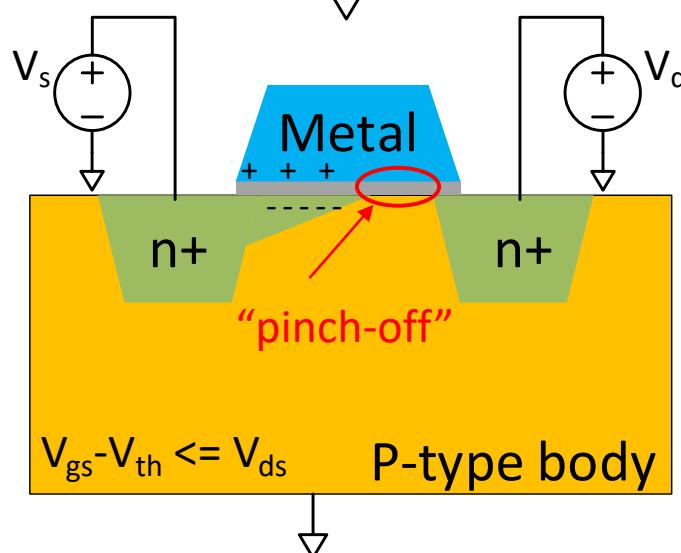
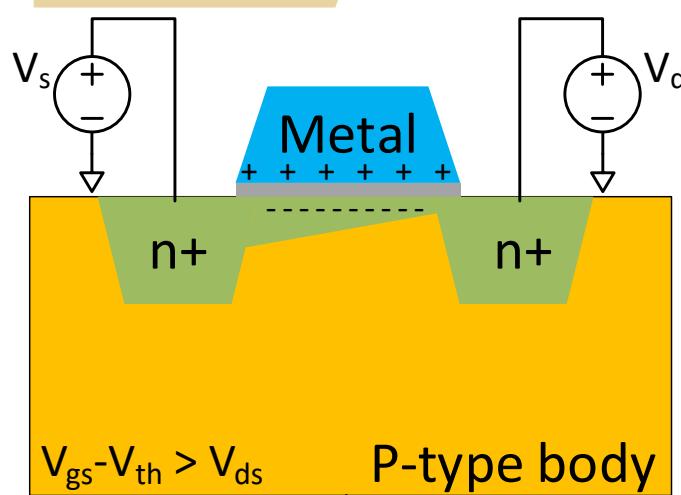


But if there is no channel, how do e^- get over to the drain?



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Channel Length Modulation

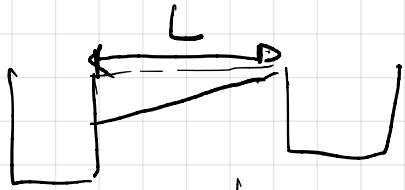


But if there is no channel, how do e⁻ get over to the drain?

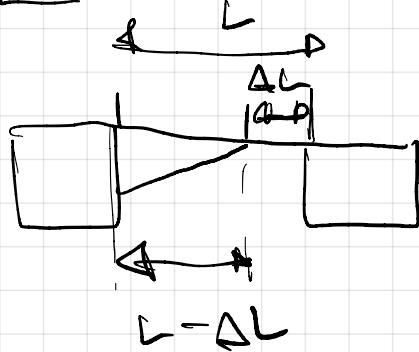
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$$I = I_s = \frac{1}{2} \beta (V_{GS} - V_{th})^2$$

$$\beta = \mu C_o \times \frac{W}{L}$$



$$\frac{1}{L} \rightarrow \frac{1}{L - \Delta L}$$



$$f(\Delta L) = \frac{1}{L - \Delta L}$$

$$f(0) = \frac{1}{L}$$

$$\frac{df}{d\Delta L} = \frac{d}{d\Delta L} (L - \Delta L)^{-1}$$

$$= \frac{-1}{(L - \Delta L)^2} \cdot (-1) = \frac{1}{(L - \Delta L)^2}$$

$$\left. \frac{df}{d\Delta L} \right|_{\Delta L \approx 0} = \frac{1}{L^2}$$

$$\frac{1}{L - \Delta L} \approx \frac{1}{L} + \frac{1}{L^2} \Delta L + O(\Delta L^2)$$

$$f(x) = f(0) + f'(0)x + \frac{1}{2} f''(0)x^2 + \frac{1}{6} f'''(0)x^3$$

Taylor series

$\frac{1}{6}$

$$\frac{1}{L - \Delta L} \approx \frac{1}{L} + \frac{\Delta L}{L^2}$$

$$\begin{aligned}
 I &= \frac{1}{N} \beta (V_{GS} - V_{th})^2 \\
 &= \frac{1}{N} \mu_N C_{ox} \left(\frac{1}{L - \Delta L} \right) (V_{GS} - V_{th})^2 \\
 &= \frac{1}{N} \mu_N C_{ox} (V_{GS} - V_{th})^2 \left[\frac{1}{L} + \frac{\Delta L}{L^2} \right] \\
 &= \frac{1}{N} \mu_N C_{ox} (V_{GS} - V_{th})^2 (1 + \Delta L/L) \\
 &= \frac{1}{N} \beta (V_{GS} - V_{th})^2 (1 + \Delta L/L)
 \end{aligned}$$

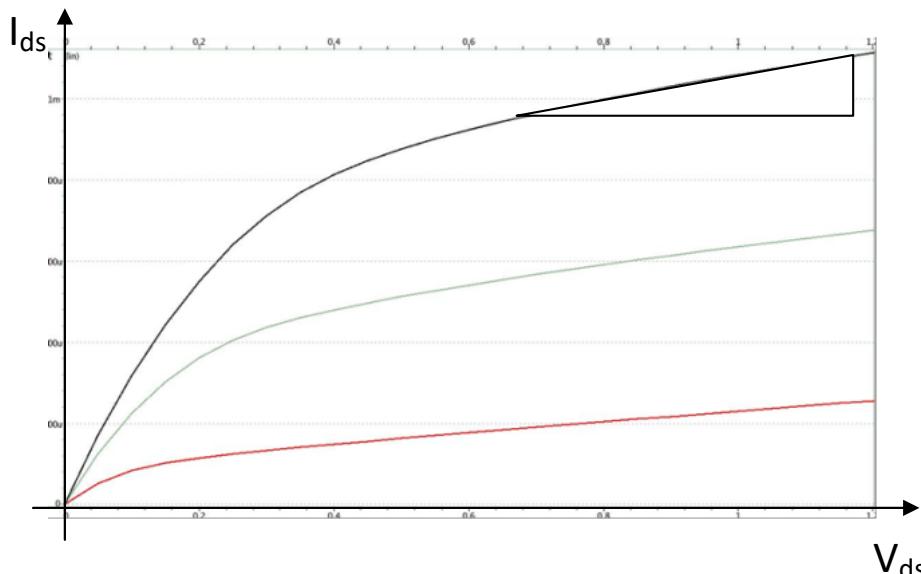


$$\frac{\Delta L}{L} \approx \gamma V_{DS}$$

$$I = \frac{1}{N} \beta (V_{GS} - V_{th})^2 (1 + \gamma V_{DS})$$

Channel Length Modulation

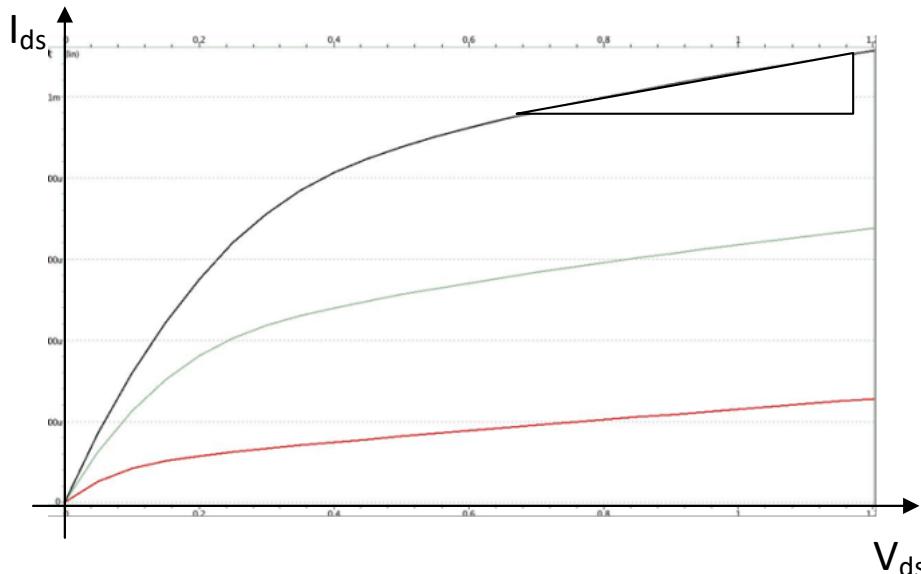
- Simplifying assumption:
 - Fractional change in channel length is proportional to V_{DS}
 - If ΔL is the depletion width, Let $\frac{\Delta L}{L} = \lambda V_{ds}$



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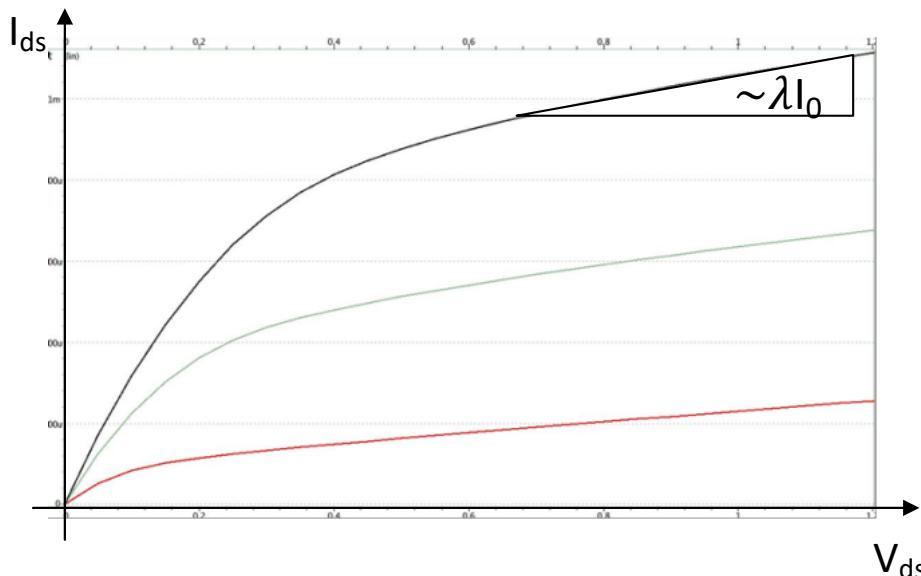
What is the gradient of this line?



Channel Length Modulation

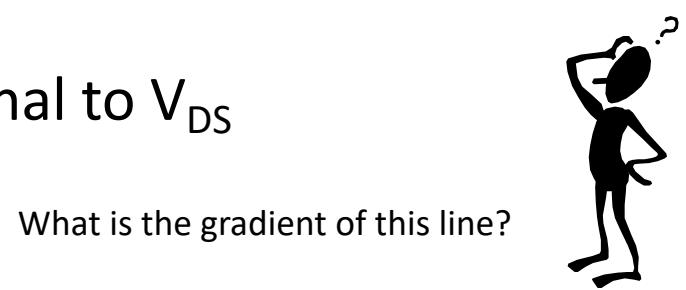
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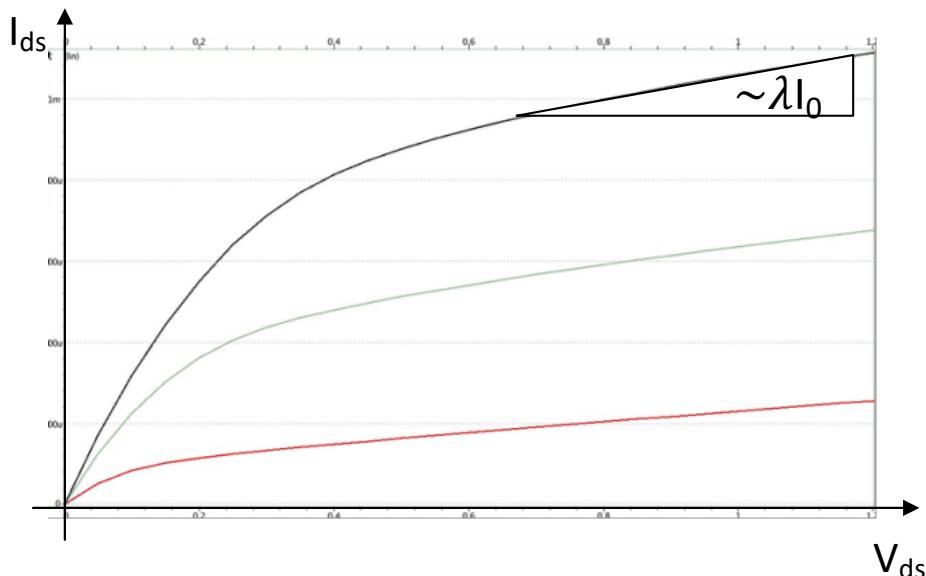


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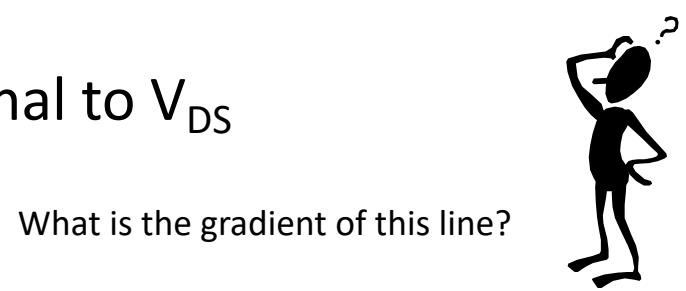


$$I_{ds} = \frac{1}{2} \mu C_{ox} \frac{W}{(L - \Delta L)} (V_{gs} - V_{th})^2$$



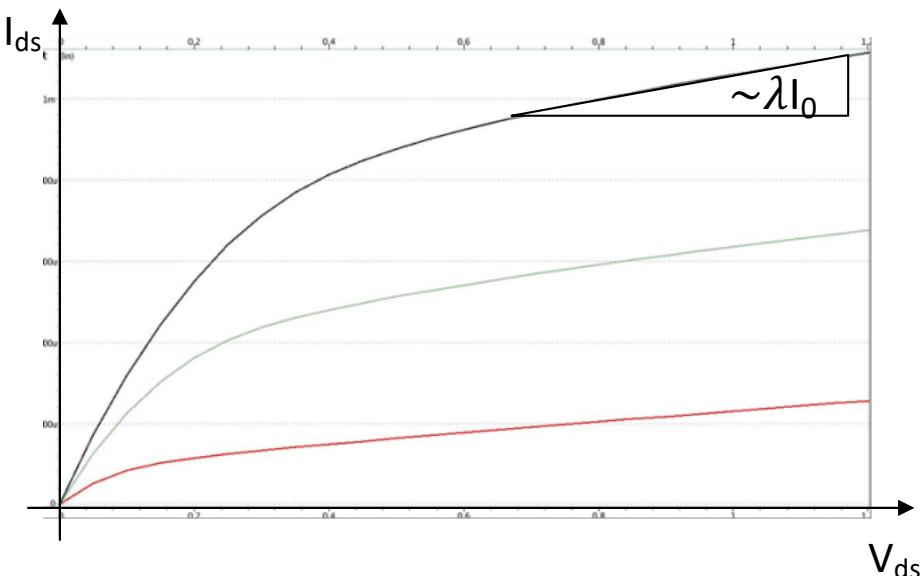
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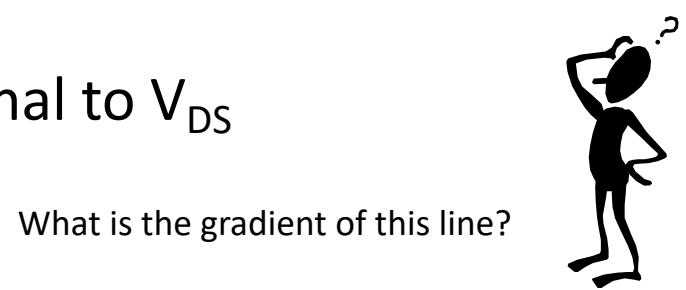
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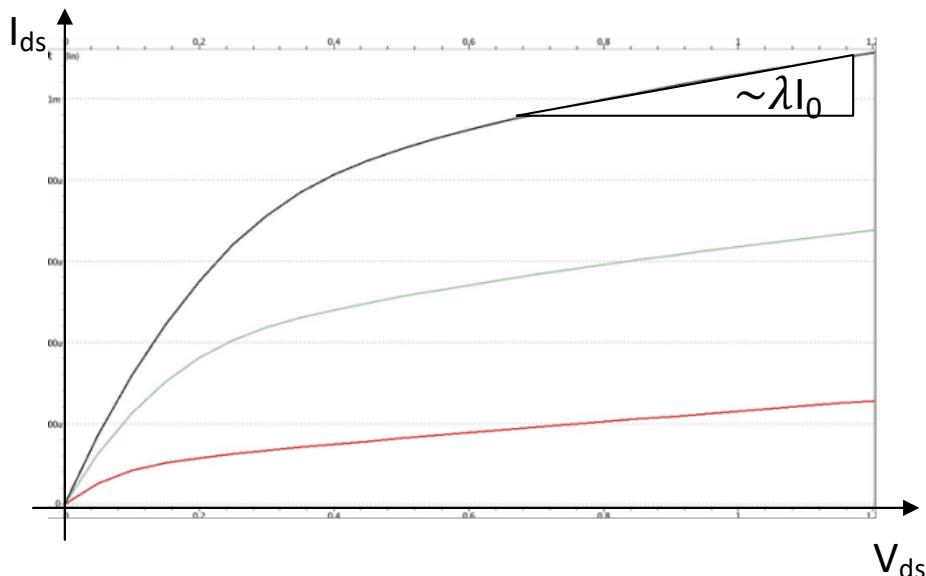


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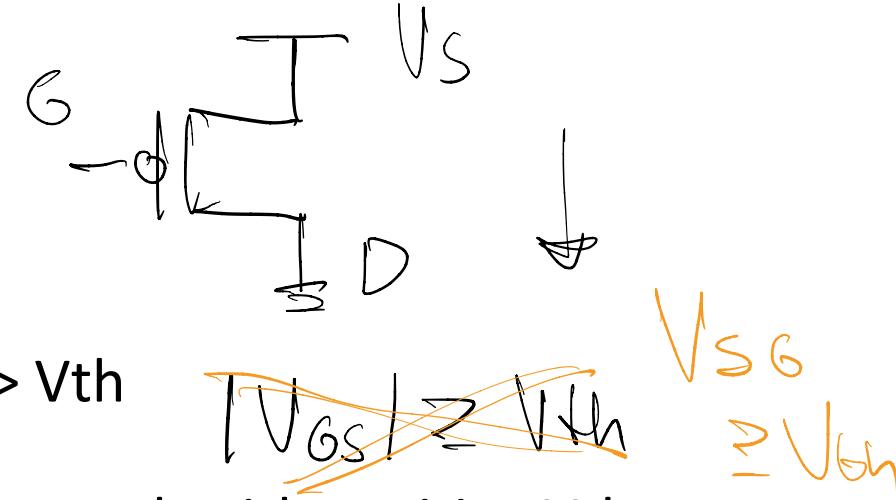


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PMOS Operation

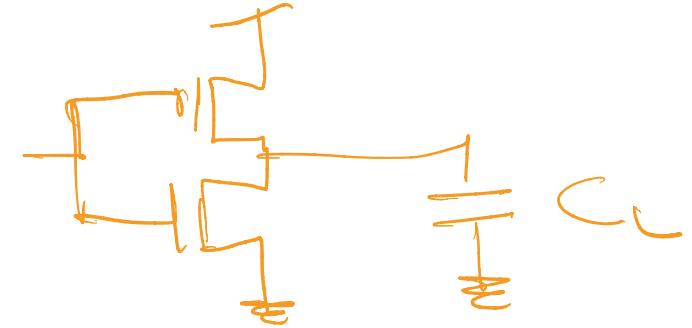
- Essentially a dual of the NMOS device operation
- For conduction: $V_g - V_s < -V_{th} \rightarrow V_s - V_g > V_{th} \rightarrow V_{sg} > V_{th}$
 - Gate overdrive continues to have to exceed V_{th}
- A lot more convenient to work with V_{sg} , V_{sd} and always work with positive V_{th} values (convention adopted in this class)
- Exercise: Derive the current equation of the PMOS device
- Note: PMOS carrier μ_p is lower than NMOS μ_n $\rightarrow \downarrow$ current drive for the same gate overdrive.



V_{sg} , V_{sd} , V_{th} relationship	PMOS operating region
$V_{sg} < V_{th}$	Cutoff (Not conducting)
$0 < V_{sg} - V_{th} < V_{sd}$	Saturation
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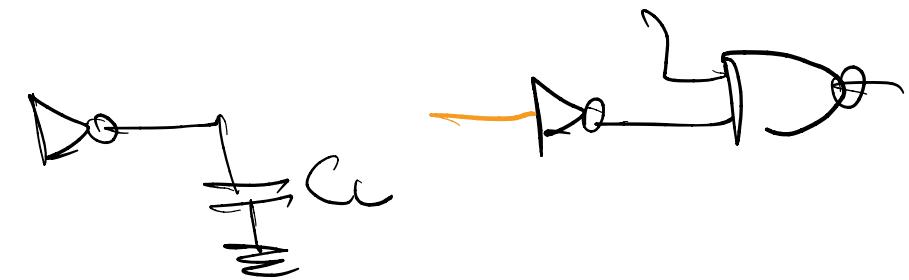


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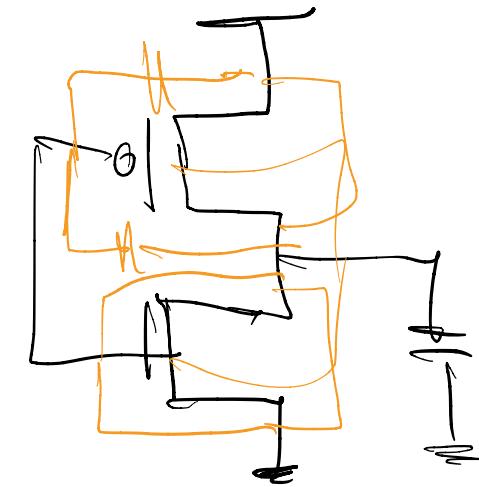
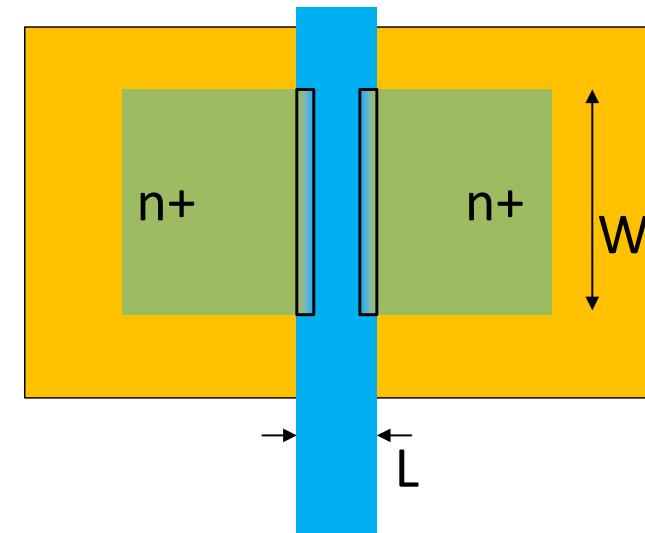
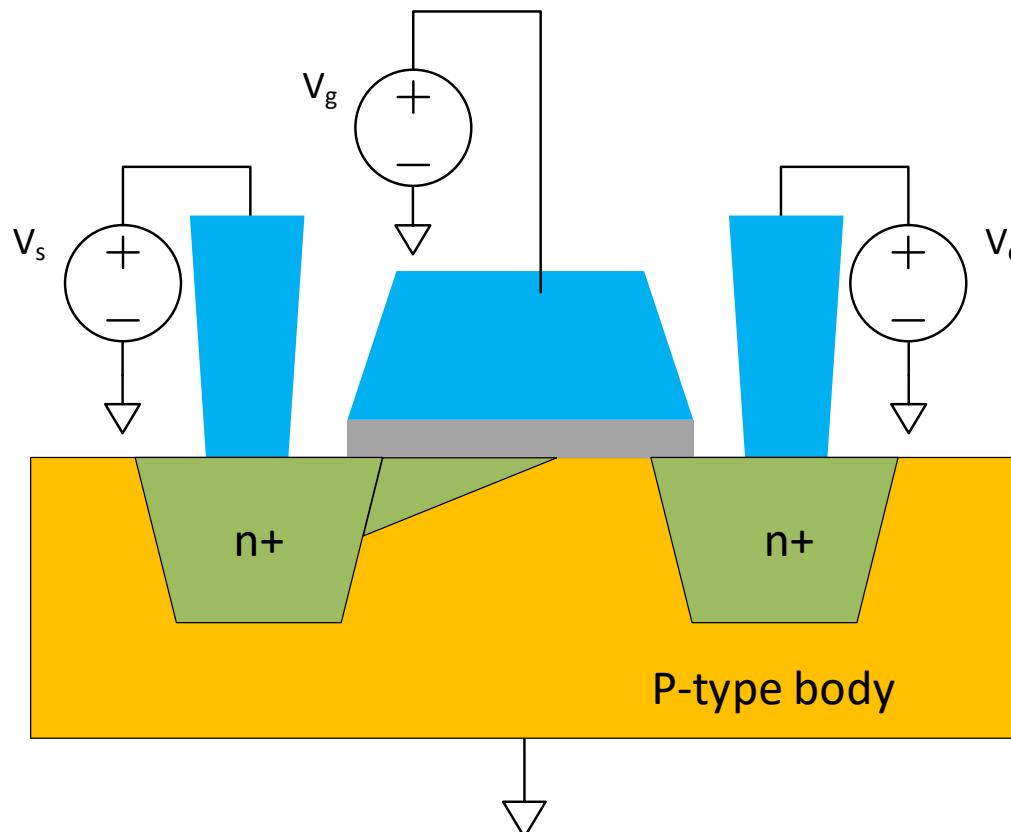
How can I fix that if I want equal drive strength?



MOSFET Gate Capacitance

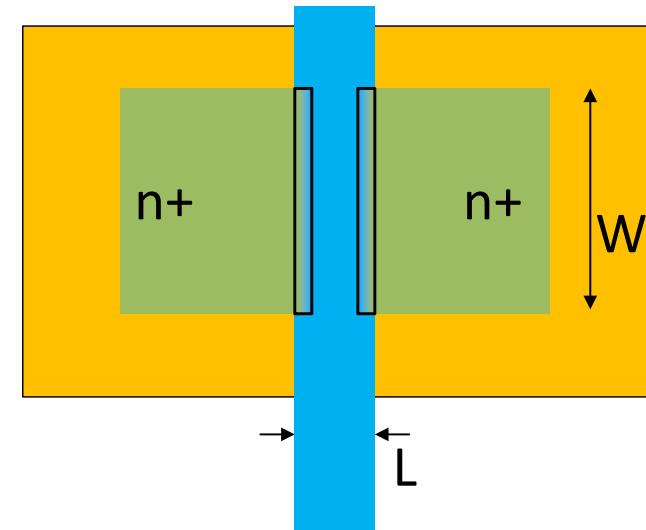
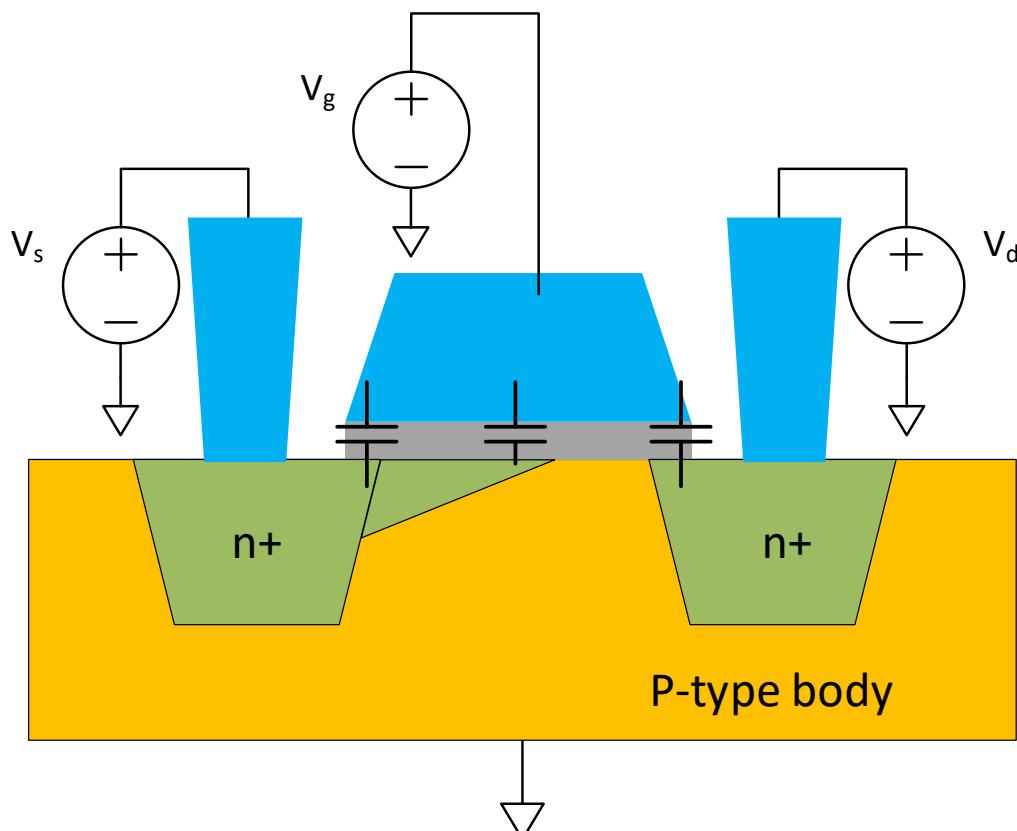


- Zeroth order, $\text{Cap} = W * L * C_{\text{ox}}$
 - Overlap capacitance (Gate-source, Gate-drain)
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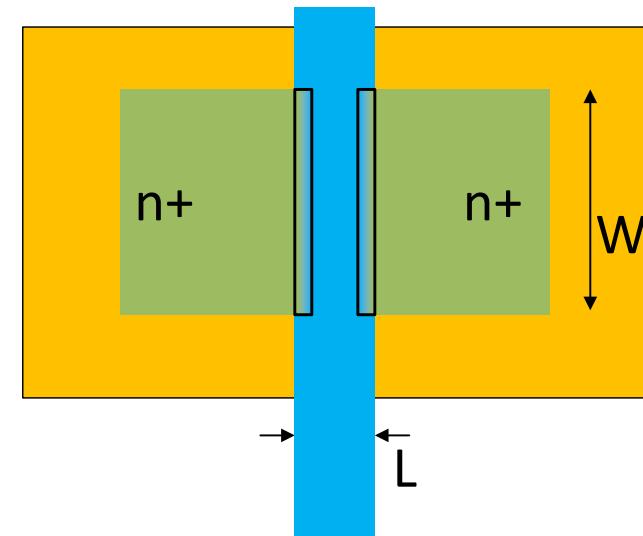
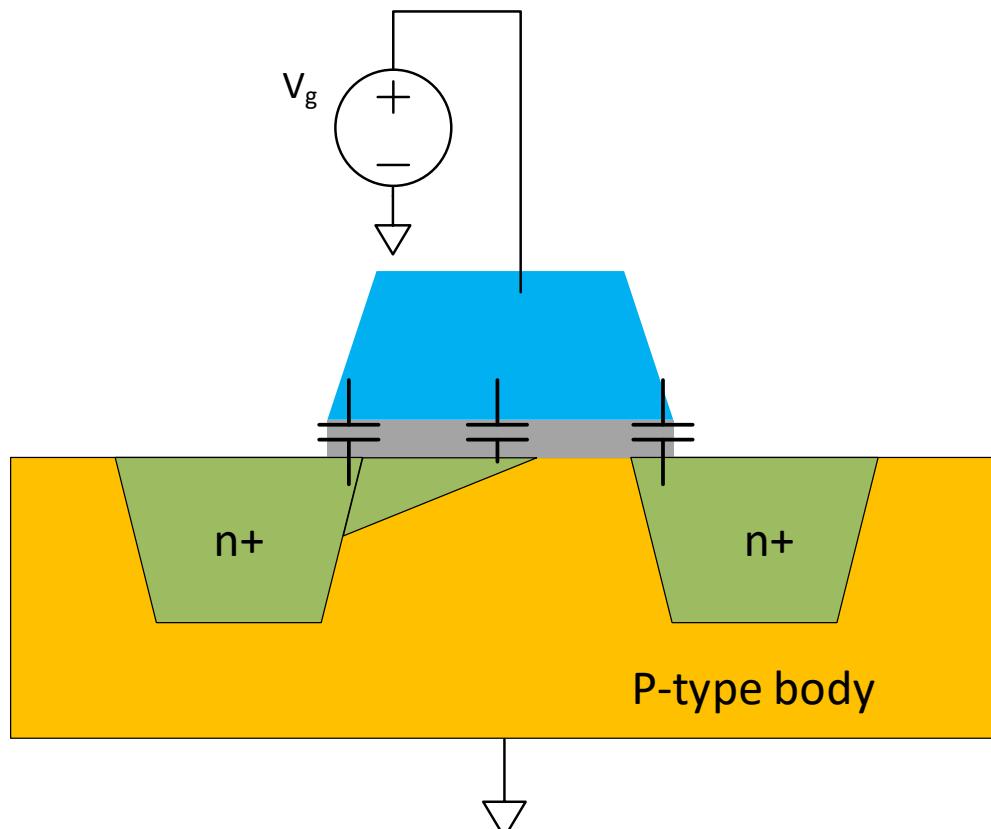
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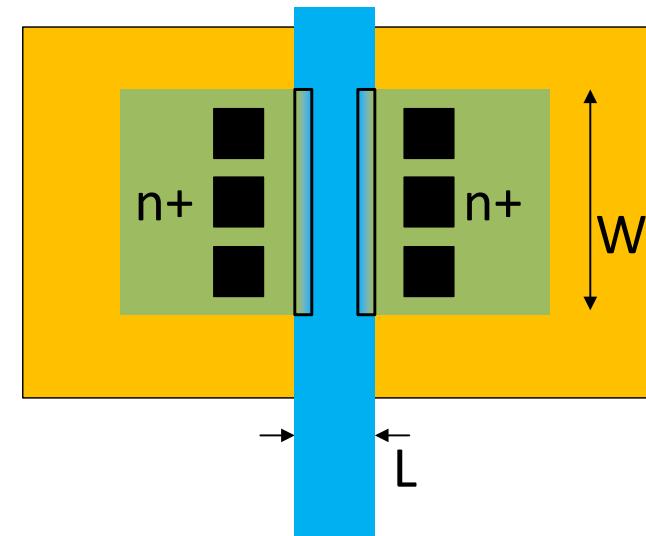
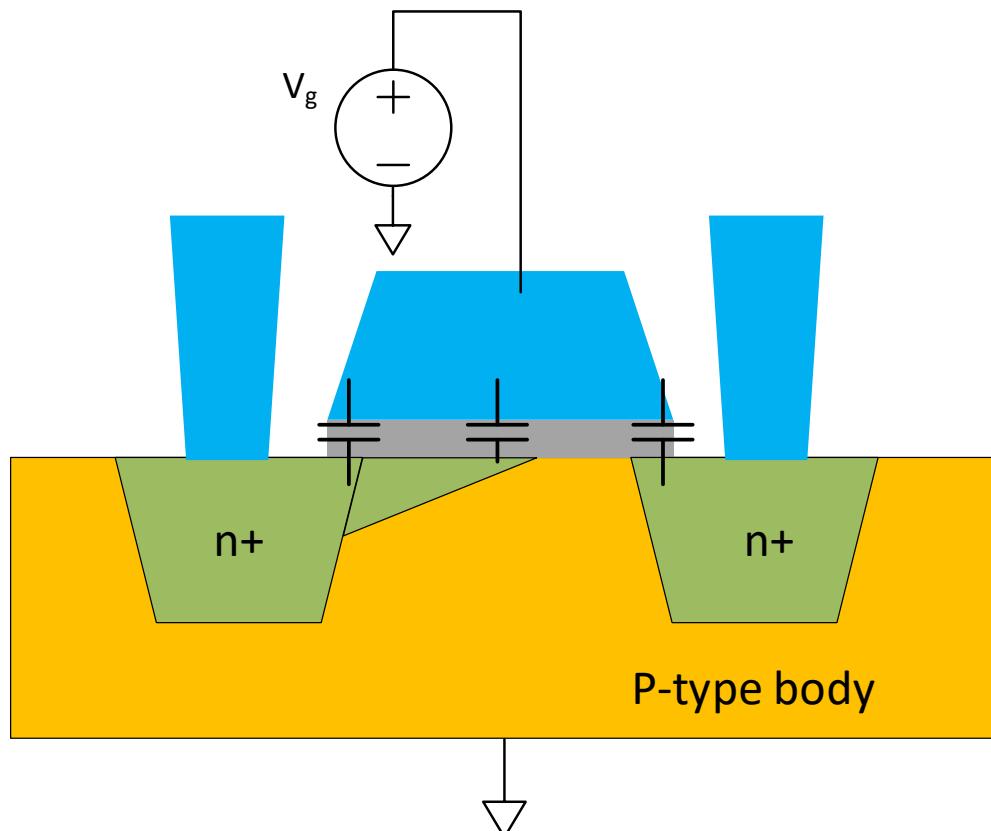
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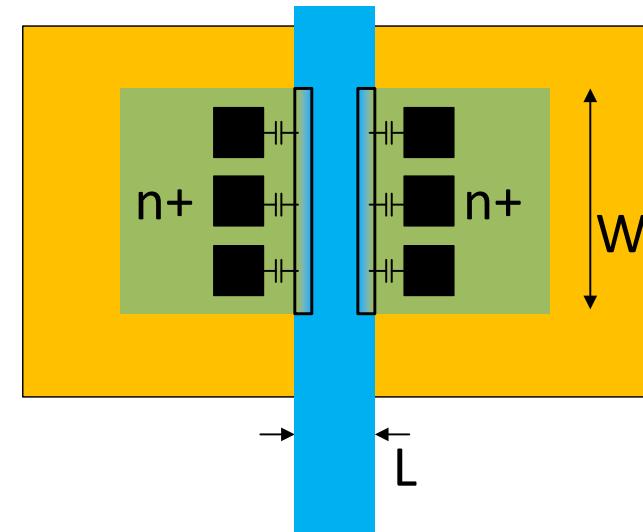
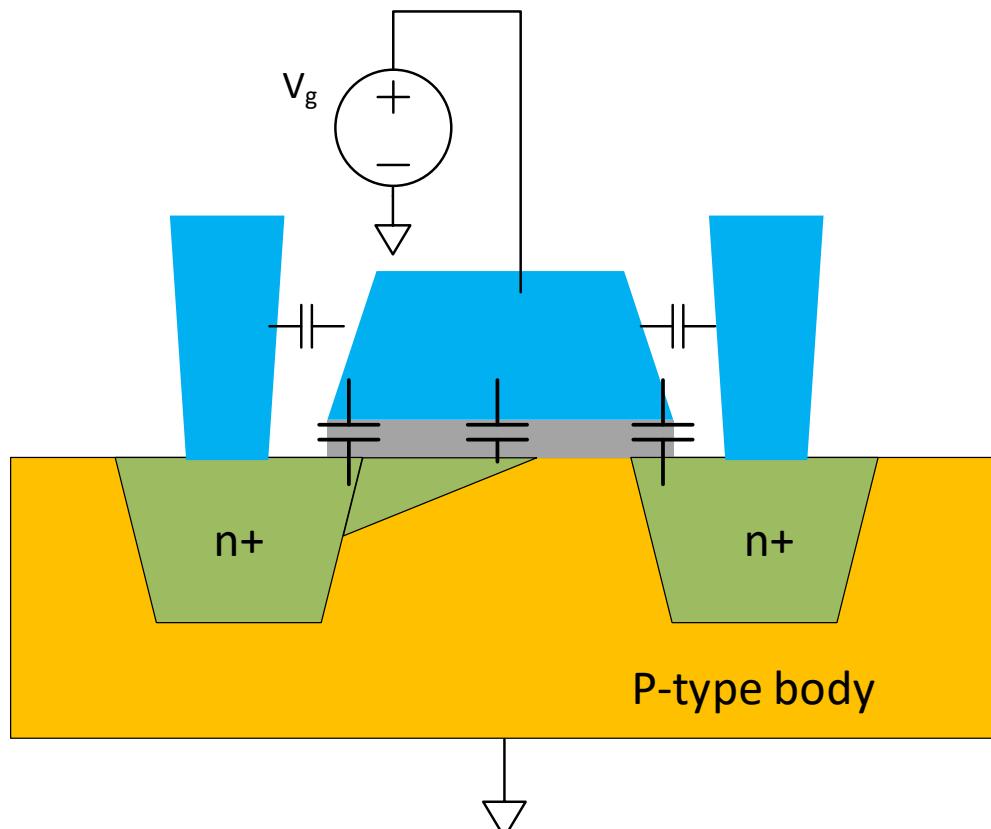
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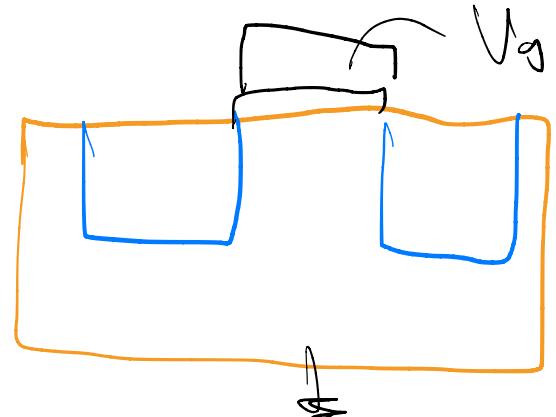
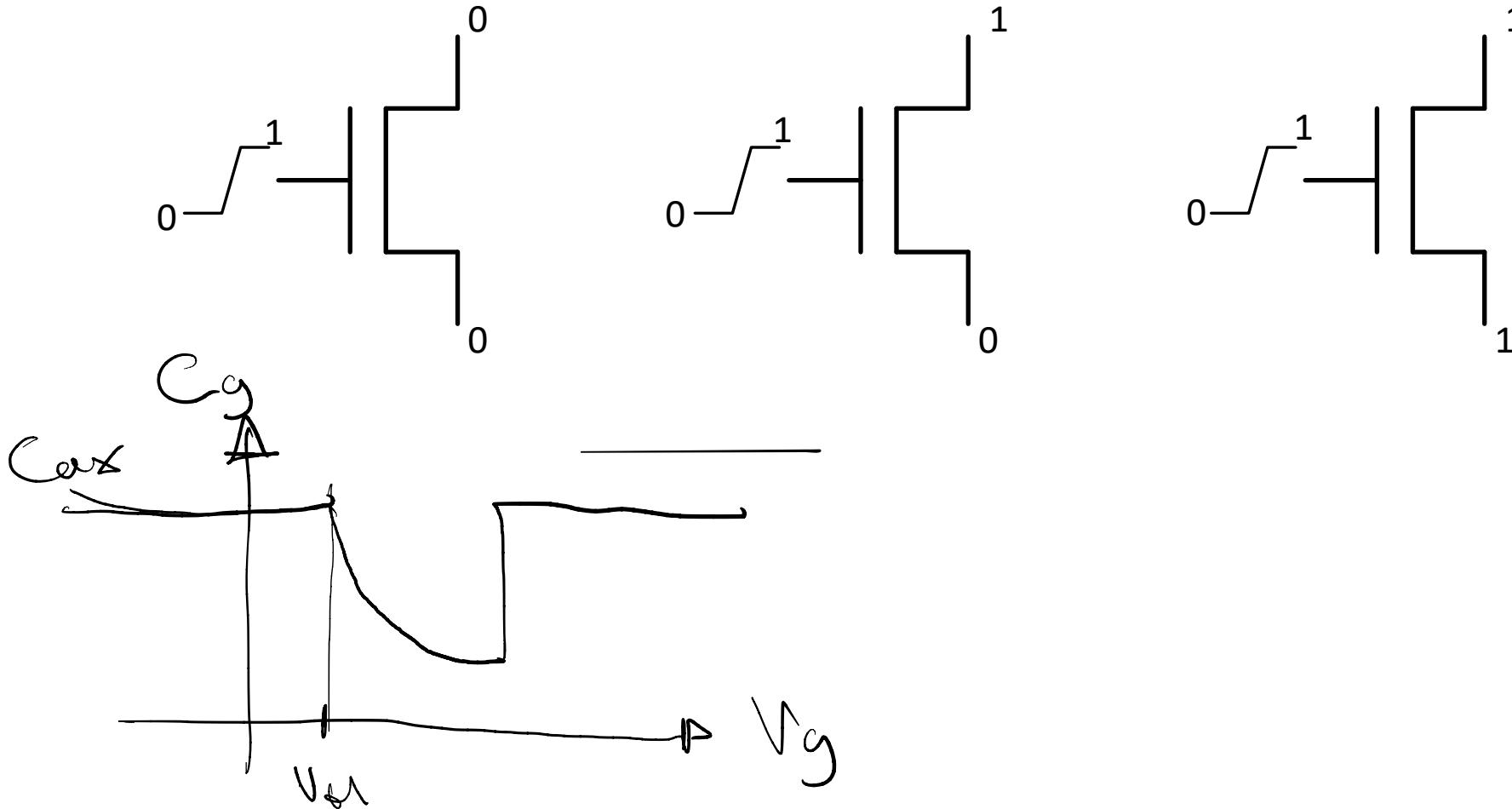
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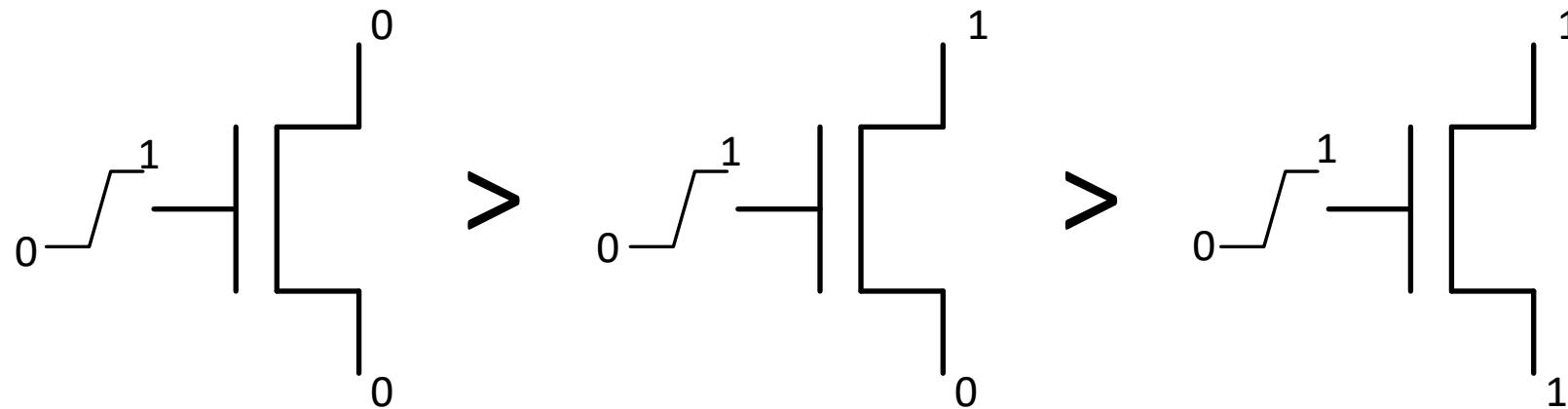
MOSFET Gate Capacitance

- Cap depends on fet state: What is the order below?



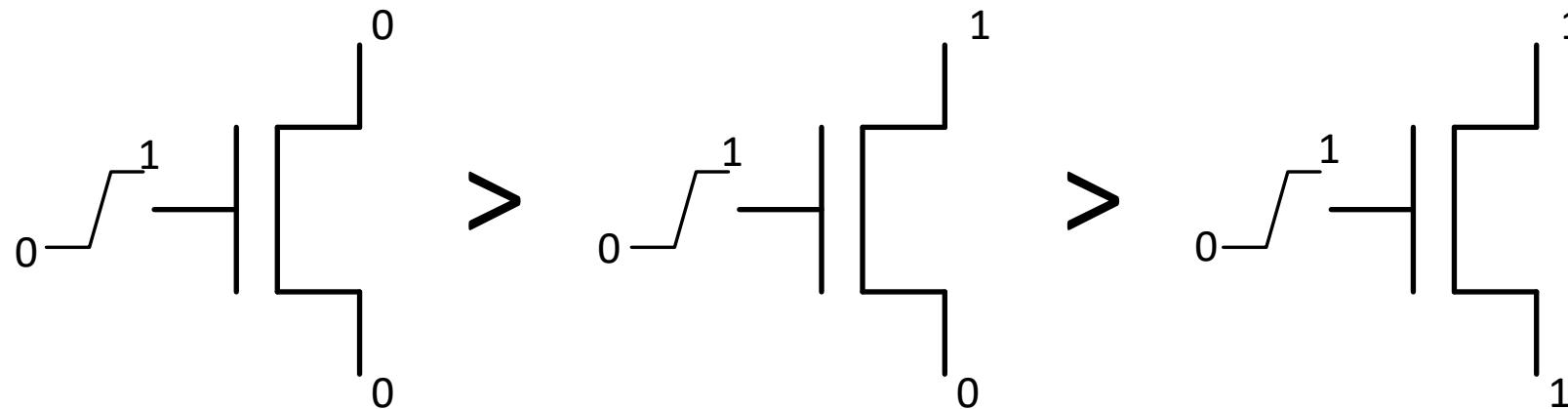
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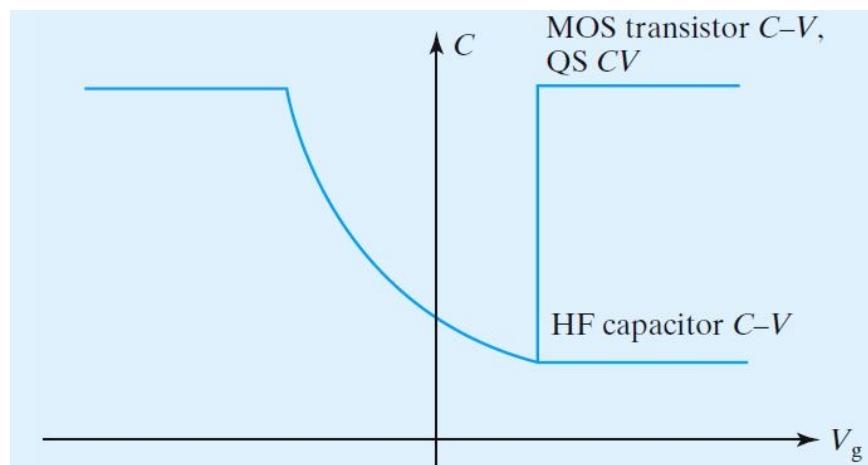
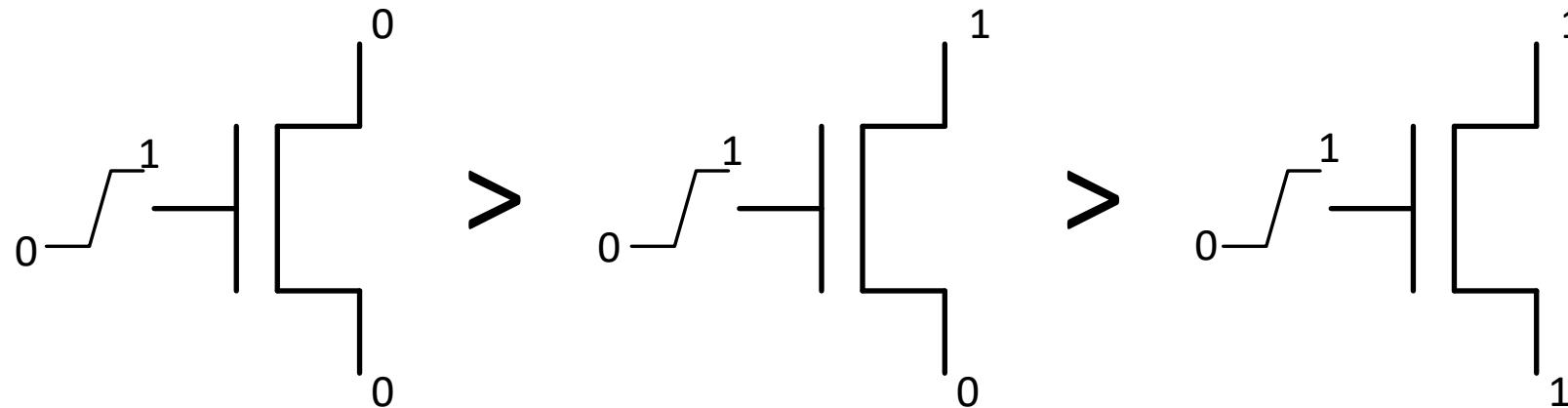


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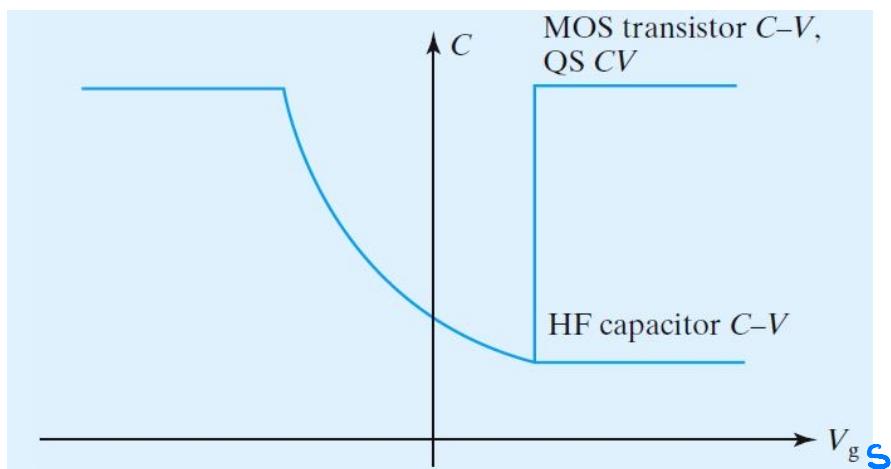
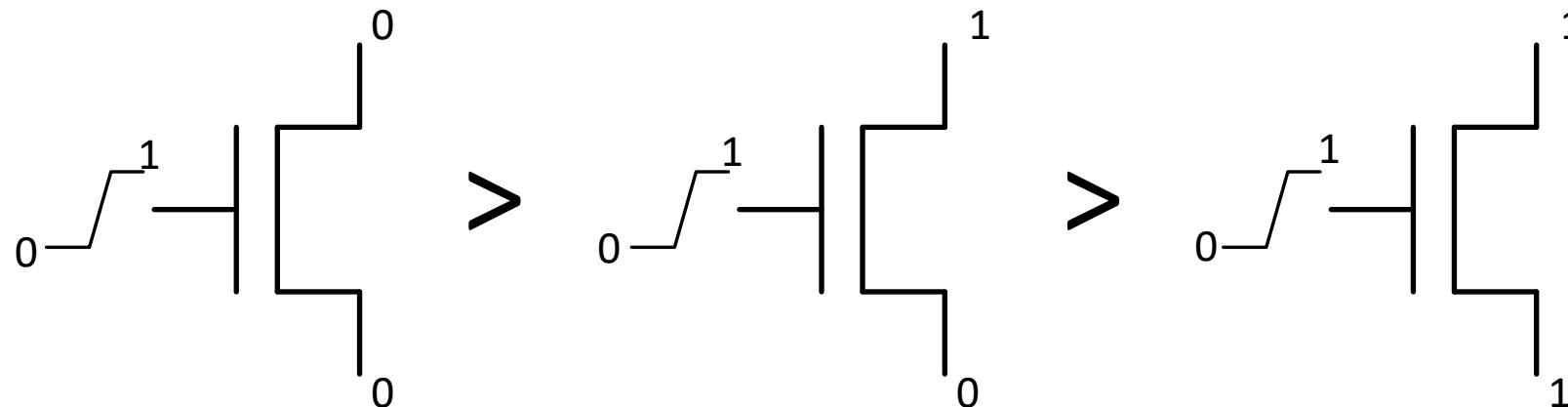
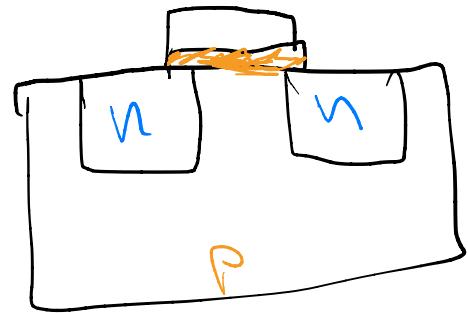


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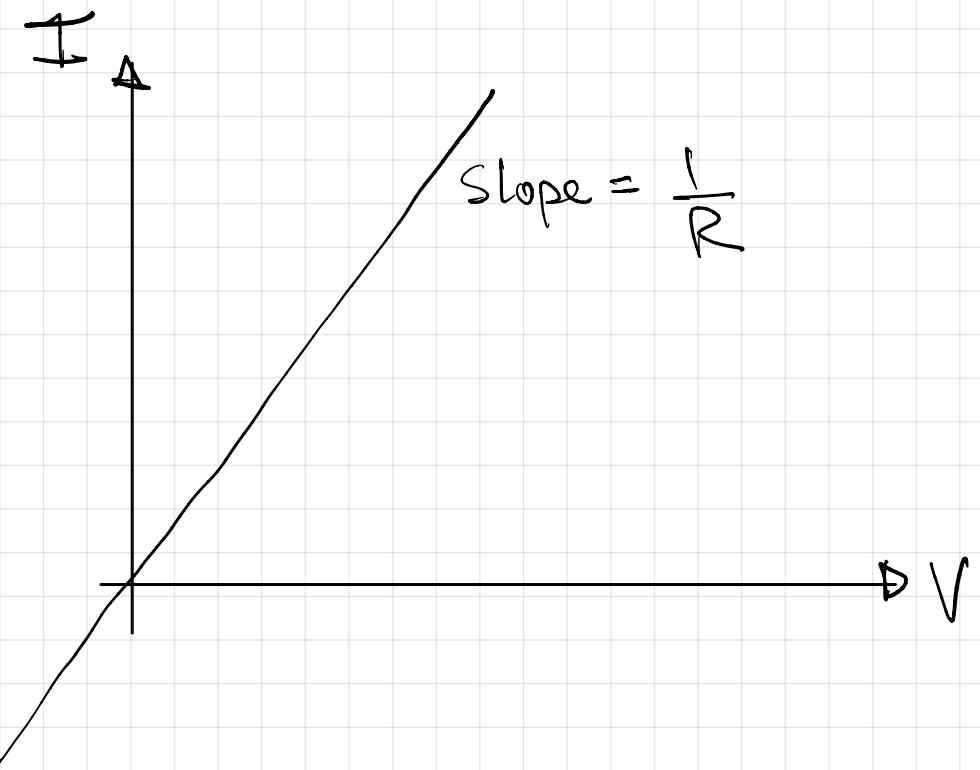
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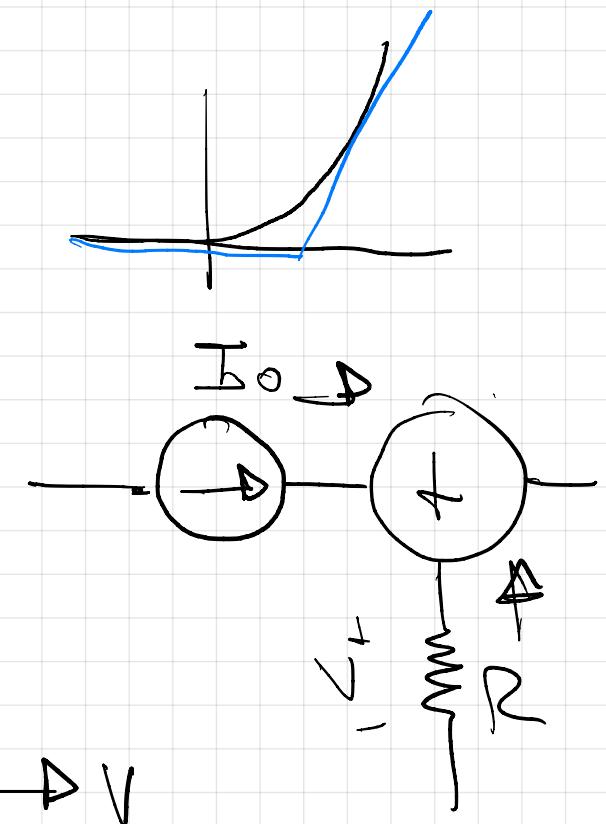
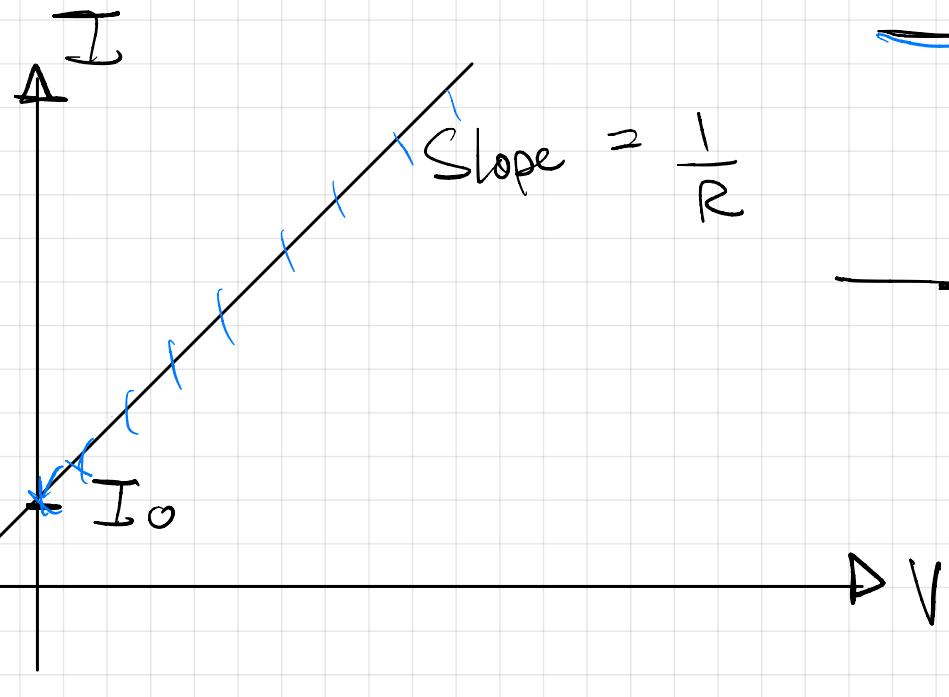
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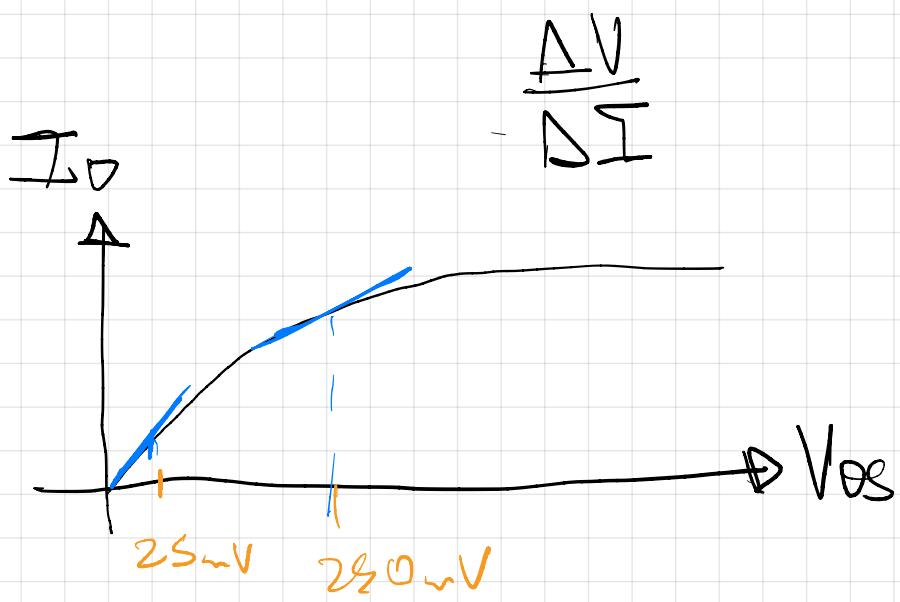
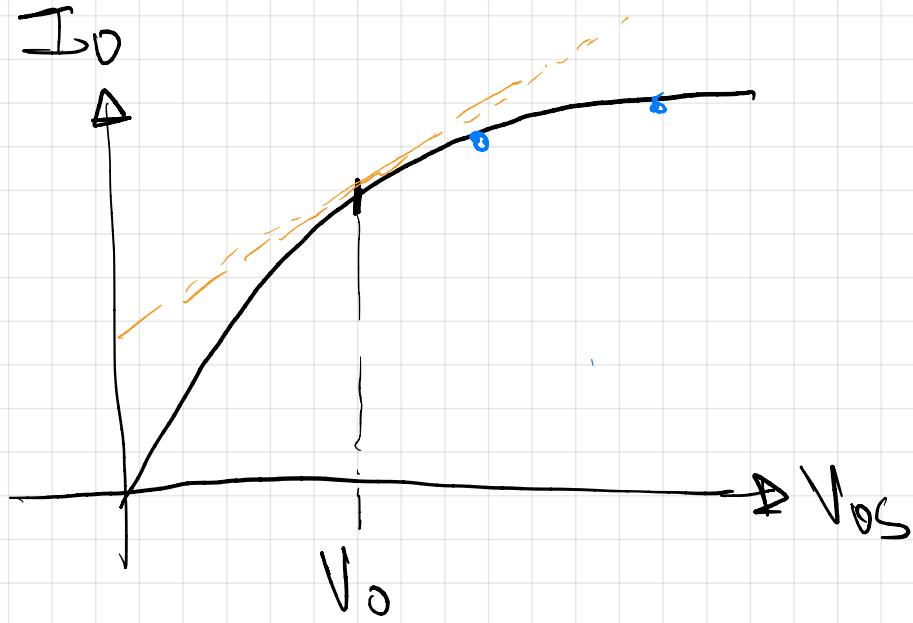




$$V = I \cdot R$$

$$I = \frac{V}{R}$$



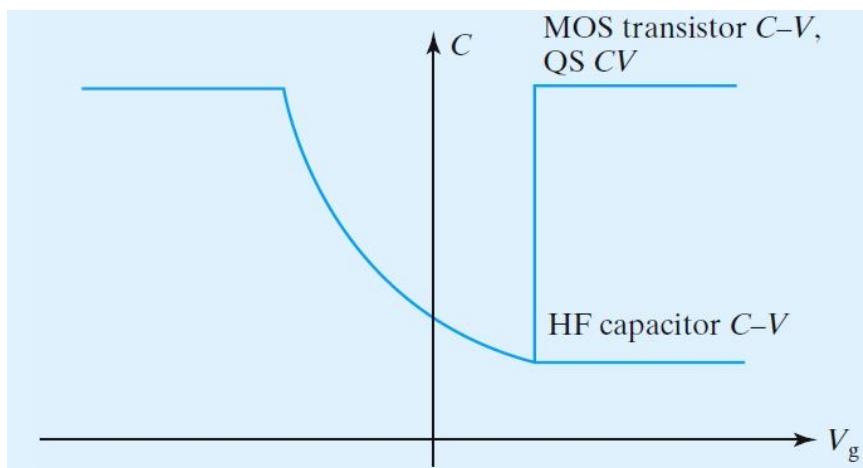
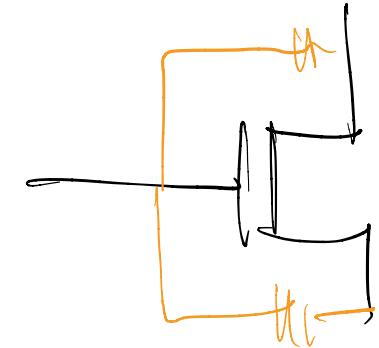
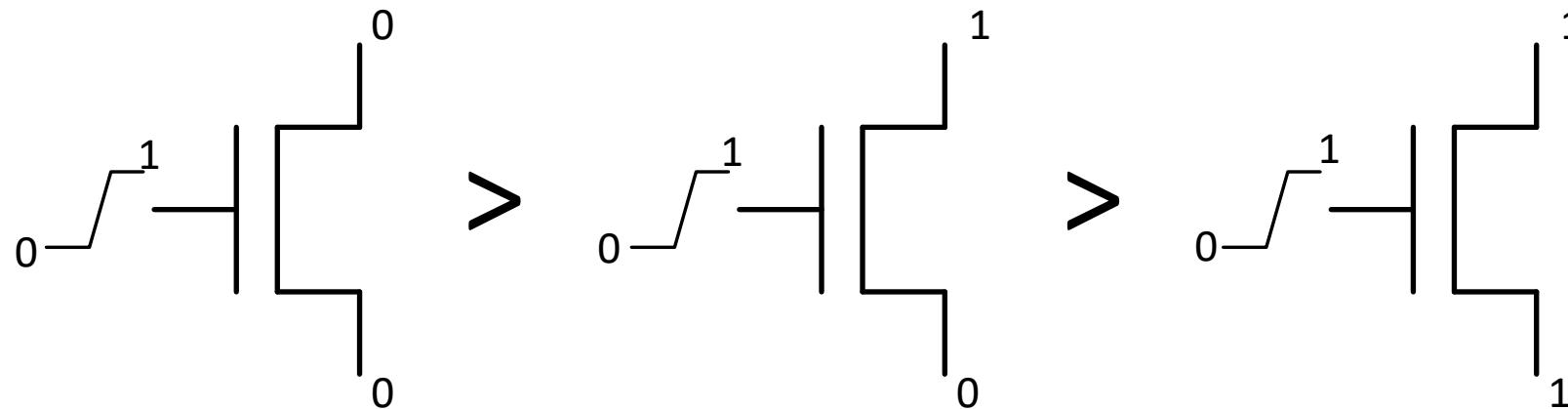


$$I(V) \approx I_0 + \frac{1}{R} V$$

$$I(0) + I'(0) \cdot V + I''(0) \frac{V^2}{2} + \dots$$

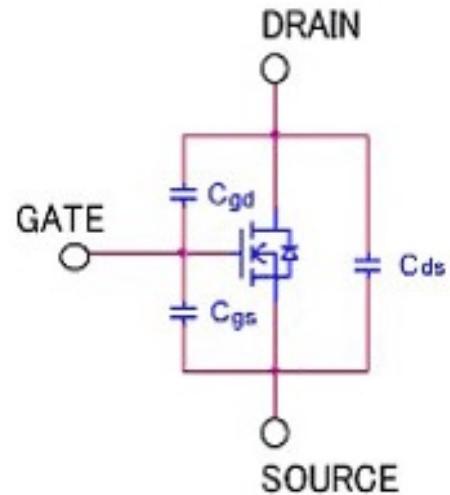
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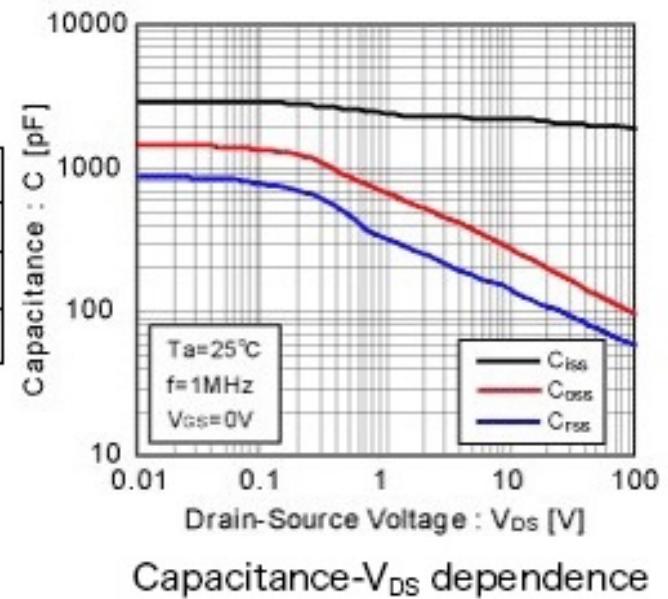


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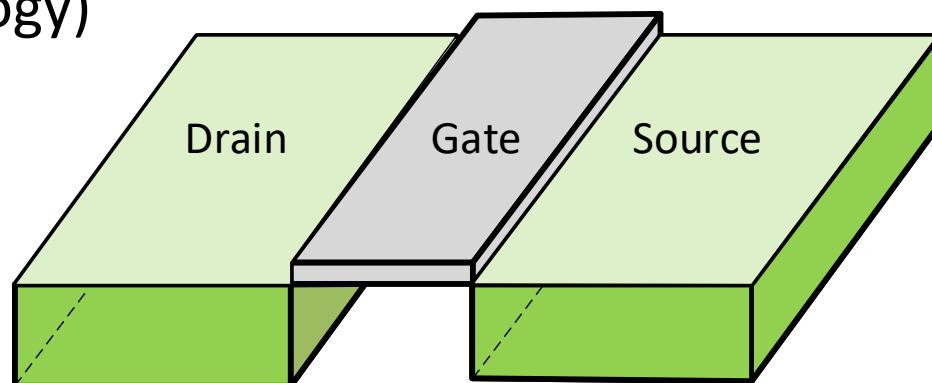
Symbol	Expression	Meaning
C_{iss}	$C_{gs} + C_{gd}$	Input capacitance
C_{oss}	$C_{ds} + C_{gd}$	Output capacitance
C_{rss}	C_{gd}	Feedback capacitance



Taken from <https://techweb.rohm.com/knowledge/si/s-si/03-s-si/4873>

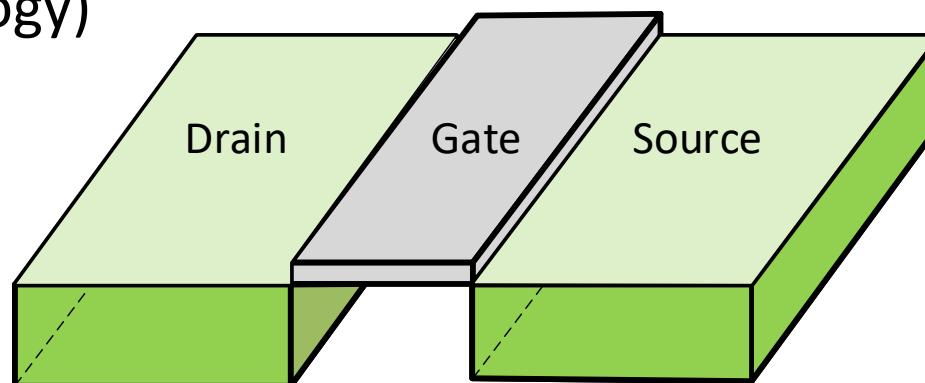
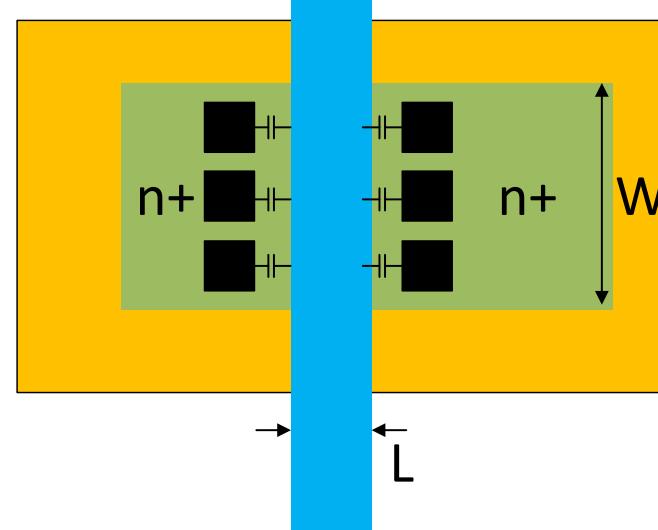
Junction Capacitance

- Capacitance of the depletion region
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 - Avoiding poor layout decisions (Geometry, topology)



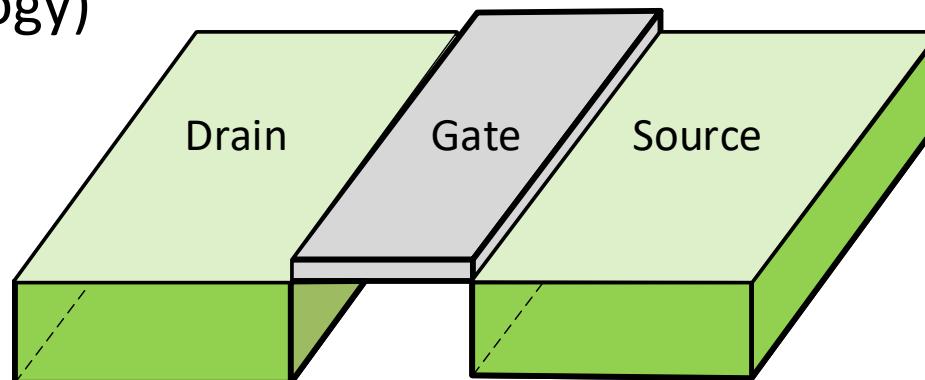
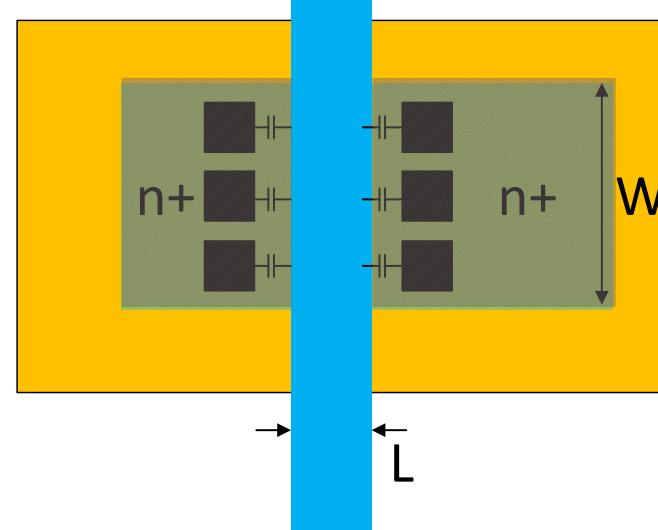
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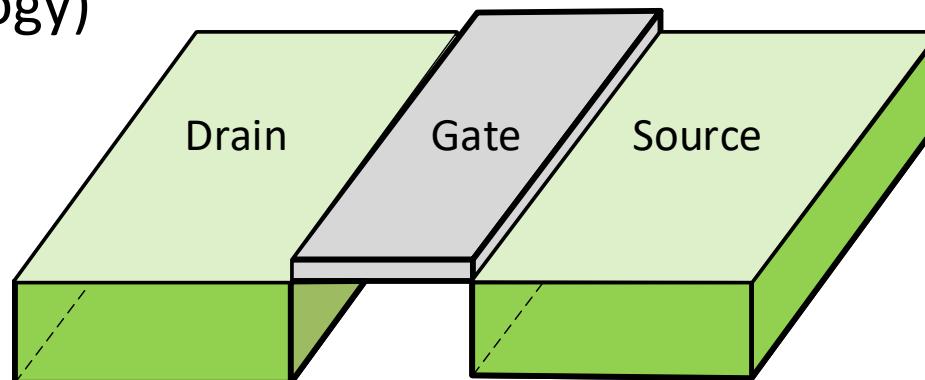
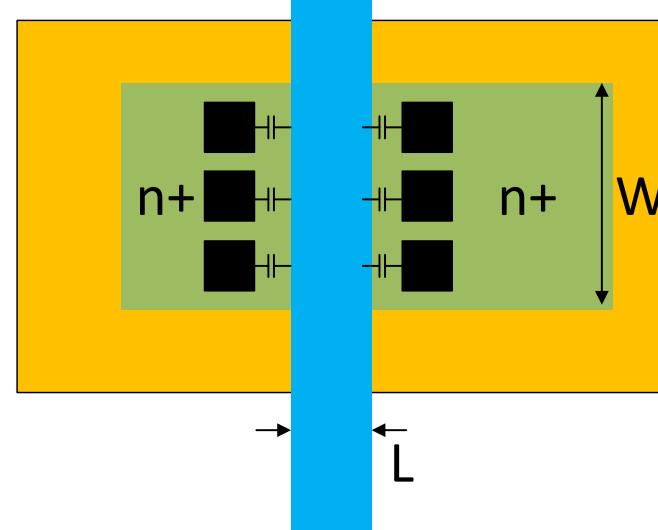
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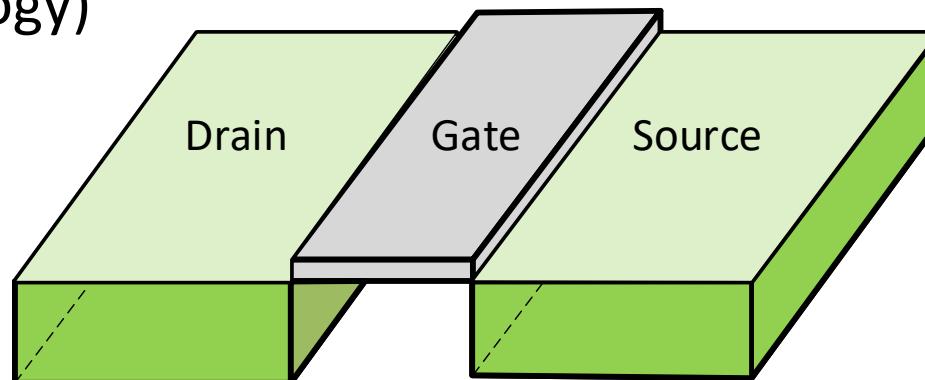
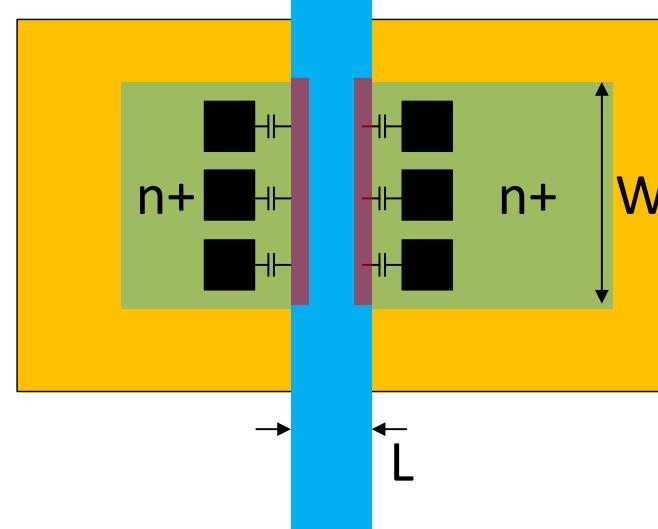
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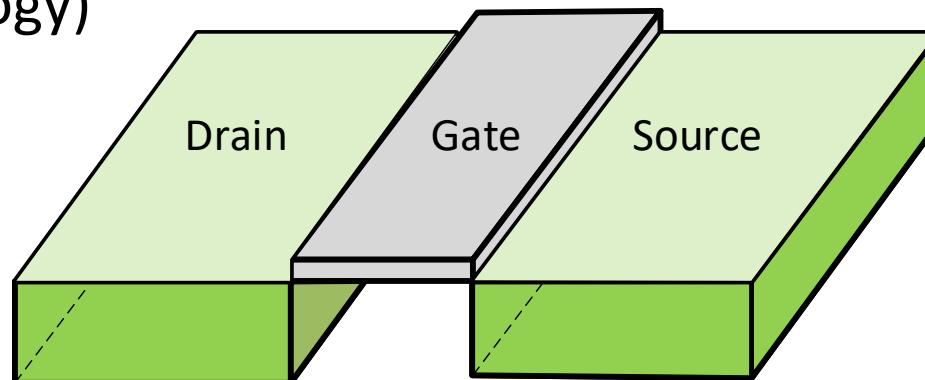
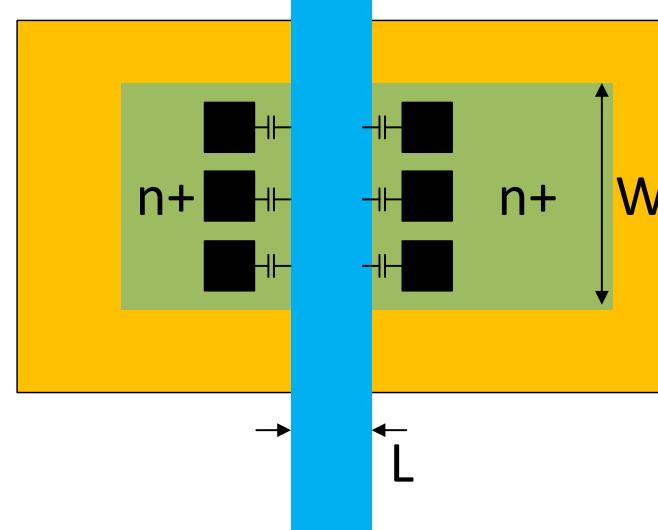
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 - Avoiding poor layout decisions (Geometry, topology)



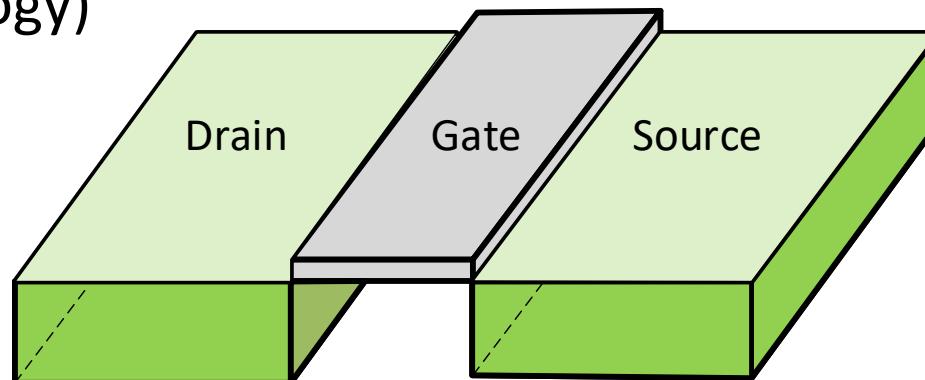
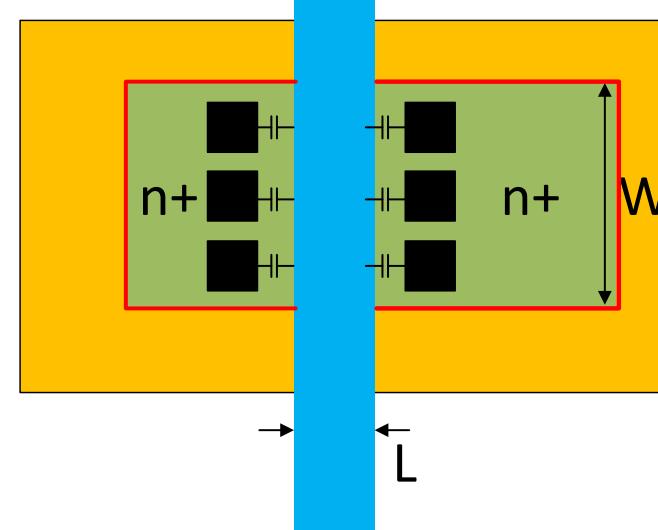
Junction Capacitance

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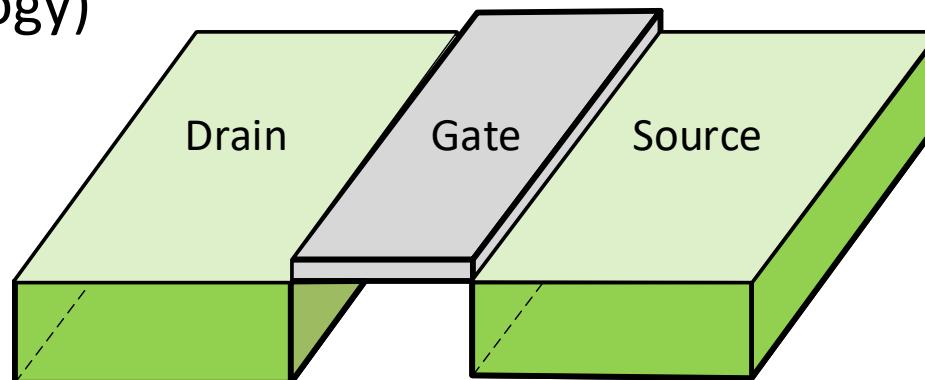
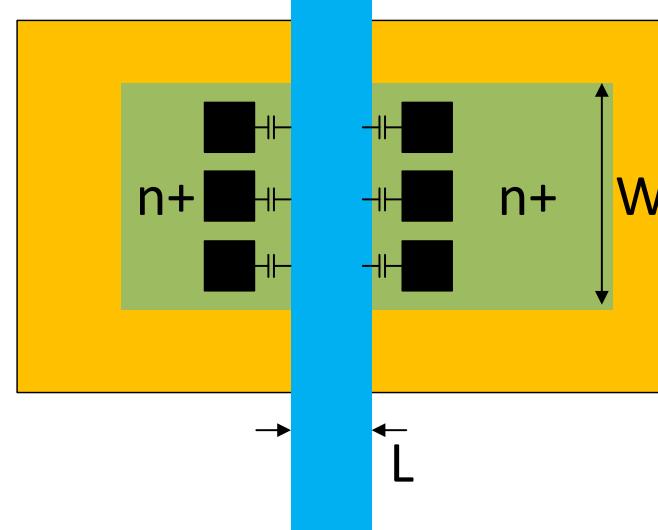
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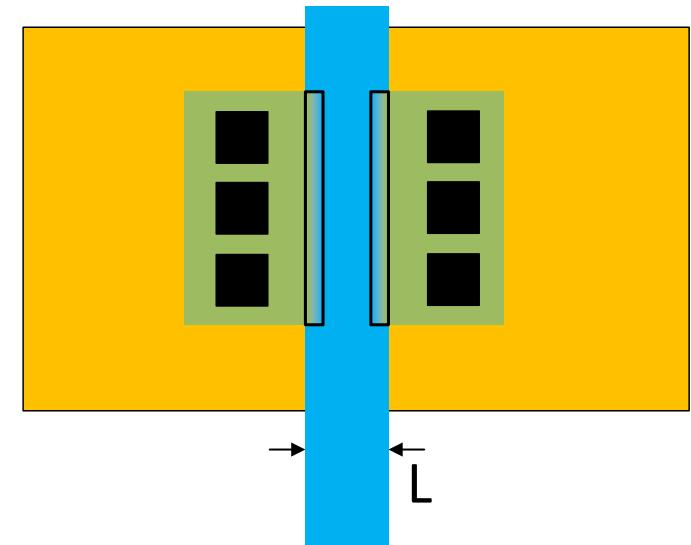
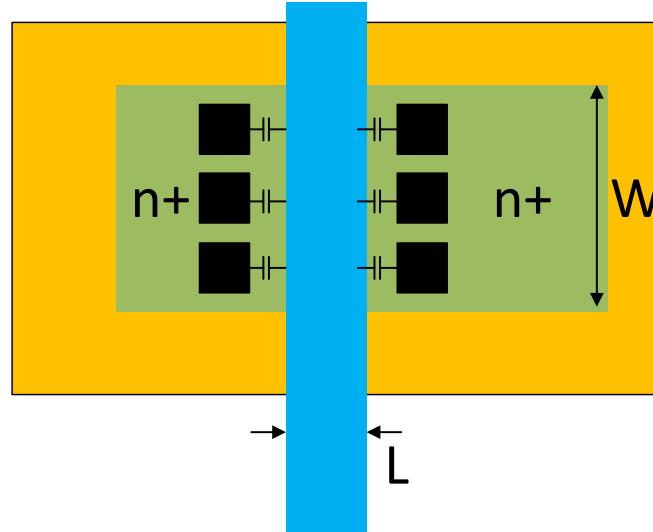
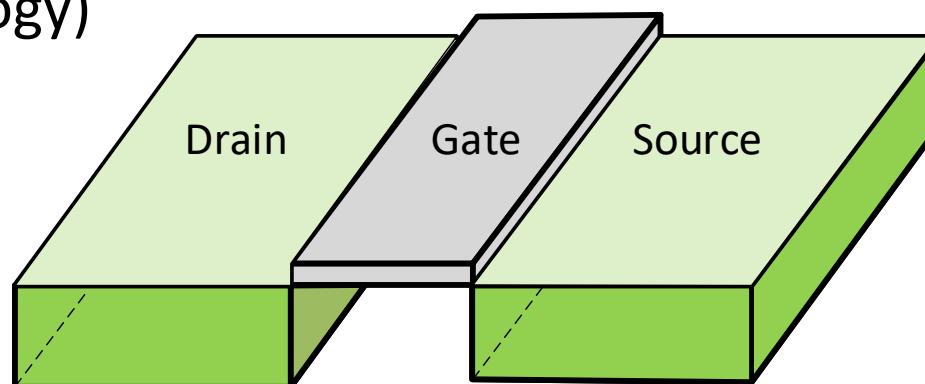
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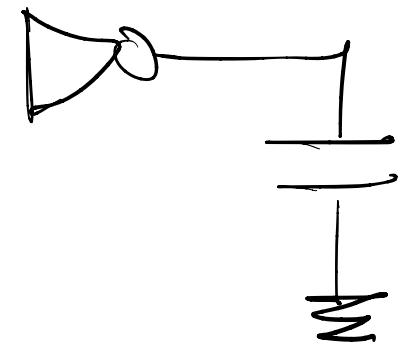
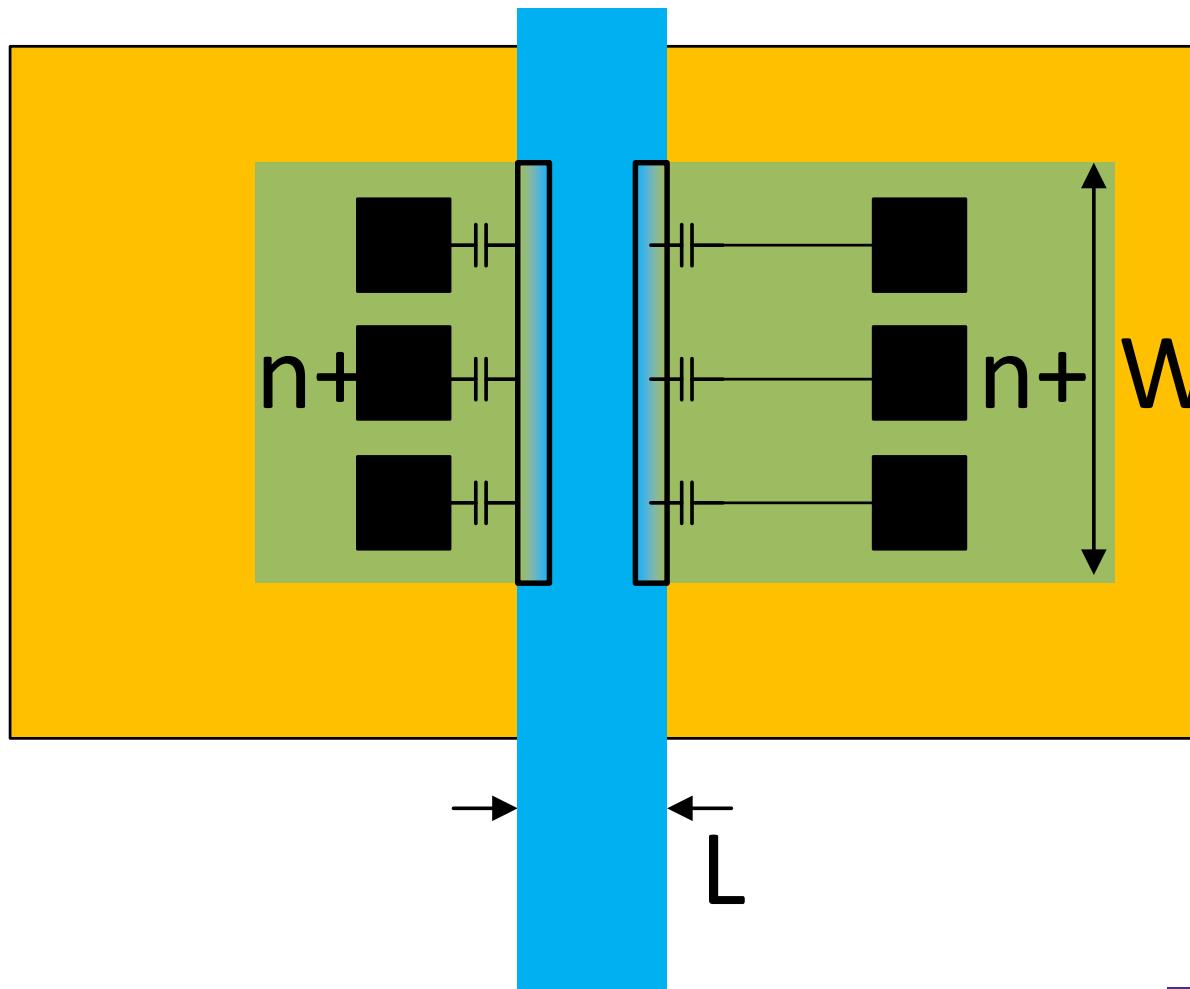
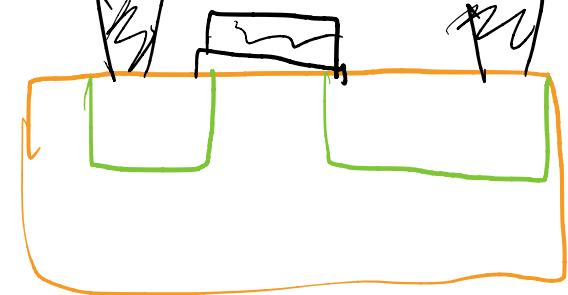


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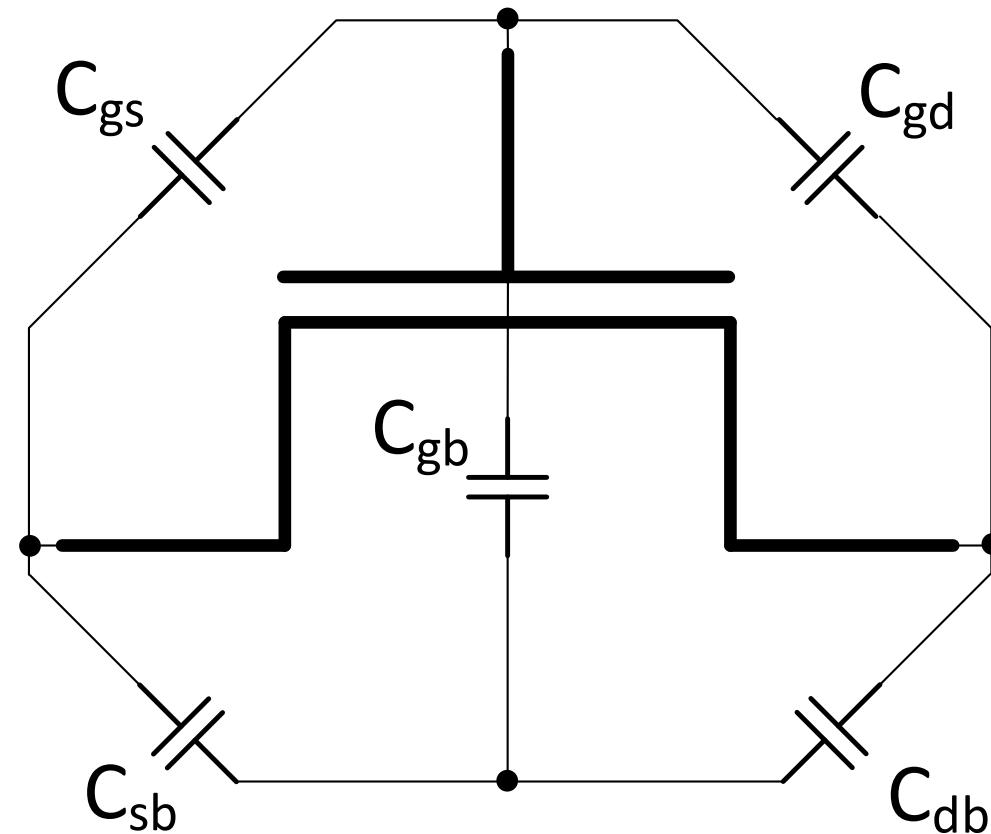


Is This a Good Idea?

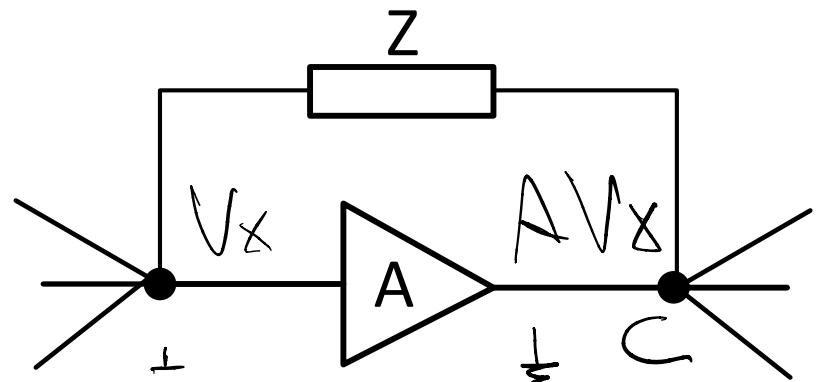


Capacitance of a MOS transistor

- $C_{\text{gate}} = W * L * C_{\text{ox}}$
- $C_{\text{source}} = C_j(W) + C_{gs}(W)$
- $C_{\text{drain}} = C_j(W) + C_{gd}(W)$

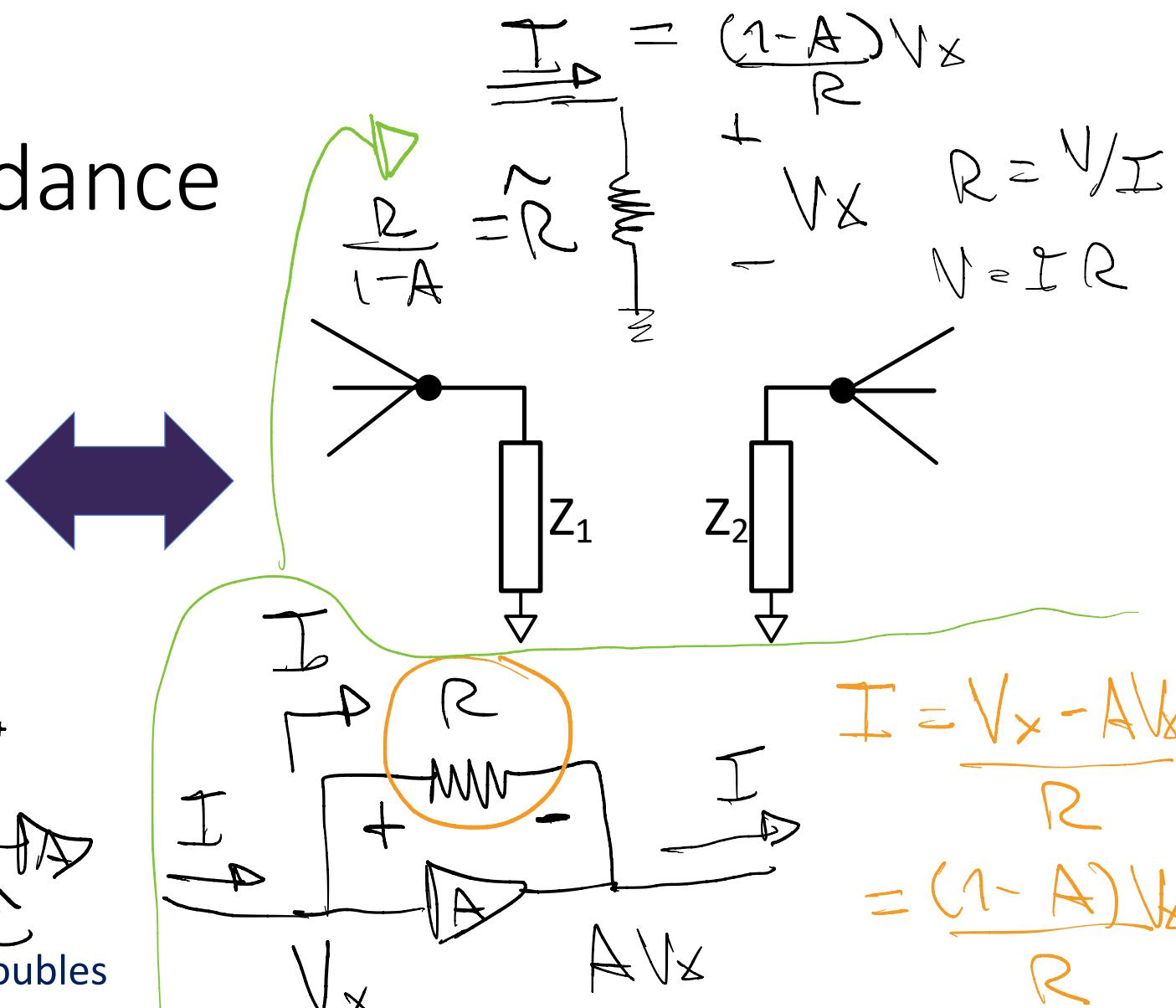


Detour: Miller impedance

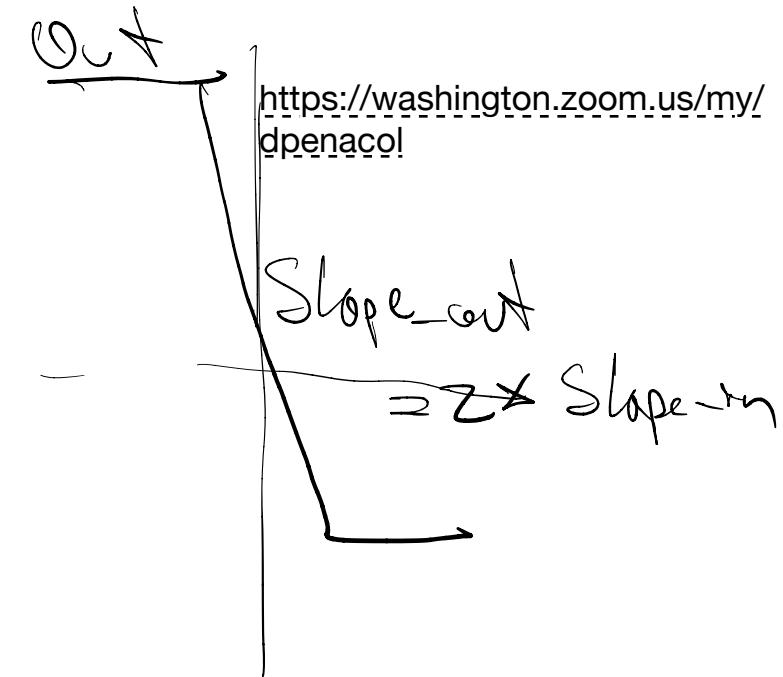
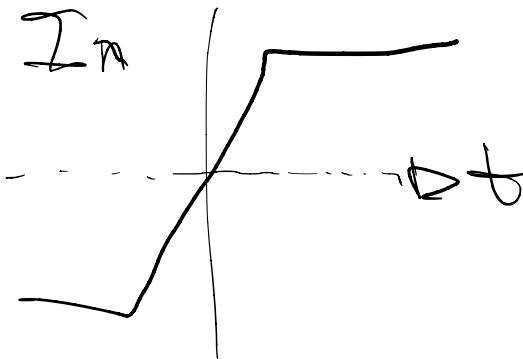
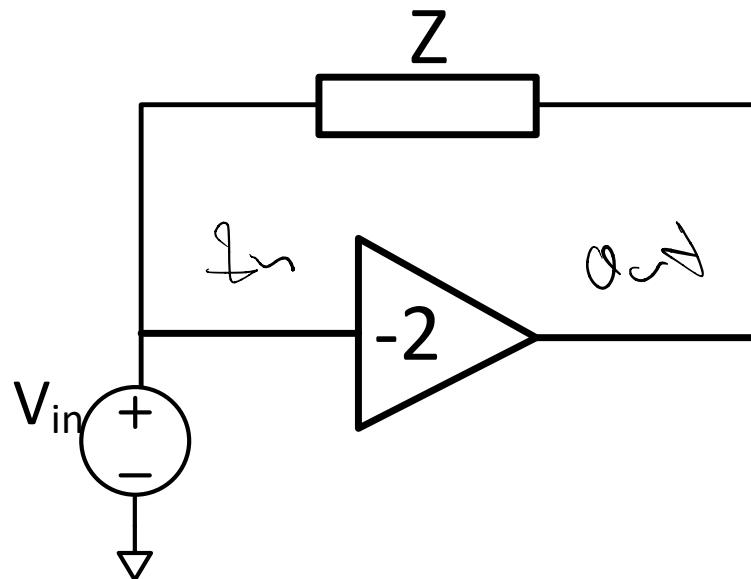


- $Z_1 = Z/(1-A)$,
- $Z_2 = Z/(1-A^{-1})$,
- Specifically, if $A=-1$
 - $Z_1 = Z_2 = Z/2$
 - If Z is a capacitance, Capacitance doubles

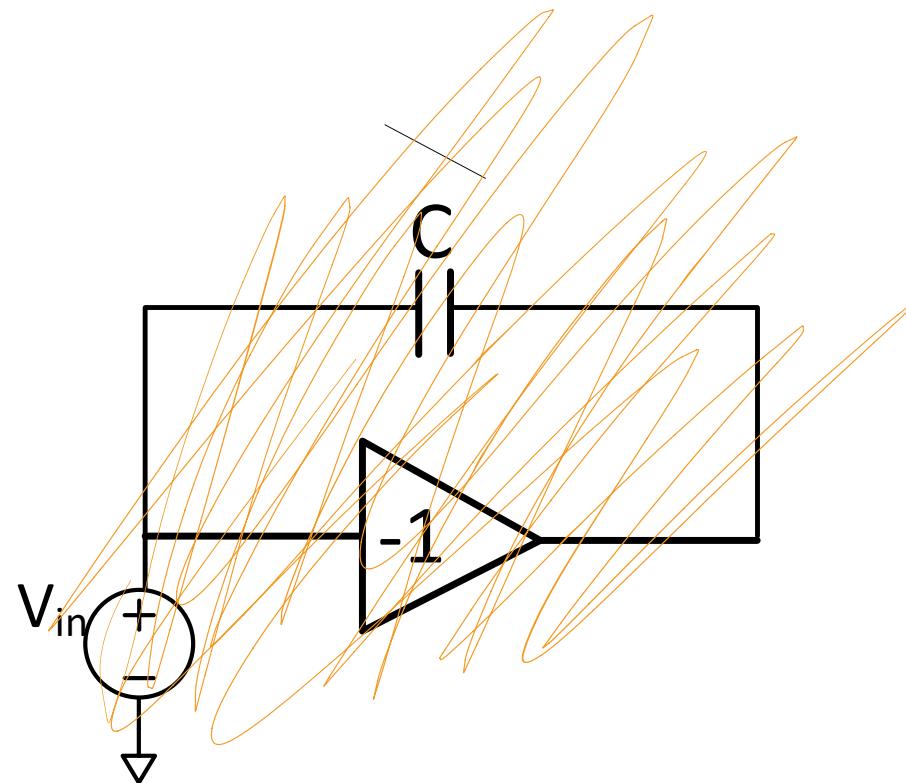
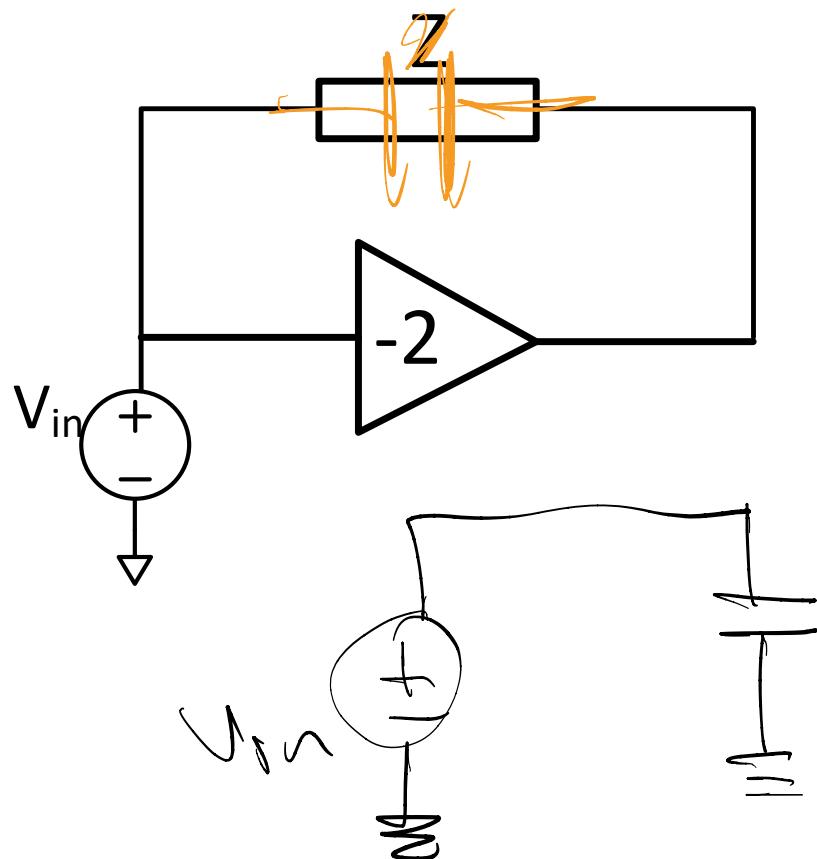
$$\frac{1}{T} C \quad \frac{1}{SC} \quad | \quad \frac{1}{T} \tilde{C} \quad | \quad \frac{1}{T} = \frac{1}{(1-A)C} \quad \frac{1}{(1-A)SC}$$



Quick Example



Quick Example



$$C_3 = C(1 - (-2))$$

n

$$I_{sat} = \frac{1}{2} \beta (V_{DS} - V_{th})^n$$

$$I = \frac{1}{2} \beta (V_{DS} - V_{th})^n (1 + 2V_{DS})$$

$\underbrace{\hspace{10em}}$
 A

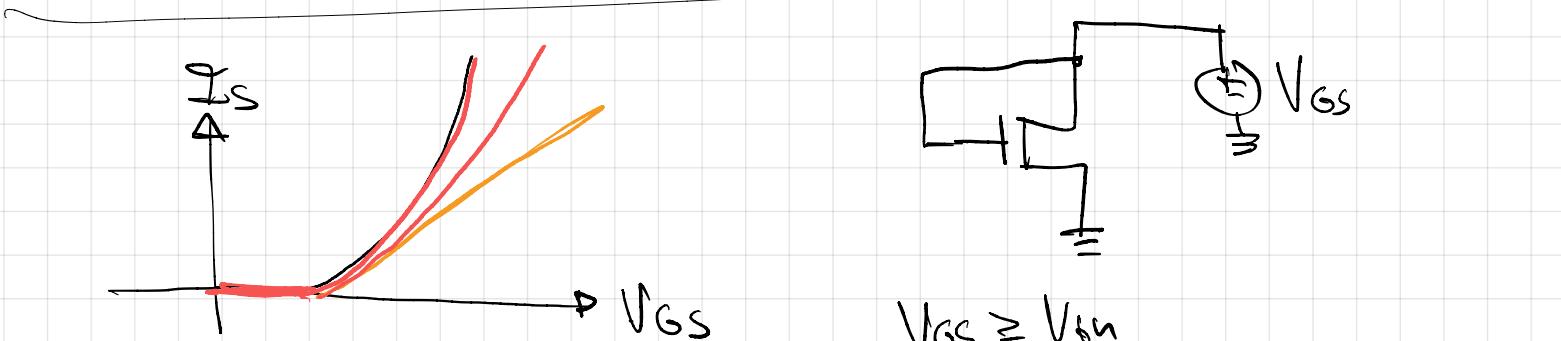
V^{-1}

error (λ, V_{th}, β)

min error

λ, V_{th}, β

$V_{th} > 0$



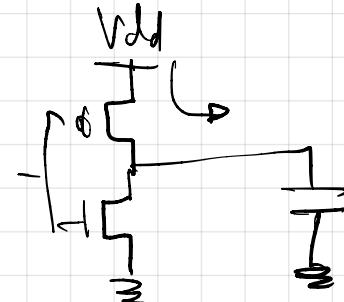
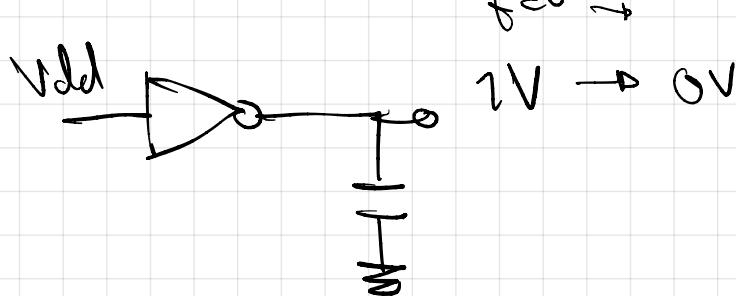
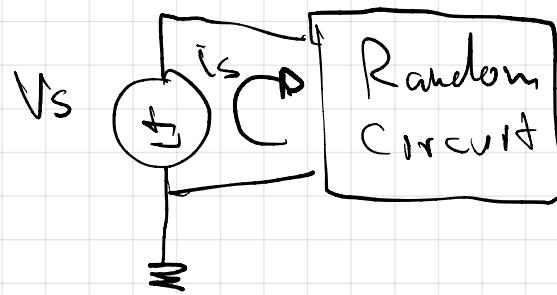
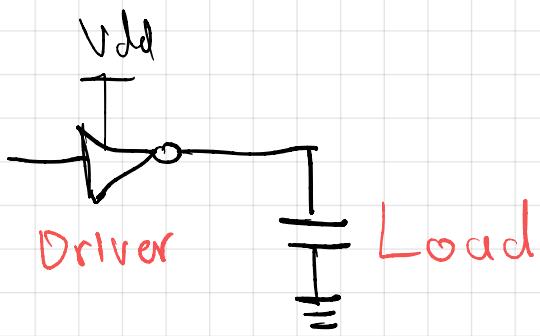
$$V_{GS} \geq V_{th}$$

$$V_{DS} \geq V_{GS} - V_{th}$$

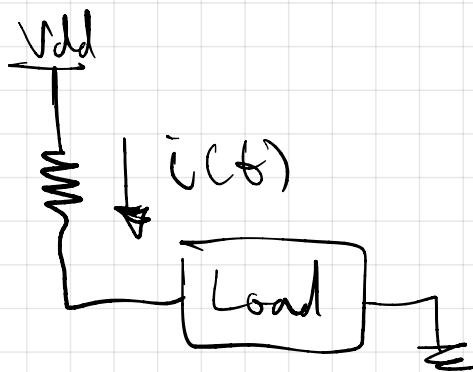
$$I = \frac{1}{2} \beta (V_{GS} - V_{th})^n$$

$$\log I = \log(\beta/2) + n \log(V_{GS} - V_{th})$$

$$\log I = \log(\beta/2) + n X$$



$E_T \cdot \underline{\text{Transitions}}$
Second

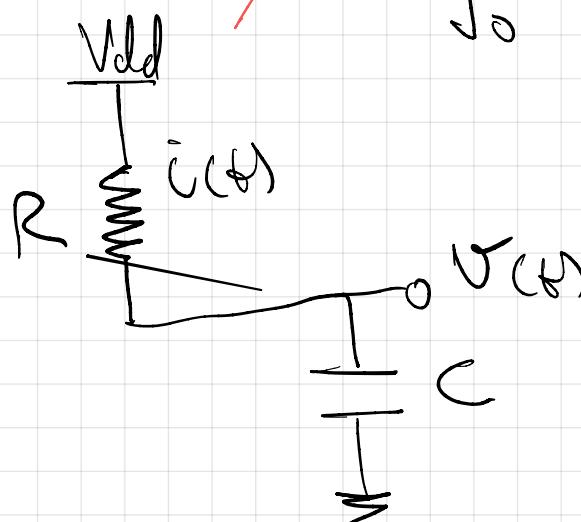
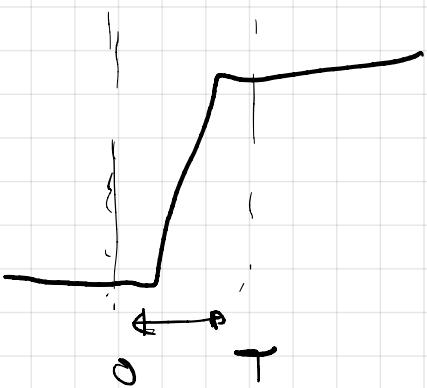


$$E = \int_0^T V_{dd} \cdot i(t) dt$$

$$\Rightarrow \int_0^T V_{dd} \cdot C \frac{dV(t)}{dt} dt$$

$$= \int_{V(0)}^{V(T)} V_{dd} C dv$$

$$= \int_0^{V(T)} V_{dd} C dv$$



$$i(t) = \frac{V_{dd} - V(t)}{R}$$

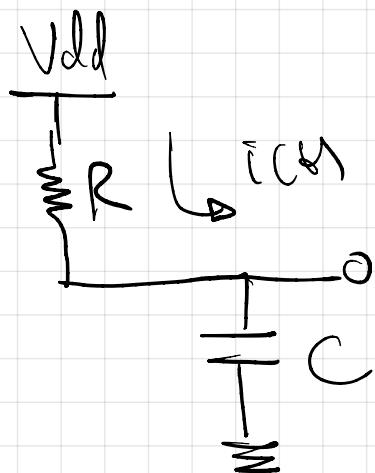
$$i(t) = C \cdot \frac{dV(t)}{dt}$$

$$E = \int_0^{V_{dd}} V_{dd} C dV$$

$$= V_{dd} \cdot C \int_0^{V_{dd}} dV = V_{dd} \cdot C \cdot V \Big|_0^{V_{dd}}$$

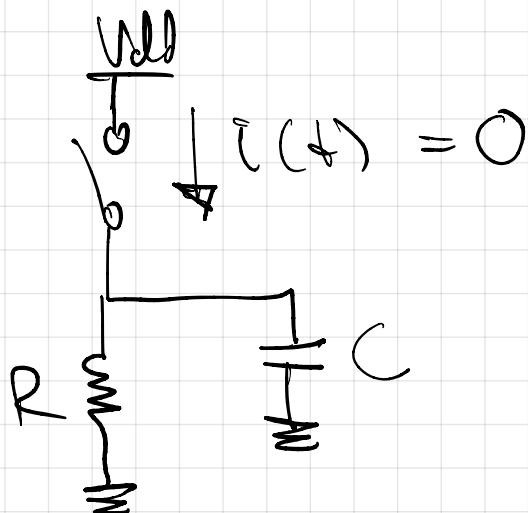
$$= V_{dd} \cdot C \cdot V_{dd}$$

$$= C V_{dd}^2$$



$$E_{0 \rightarrow T} = C V_{dd}^2$$

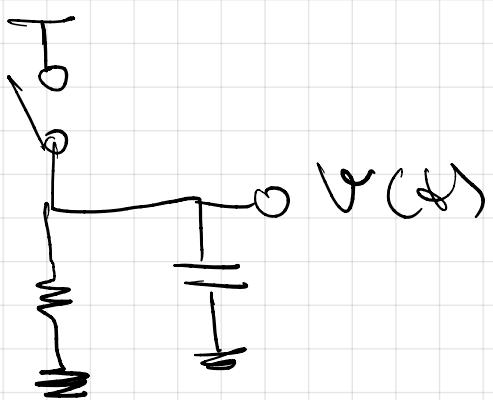
What about $E_{T \rightarrow 0}$?



$$E_{T \rightarrow 0} = 0$$

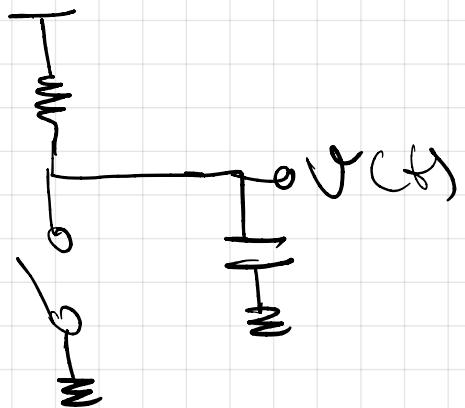
$$= \int_0^T V_{dd} i(t) dt = \int_0^T 0 dt = 0$$

More intuitive explanation



$$V(t=0) = V_{dd}$$

$$E_c = \frac{1}{2} CV_{dd}^2$$



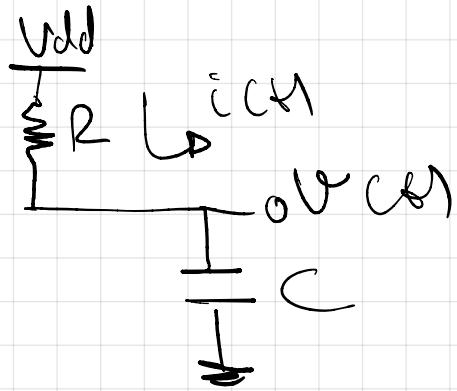
$$V(t=0) = 0$$

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Chih-Hsiang Huang
ISSCC 2022

$$P = C V_{dd}^2 \Delta f$$

What about delay?



$$V(t=0) = 0V$$

$$\begin{aligned} i(t) &= \frac{V_{dd} - V(t)}{R} \\ &= C \frac{dV(t)}{dt} \end{aligned}$$

$$\frac{V_{dd}}{R} - \frac{V(t)}{R} = C \frac{dV}{dt}$$

$$V_{dd} = RC \frac{dV}{dt} + V$$

$$V_h = Ae^{\lambda t}$$

$$0 = RC\lambda + V$$

$$V_h(t) = A e^{-t/RC}$$

$$\Rightarrow \lambda = -\frac{1}{RC}$$

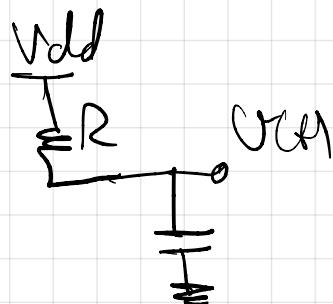
$$V_p(t) = V_{dd}$$

$$V(t) = A e^{-t/RC} + V_{dd}$$

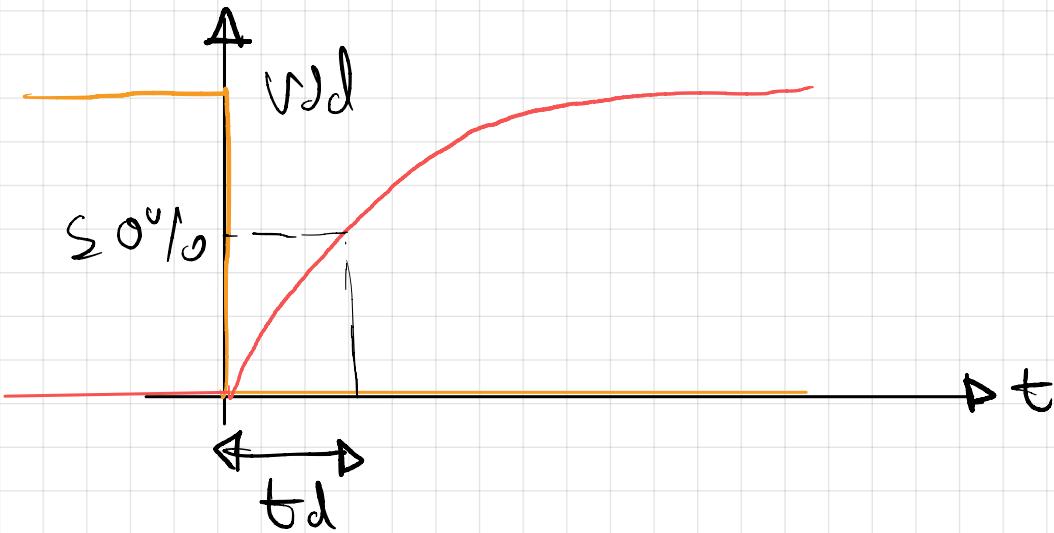
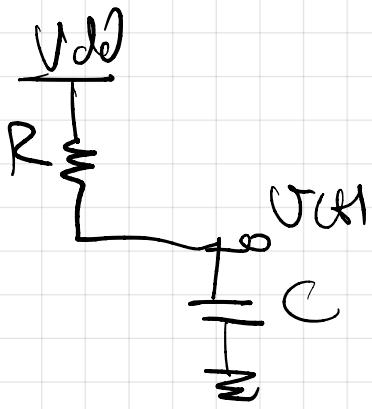
$$V(0) = 0 = A e^{-0/RC} + V_{dd}$$

$$A = -V_{dd}$$

$$V(t) = V_{dd}(1 - e^{-t/RC})$$



$$V(t) = V_{dd} (1 - e^{-t/RC})$$



$$V(t_d) = 0.5V_{dd} = V_{dd} (1 - e^{-t_d/RC})$$

$$\Rightarrow 0.5 = 1 - e^{-t_d/RC}$$

$$\Rightarrow e^{-t_d/RC} = 0.5$$

$$-\frac{t_d}{RC} = \ln(0.5) = -\ln\left(\frac{1}{0.5}\right) = \ln 2$$

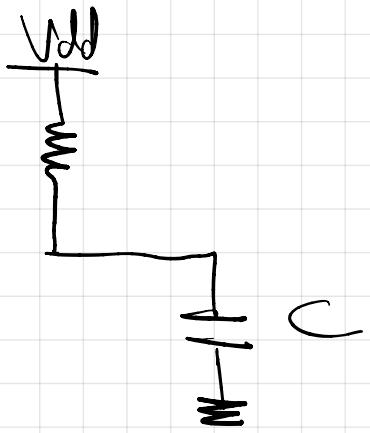
$$\Rightarrow \frac{t_d}{RC} = \ln 2$$

$$\Rightarrow t_d = RC \ln 2$$

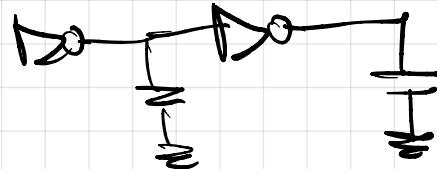
$$E = CV_{dd}^2$$

$$t_d = R C \ln(2)$$

$$E \approx C V_{dd}^2$$

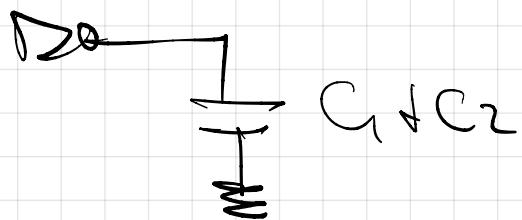
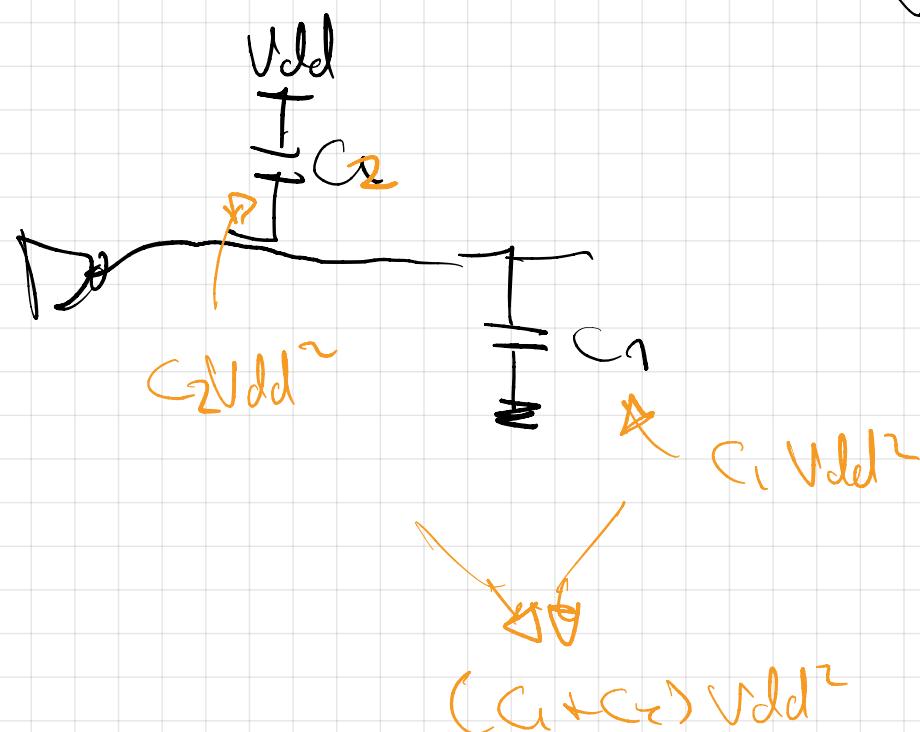


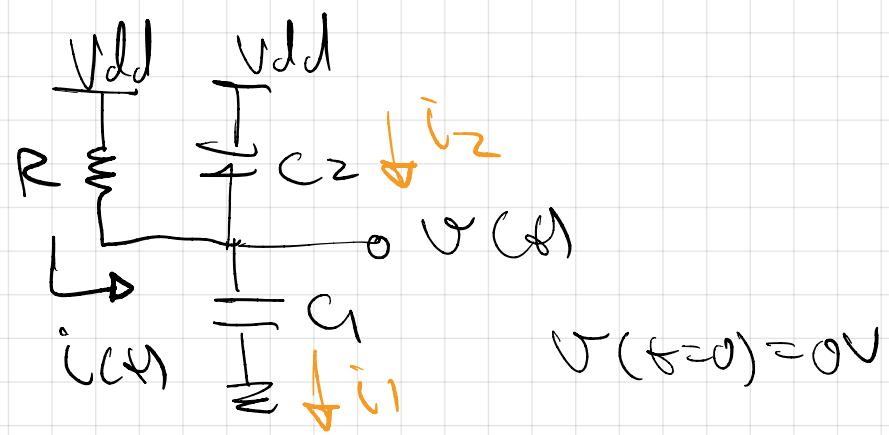
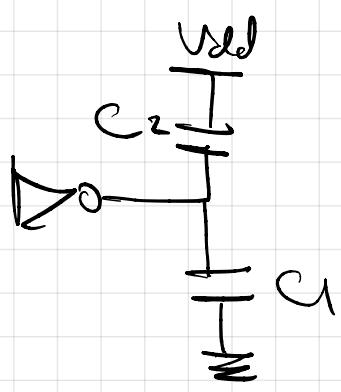
$$I = C \cdot \frac{V}{L}$$



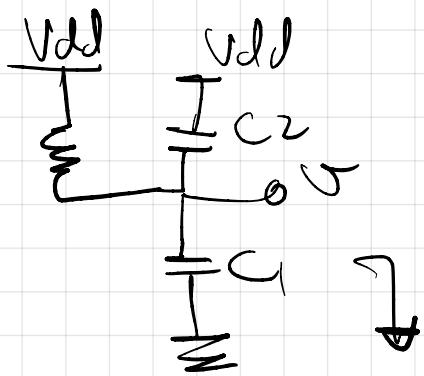
Logic effort

Weste Harris





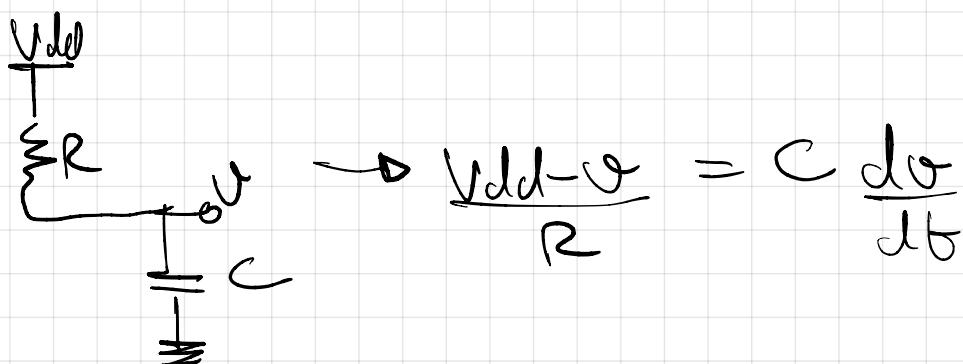
$$\begin{aligned}
 \dot{V}(t) &= \frac{V_{DD} - V}{R} = i_1 - i_2 = C_1 \frac{dV}{dt} - C_2 \frac{d(V_{DD} - V)}{dt} \\
 &= C_1 \frac{dV}{dt} - C_2 \frac{dV_{DD}}{dt} + C_2 \frac{dV}{dt}
 \end{aligned}$$



$$= C_1 \frac{dV}{dt} + C_2 \frac{dV}{dt}$$

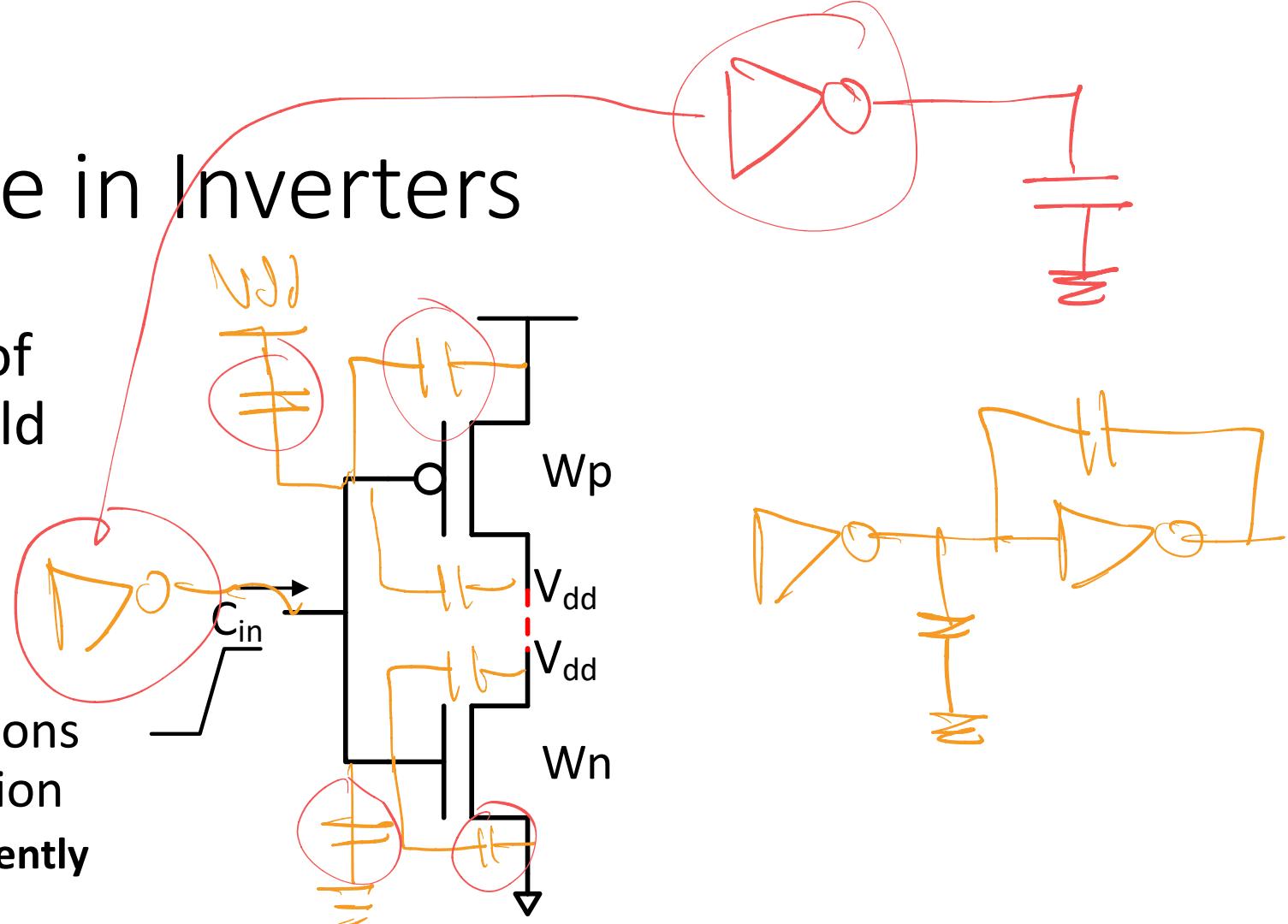
$$= (C_1 + C_2) \frac{dV}{dt}$$

$$\frac{V_{DD} - V}{R} = (C_1 + C_2) \frac{dV}{dt}$$



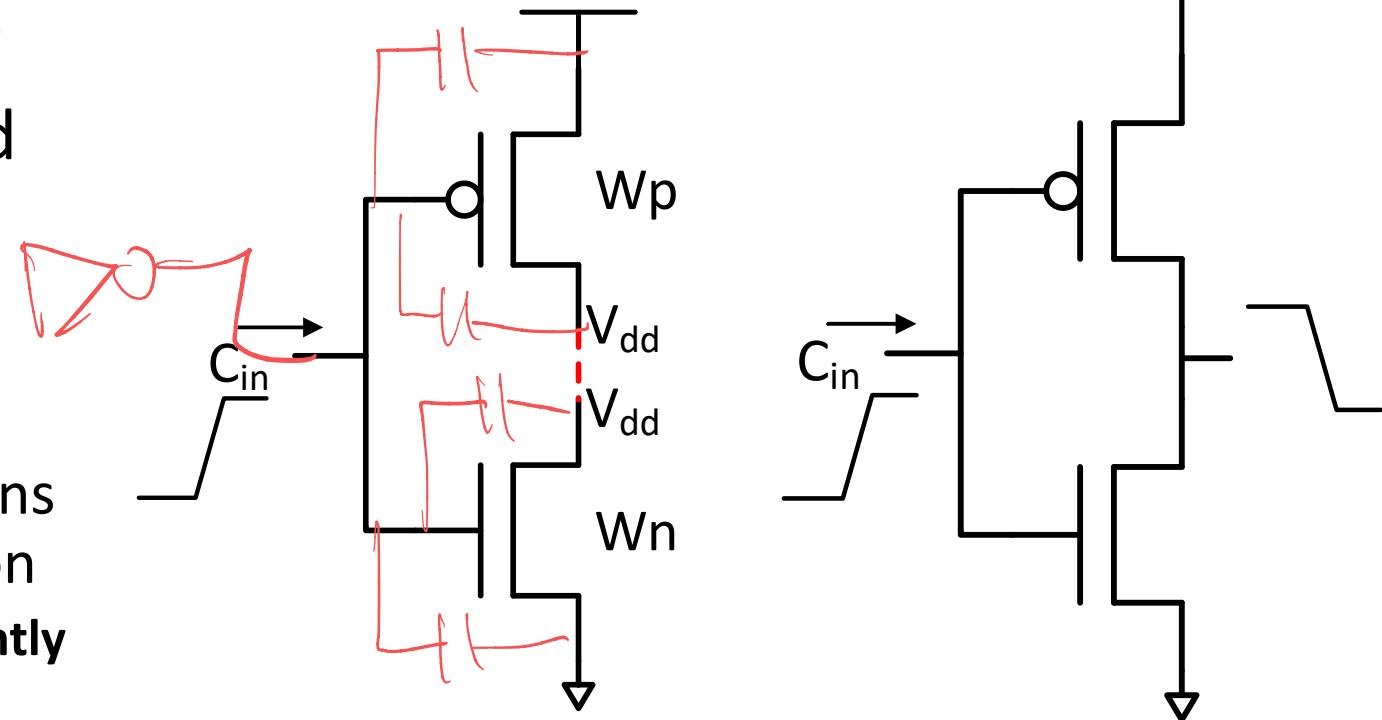
Miller Capacitance in Inverters

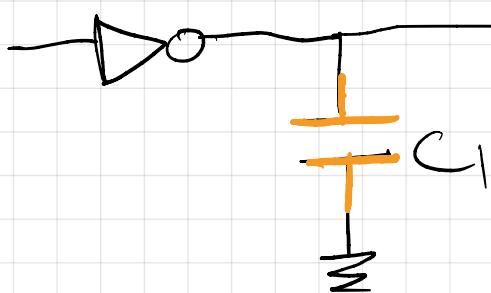
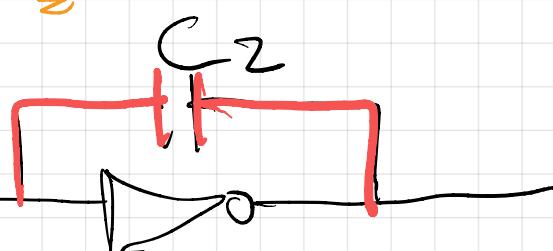
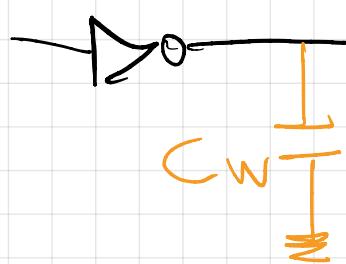
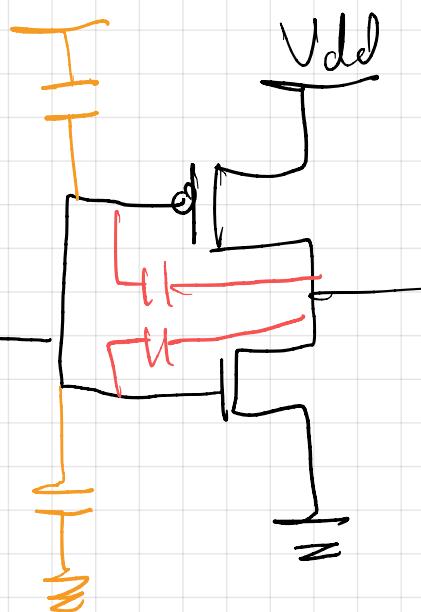
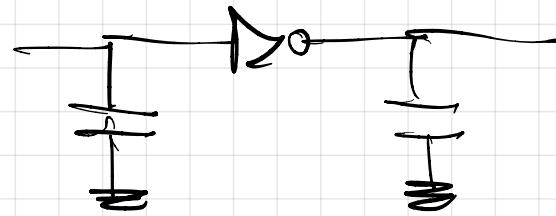
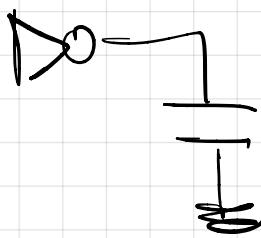
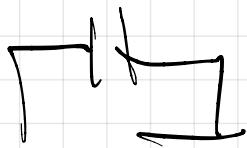
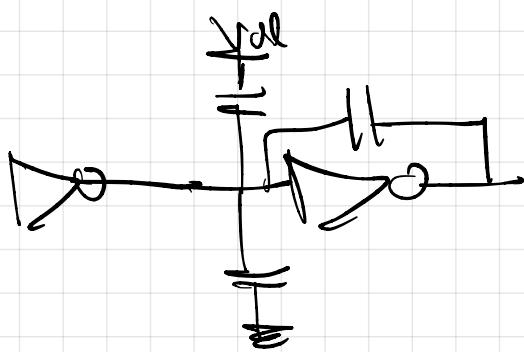
- Write down C_{in} in terms of C_{gs}, C_{gd} (Drain voltages held constant)
- C_{in} in terms of C_g^* for an inverter:
- Source, Drain voltage transitions result of Gate voltage transition
 - Affects delay and power **differently**



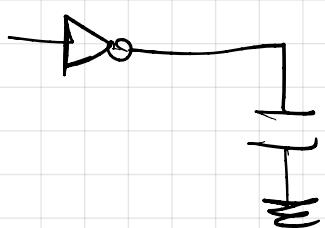
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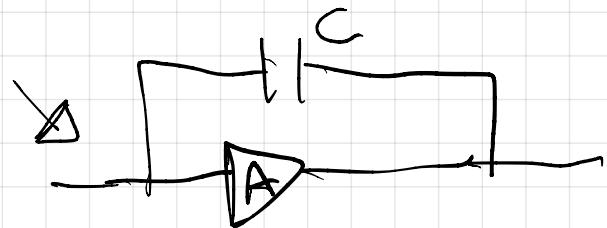
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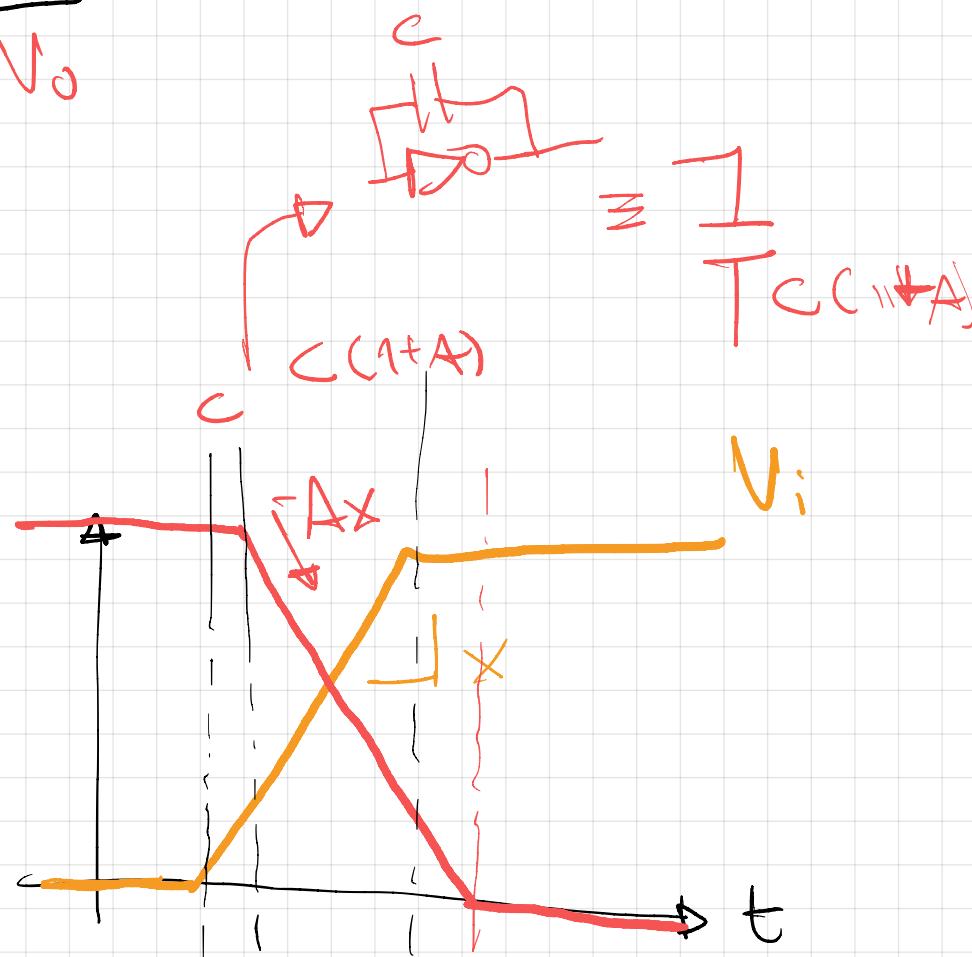
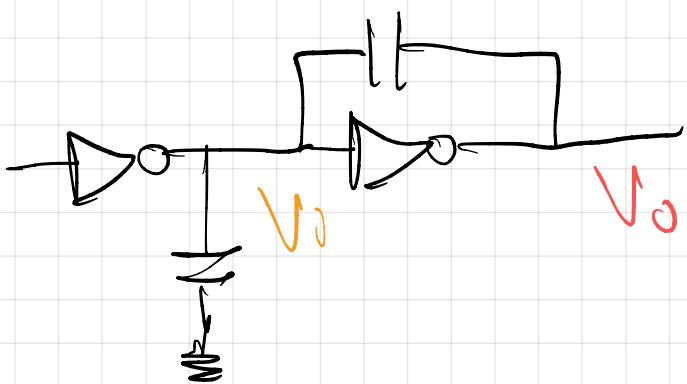
Can we get something like

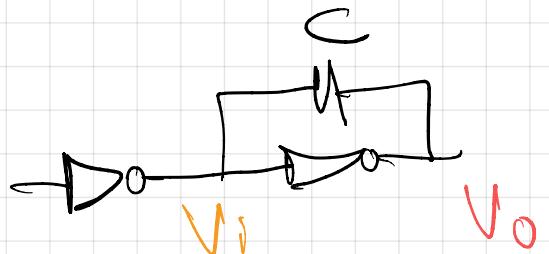
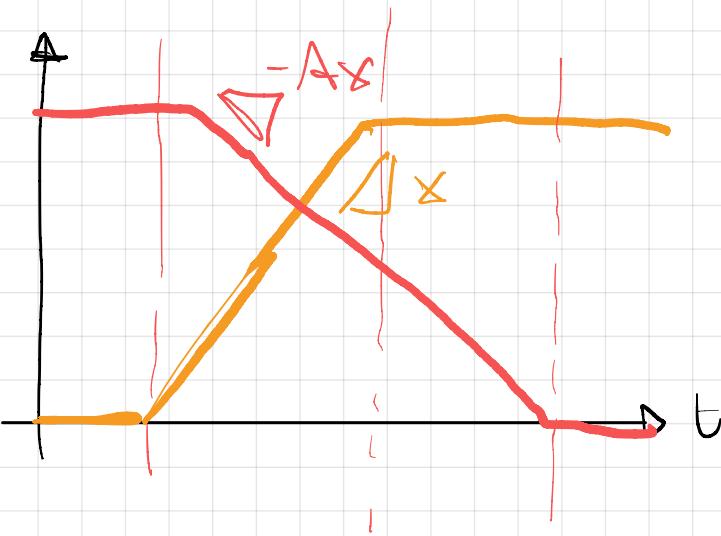




\equiv

$$\frac{1}{T} C (1 - A)$$





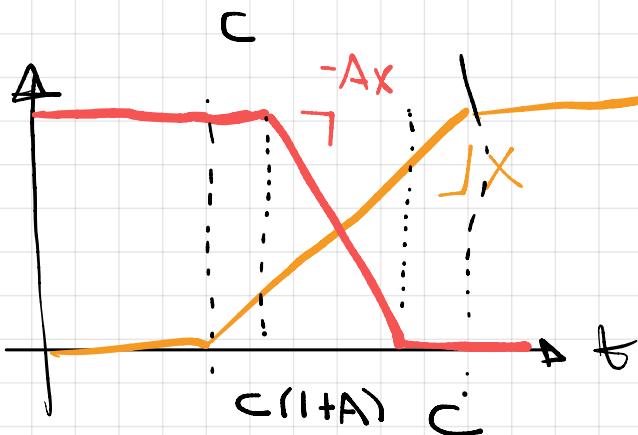
$$\frac{1}{T} \leq C(1+A)$$

Case I: red is slower

$$0 < A \leq 1$$

$$\begin{aligned} & C(1+A) \\ & \leq C(1+1) \\ & = 2C \end{aligned}$$

Case II red is faster



$$A \geq 1$$

$$C(1+A)$$

$$\begin{aligned} \tau_1 &= \frac{V_{dd}}{Ax} \\ \tau_2 &= \frac{V_{dd}}{x} \end{aligned}$$

$$\begin{aligned} & \frac{V_{dd}}{Ax} & C(1+A) \\ & \frac{V_{dd}}{x} - \frac{V_{dd}}{Ax} & C \end{aligned}$$

$$C(1+A) \frac{V_{dd}}{A} + C \left[\frac{V_{dd}}{A} - \frac{V_{dd}}{A} \right]$$

$$\frac{V_{dd}}{A}$$

$$= \frac{CV_{dd}}{\frac{V_{dd}}{A}} \left[\frac{1+A}{A} + 1 - \frac{1}{A} \right] = C(1+1) - 2C$$

Time

C_{ap}

$C(1+A)$

$$\frac{V_{dd}}{A}$$

$$\frac{1}{2} \frac{V_{dd}}{A} - \frac{V_{dd}}{A} C$$



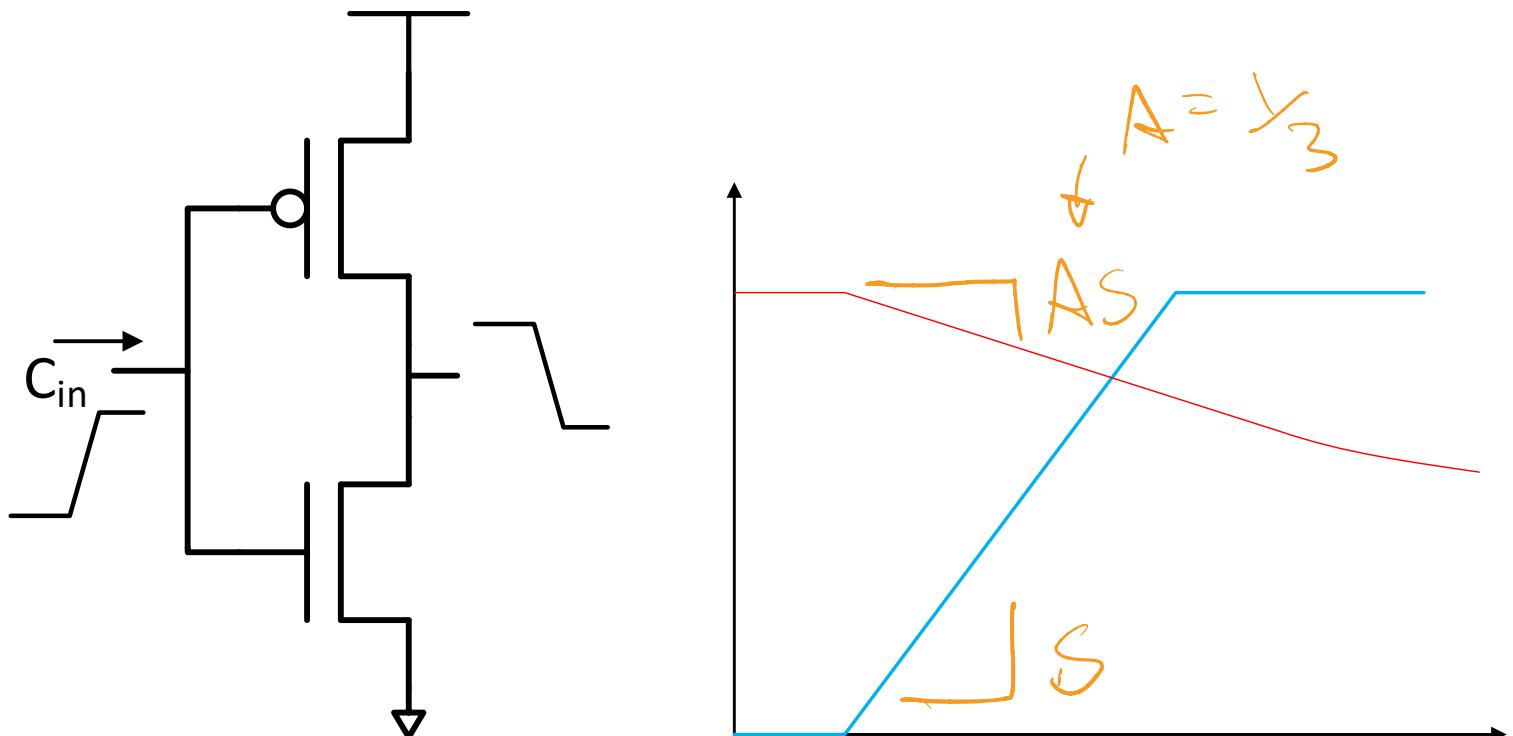
~~2C~~

3C



Miller Capacitance in Inverters (contd.)

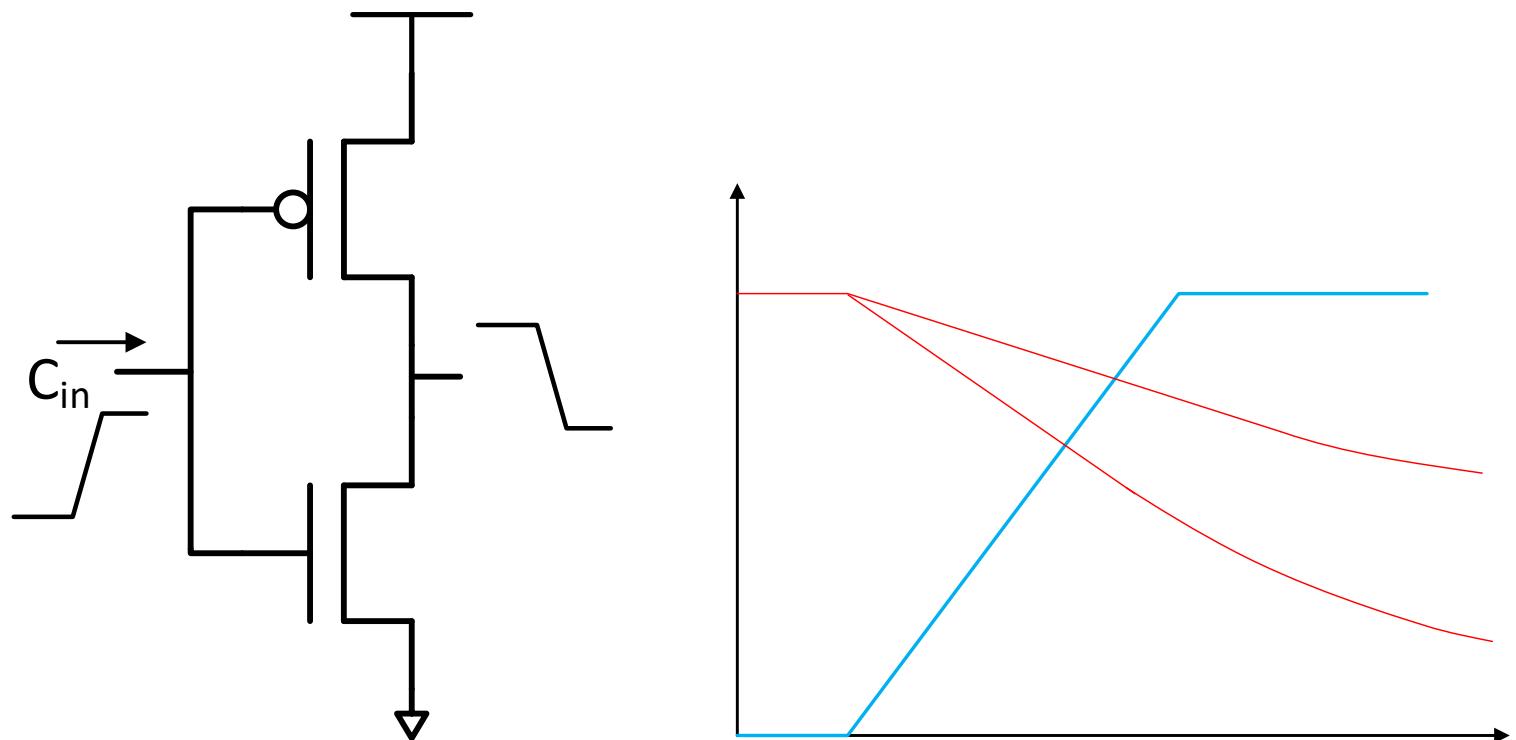
- Perceived capacitance different for power and delay
 - Faster transition rate \Leftrightarrow Higher miller cap, but for a shorter time
 - Energy impact (C_{gd} increases by a factor of ~ 2)
 - Delay impact (maximum delay-relevant miller cap multiplier is ~ 3)



$$A = -\frac{1}{3}$$

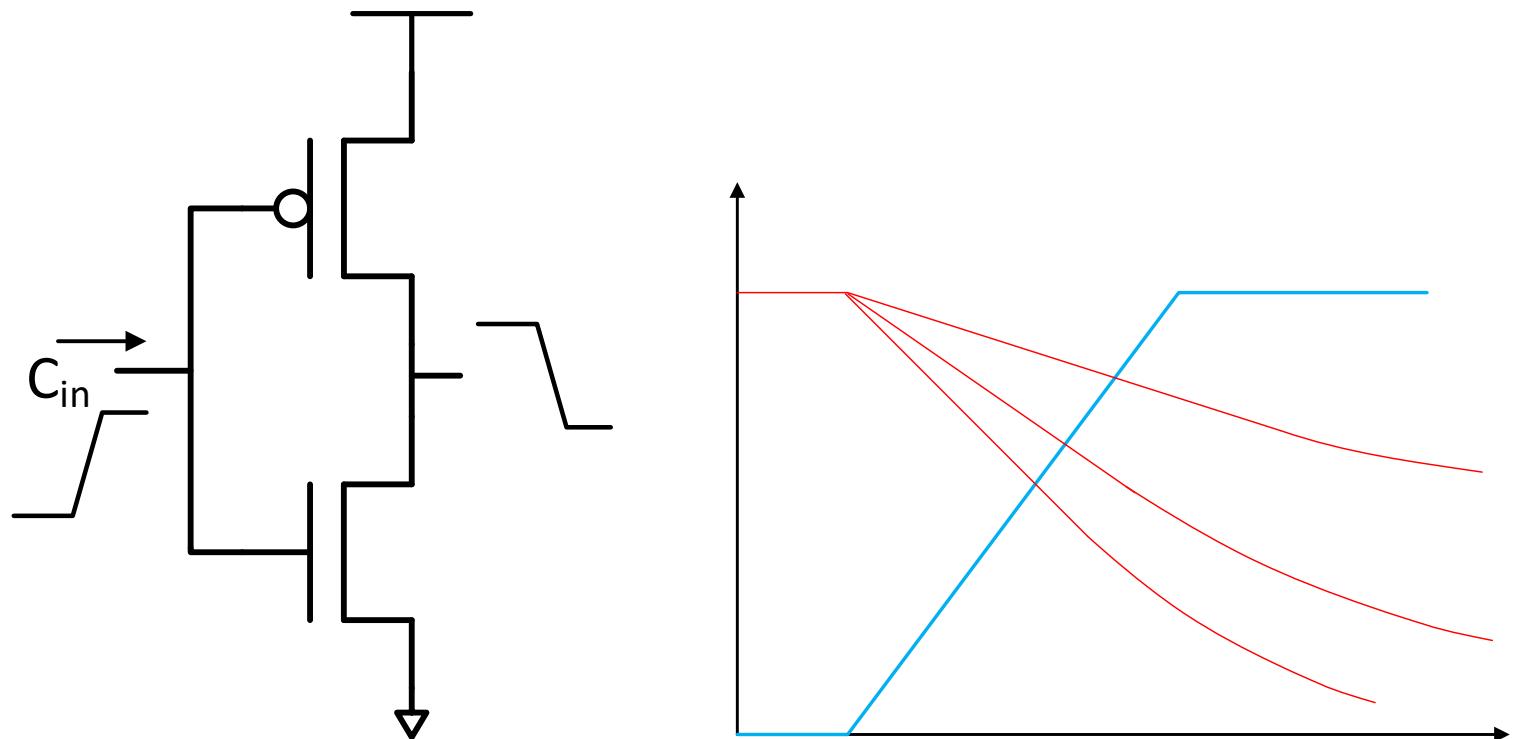
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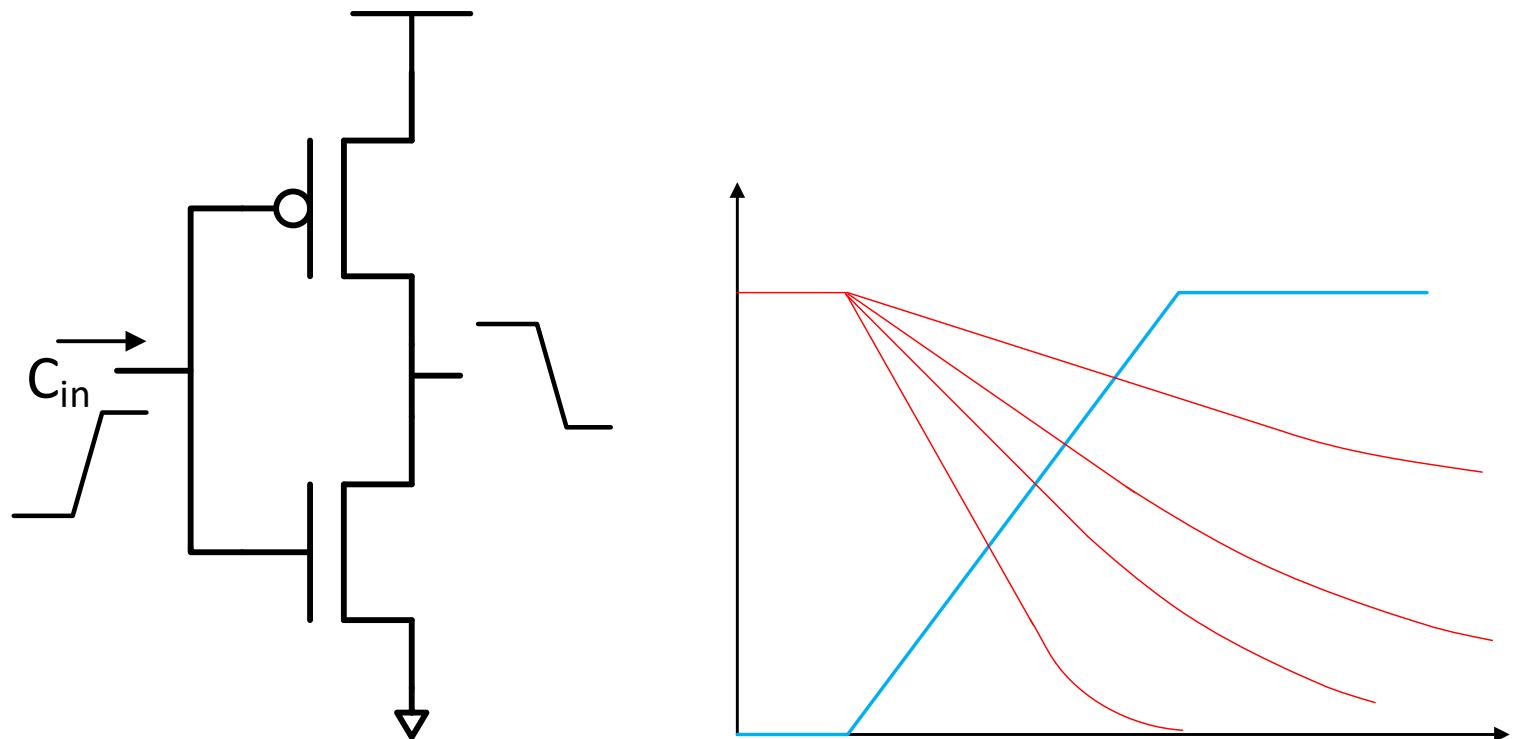
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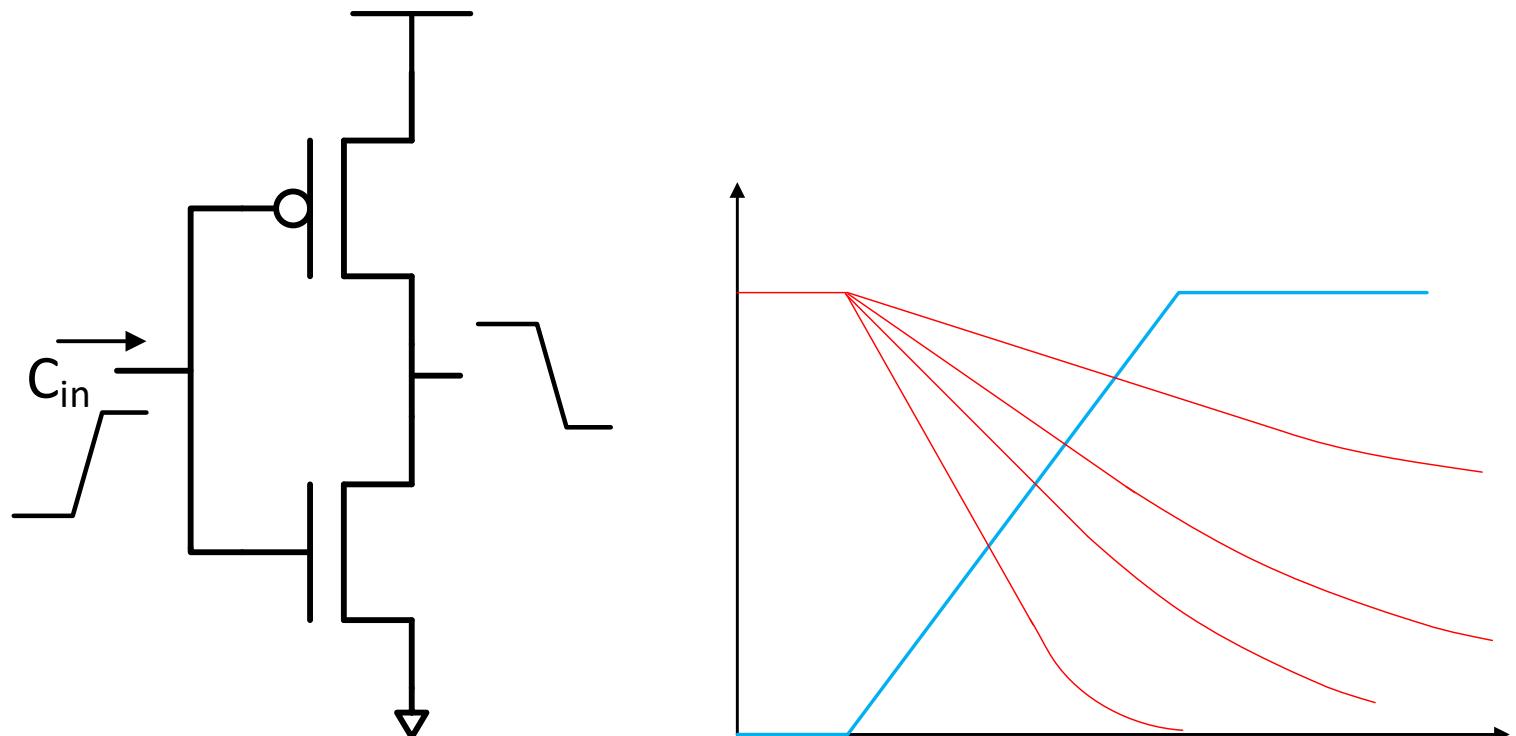
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 - Energy impact (C_{gd} increases by a factor of ~ 2)
 - Delay impact (maximum delay-relevant miller cap multiplier is ~ 3)



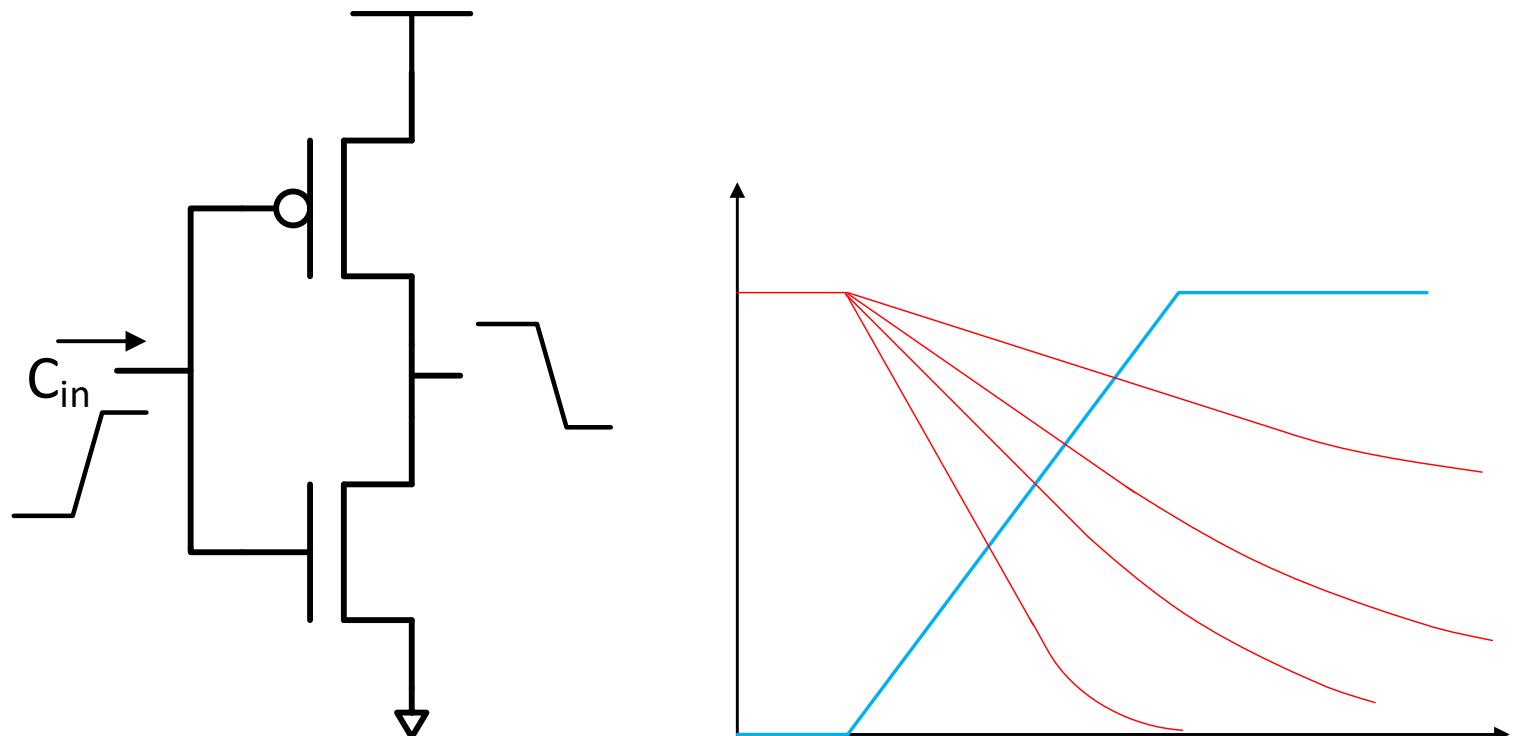
Miller Capacitance in Inverters (contd.)

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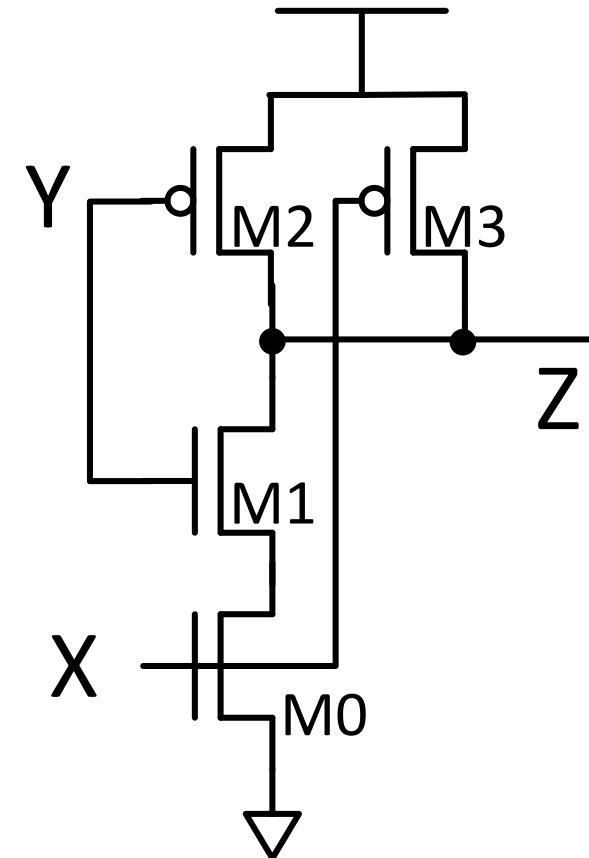
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- Miller cap affects both input and output



Miller Capacitance in CMOS gates

- Breakout: What signal transitions result in the worst case input cap for M1?



Reading Assignments

- Required:
 - From sand to a wafer:
<http://www.youtube.com/watch?v=i8kxymmjdoM>
 - Nice video of simplified process fabrication step at :
http://www.youtube.com/watch?v=OBiu2agne_U
 - Slightly more up-to-date overview of process fabrication
<http://www.youtube.com/watch?v=-GQmtITMdas&list=PL17EE400FD24FFE20&index=7>
- Recommended :
 - Section 1.5
 - Weste&Harris , Chapter 2-2.2
- Optional
 - Weste & Harris , Chapter 2-2.4

Reading assignment

- Section 1.5
- Optional Reading
 - Read up on body effect
 - Velocity saturation and the short channel transistor model