

# Lecture topics

## Background

L1 - Introduction

L2 - CMOS Logic

L3 - Basic MOSFET Theory

## VLSI Basics

L4 - Inverter Fabrication and Layout

L5 - The CMOS Inverter (Noise Margin and DC Characteristics)

L6 - Delay of CMOS Gates

L7 - Power Consumption of CMOS Gates

L8 - Timing Elements (Flip Flops and Latches)

L9 - Pipelining and Sequential Design

## VLSI Building Blocks

L10 - Register File Design

L11 - Datapath Elements

L12 - Memories

L13 - Adders

L14 - Multipliers

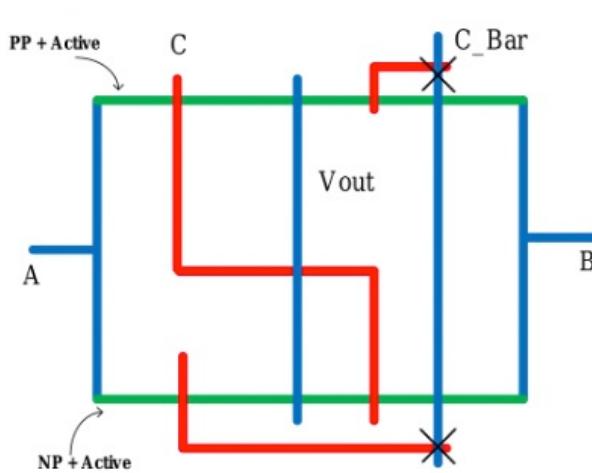
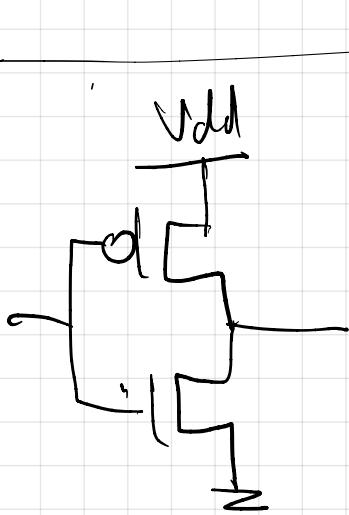
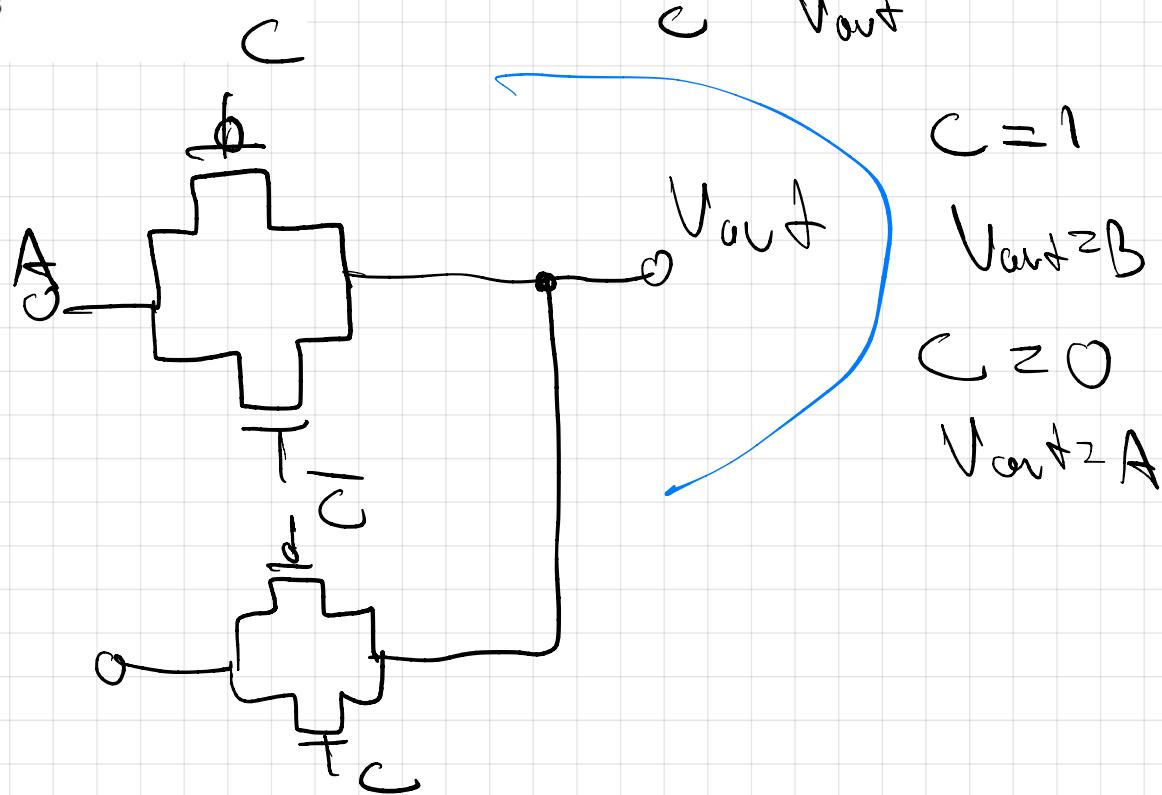
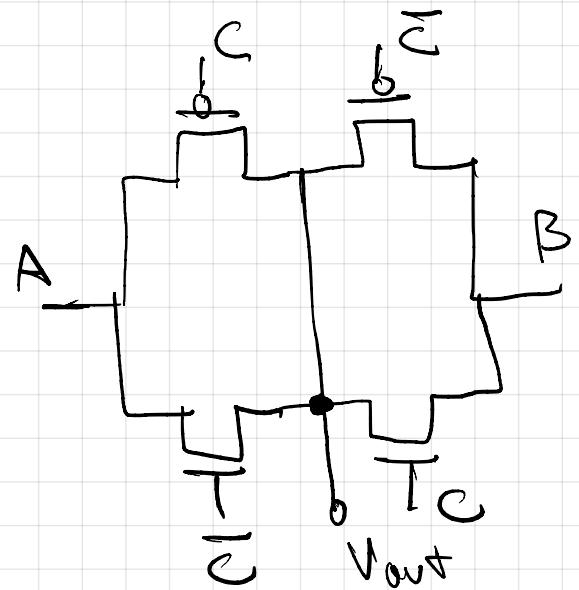


Figure 3



1. [3+3 points] For the circuit given below (Figure 1), assuming all the gates have the same delay of 2ps, calculate the latest arrival time at any of the outputs if:

- All signals arrive at the same time,  $t=0\text{ps}$
- Signals arrive at the following times ( $a=0\text{ps}$ ,  $b=10\text{ps}$ ,  $c=2\text{ps}$ ,  $d=2\text{ps}$ ,  $e=0\text{ps}$ )

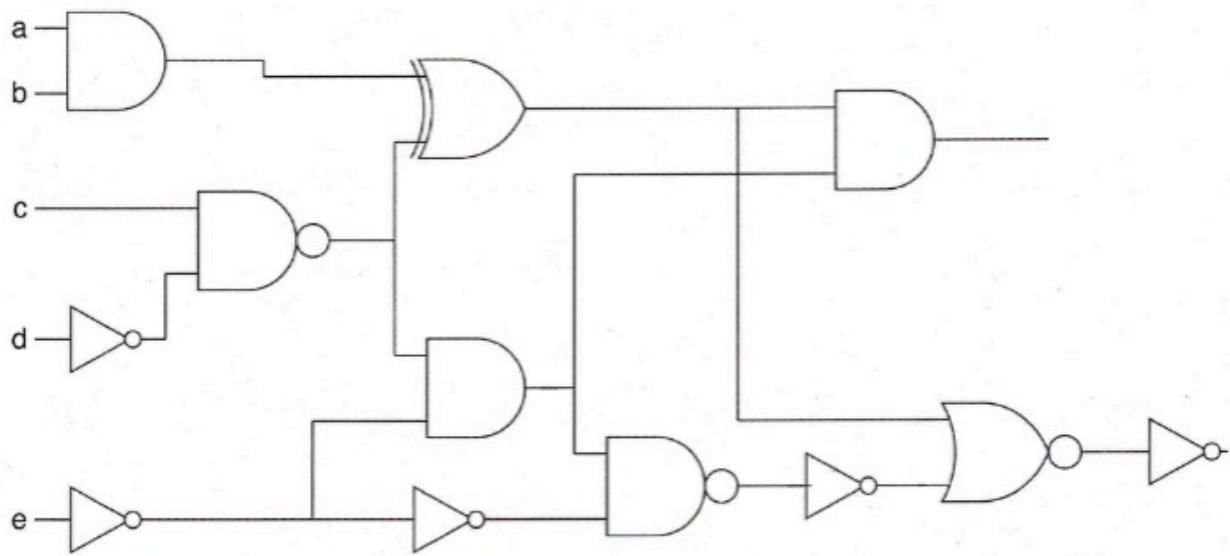


Figure 1

2. [6 points] Write down the CMOS implementation of the following Boolean function in as few **2-input nand and nor gates** as possible. You may use inverters if needed but no other gates are allowed.

$$F = ab + cd + bc + ad$$

3. [5 points] If the delay for a unit step input for the loaded inverters in Figure 2 (a) and (b) are as follows, what is the delay for (c)?

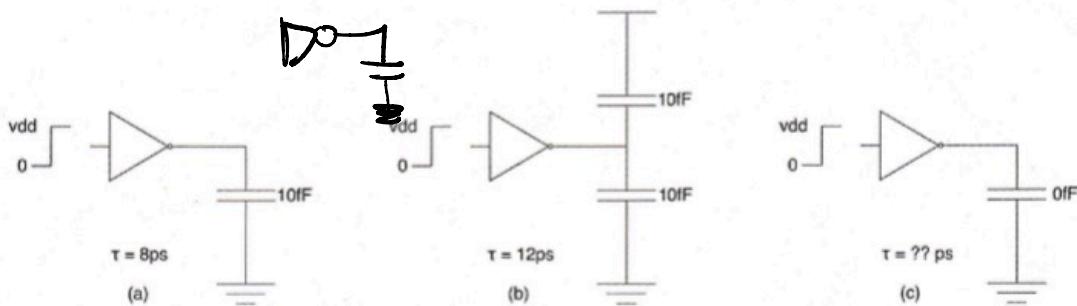


Figure 2

$$\tau = R_{\text{eff}} \cdot C + P_d$$

$$\tau \approx \frac{1}{2} \frac{C V_{dd}}{I_S}$$

$$C = C_{SL} + C_L$$

$$\tau \approx \frac{1}{2} \frac{C_{SL} V_{dd}}{I_S} + \frac{1}{2} \frac{V_{dd}}{I_S} \cdot C_L$$

Pd      Reff

$$\text{c)} \quad \tau = R_{\text{eff}} \cdot C + P_d$$

$$= P_d = 4\text{ps}$$

$$\text{a)} \quad 8\text{ps} = R_{\text{eff}} \cdot 10\text{fF} + P_d$$

$$\text{b)} \quad 12\text{ps} = R_{\text{eff}} \cdot 20\text{fF} + P_d$$

$$16\text{ps} = R_{\text{eff}} \cdot 20\text{fF} + 2P_d$$

$$4\text{ps} = P_d$$

4. [8 points] For the following circuit (Figure 3), assuming the inverters are sized such that the rising waveforms at b and c are identical, and the falling waveform at a has the same 50% crossover point and transition time as b and c. Find the rise delay for the given transition at b.

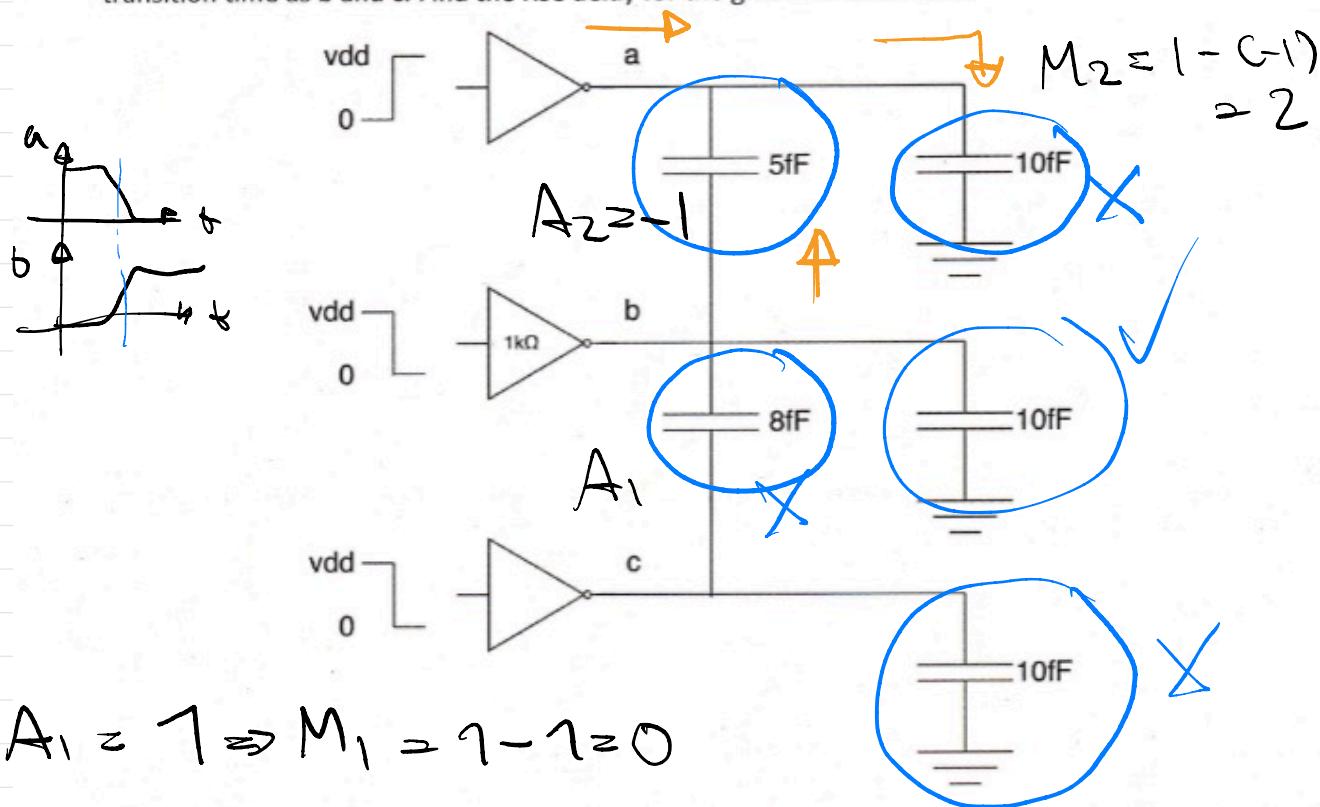
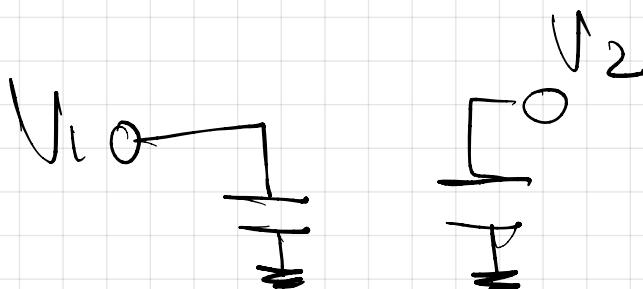
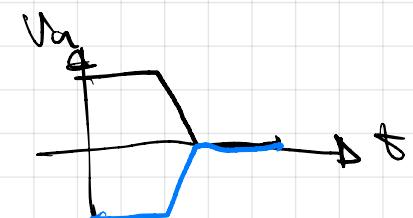
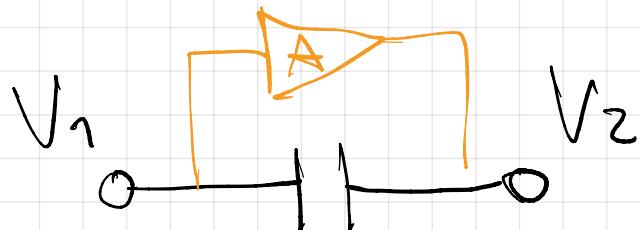
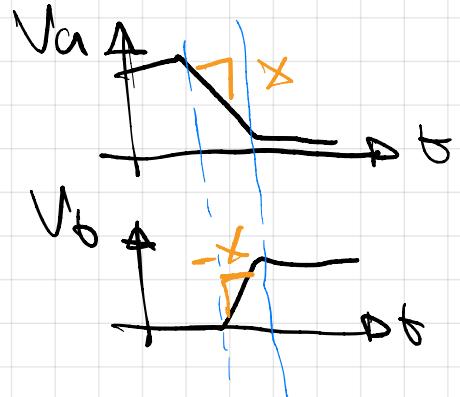


Figure 3

$$\tau = R_{\text{eff}} \cdot C + R_d \cdot C$$

$\approx 1 \text{ k}\Omega \cdot 10 \text{ fF}$

$$C_b = 10 \text{ fF} + (5 \text{ fF}) \cdot 2$$



5. [5+4+4+2 points] For the following circuit (Figure 7)

- draw the transfer function. Label only the the points that mark transitions in operating region for the inverter (i.e. where any of the devices changes its mode of operation such as from linear to saturation for example). **Do not solve for  $V_{out}$  when  $V_{in}=0$  or  $V_{in}=V_{dd}$**  Note,  $V_{th}$  is -0.2 for both nmos and pmos. Your sketch will be graded on the general shape of the curve.
- When pmos is at the edge of saturation/linear
- When nmos is at the edge of saturation/linear
- $V_i = V_{dd}/2$

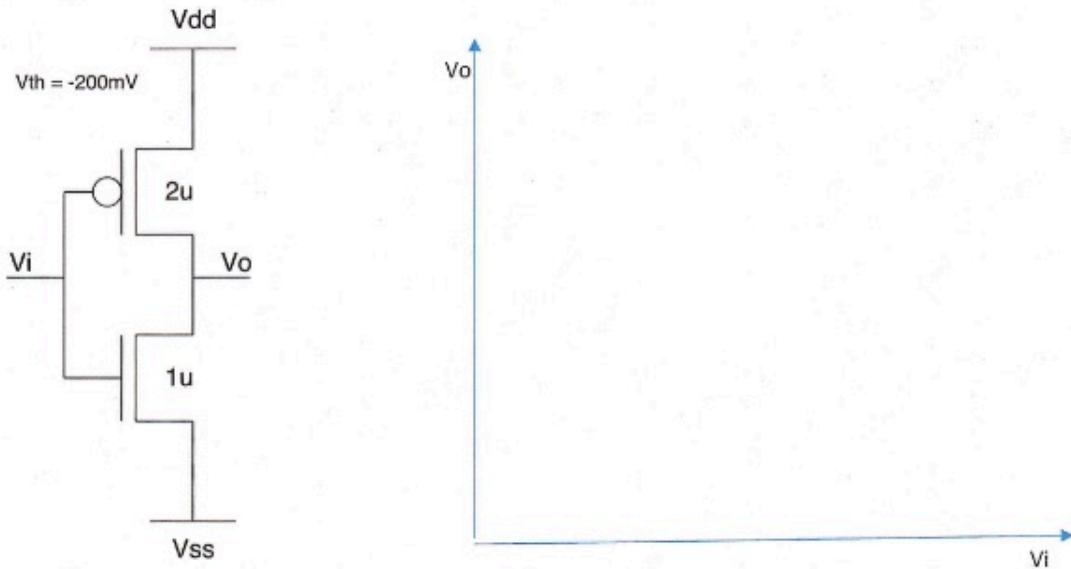


Figure 4

6. [10 + 5 = 16 points] Consider the novel gate topology proposed in Figure.
- Sketch the DC transfer function of such a gate assuming  $V_{dd}=1V$ . Label all points of transition in the operating region of either transistor. **Do not solve for  $V_{out}$  values when  $V_{in}=0$**  (too much repetitive work). You will be evaluated based on the shape of the curves and labeling of key points.
  - What is the disadvantage of implementing long cascades of such a logic gate in terms of voltage values corresponding to logic 1 and logic 0 (Write your answer down in no more than 10 words)

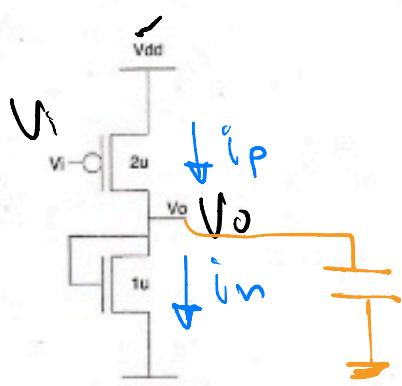


Figure 5

$$i_P = i_N$$

PMOS:  $V_{SG} = V_{dd} - V_i$

NMOS

$$V_{SD} = V_{dd} - V_o$$

$$V_{GS} = V_o - V_{ss} \xrightarrow{AO} = V_o$$

$$V_{DS} = V_o$$

NMOS : Cutoff?  $V_{gs} \geq V_{th}$  cutoff ( $V_o < V_{th}$ )

$V_o \geq V_{th}$  saturation

Saturation?  $V_{gs} - V_{th} \leq V_{ds}$   
Yes  $V_o - V_{th} \leq V_o$

PMOS: Cutoff  $V_{sg} < V_{th}$

$$V_{dd} - V_{in} < V_{th}$$

$$V_{dd} - V_{th} < V_{in}$$

Assume it's on:  $V_{dd} - V_{in} \geq V_{in}$

Saturation?

$$V_{sg} - V_{th} < V_{ds}$$

$$V_{dd} - V_{in} - V_{th} < V_{dd} - V_o$$

$$-V_{in} - V_{th} < +V_o$$

$$V_{in} + V_{th} \geq V_o$$

NMOSI

cutoff

$$V_o < V_{th}$$

saturation:

$$V_o \geq V_{th}$$

PMOSI

cutoff

$$V_{dd} - V_{th} < V_m$$

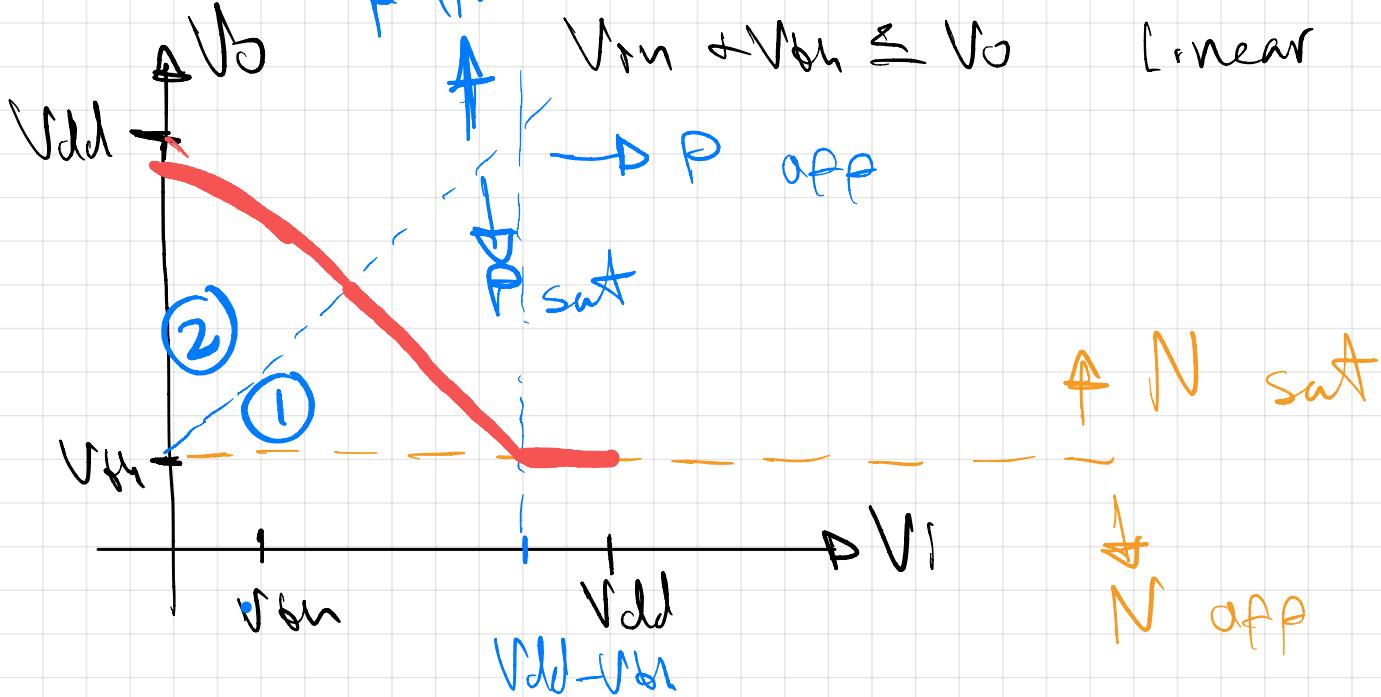
$P_{lin}$

$$V_m + V_{th} > V_o$$

$$V_m + V_{th} \leq V_o$$

saturation

linear



$$\textcircled{1} \quad I_{Dsat} = I_{Nsat}$$

~~$\mu_p C_{ox}$~~

~~$$\frac{1}{2} \cancel{\mu_p} \frac{W_p}{C} (V_{gs} - V_{th})^2 = \frac{1}{2} \cancel{\mu_n} \frac{W_n}{L} (V_{gs} - V_{th})^2$$~~

$\mu_n C_{ox}$

$$(V_{dd} - V_m - V_{th})^2 = (V_o - V_{th})^2$$

$$\Rightarrow V_{dd} - V_m - V_{th} \approx V_o - V_{th}$$

$$\Rightarrow V_o = V_{dd} - V_m$$

\textcircled{2}

$$\beta = \mu_n C_{ox} W$$

$$\beta = \mu_n C_{ox}$$

7. [2+6 points] For the given circuits in Figure 9, (a) and (b), find  $V_o$  and the state in which device A and B is in (linear/saturation/cutoff). Assume no leakage in the transistors. Fill up Table 1 to indicate your answers.

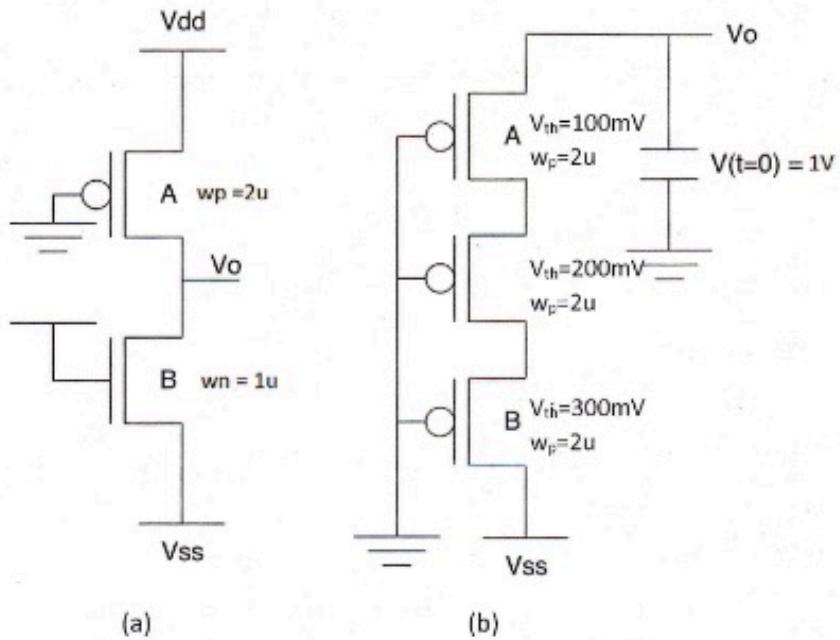


Figure 6

Table 1

	$V_o$	State of device A	State of device B
(a)			
(b)			

8. [3+4+2 points] For the circuit in Figure 10 (a), a unit step input is applied at  $t=0$ s. Assume all load capacitance is  $10\text{fF}$  in this problem. **Assume a  $V_{th}$  of 0.5V.**
- What should be the value of  $W$  for which current through the NMOS at  $t=0+$  is equal in Fig. 7a and Fig. 7b?
  - What is the time at which  $V_c=0.5\text{V}$  for Fig. 7a?
  - What is the time at which  $V_c=0.5\text{V}$  for Fig. 7b?

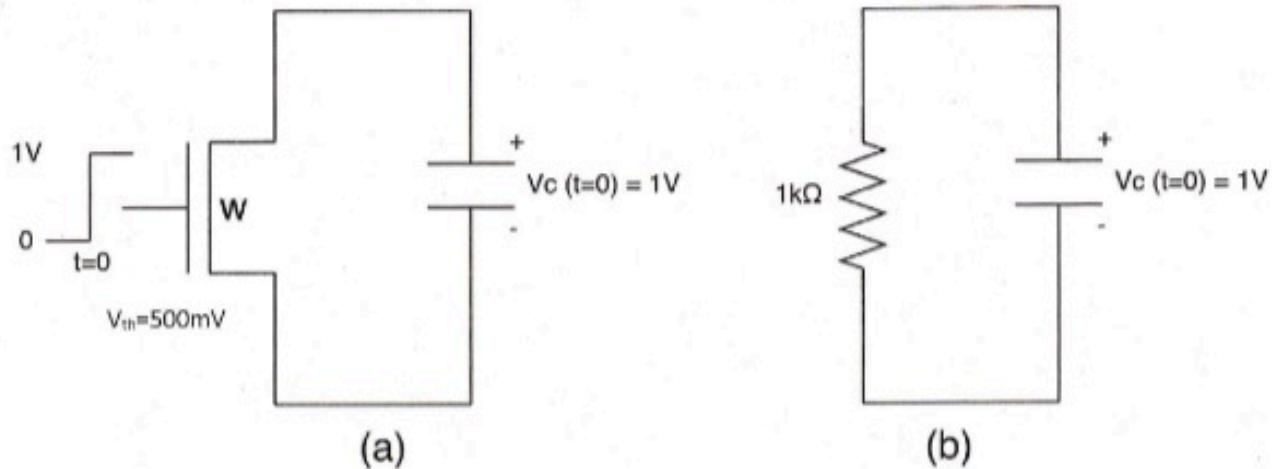


Figure 7