EE476 Midterm Examination /80

12/9/21

I have not received nor obtained help from anyone in the completion of this examination. During the course of this mid-term examination I have not engaged with any form of communication with my peers on any aspect of the contents of this exam. I understand that strict action will be taken resulting from my failure to comply with the mid-term examination policy. I also understand that it is my duty to not only adhere to the mid-term exam policy, but also report any other individual(s) who are violating this policy.

Name: _____

Signature: _____

Duration: 1 h 50m

Assumed that all devices have 0 leakage current. Unless otherwise stated, the following default parameters apply:

Vdd	1V
ε_r (Silicon-di-Oxide)	3.8
ε_0	8.85 E-12 F/m
λ	0
T_{ox}	100A
μ_n	500cm^2/V
μ_p	250cm^2/V
$V_{thn} = V_{thp}$	0.2V
W_n	1µm
W_p	2µm
Beta-ratio	2
L_n=L_p	60nm

N-channel MOSFET

Cut Off	$V_{GS} \le V_T$	$I_{DS} = 0$
Linear	$V_{GS} > V_T$, $V_{DS} \le V_{GS} - V_T$	$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$
Saturation	$V_{GS} > V_T$, $V_{DS} > V_{GS} - V_T$	$I_{DS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$

1. [3+3 points] For the circuit given below (Figure 1), assuming all the gates have the same delay of 2ps, calculate the latest arrival time at any of the outputs if:
    a. All signals arrive at the same time, t=0ps
    b. Signals arrive at the following times (a=0ps, b=10ps, c=2ps, d=2ps, e=0ps)

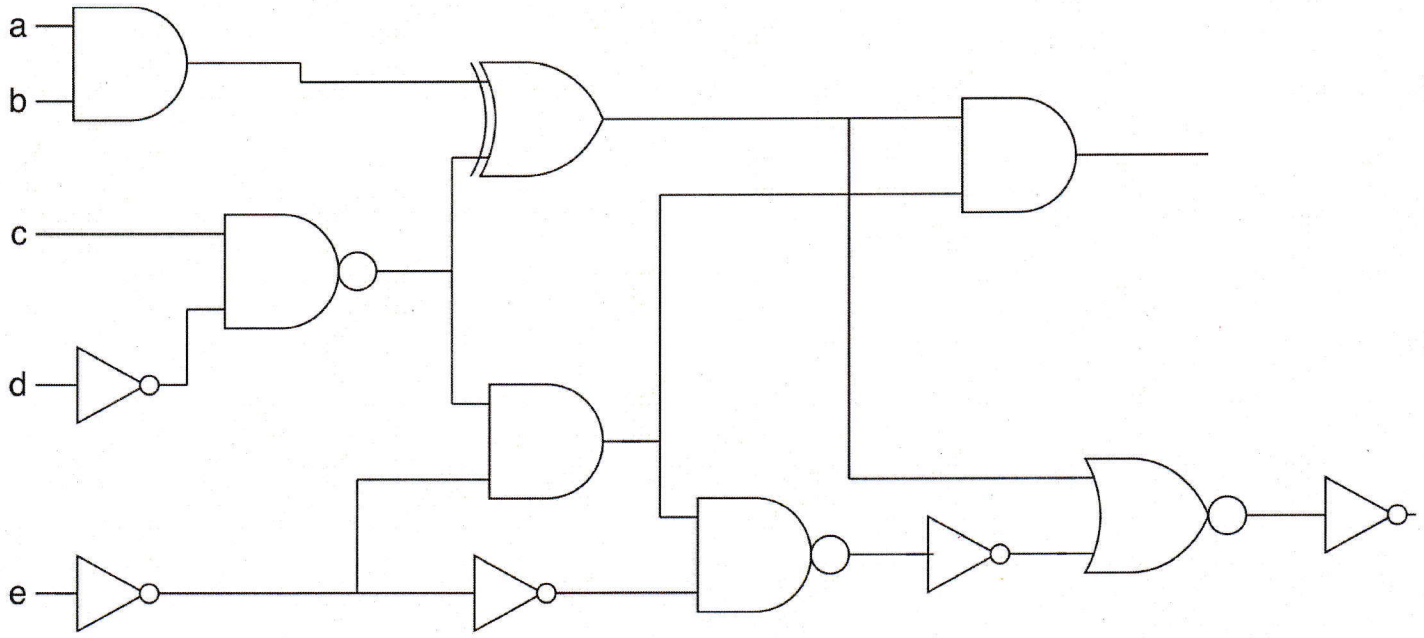

Figure 1

2. [6 points] Write down the CMOS implementation of the following Boolean function in as few **2-input nand and nor gates** as possible. You may use inverters if needed but no other gates are allowed.

$$F = ab + cd + bc + ad$$

3. [5 points] If the delay for a unit step input for the **loaded inverters** in Figure 2 (a) and (b) are as follows, what is the delay for (c)?

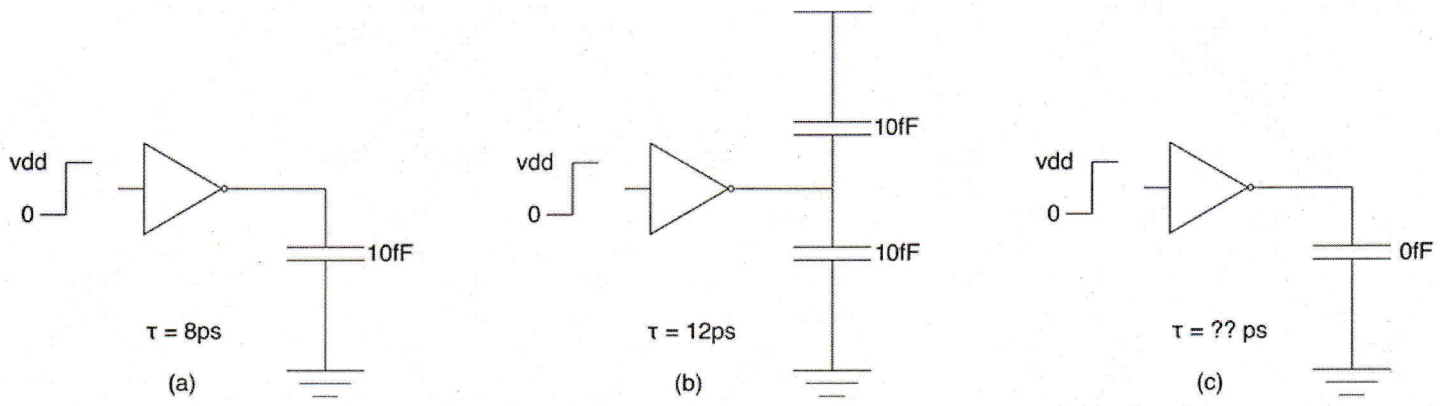

Figure 2

4. [8 points] For the following circuit (Figure 3), assuming the **inverters** are sized such that the rising waveforms at b and c are identical, and the falling waveform at a has the same 50% crossover point and transition time as b and c. Find the rise delay for the given transition at **b**.

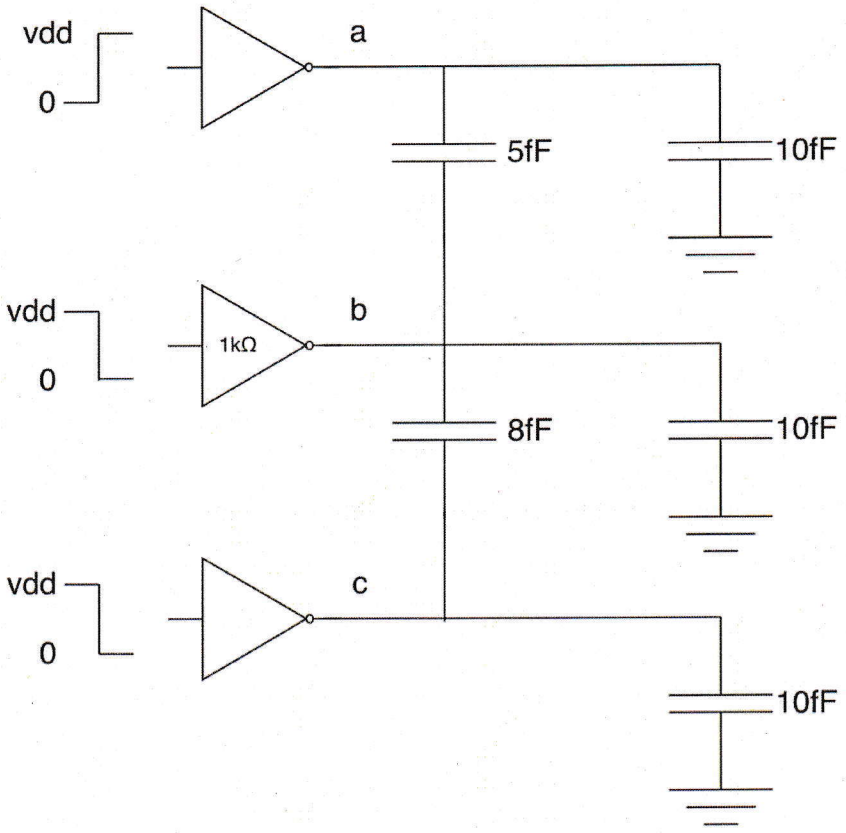

Figure 3

5. [5+4+4+2 points] For the following circuit (Figure 7)
    a. draw the transfer function. Label only the the points that mark transitions in operating region for the inverter (i.e. where any of the devices changes its mode of operation such as from linear to saturation for example). **Do not** solve for Vout when V_{in}=0 or V_{in}=V_{dd} Note, **V_{th} is -0.2 for both nmos and pmos**. Your sketch will be graded on the general shape of the curve.
    b. When pmos is at the edge of saturation/linear
    c. When nmos is at the edge of saturation/linear
    d. Vi = Vdd/2

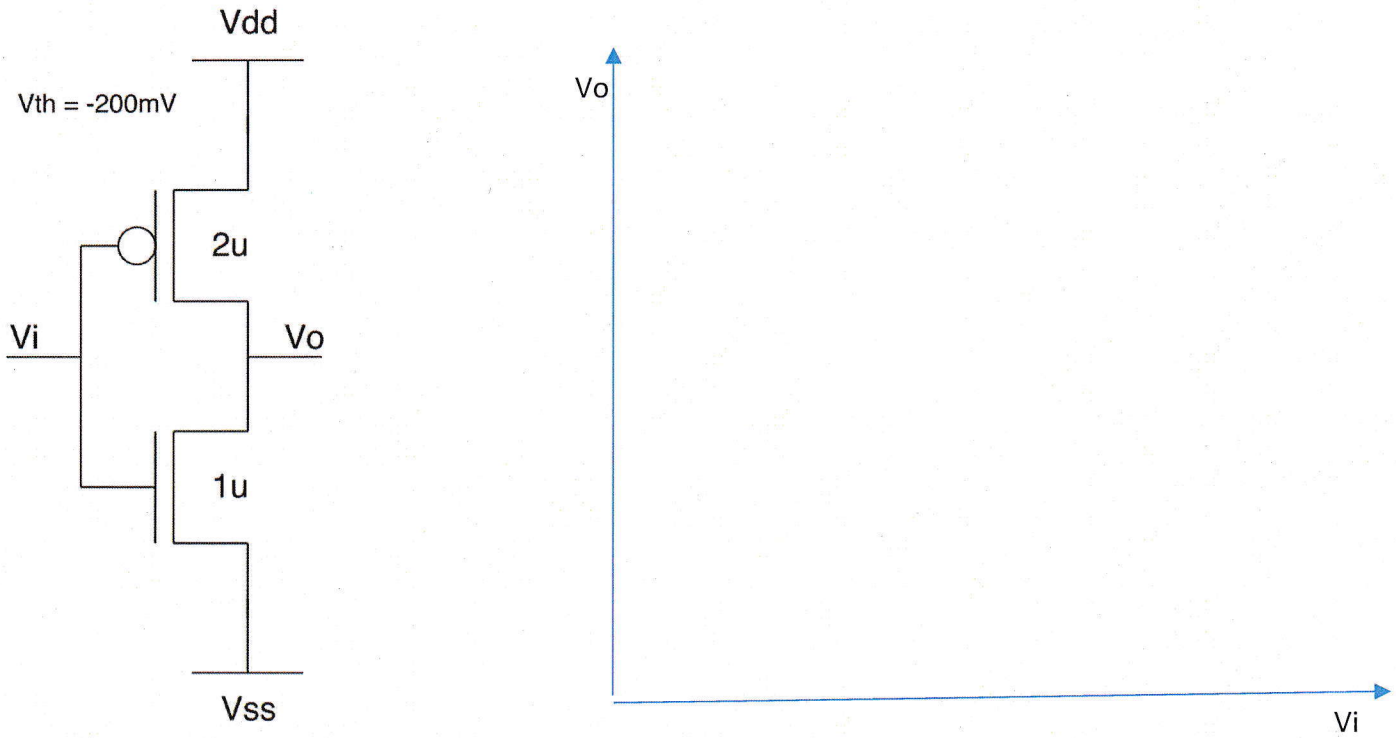

Figure 4

6. [10 + 5 = 16 points] Consider the novel gate topology proposed in Figure.
   a. Sketch the DC transfer function of such a gate assuming V_{dd}=1V. Label all points of transition in the operating region of either transistor. **Do not solve for** V_{out} values when V_{in}=0 (too much repetitive work). You will be evaluated based on the shape of the curves and labeling of key points.
   b. What is the disadvantage of implementing long cascades of such a logic gate in terms of voltage values corresponding to logic 1 and logic 0 (Write your answer down in **no more than 10 words**)

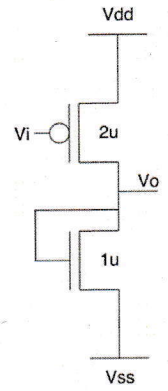

Figure 5

7. [2+6 points] For the given circuits in Figure 9, (a) and (b), find Vo and the state in which device A and B is in (linear/saturation/cutoff). Assume no leakage in the transistors. Fill up Table 1 to indicate your answers.

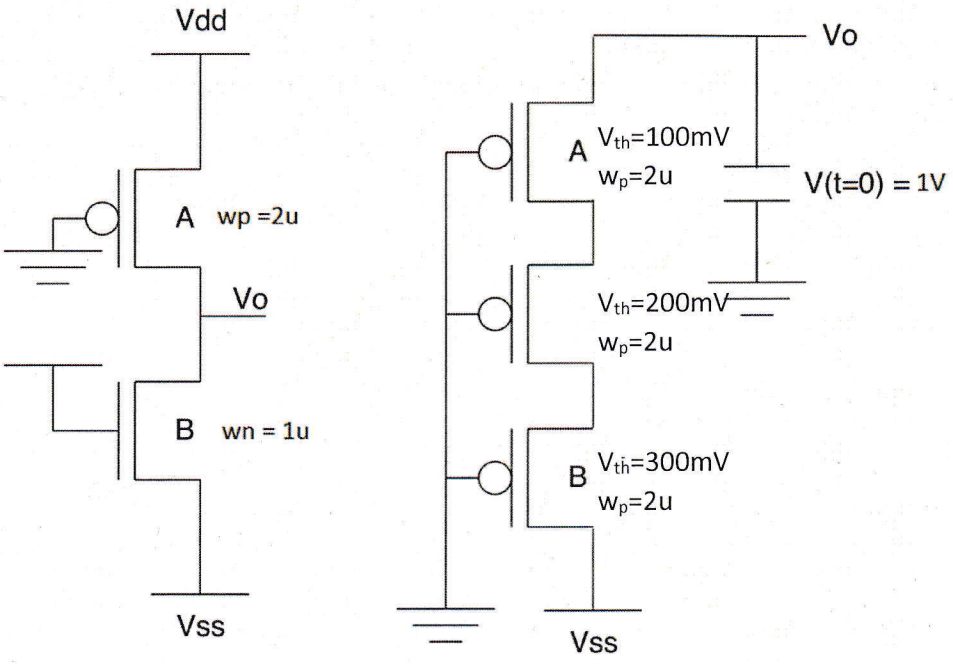

Figure 6

Table 1

	Vo	State of device A	State of device B
(a)			
(b)			

8. [3+4+2 points] For the circuit in Figure 10 (a), a unit step input is applied at t=0s. Assume all load capacitance is 10fF in this problem. **Assume a V_{th} of 0.5V**.
    a. What should be the value of *W* for which current through the NMOS at t= 0+ is equal in Fig. 7a and Fig. 7b?
    b. What is the time at which V_c=0.5V for Fig. 7a?
    c. What is the time at which V_c=0.5V for Fig. 7b?

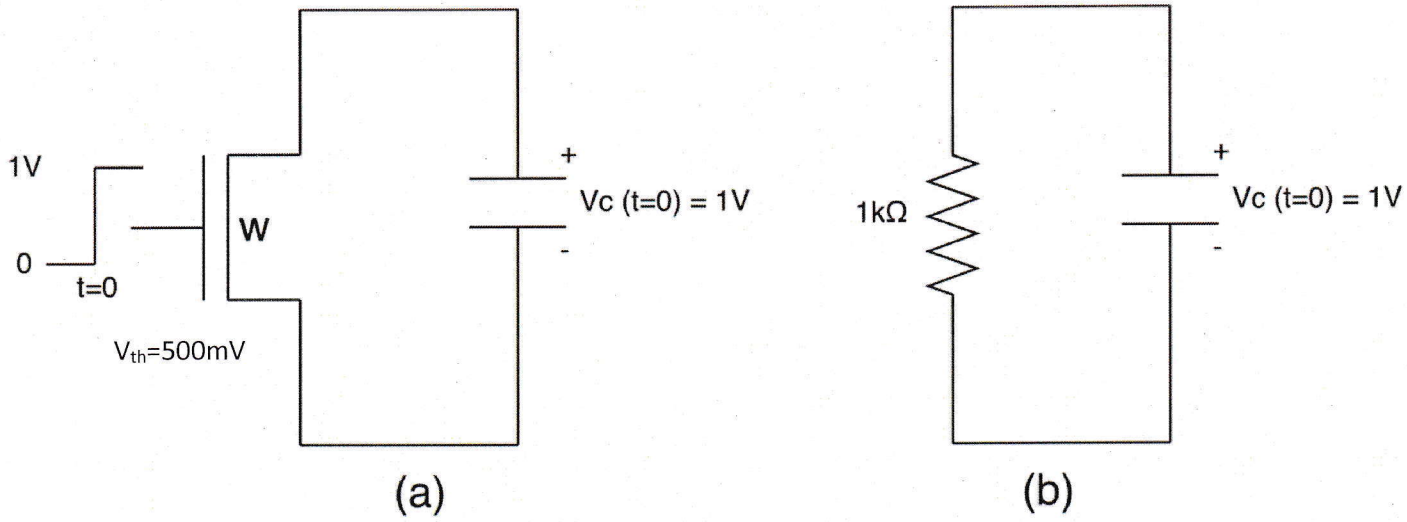

Figure 7

9. [8 points] Consider the timing element shown in Fig. 8. When considering the timing implications of this structure, consider it a timing element referenced at the rising edge of clock.
    a. When does it capture data at its input?
    b. When does it release data at its output?
    c. What is one advantage of such a structure (from a timing perspective)?
    d. What is one disadvantage of such a structure (from a timing perspective)?

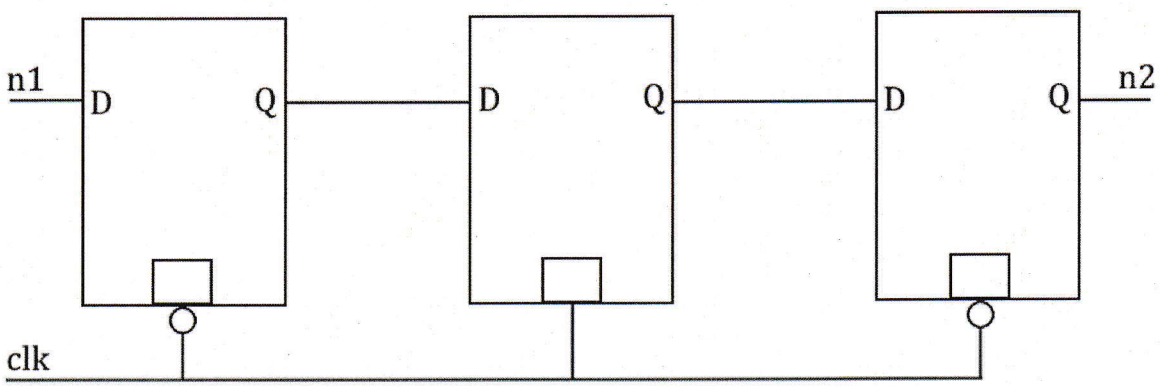

Figure 8