EE476 Midterm Examination /75

12/2/20

I have not received nor obtained help from **anyone other than my randomly assigned mid-term teammate** in the completion of this examination. Specifically, I have not entered into any type of discussion (verbal, text, figure or any other form of communication medium) regarding material in this exam or any theoretical material covered in this course with anybody during the course of the exam. I understand that it is my duty to not only adhere to the mid-term exam policy, but also report any other individual(s) who are violating this policy.

Name: _____

Signature: _____

Duration: Wed 12.01pm to Friday (12/4/20) @11.59pm

Unless otherwise stated, the following default parameters apply:

Vdd	1V
ε_r (Silicon-di-Oxide)	3.8
ε_0	8.85 E-12 F/m
λ	0
T_{ox}	100A
μ_n	500cm^2/V
μ_p	250cm^2/V
$V_{thn} = V_{thp}$	0.2V
W_n	1µm
W_p	2µm
Beta-raio	2
$L_n=L_p$	60nm
V_{dd}	1V

N-channel MOSFET

Cut Off	$V_{GS} \le V_T$	$I_{DS} = 0$
Linear	$V_{GS} > V_T,\ V_{DS} \le V_{GS} - V_T$	$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$
Saturation	$V_{GS} > V_T,\ V_{DS} > V_{GS} - V_T$	$I_{DS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$

1. [5 points] Write down the CMOS implementation of the following Boolean function in as few gates as possible. Assume you get inverted input signals for free, and **you can use only nand and nor gates**:

$$F = ab + \bar{a}c + bc$$

2. [5 points] Construct a 2-input XOR gate using 2-input NAND gates **and NAND gates only**.

3. [3+3+3=9 points]Consider the figures shown below.
   a. For the circuit in Fig. 1a what is the delay associated with a step transition (one rising and one falling) as shown in the figure. Assume that output resistance of the inverters is 1kΩ

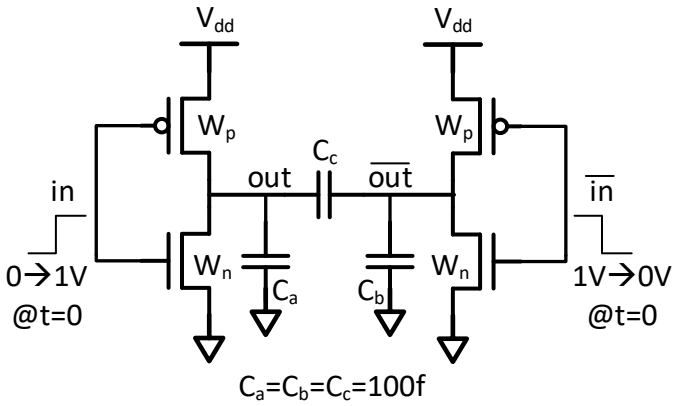


Figure 1a

b. Consider Fig. 1b below: Assume that output resistance of the inverters is driving za are 1kΩ. Assume worst case conditions for the circuit driving zb so that the delay between za and zb is as high as possible. What is the worst case delay for the a→za transition.
c. Consider Fig. 1b below: Assume that output resistance of the inverters is driving za are 1kΩ. Assume best case conditions for the circuit driving zb so that the delay between za and zb is as low as possible. What is the best case delay for the a→za transition.

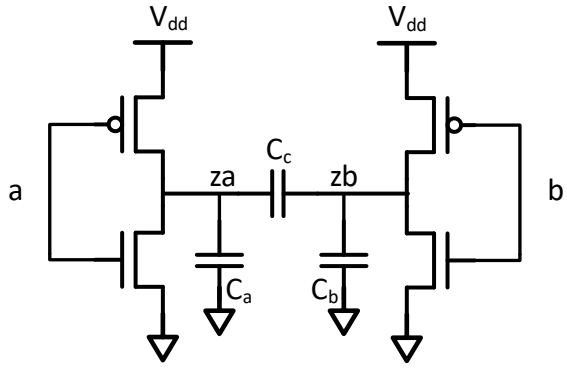


Figure 1b

4. [3+1 = 4 points] Consider the stick diagram in figure 2.
    a. Write down the boolean equation describing the gate
    b. What is the functionality of the gate. Don't give us a formula, just describe the function?

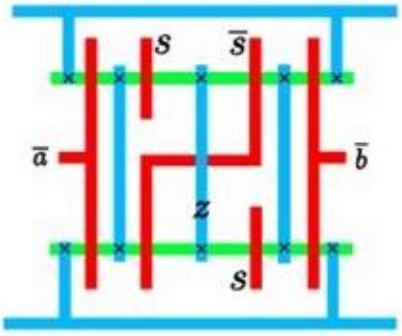


Figure 2

5. [4 points] Consider the logical circuit shown in Figure 3. Draw the minimal transistor-level cmos complex gate implementation of the gate.

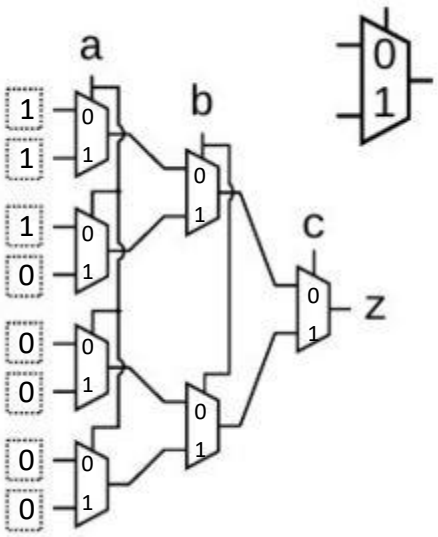


Figure 3

6. [5+5=10points]
    a. Consider the inverter shown in Figure 4a. Draw the transfer function of the inverter
    b. Consider the inverter shown in Figure 4b. Overlay the transfer function of this inverter over your solution from 6a above.

DRAW YOUR FINAL ANSWERS OVERLEAF ON THE PROVIDED AXES. Be sure to label key points of the transfer function such as transitions from linear/cutoff/saturation etc.

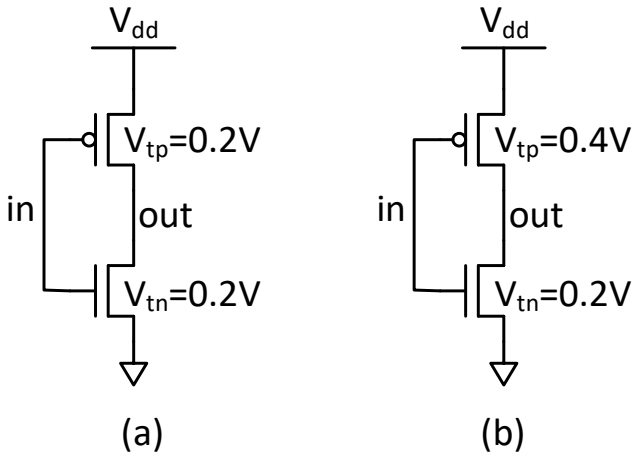
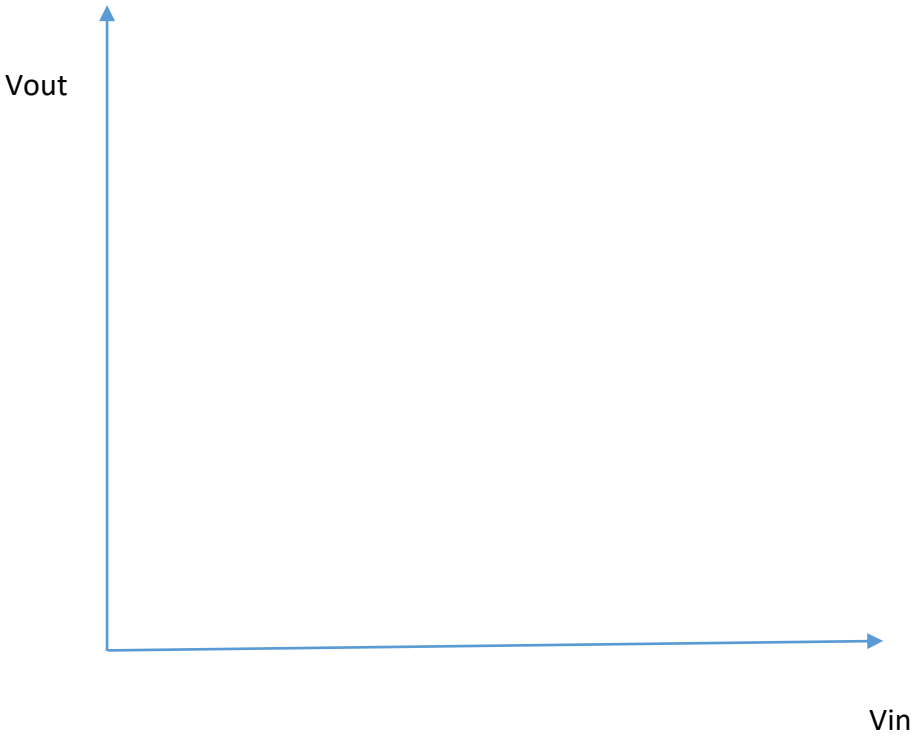


Figure 4



7. [5+5 =10 points] Consider the digital circuit shown in Figure 5. Optimize the circuit to only use inverting CMOS gates (replace ANDs and ORs with NORs and NANDS), you're free to leave XORs alone. You **must convert any MUX to an inverting mux.** You *may* need inversion of inputs to make this work and that would be ok.

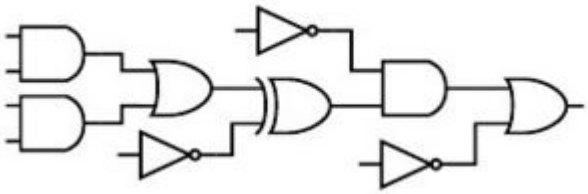


Figure 5

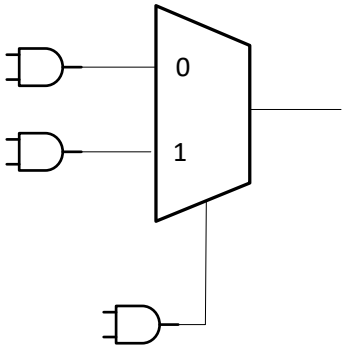


Figure 6

8. [3 + 3 + 3 =9 points] Note the delay for a unit step input for the **loaded inverters** in Figure 7 (a) and (b).

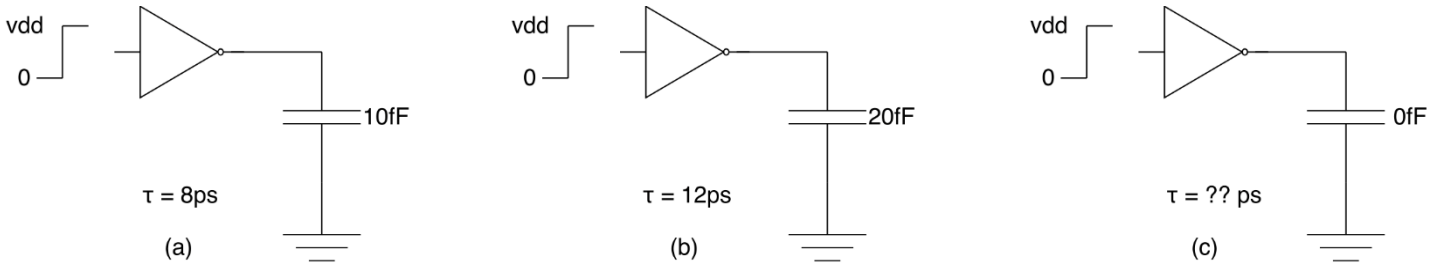


Figure 7

a. What is the delay for (c)?

b. What is the effective resistance of the inverter?

c. Estimate the resistance of this inverter at Vdd = 0.6V, Vth= 0.3V (Note that the delays reported above were for Vdd = 1V, Vth = 0.2V)

9. [12 points] Consider the inverter cascade in Fig. 8. **Use the delay formulation of $\tau = R_i C_{i+1}$ to figure out inverter input capacitance assignments for x and y that will minimize the delay through the chain from *in* to *out*.** Note that the standard geometric formula does not apply because the wire loading on the inverters is too large to be ignored. (Hint: Formulate the problem using first principles and then use the same maximization/minimization approach. If you really must, or have a deep aversion for evaluating derivatives, you're welcome to use python/perl/Excel-solver/Matlab or pretty much any solver mechanism to figure out your answer as well).

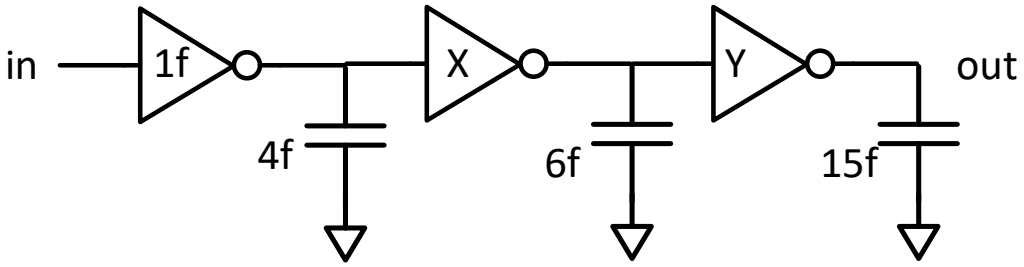
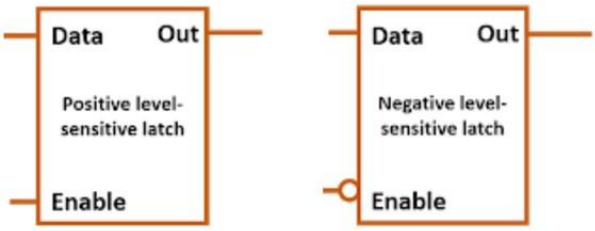


Figure 8

10. [9+3+4 = 17 points] For this problem, consider the standard cells that are constructed from the sub-blocks below:



T_{setup} = 100p
T_{hold} = -30p
T_{dq} = 140p
T_{cq} = 120p

T_{setup} = 100p
T_{hold} = -30p
T_{dq} = 140p
T_{cq} = 120p

Figure 9

a. Consider the standard cell constructed in Fig. 10 below
   i. Is this structure a timing element?
   ii. Does it sample data on an "edge" or level?
   iii. What level or edge is data sampled on?
   iv. Is data released on Q on an edge or a level?
   v. What level or edge is the data produced on Q?
   vi. What is your best estimate for its setup time ?
   vii. What is your best estimate for the clk-Q delay of the structure?
   viii. What is the pipelining overhead of this flip-flop?
   ix. What is the hold-immunity of this structure?

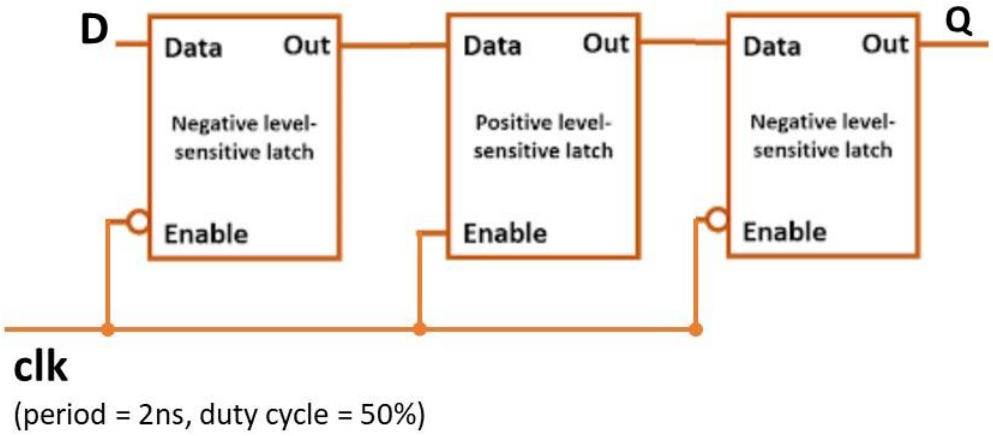


Figure 10.

b. Consider the flip-flop constructed in Fig. 11.
   i. What is your best estimate of setup time for this flip-flop?
   ii. What is your best estimate of hold time for this flip-flop?
   iii. Are there any other timing concerns with this flip-flop?

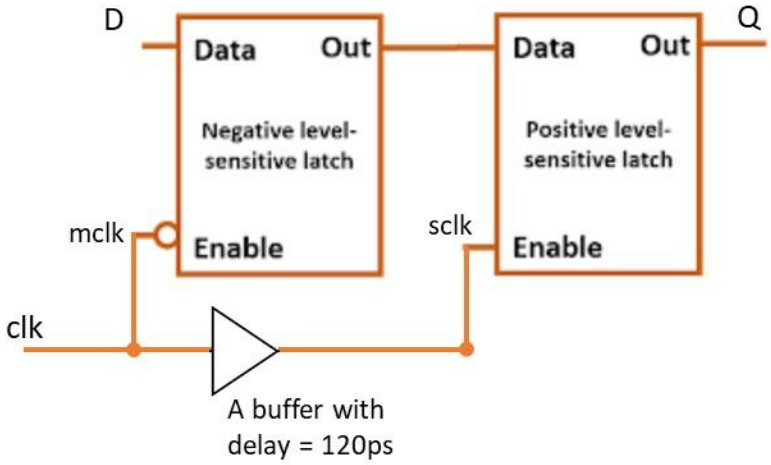


Fig. 11

c. Finally, consider the standard cell construction of Fig. 13
   i. What is your best estimate of setup time for this flip-flop?
   ii. What is your best estimate of hold time for this flip-flop?
   iii. What is your best estimate of T_{CQ} for this flip-flop?
   iv. What is the race immunity of this flop?
   v. What is the pipelining overhead of this flop?

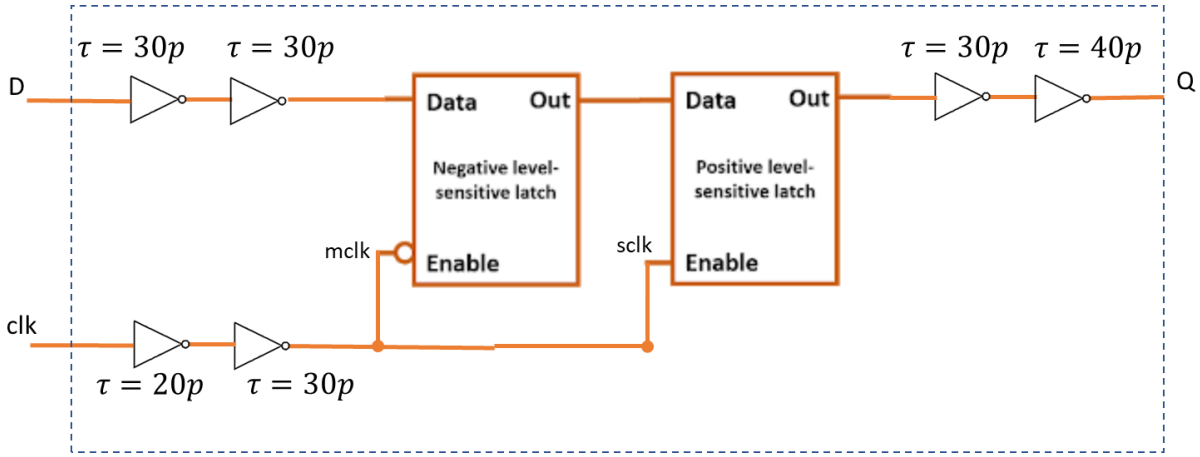


Fig. 13