

Lecture 3: Basic MOSFET Theory

Based on material prepared by prof. Visvesh S. Sathe

Acknowledgements

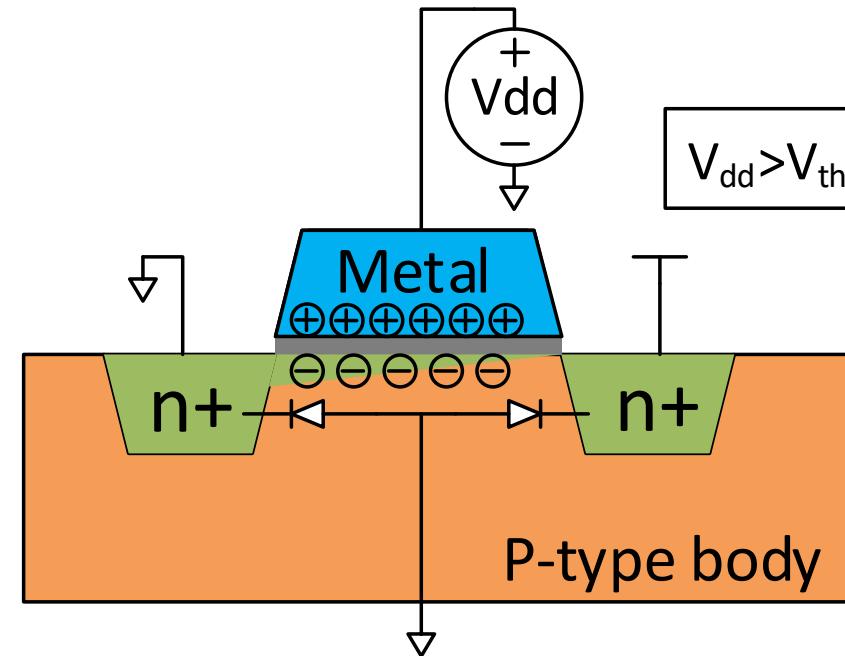
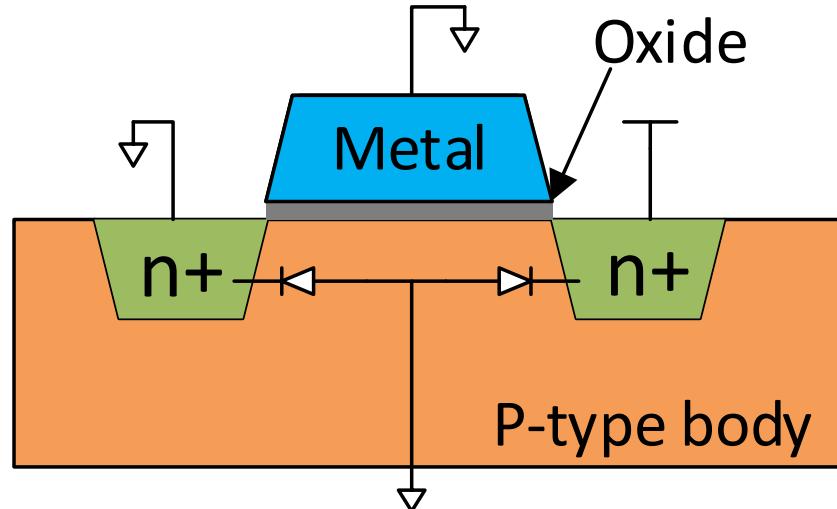
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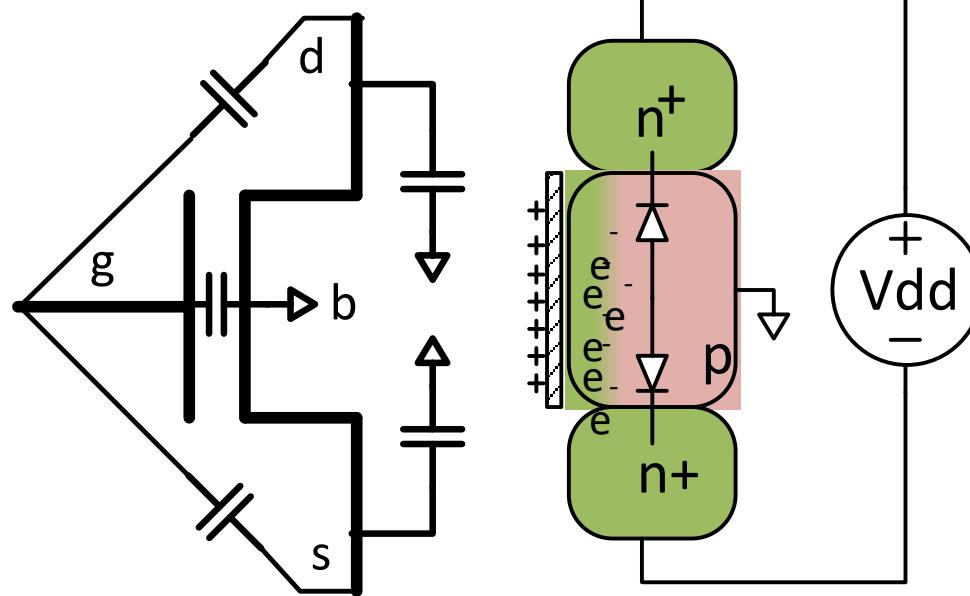
UW (2013-2022)
GaTech (2022-present)

The MOS Structure



- Metal Oxide Semiconductor
 - “Metal” implemented as poly-crystalline silicon (polysilicon) till recently
 - Conductor-insulator-semiconductor “sandwich”
 - Changing the voltage across Metal-Semiconductor varies the properties of the semiconductor

Quick Detour: Parasitic Capacitance



- What is capacitance exactly?
 - So what's so bad about it?
 - V-driven, not Q-driven
 - Low C → Lower Q, faster, lower energy
 - Smaller is faster (Dennard's law)
 - Major Parasitic contributors
 - MOSFET gates, MOSFET source/drain, wire

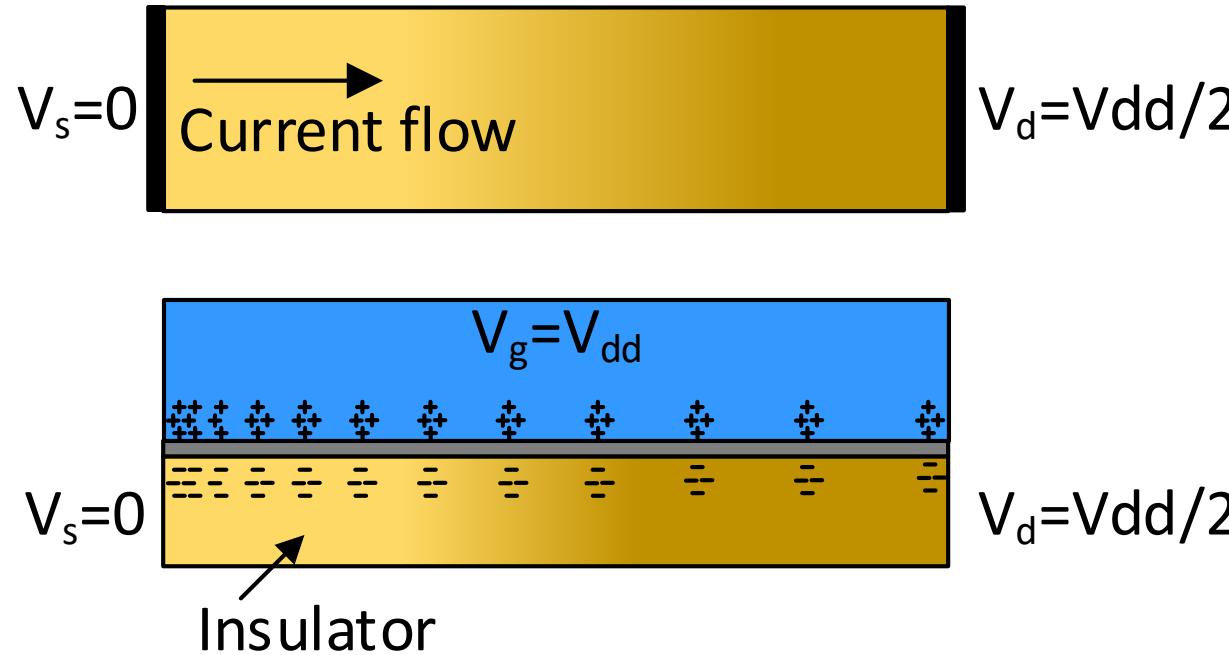
Impact

- Circuit Speed (Digital)
- Power (Digital)
- Bandwidth (Analog)
- Stability (Digital, Analog)

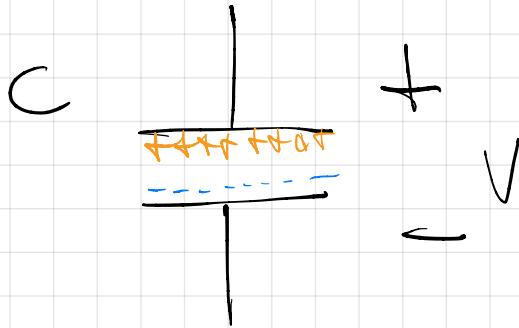
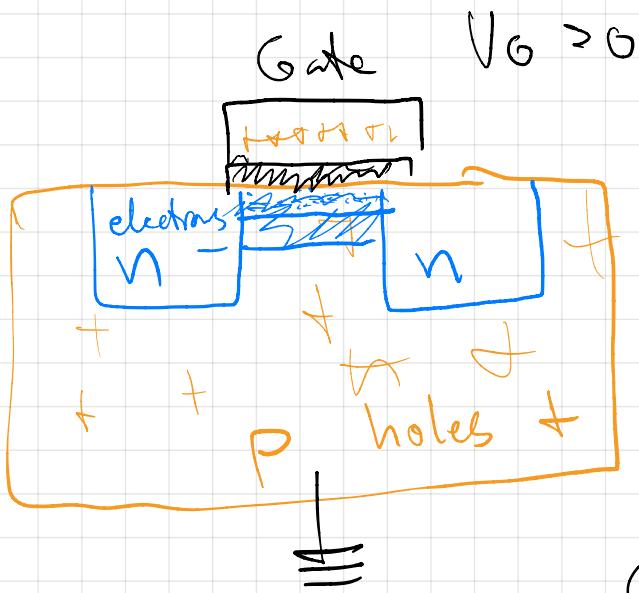
Calculate the per-unit length capacitance of an infinitely long cylindrical wire, diameter d in free space



MOS Transistor – A 10K foot view

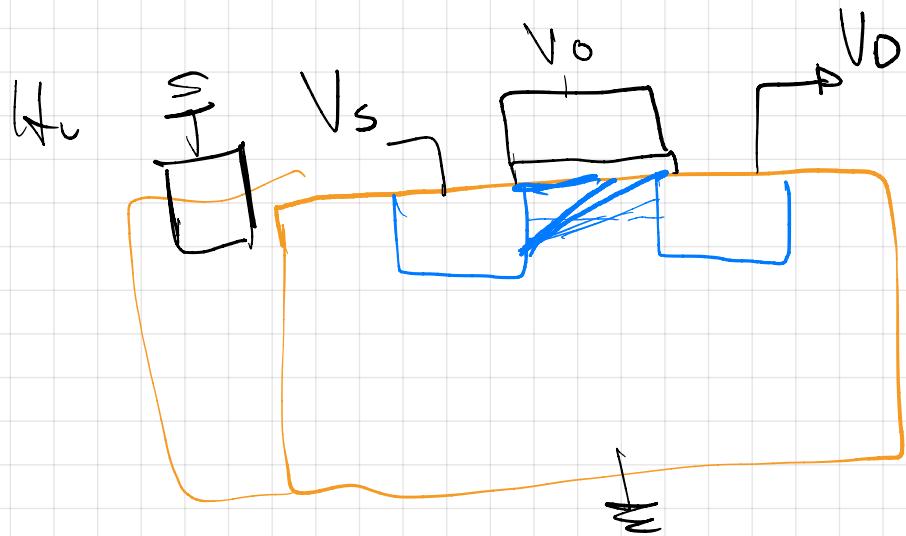


- Capacitor charge buildup allows for a “channel” to form
- Charge density not uniform → ? Impact on R. ? Impact on $V(x)$
- How can I reduce the resistance of this device further?

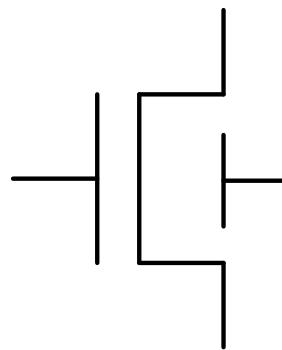


$$Q = CV$$

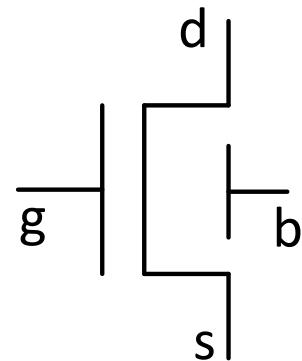
Charging
Neumann



MOS Transistor – A Strictly Intuitive View

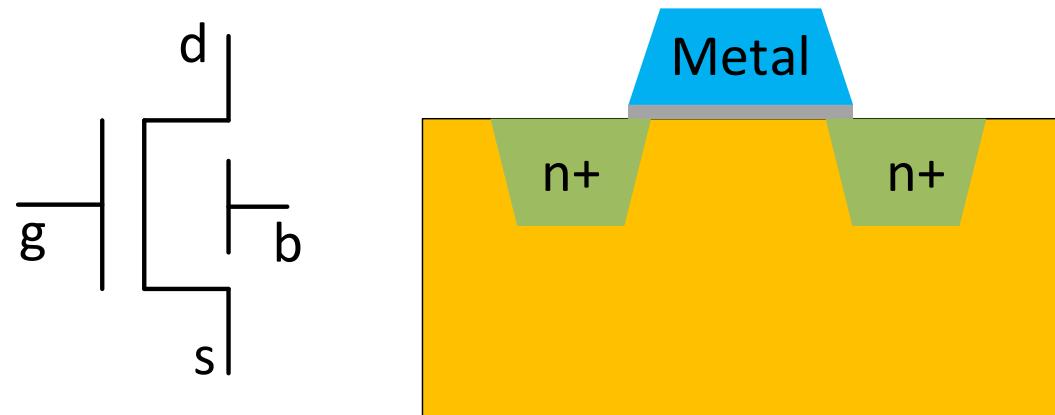


MOS Transistor – A Strictly Intuitive View

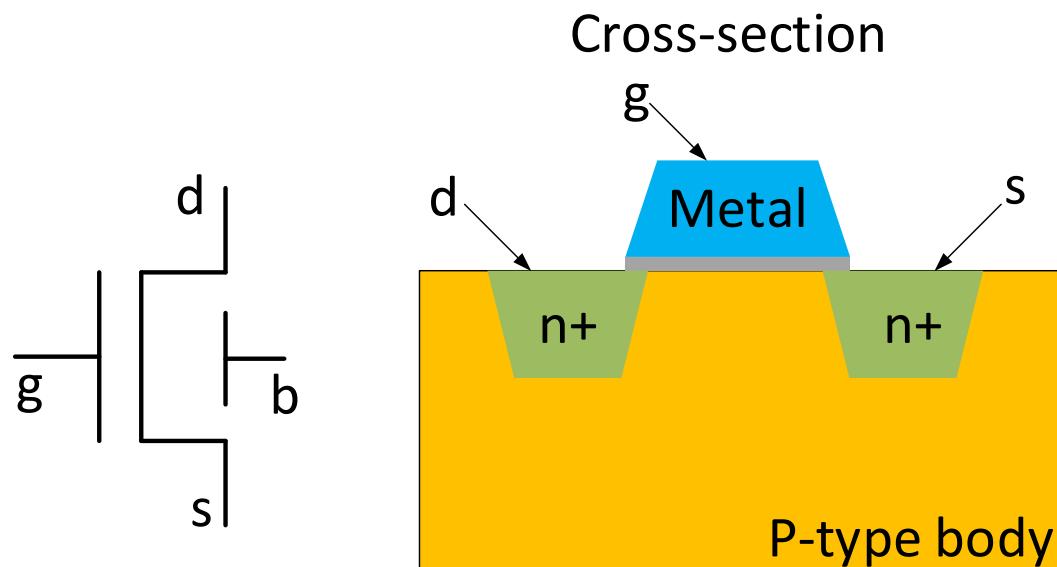


MOS Transistor – A Strictly Intuitive View

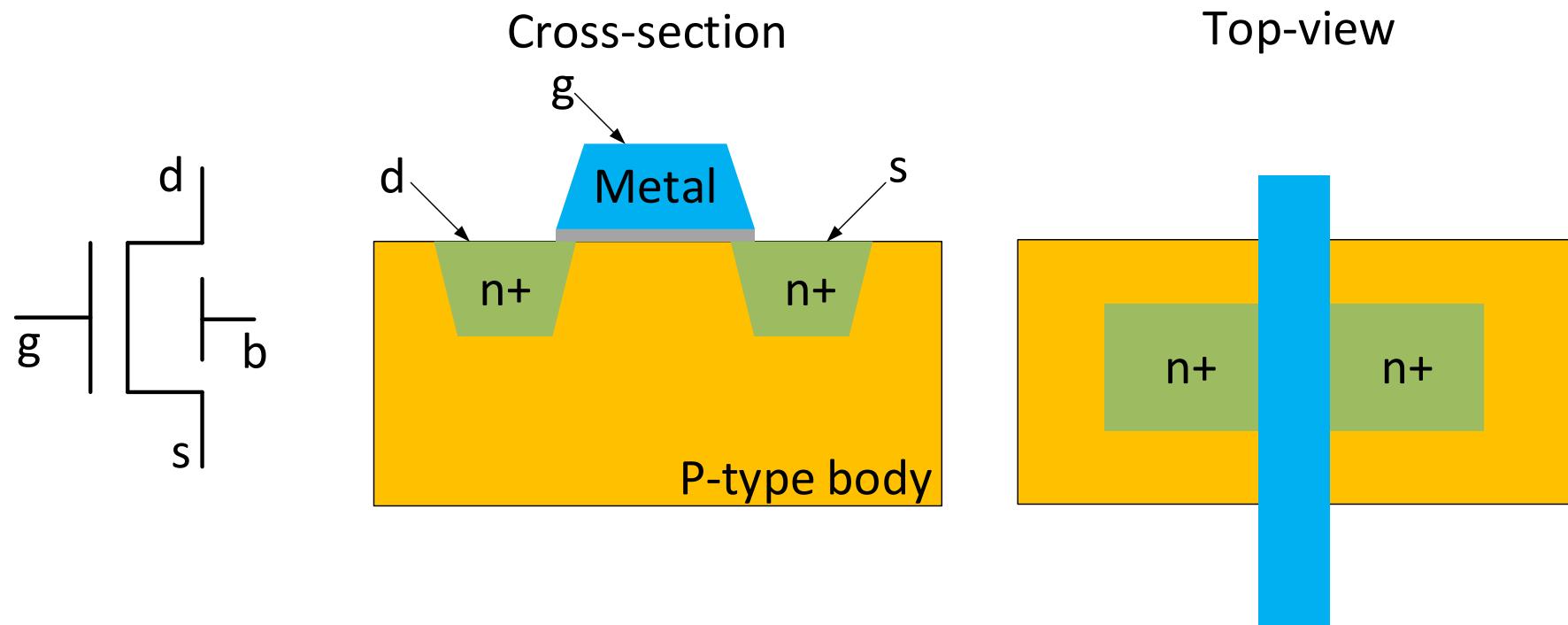
Cross-section



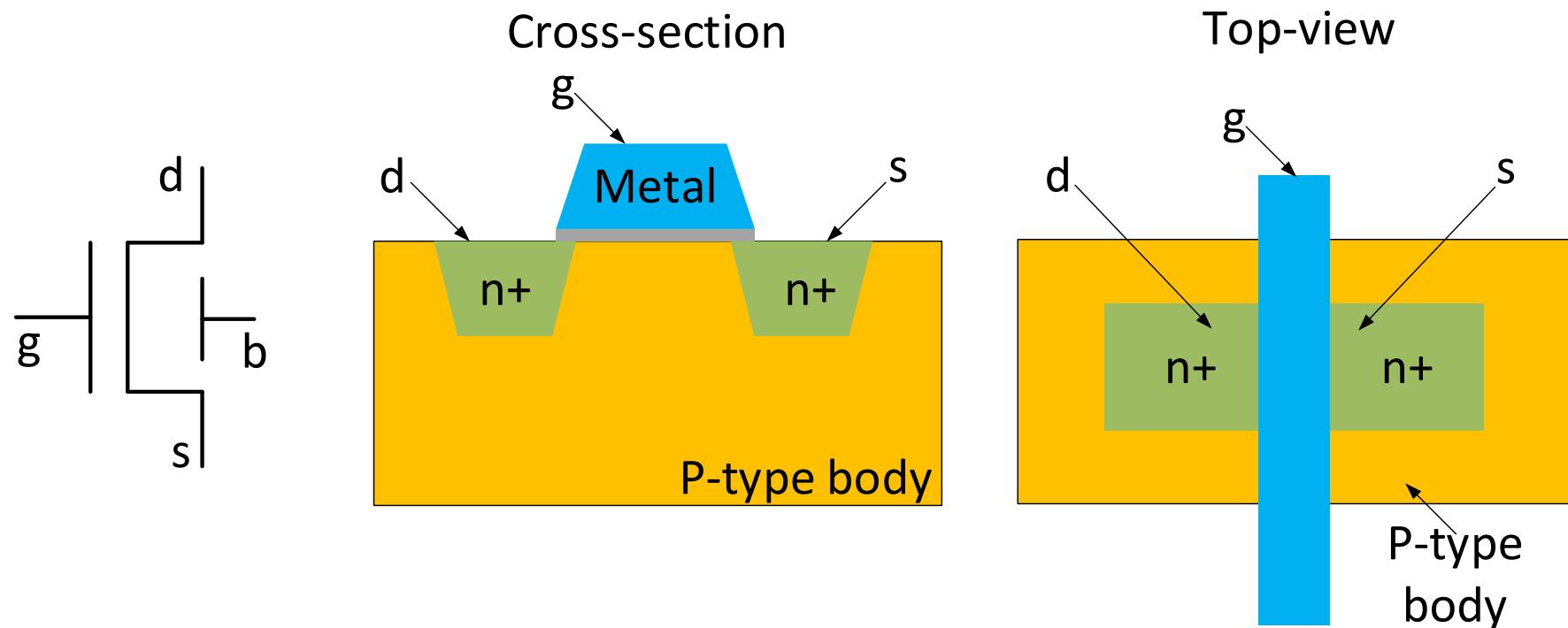
MOS Transistor – A Strictly Intuitive View



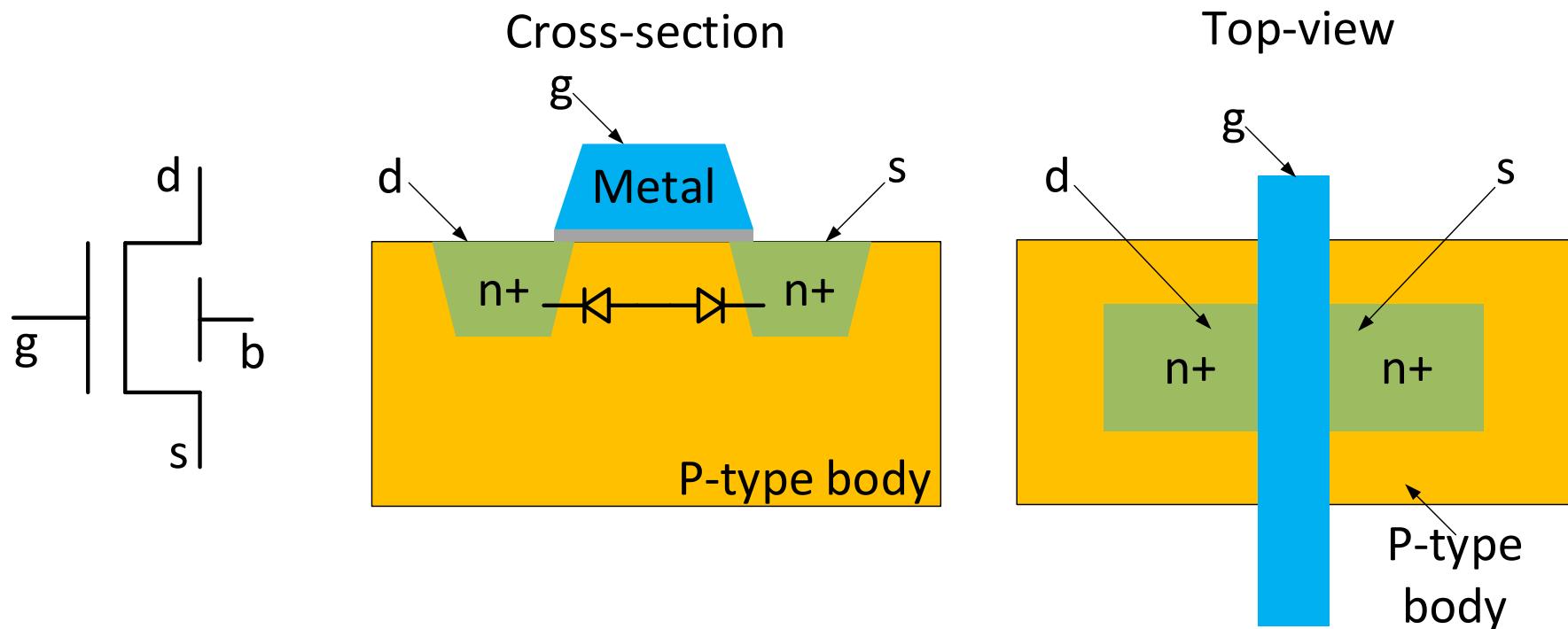
MOS Transistor – A Strictly Intuitive View



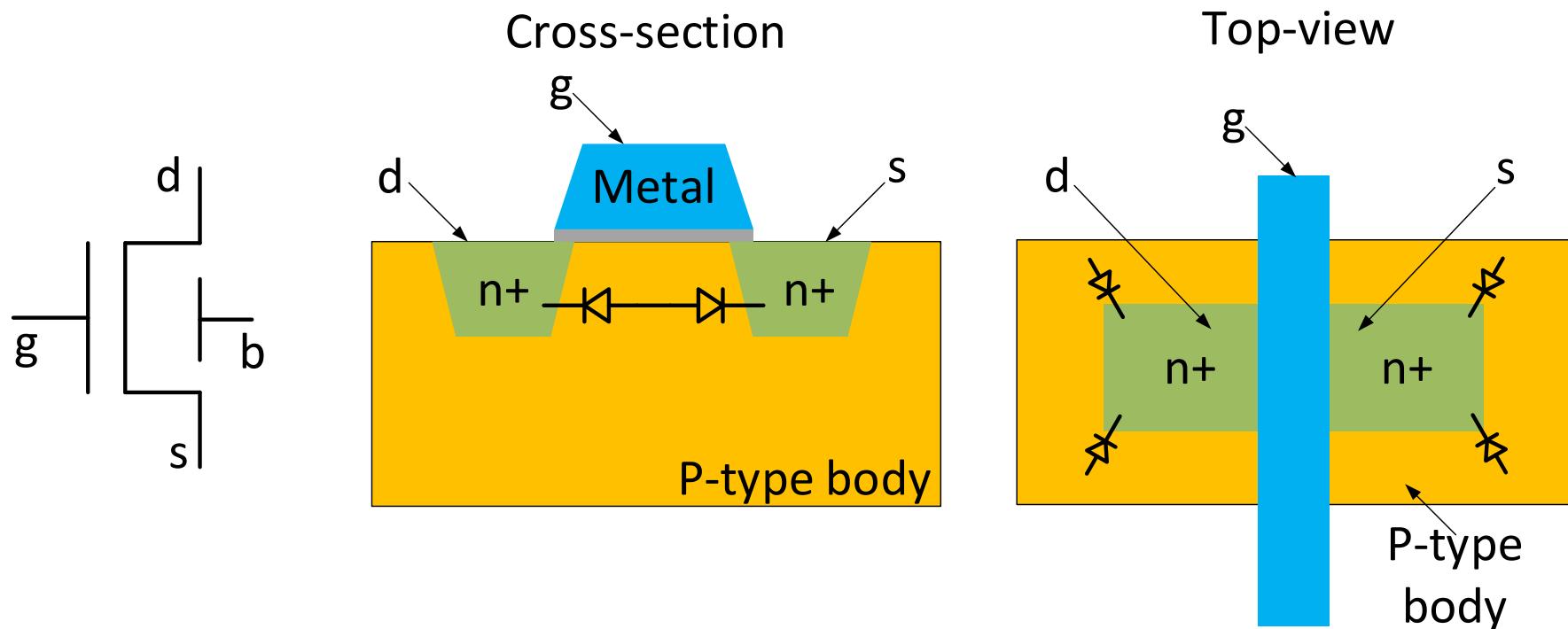
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MOS Transistor – A Strictly Intuitive View

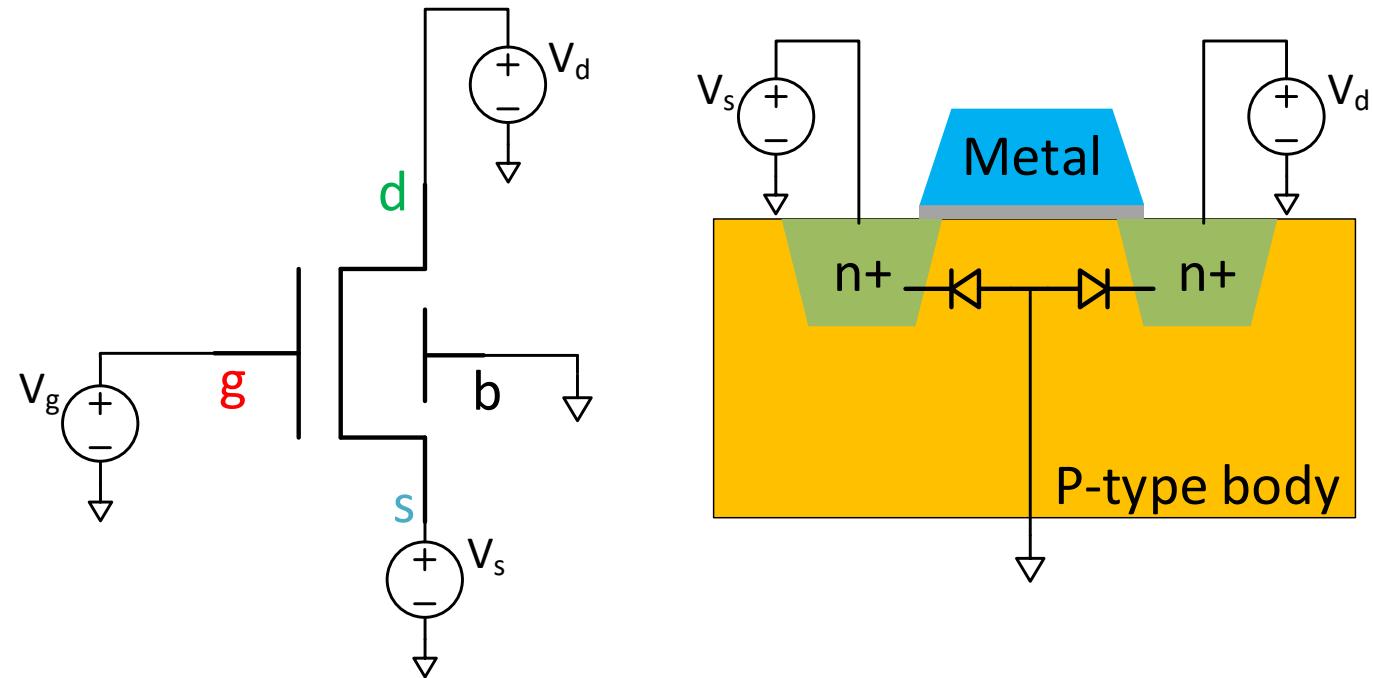


MOS Transistor – A Strictly Intuitive View

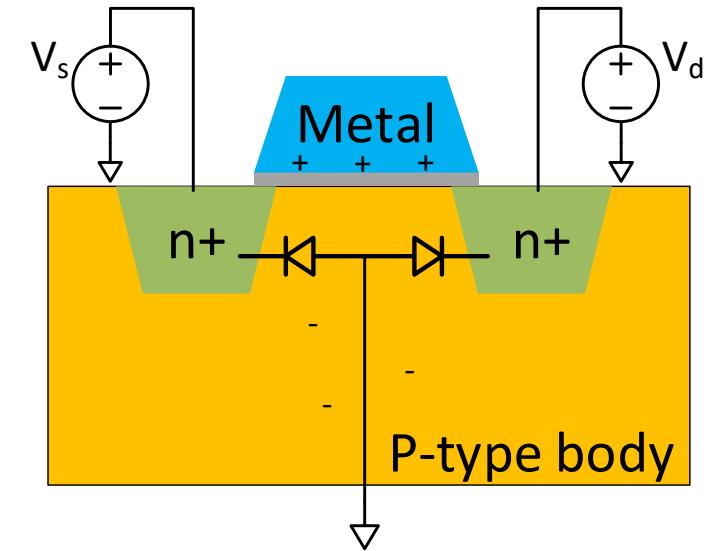
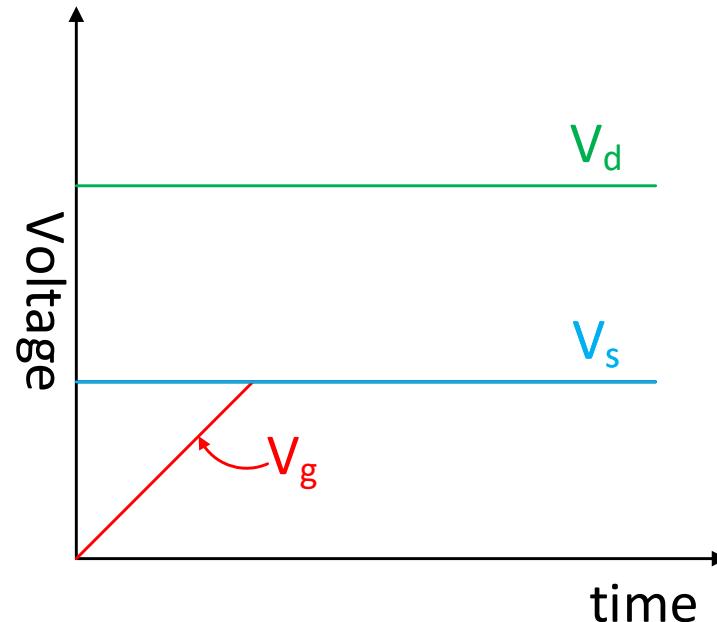
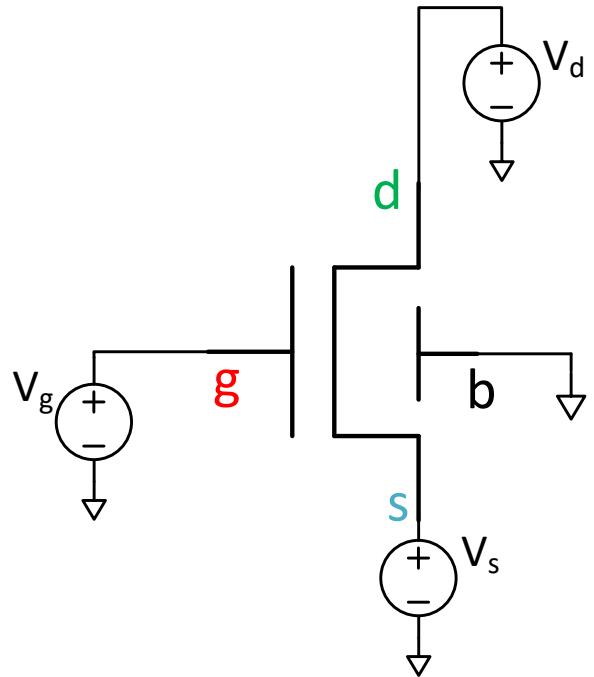


MOS Transistor – A Strictly Intuitive View

- For this course
 - Body of an **nmos** device is always tied to **ground**
 - Body of a **pmos** device is always tied to **Vdd**

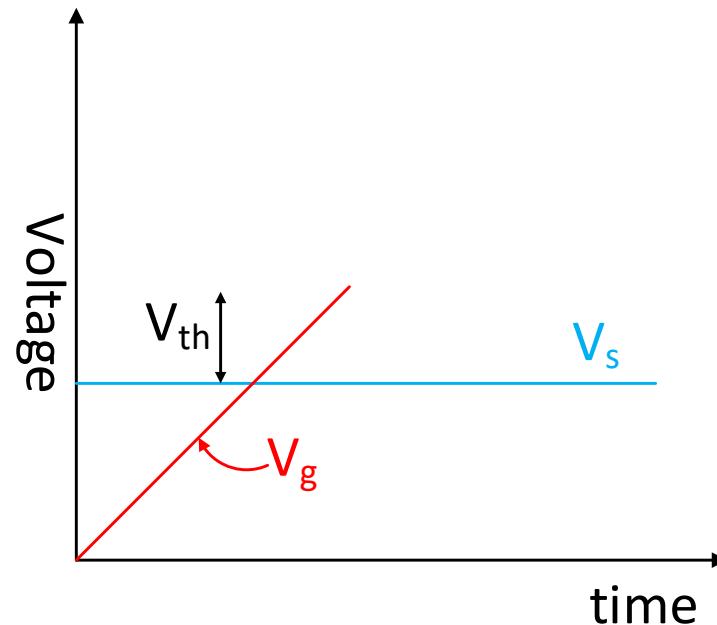
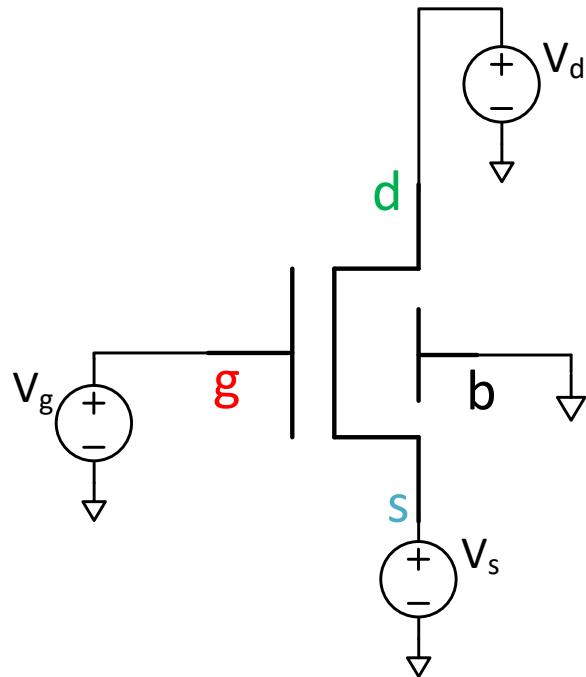


MOS Transistor – A Strictly Intuitive View

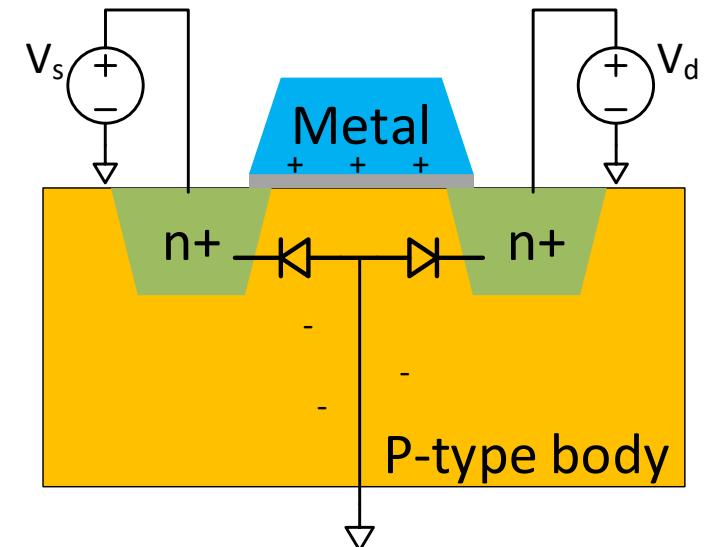


- Initially $V_g < V_s$
- No channel formed

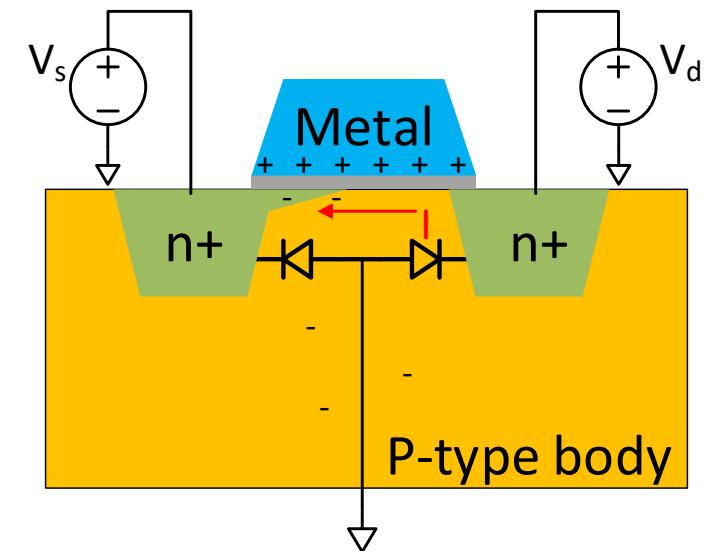
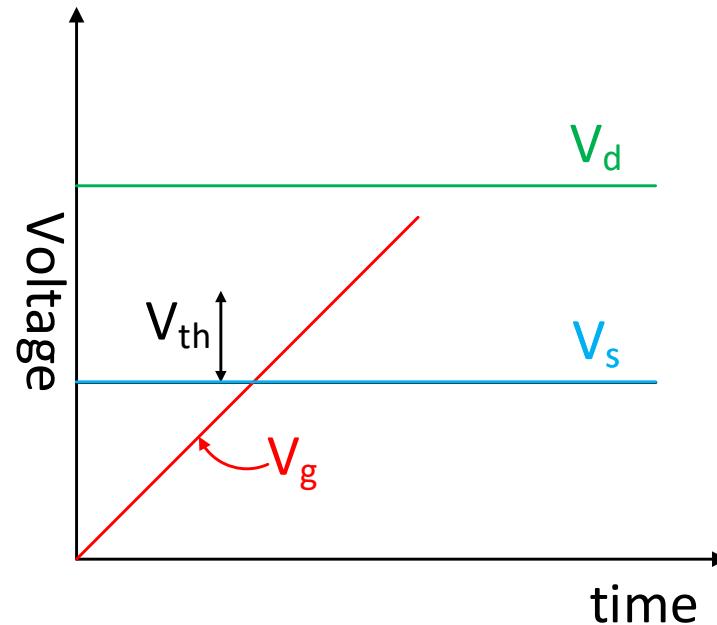
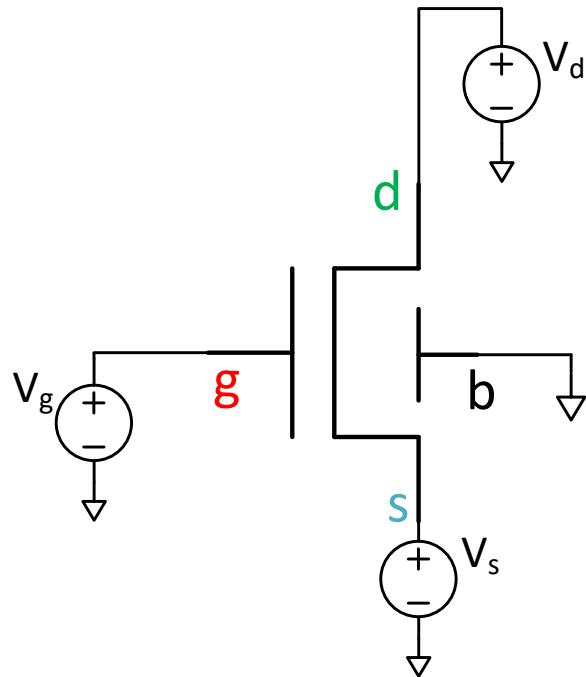
MOS Transistor – A Strictly Intuitive View



- Initially $V_g > V_s$
- But $V_g - V_s < V_{th} \rightarrow$ No channel formed
- $V_g - V_s \rightarrow V_{gs}$
- $V_{gs} - V_{th} = V_{gs}'$ (Also called gate overdrive)

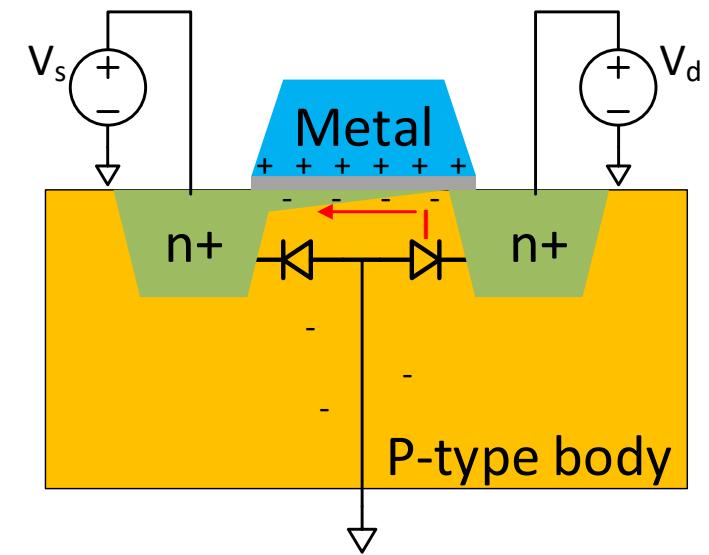
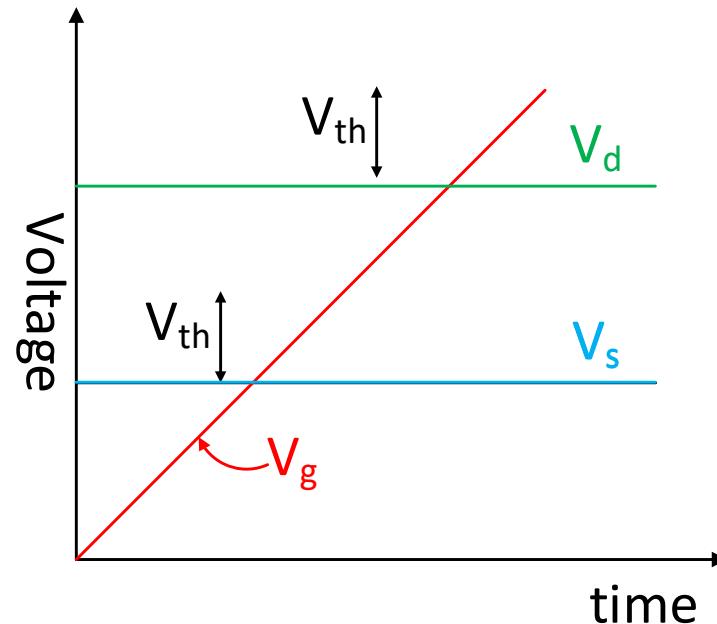
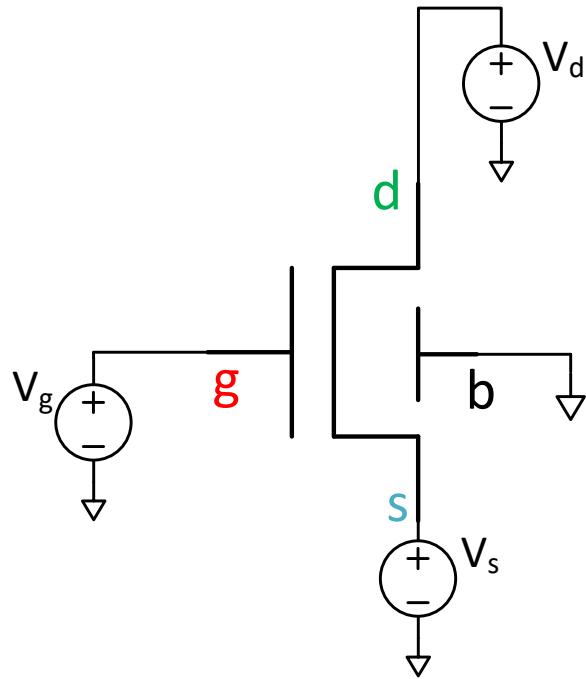


MOS Transistor – A Strictly Intuitive View



- Channel begins forming as $V_g - V_s > V_{th} \equiv V'_{gs} > 0$ (+gate overdrive)
- Channel still does not extend to L
- Channel not very thick

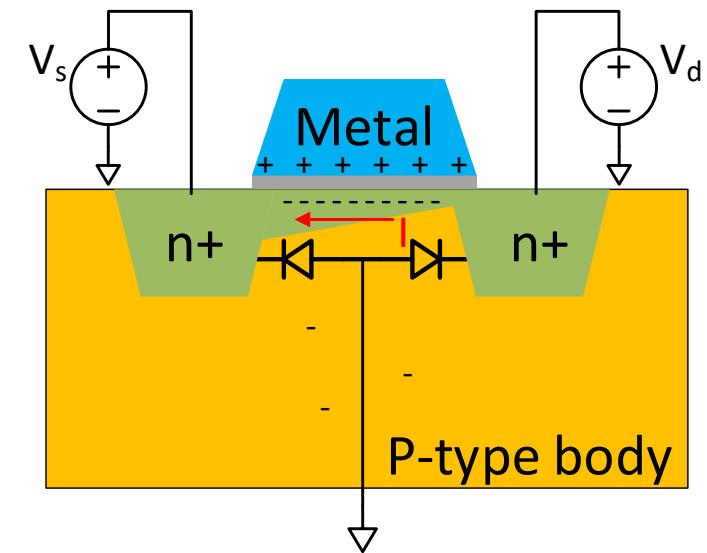
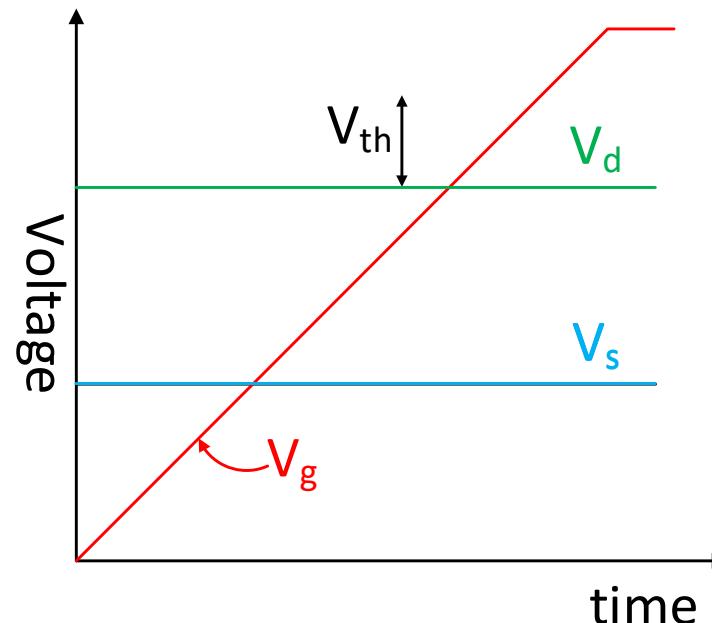
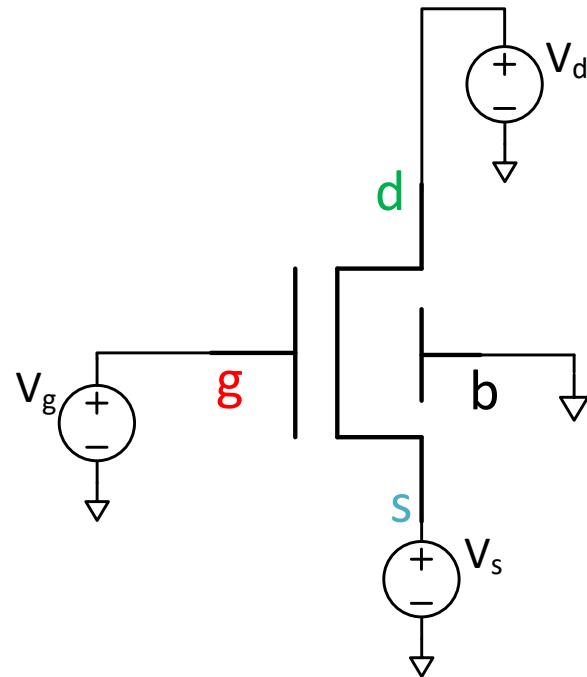
MOS Transistor – A Strictly Intuitive View



- Channel begins to form as $V_g - V_s > V_{th}$
- Channel still does not extend to L
- Channel thickness increasing

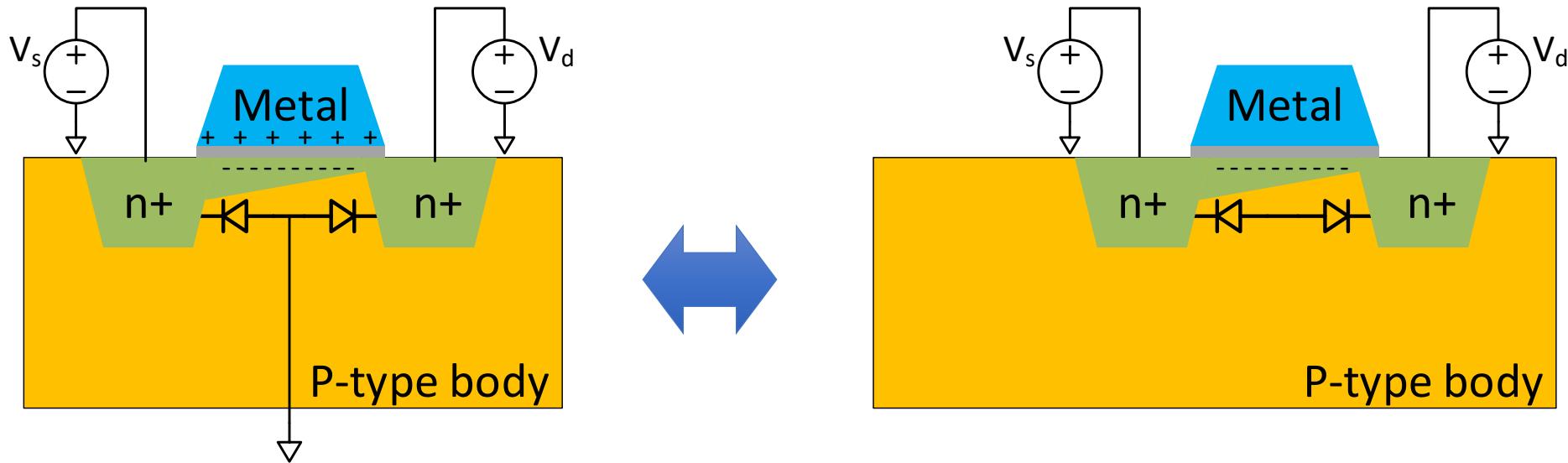
HERE

MOS Transistor – A Strictly Intuitive View

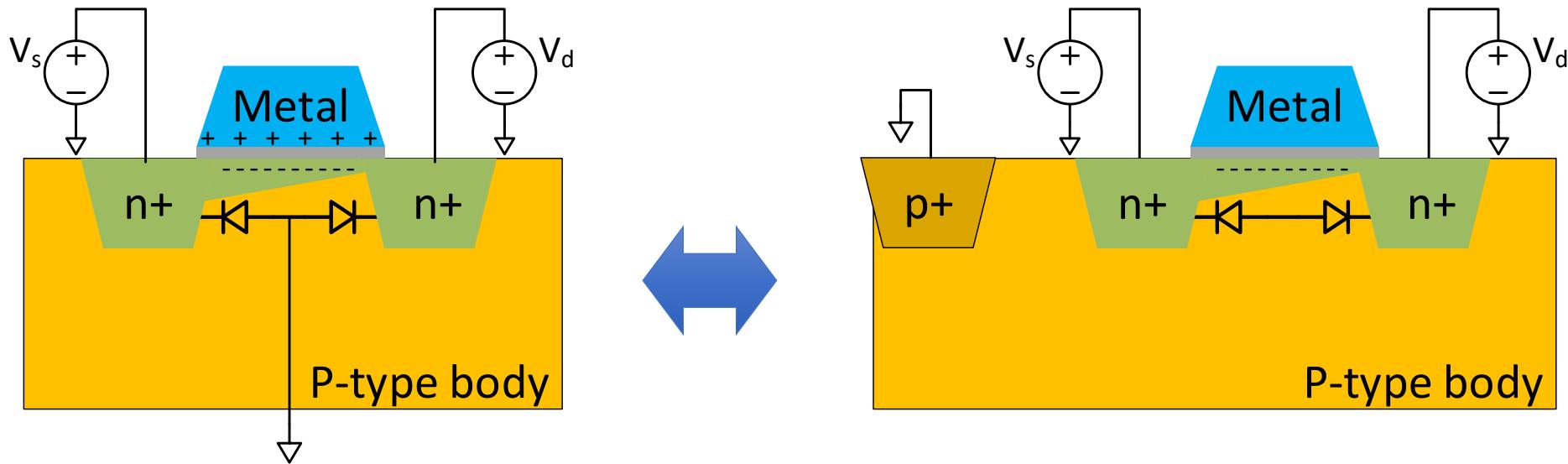


- Channel extends to L as $V_g - V_d > V_{th}$
- Channel thicker now $\rightarrow \downarrow$ resistance
- Thickness varies along channel!

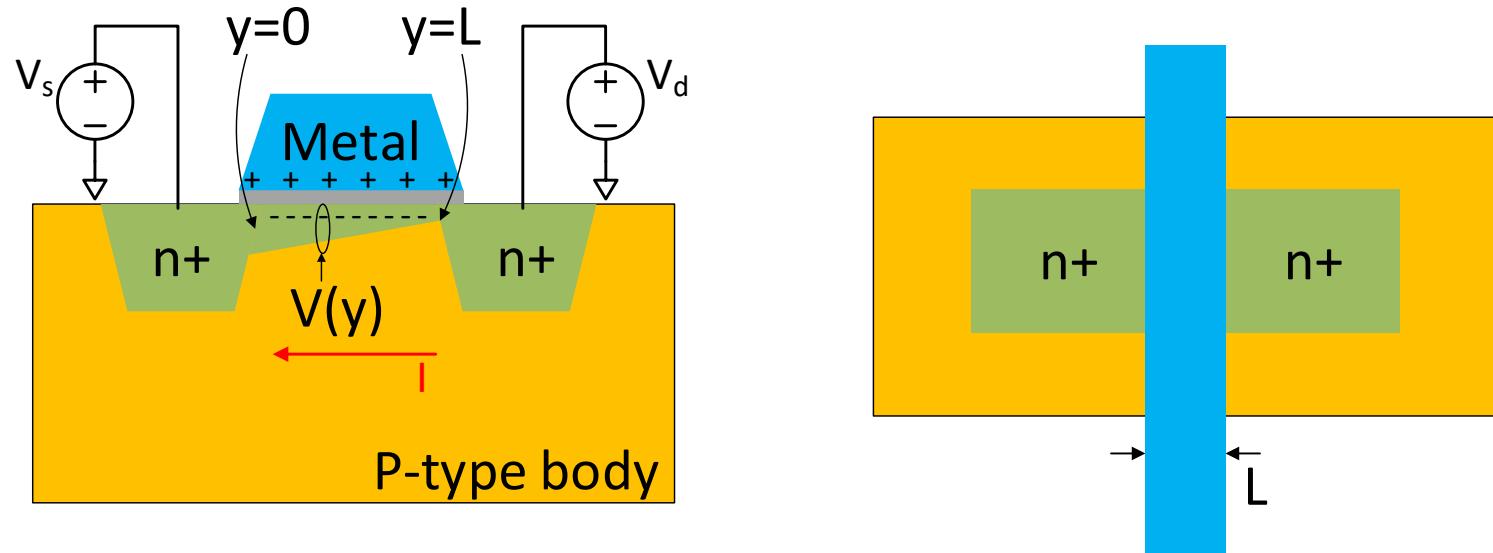
The Substrate Contact



The Substrate Contact



The Ideal Shockley MOSFET model



- Analyze the MOS device in the linear region: $V_{gs} - V_{th} = V_{gs}' > V_{ds}$
- Recall that channel is fully formed
- Steady-state → Current is the same at any point y along the channel

MOSFET Current Flow

$I =$

MOSFET Current Flow

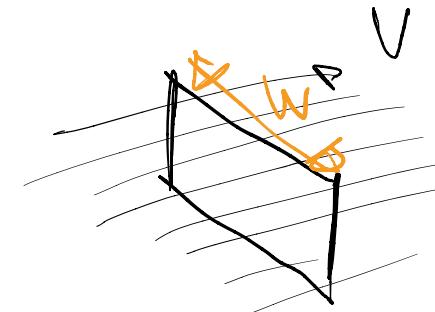
$$I = W$$

MOSFET Current Flow

$$I = W \cdot Q_d$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$



MOSFET Current Flow

$$\begin{aligned}I &= W \cdot Q_d \cdot v \\&= W \cdot C_{ox}\end{aligned}$$

MOSFET Current Flow

$$Q = C V$$

$$\begin{aligned}I &= W \cdot Q_d \cdot v \\&= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right)\end{aligned}$$

MOSFET Current Flow

$$\begin{aligned}I &= W \cdot Q_d \cdot v \\&= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y\end{aligned}$$

MOSFET Current Flow

$$\begin{aligned}I &= W \cdot Q_d \cdot v \\&= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y \\&= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu \frac{\partial V}{\partial y}\end{aligned}$$

MOSFET Current Flow

$$\begin{aligned}I &= W \cdot Q_d \cdot v \\&= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y \\&= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu \frac{\partial V}{\partial y} \\I dy &= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu dV\end{aligned}$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$

$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y$$

$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu \frac{\partial V}{\partial y}$$

$$I dy = W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu dV$$

Integrating both sides gives ...

$$\int_0^L I dy =$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$

$$= W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu E_y$$

$$= W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu \frac{\partial V}{\partial y}$$

$$I dy = W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu dV$$

Integrating both sides gives ...

$$\int_0^L I dy = \int_0^{V_{ds}} W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu dV$$

MOSFET Current Flow

$$\begin{aligned}I &= W \cdot Q_d \cdot v \\&= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y \\&= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu \frac{\partial V}{\partial y}\end{aligned}$$

$$I dy = W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu dV$$

Integrating both sides gives ...

$$\int_0^L I dy = \int_0^{V_{ds}} W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu dV$$

$$IL = \mu C_{ox} W \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$

$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y$$

$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu \frac{\partial V}{\partial y}$$

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Integrating both sides gives ...

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$$IL = \mu C_{ox} W \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

$$I = \mu C_{ox} \frac{W}{L} \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$

$$= W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu E_y$$

$$= W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu \frac{\partial V}{\partial y}$$

$$I dy = W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu dV$$

Integrating both sides gives ...

$$\int_0^L I dy = \int_0^{V_{ds}} W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu dV$$

$$IL = \mu C_{ox} W \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

$$I = \mu C_{ox} \frac{W}{L} \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right], \quad \text{Letting } \beta = \mu C_{ox} \frac{W}{L}$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$

$$= W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu E_y$$

$$= W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu \frac{\partial V}{\partial y}$$

$$I dy = W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu dV$$

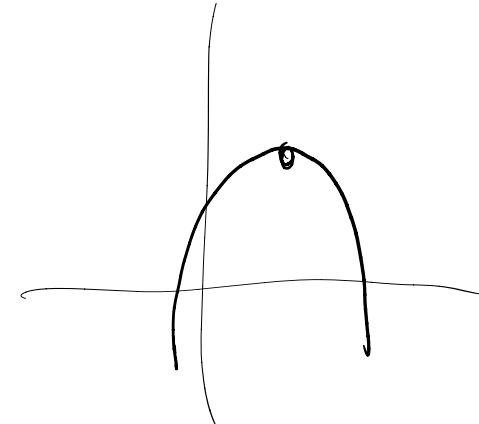
Integrating both sides gives ...

$$\int_0^L I dy = \int_0^{V_{ds}} W \cdot C_{ox} (V_{gs} - V_{th} - V(y)) \cdot \mu dV$$

$$IL = \mu C_{ox} W \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

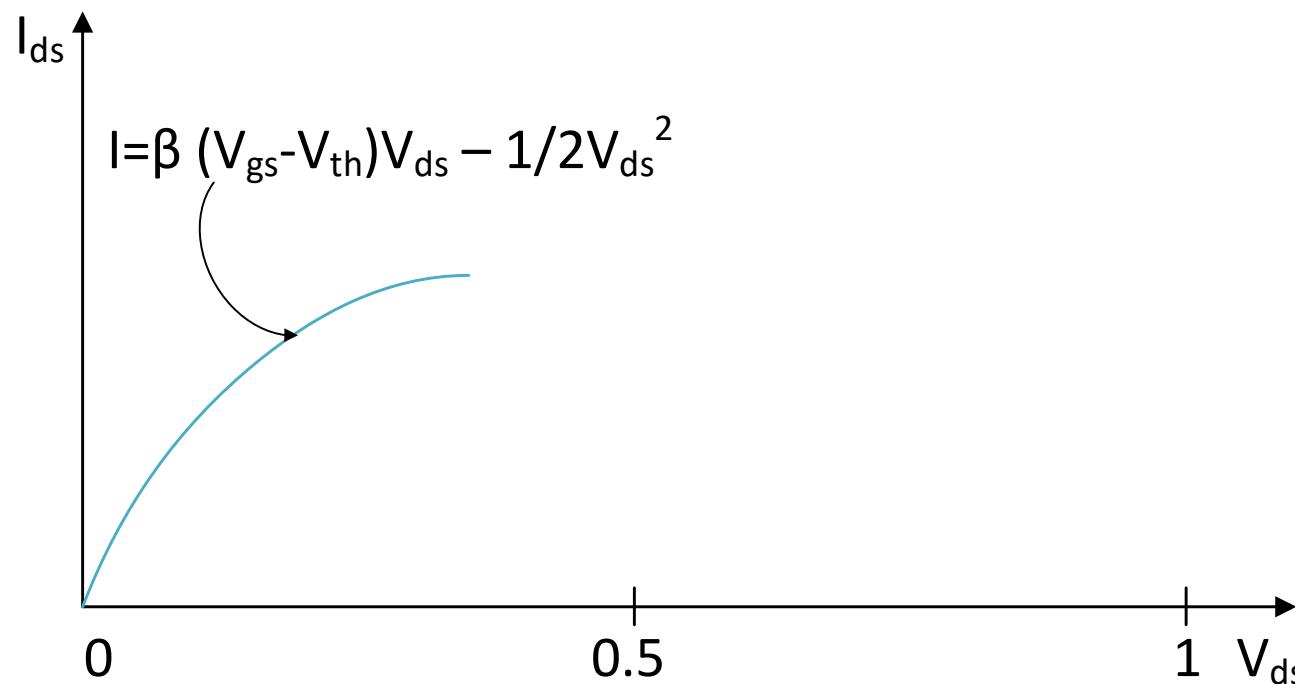
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$$I = \beta \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$



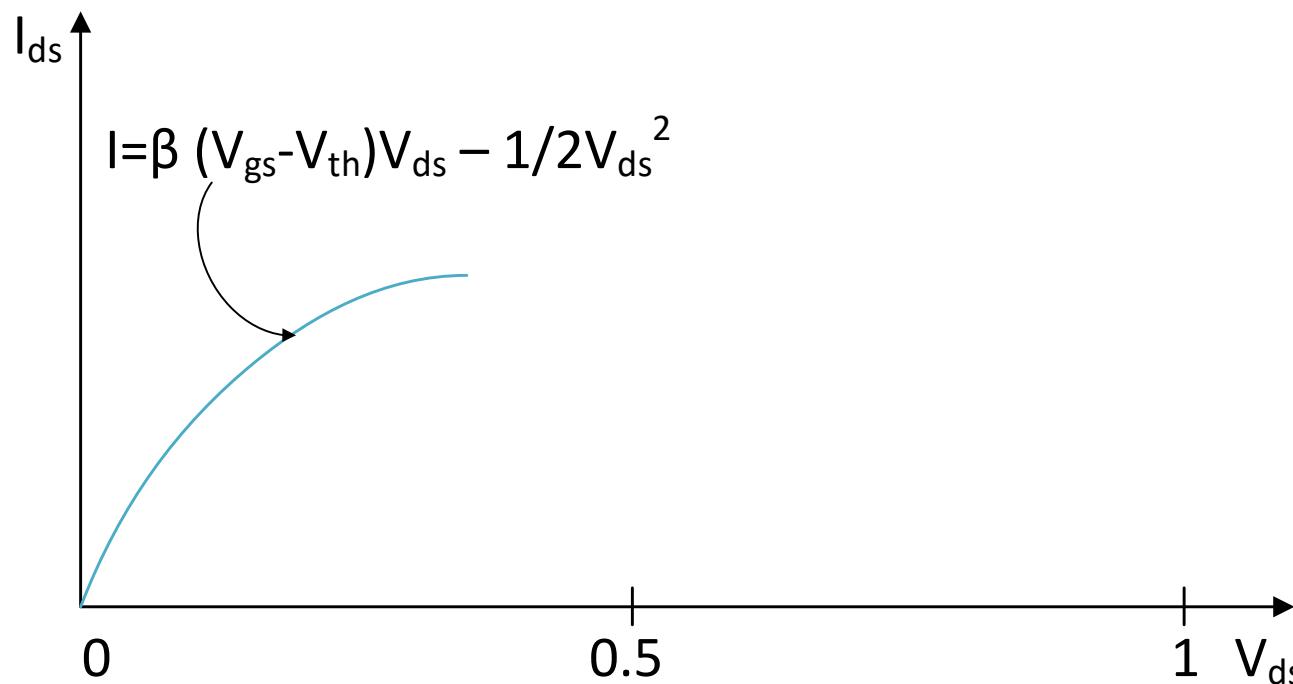
MOSFET Operation: Triode region

- Equation corresponds to device in Linear (or Triode) region
 - Channel is continuous from source to drain
- Question: Plot I_{ds} vs. V_{ds} for a fixed V_{gs}



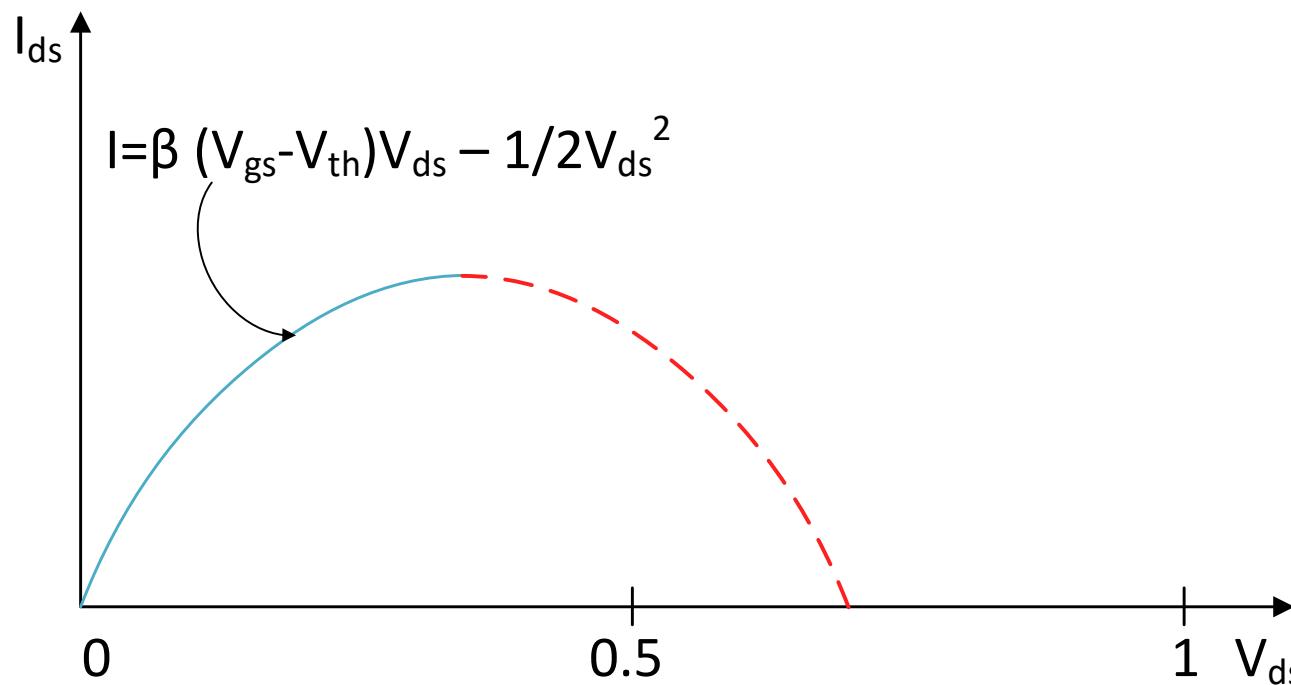
MOSFET Operation: Triode region

- Equation corresponds to device in Linear (or Triode) region
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- What happens for $V_{ds} > V_{gs} - V_{th}$?



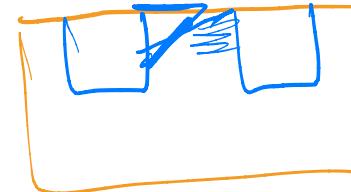
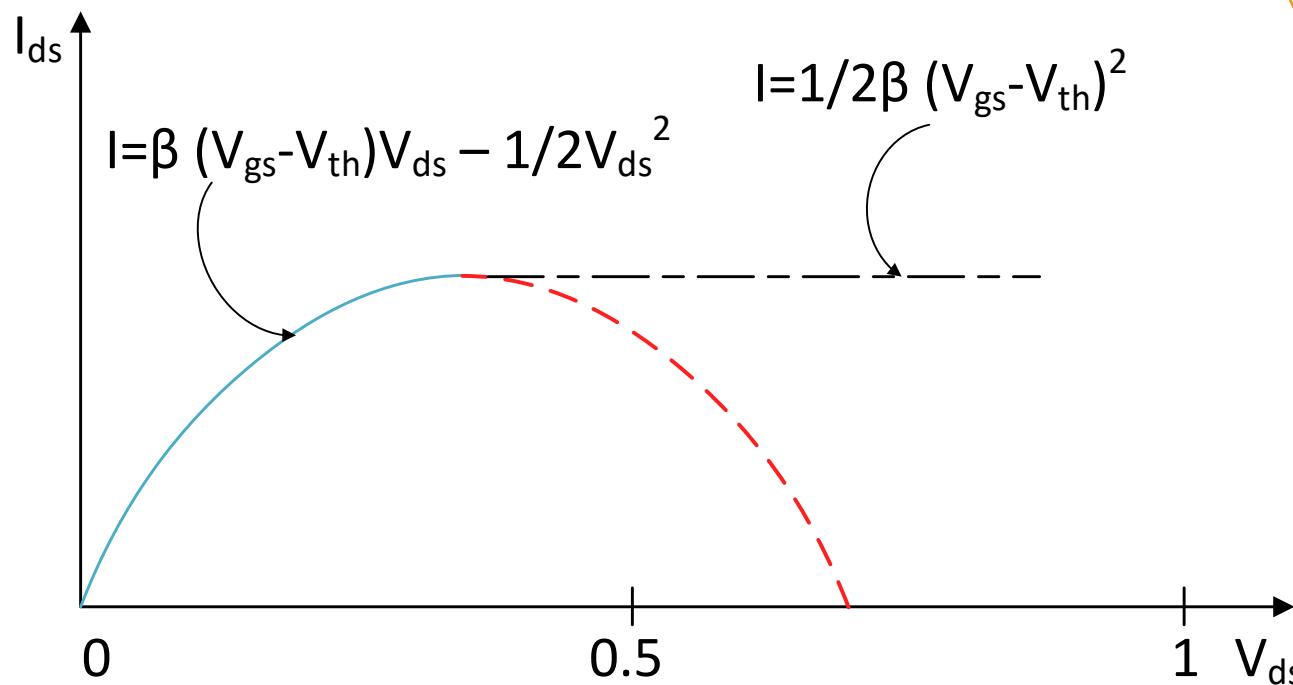
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MOSFET Operation: Triode region

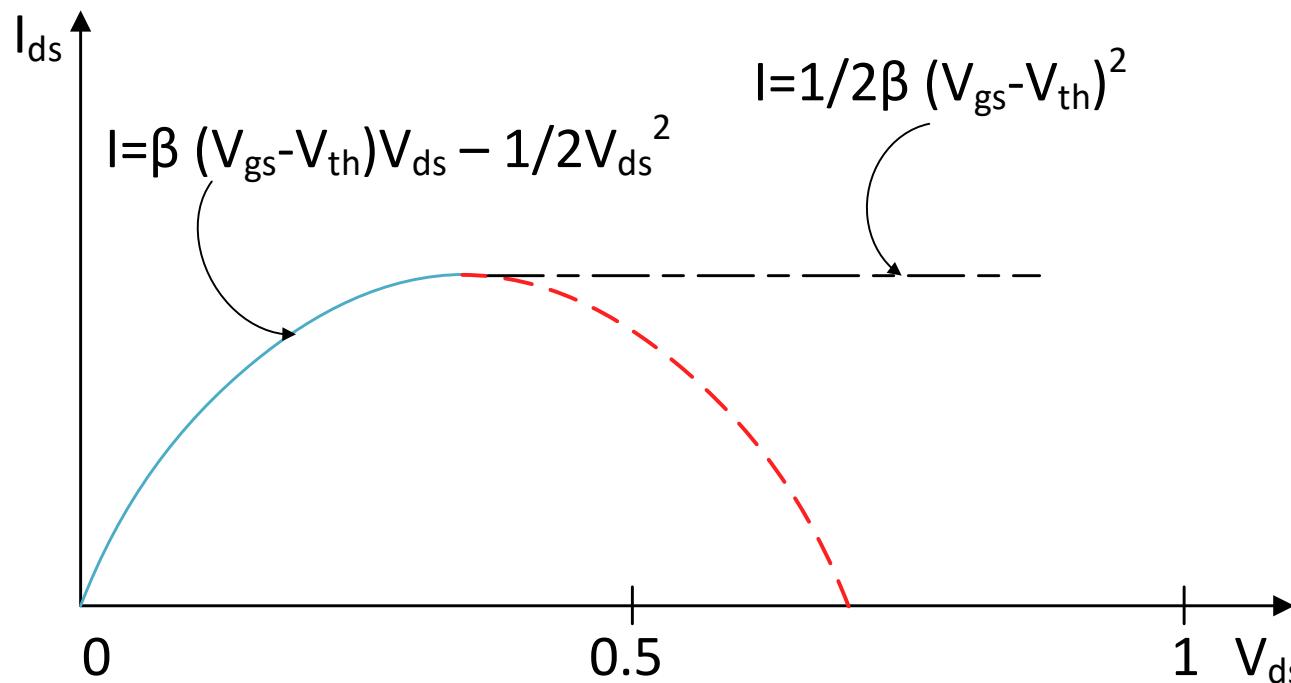
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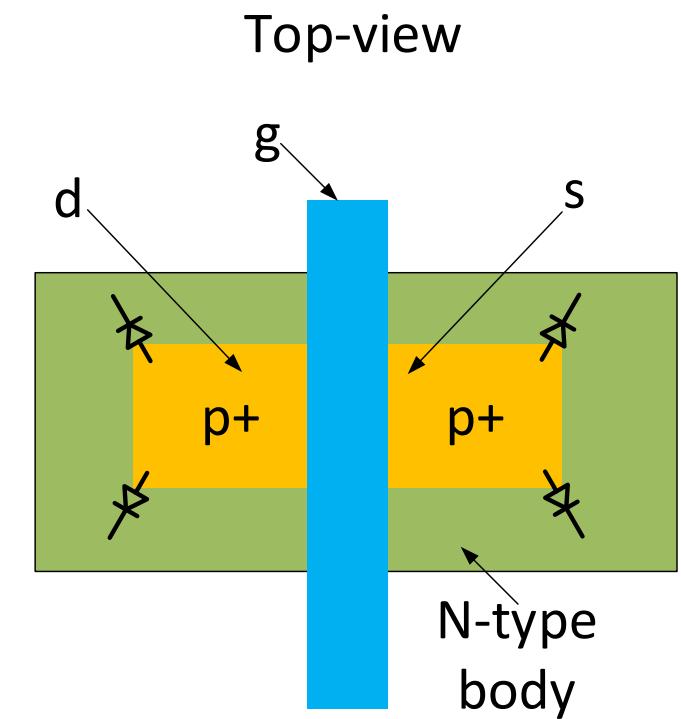
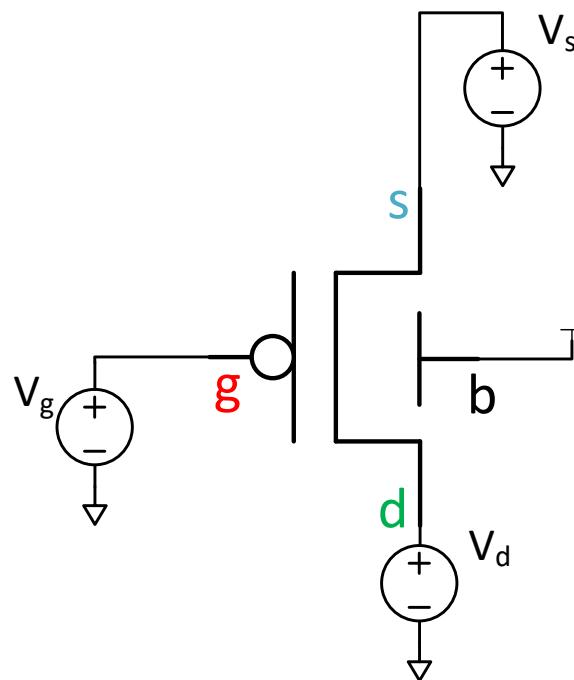
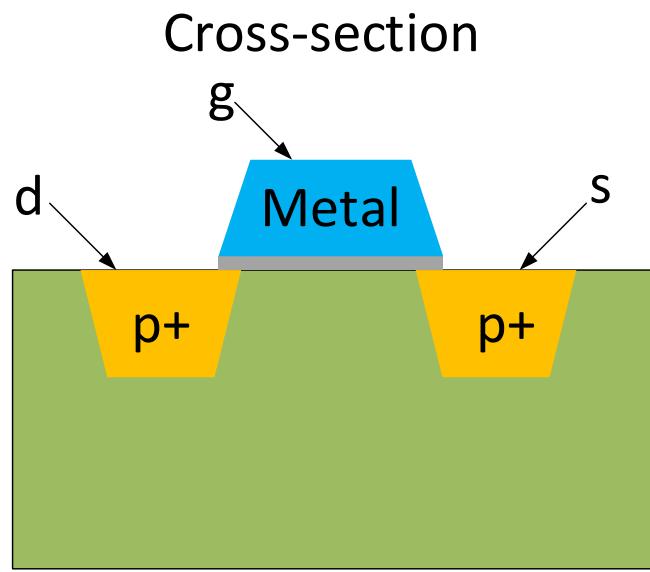
$V_{gs} < V_{th}$
cutoff
 $V_{gs} > V_{th}$
 $V_{ds} < V_{gs} - V_{th}$
Linear
Triode
 $V_{ds} \geq V_{gs} - V_{th}$
Saturation

MOSFET Operation: Triode region

- Equation corresponds to device in Linear (or Triode) region
 - Channel is continuous from source to drain
- Question: Plot I_{ds} vs. V_{ds} for a fixed V_{gs}
- What happens for $V_{ds} > V_{gs} - V_{th}$?
 - Device enters saturation
 - The channel “pinches-off” (More on this shortly)

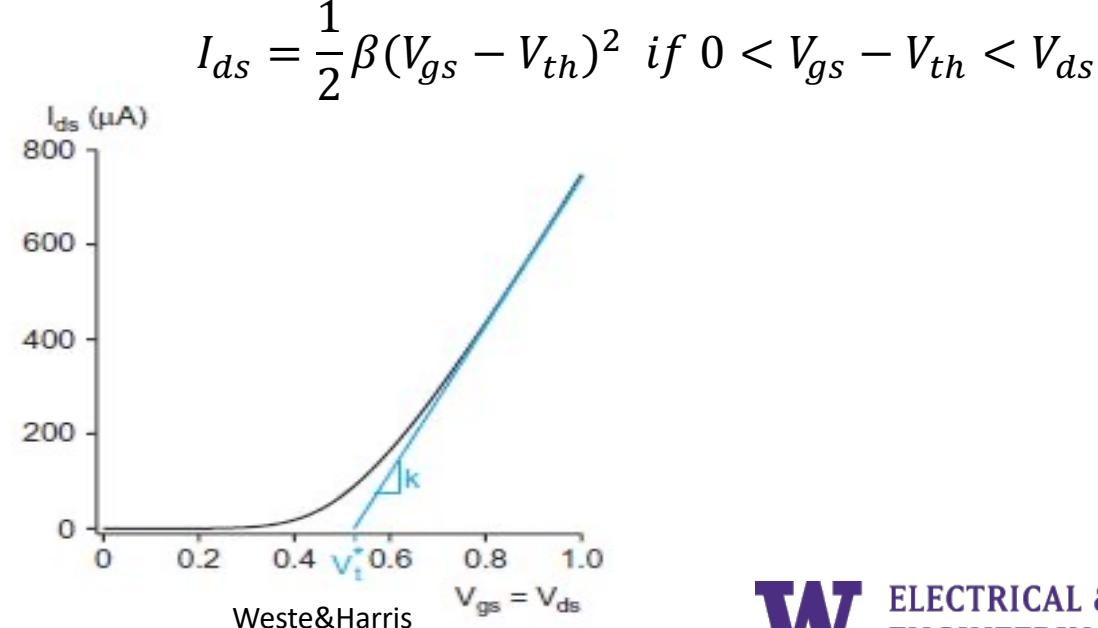
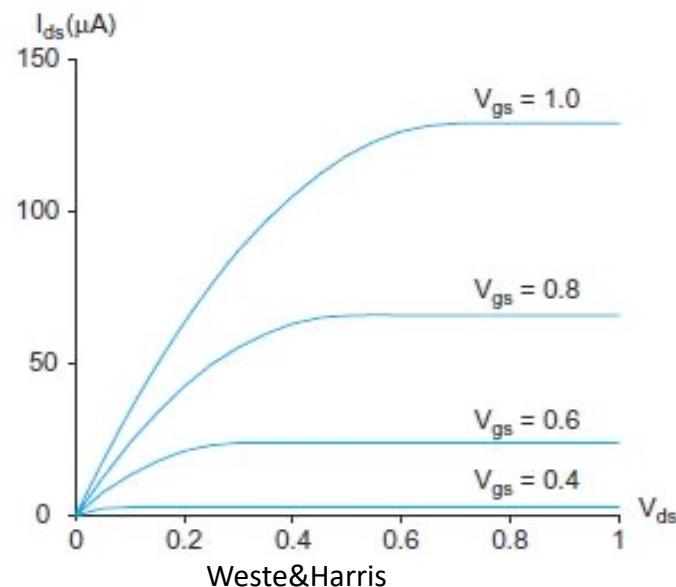


Break-out session: Figure out the PMOS...

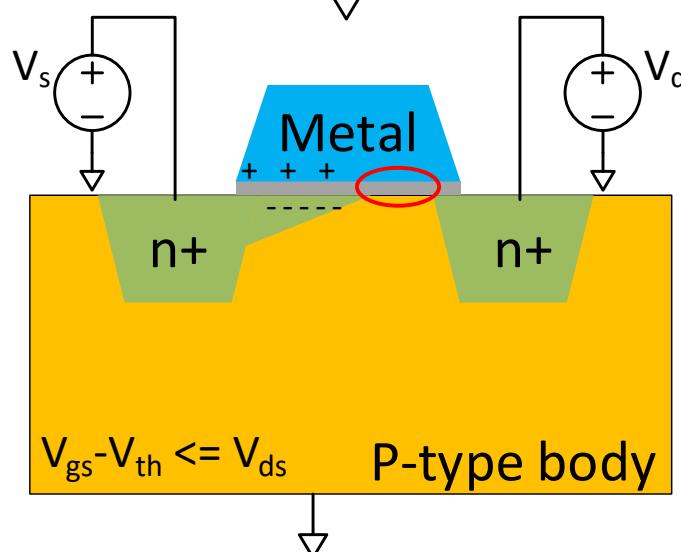
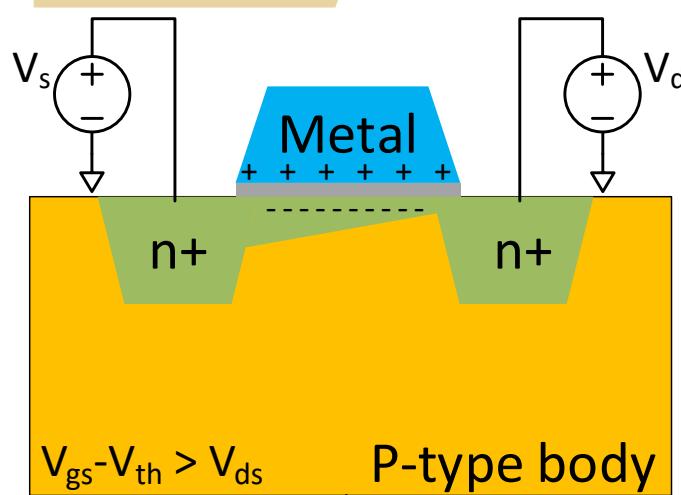


MOSFET Operation: Saturation

- Saturation condition: $V_{gs} - V_{th} \leq V_{ds}$
 - $V_{gs} - V_{th}$ (also denoted as V_{gs}') , the gate overdrive is less than the on-voltage
- Current “levels-off”
 - I_d no longer a function of V_{ds} (to the first order. More on this later)
 - Depends only on V_{gs} and V_{th}

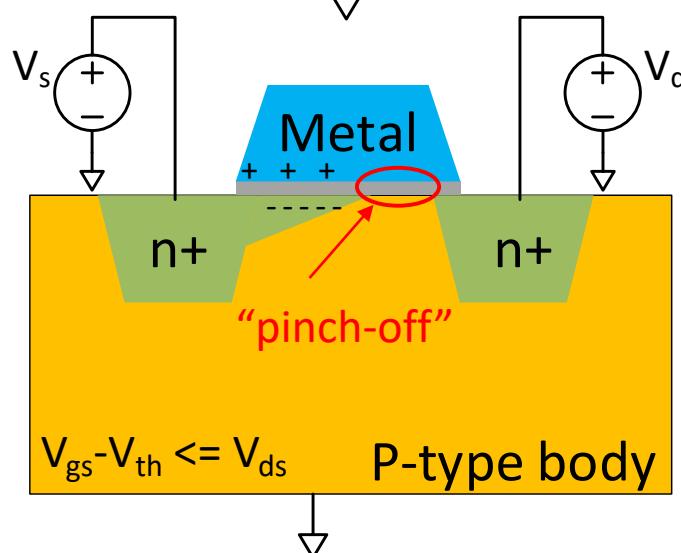
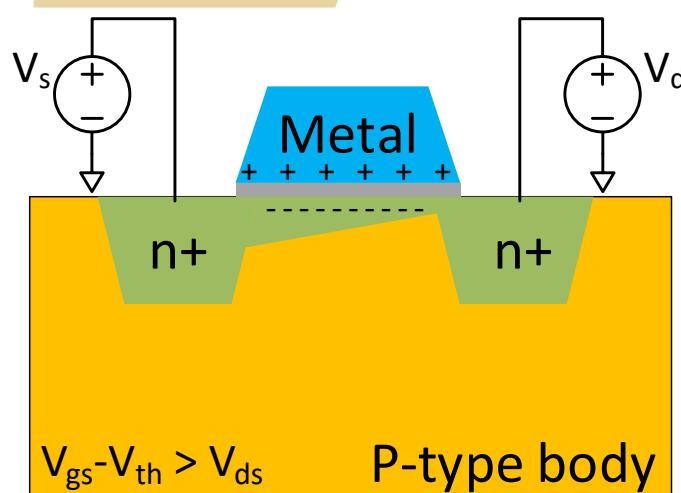


Channel Length Modulation



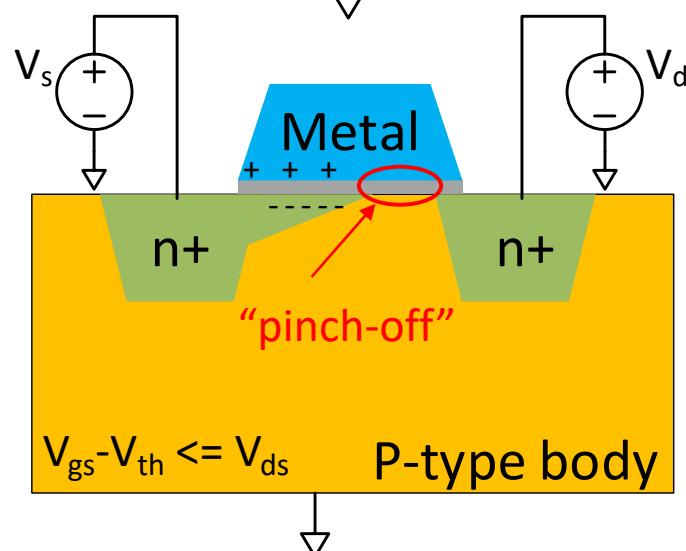
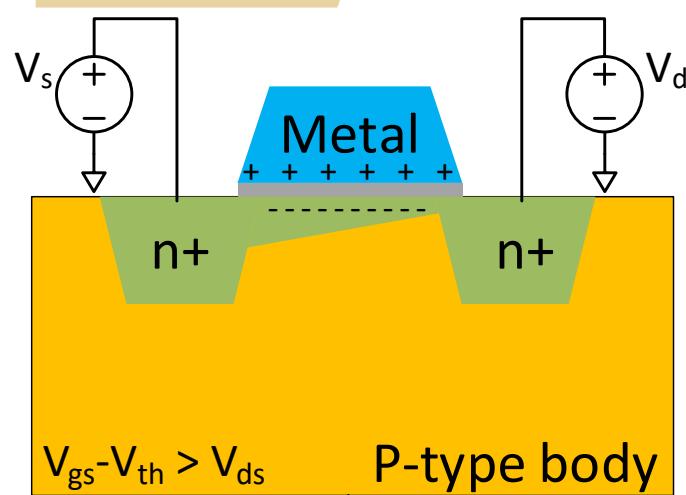
- In reality, I_{ds} is not constant as V_{ds} increases
- Depletion region forms beyond a “pinch-off” region

Channel Length Modulation



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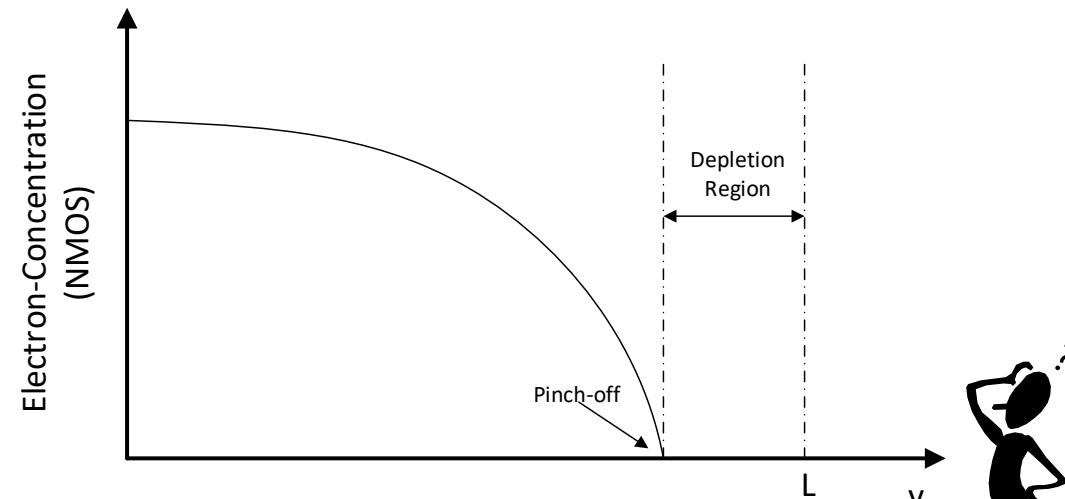
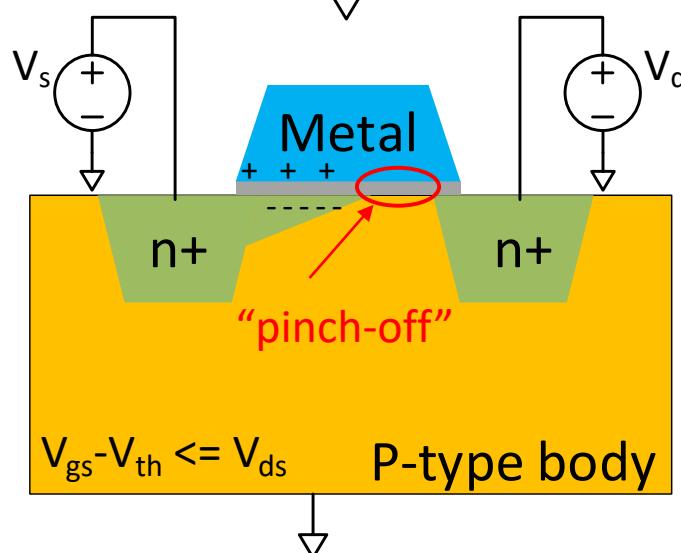
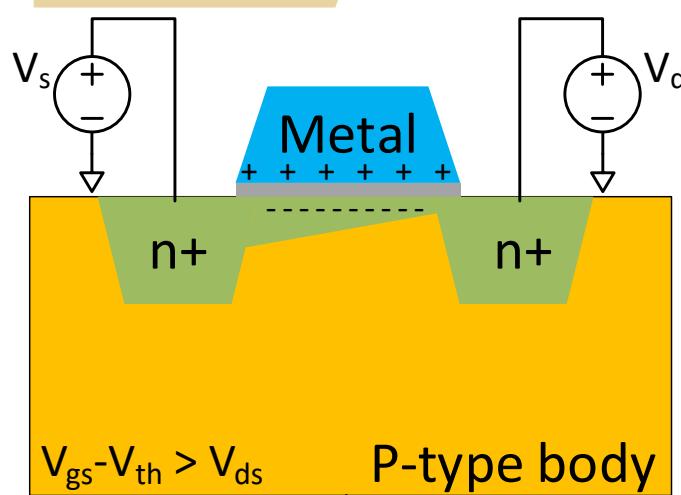


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Channel Length Modulation

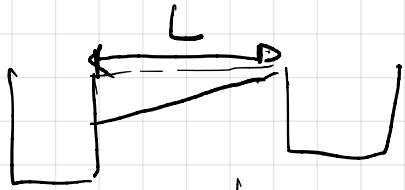


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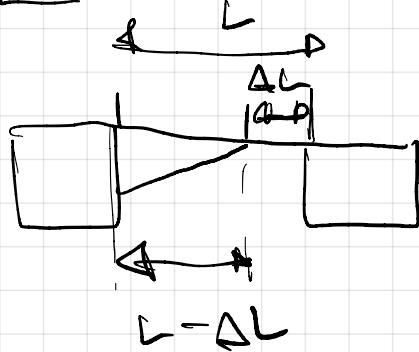
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$$I = I_s = \frac{1}{2} \beta (V_{GS} - V_{TH})^2$$

$$\beta = \mu C_o \times \frac{W}{L}$$



$$\frac{1}{L} \rightarrow \frac{1}{L - \Delta L}$$



$$f(\Delta L) = \frac{1}{L - \Delta L}$$

$$f(0) = \frac{1}{L}$$

$$\frac{df}{d\Delta L} = \frac{d}{d\Delta L} (L - \Delta L)^{-1}$$

$$= \frac{-1}{(L - \Delta L)^2} \cdot (-1) = \frac{1}{(L - \Delta L)^2}$$

$$\left. \frac{df}{d\Delta L} \right|_{\Delta L \approx 0} = \frac{1}{L^2}$$

$$\frac{1}{L - \Delta L} \approx \frac{1}{L} + \frac{1}{L^2} \Delta L + O(\Delta L^2)$$

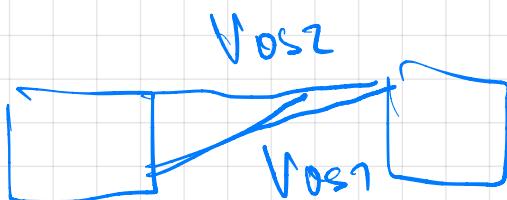
$$f(x) = f(0) + f'(0)x + \frac{1}{2} f''(0)x^2 + \frac{1}{6} f'''(0)x^3$$

Taylor series

$\frac{1}{6}$

$$\frac{1}{L - \Delta L} \approx \frac{1}{L} + \frac{\Delta L}{L^2}$$

$$\begin{aligned}
 I &= \frac{1}{N} \beta (V_{GS} - V_{th})^2 \\
 &= \frac{1}{N} \mu_W C_{ox} \left(\frac{1}{L - \Delta L} \right) (V_{GS} - V_{th})^2 \\
 &= \frac{1}{N} \mu_W C_{ox} (V_{GS} - V_{th})^2 \left[\frac{1}{L} + \frac{\Delta L}{L^2} \right] \\
 &= \frac{1}{N} \mu_W C_{ox} (V_{GS} - V_{th})^2 (1 + \Delta L/L) \\
 &= \frac{1}{N} \beta (V_{GS} - V_{th})^2 (1 + \Delta L/L)
 \end{aligned}$$

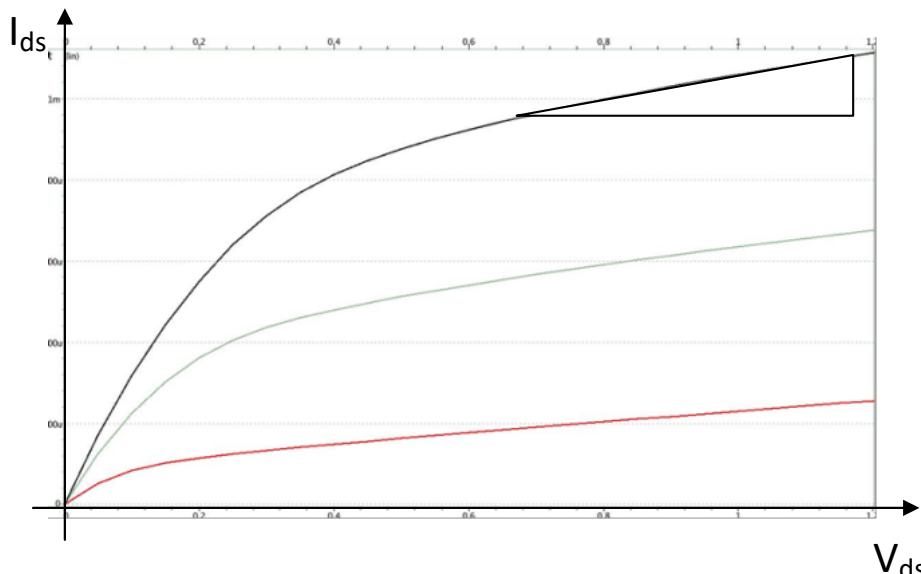


$$\frac{\Delta L}{L} \approx \gamma V_{DS}$$

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Channel Length Modulation

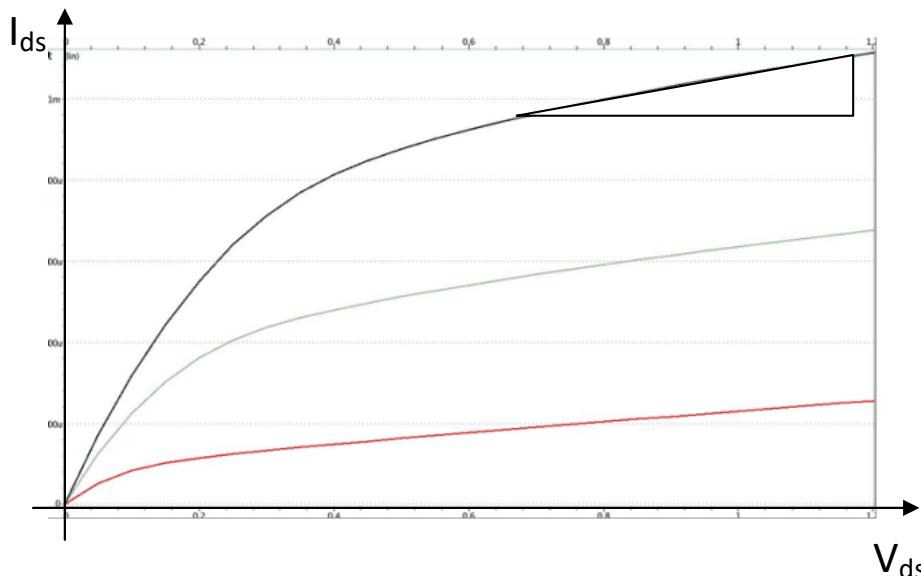
- Simplifying assumption:
 - Fractional change in channel length is proportional to V_{DS}
 - If ΔL is the depletion width, Let $\frac{\Delta L}{L} = \lambda V_{ds}$



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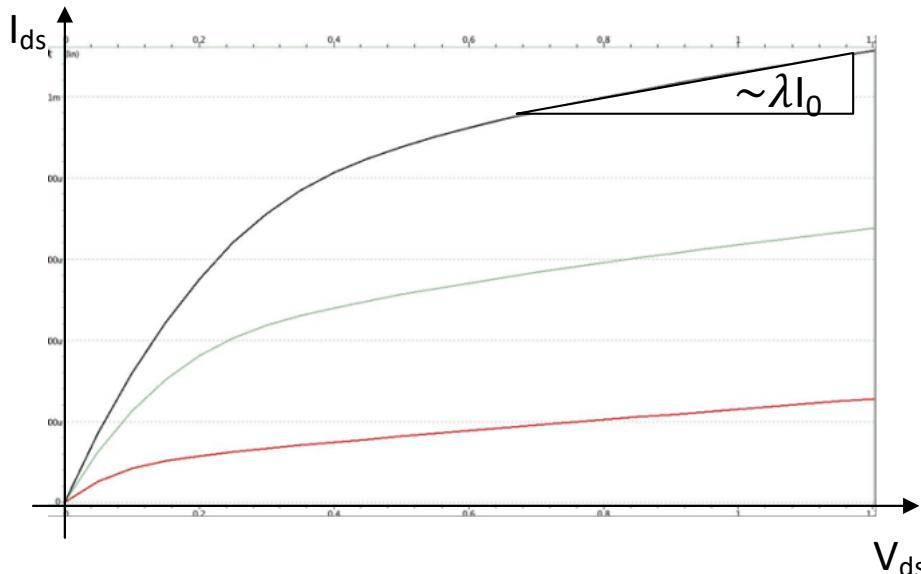
What is the gradient of this line?



Channel Length Modulation

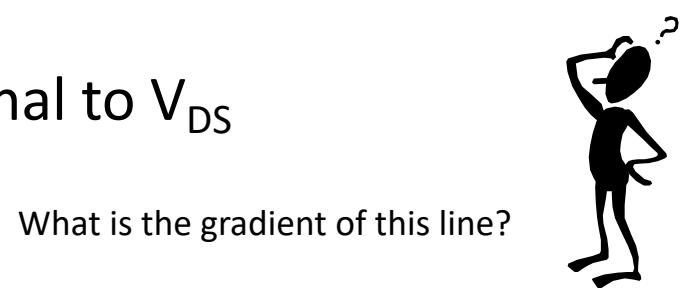
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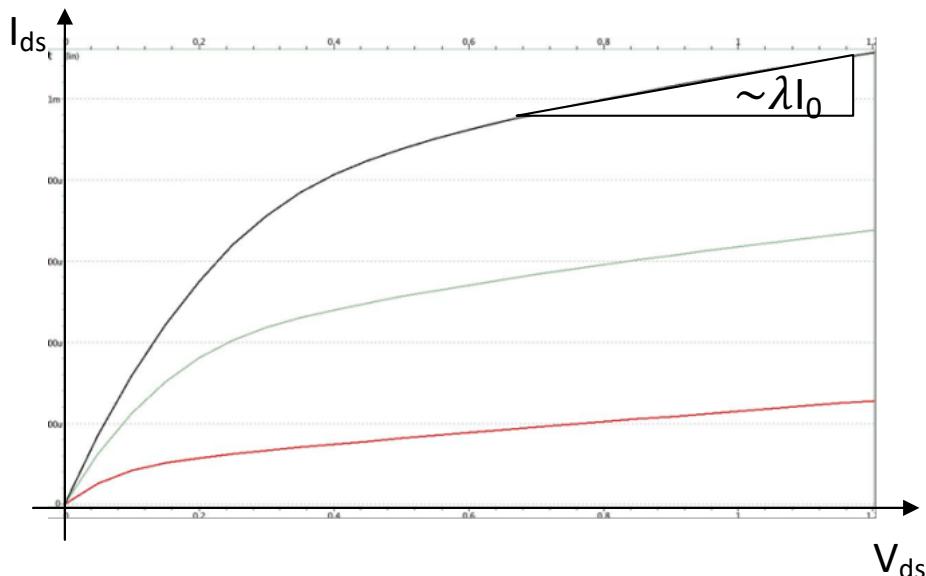


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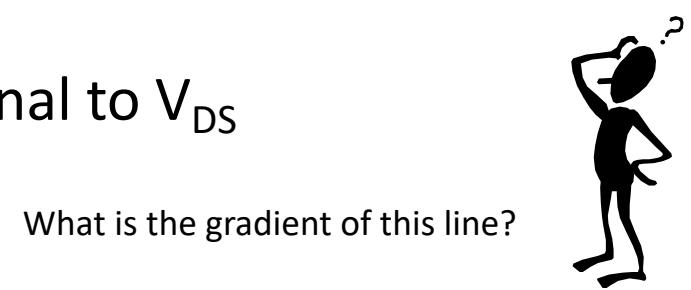


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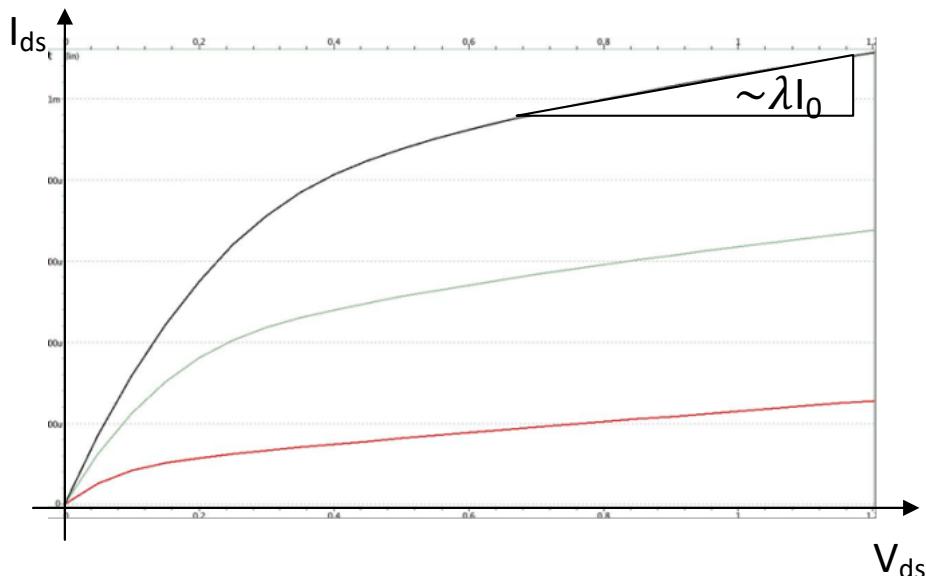
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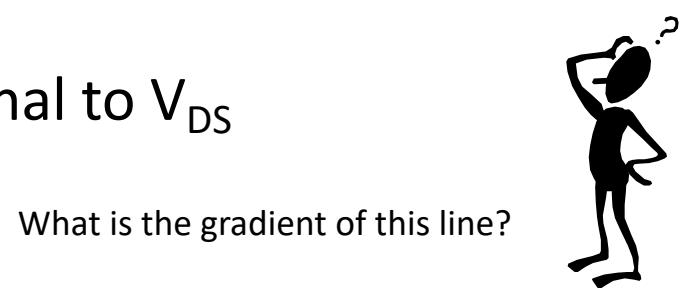
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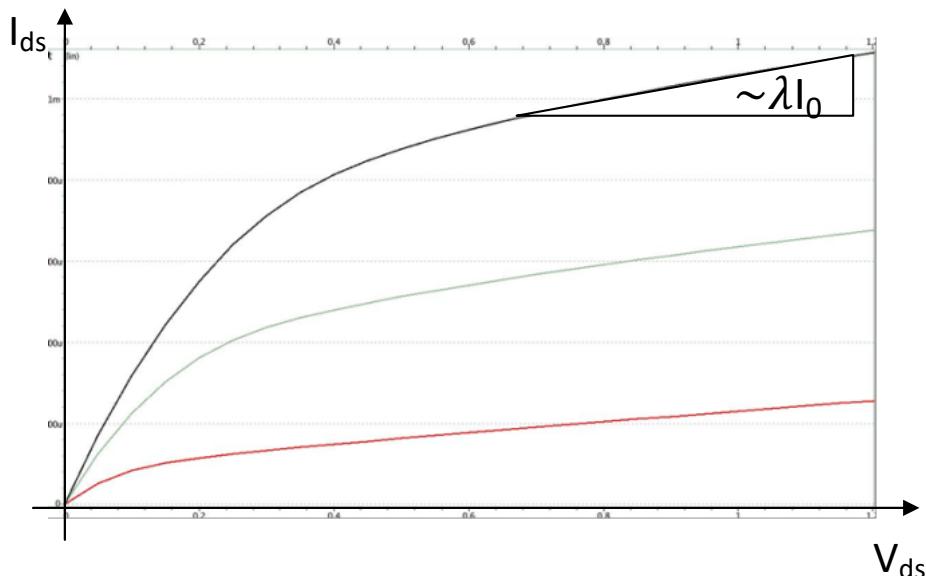


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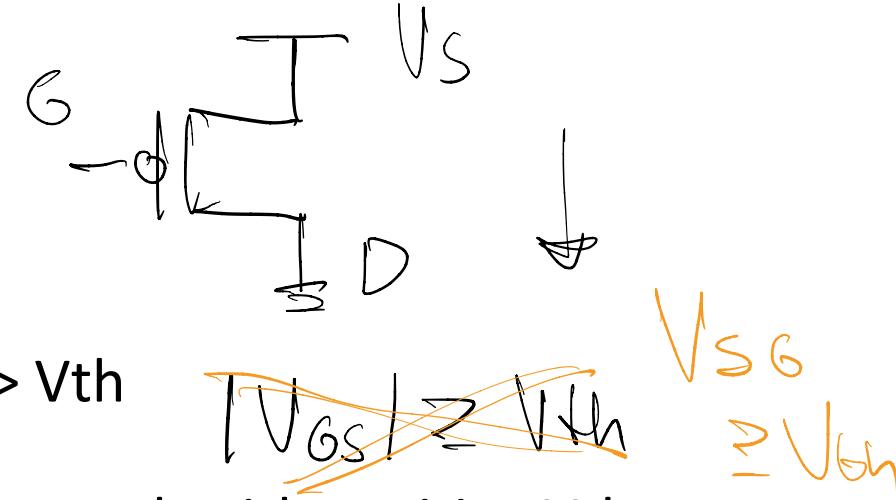


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PMOS Operation

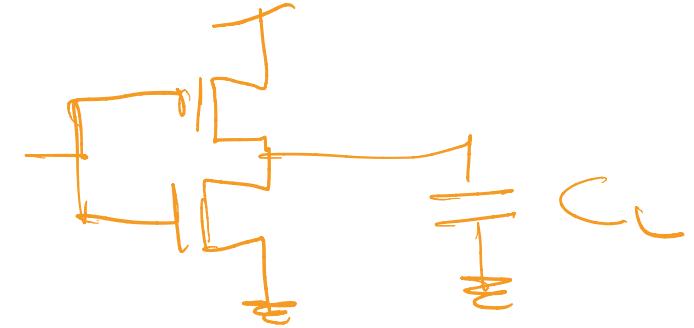
- Essentially a dual of the NMOS device operation
- For conduction: $V_g - V_s < -V_{th} \rightarrow V_s - V_g > V_{th} \rightarrow V_{sg} > V_{th}$
 - Gate overdrive continues to have to exceed V_{th}
- A lot more convenient to work with V_{sg} , V_{sd} and always work with positive V_{th} values (convention adopted in this class)
- Exercise: Derive the current equation of the PMOS device
- Note: PMOS carrier μ_p is lower than NMOS μ_n $\rightarrow \downarrow$ current drive for the same gate overdrive.



V_{sg} , V_{sd} , V_{th} relationship	PMOS operating region
$V_{sg} < V_{th}$	Cutoff (Not conducting)
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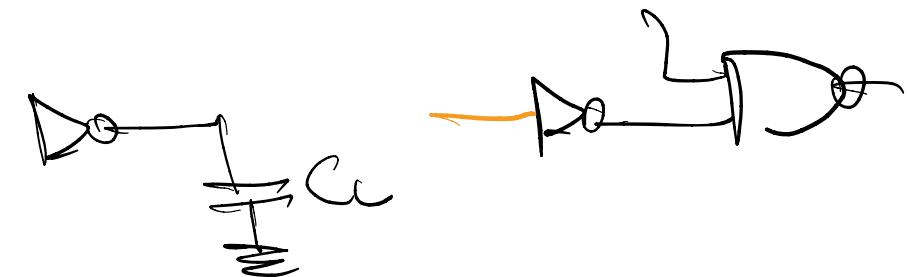


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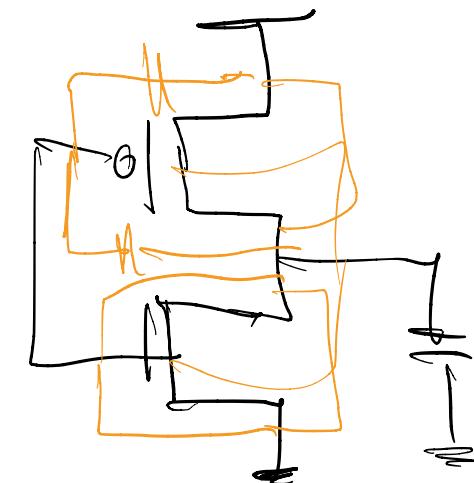
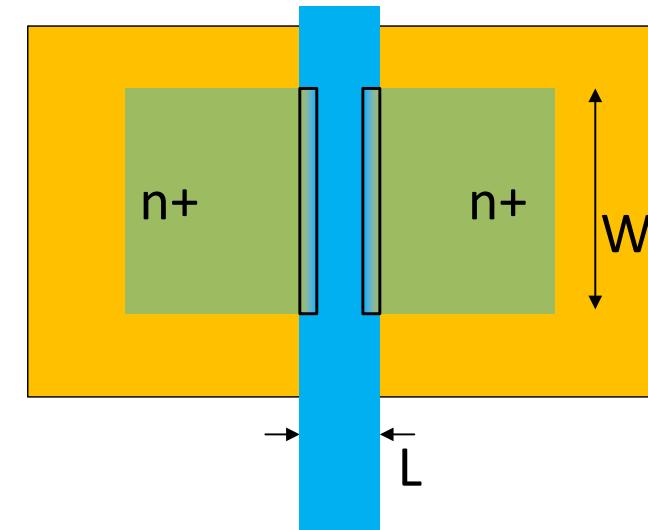
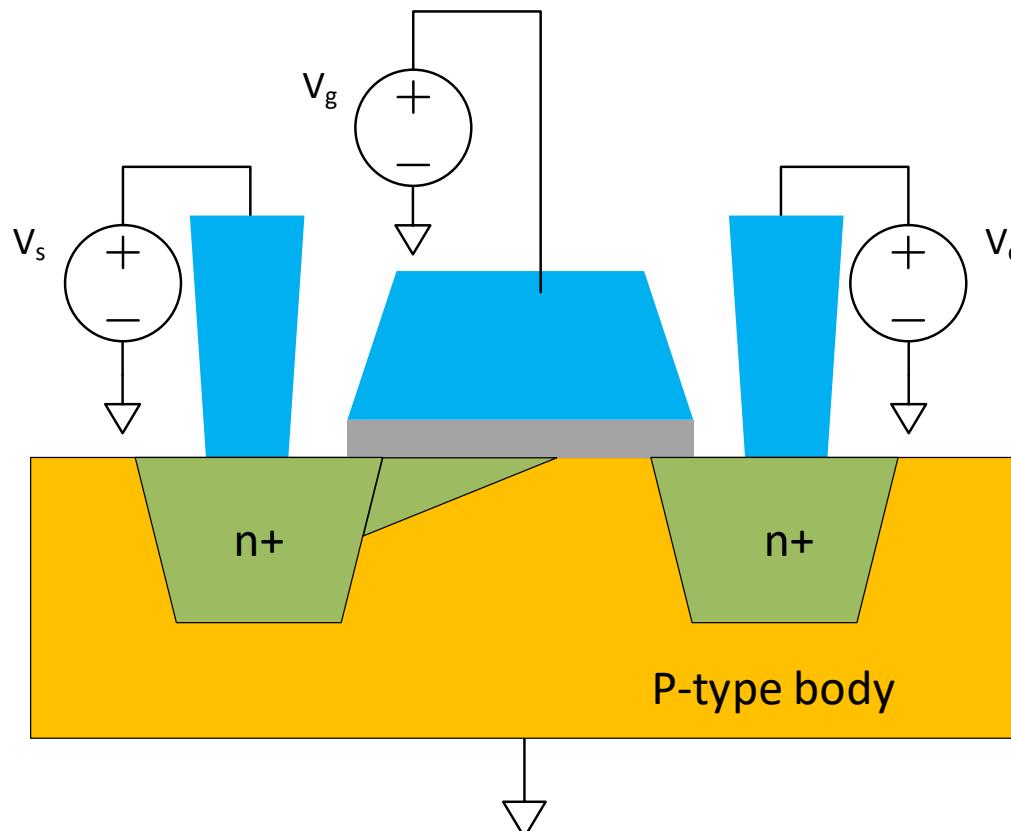
How can I fix that if I want equal drive strength?



MOSFET Gate Capacitance

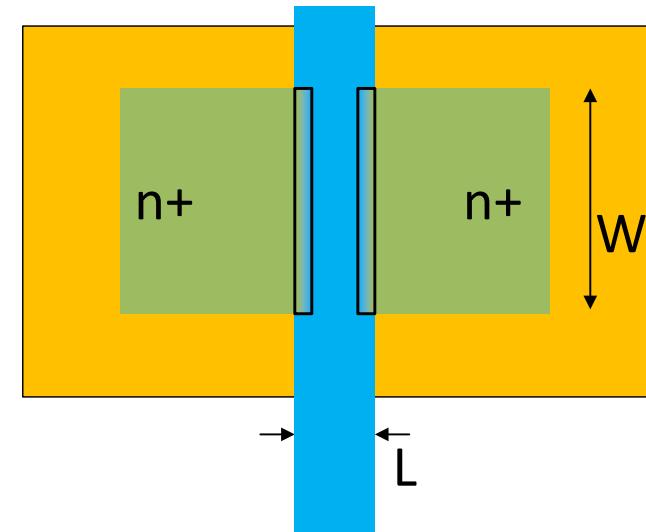
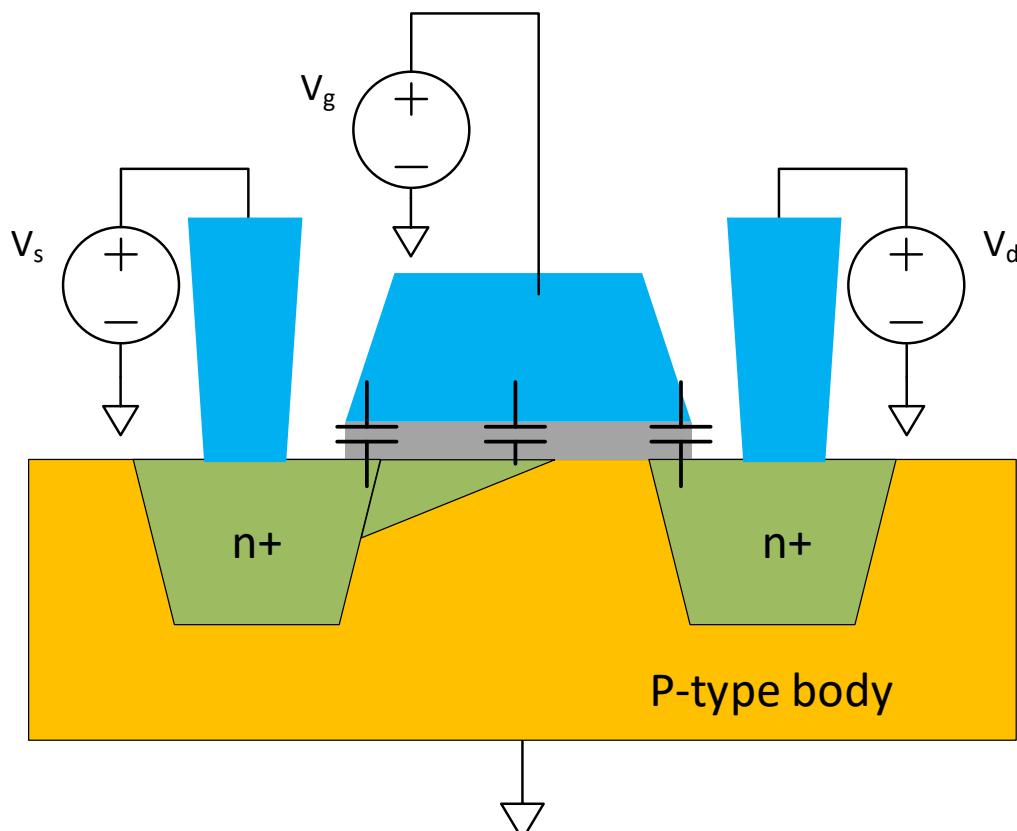


- Zeroth order, $\text{Cap} = W * L * C_{\text{ox}}$
 - Overlap capacitance (Gate-source, Gate-drain)
 - Channel-connected cap
 - Source, drain contact cap (approximately $\propto W$)



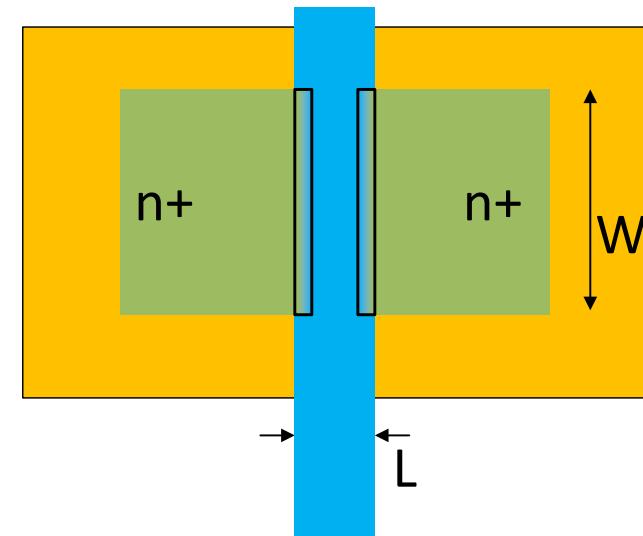
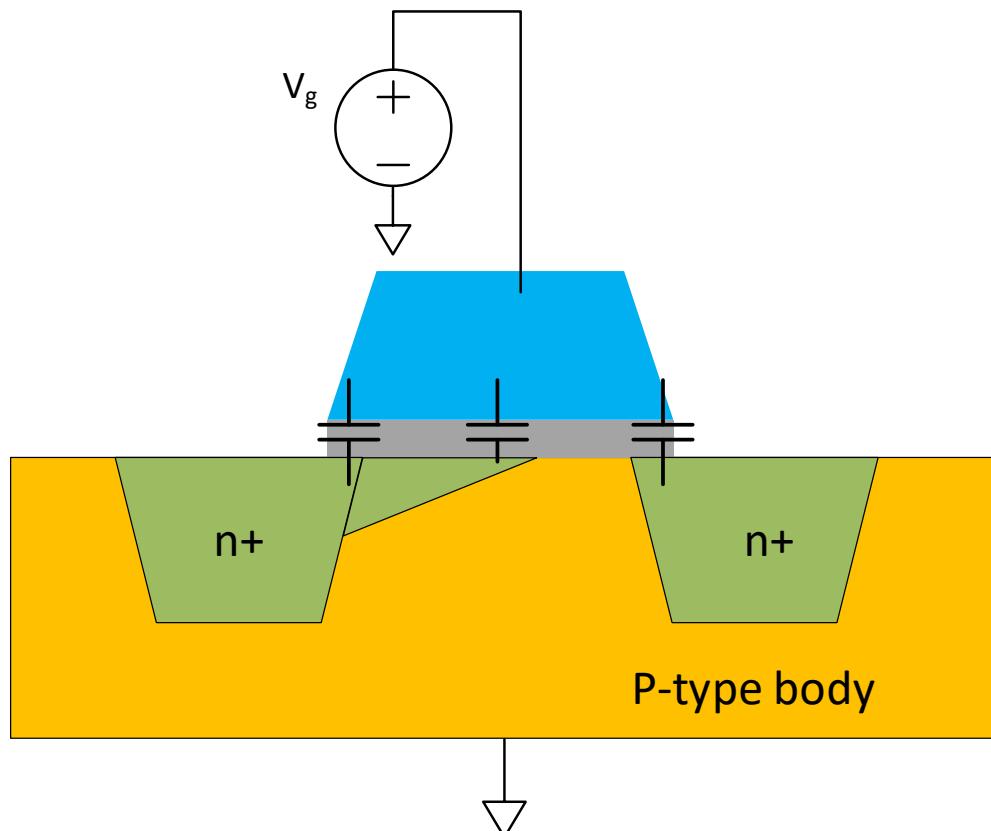
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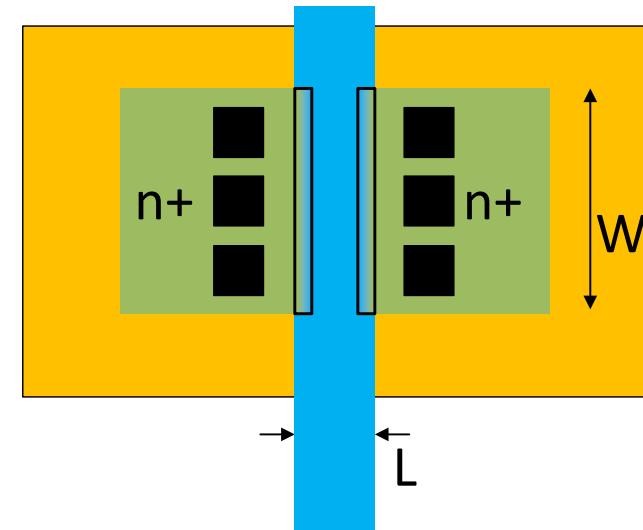
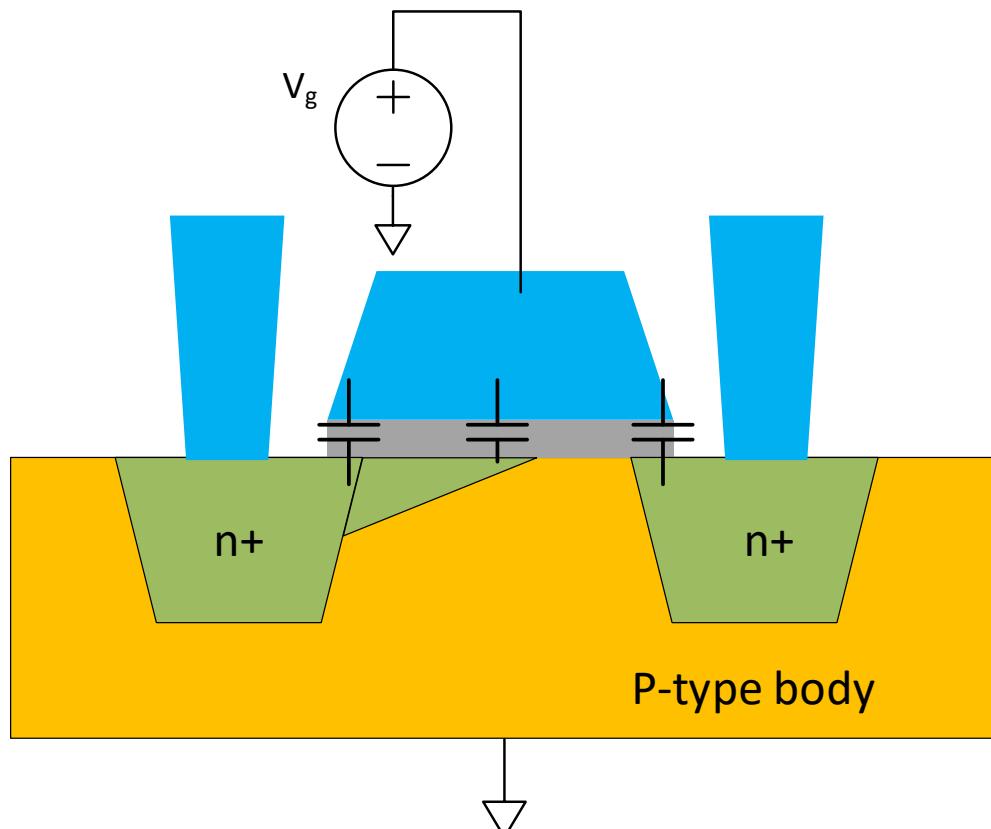
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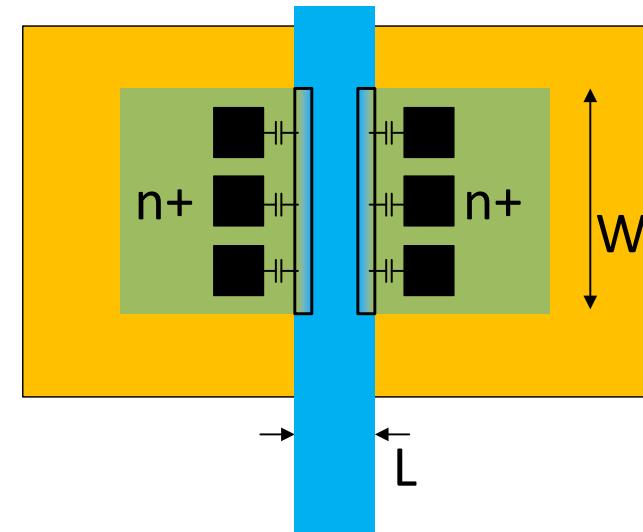
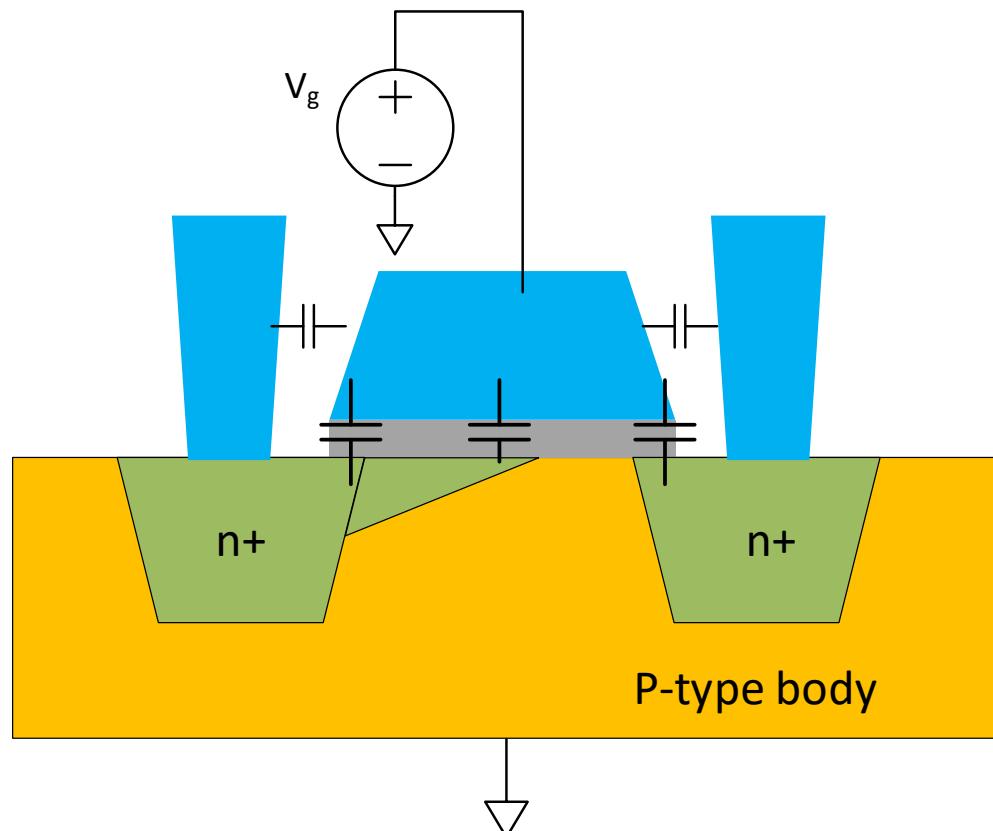
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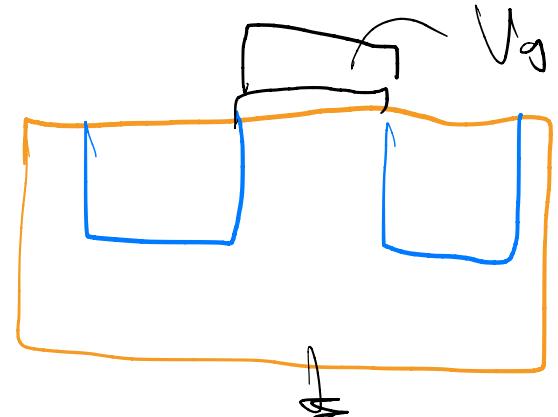
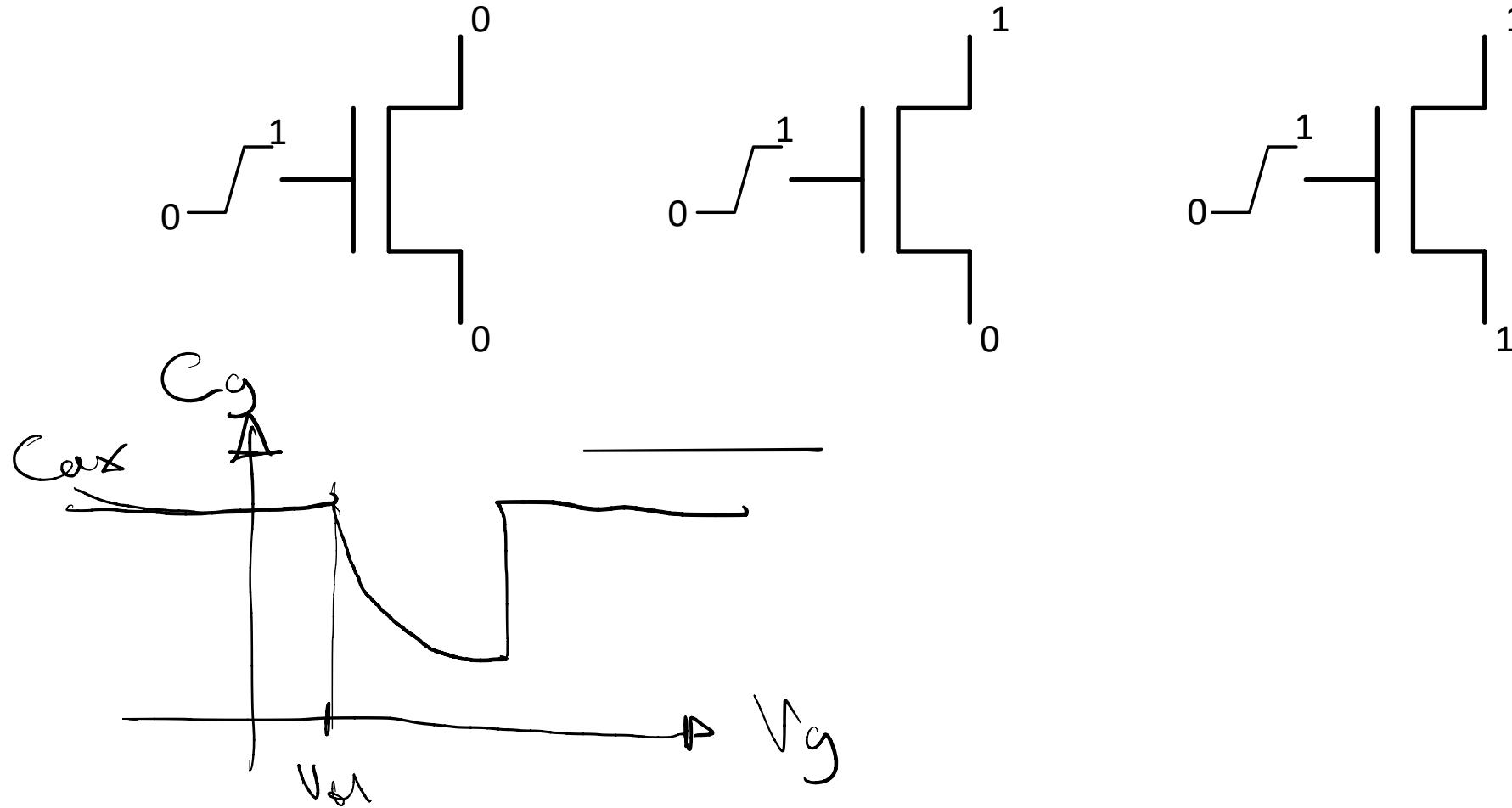
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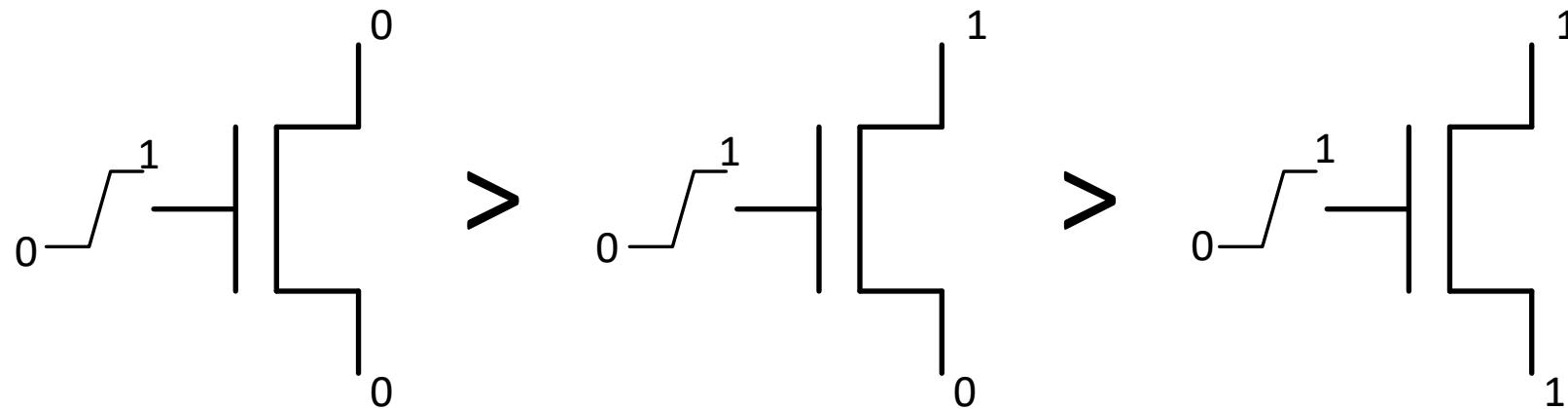
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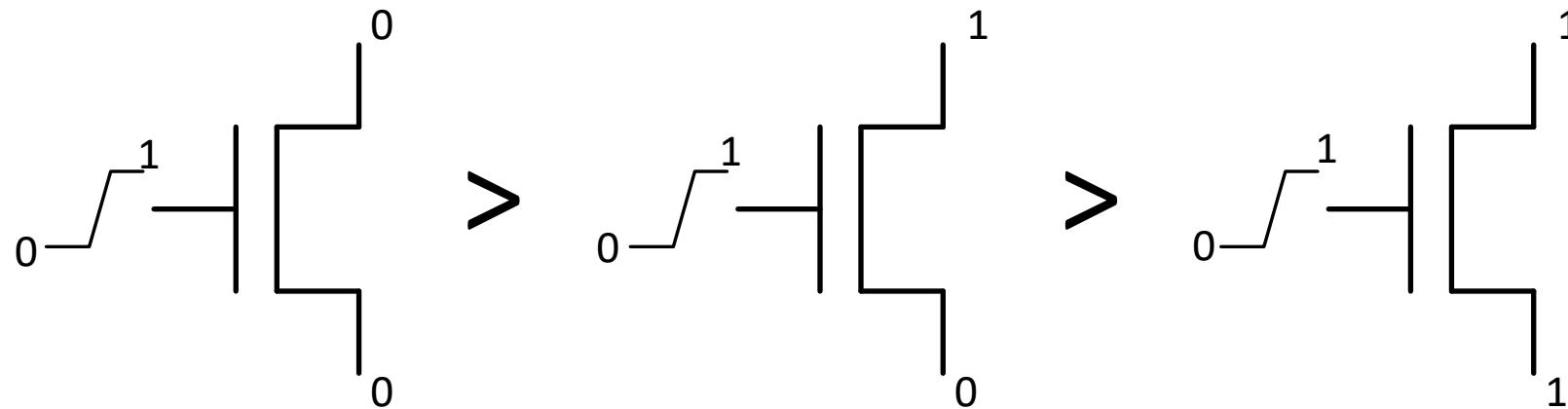
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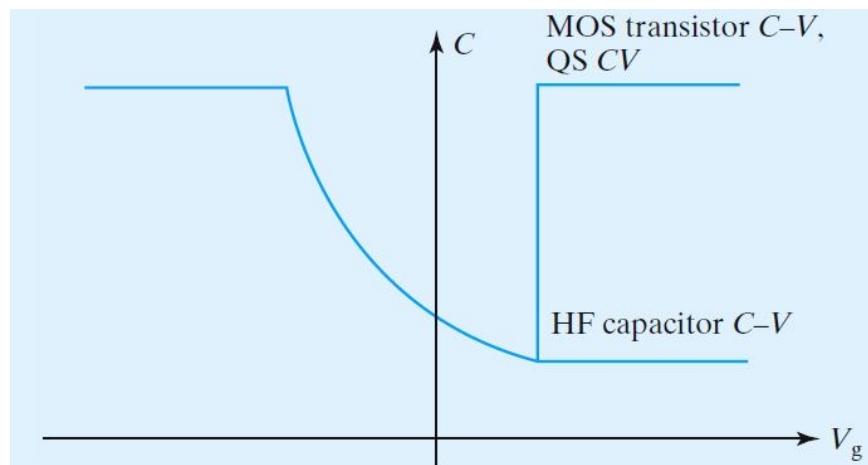
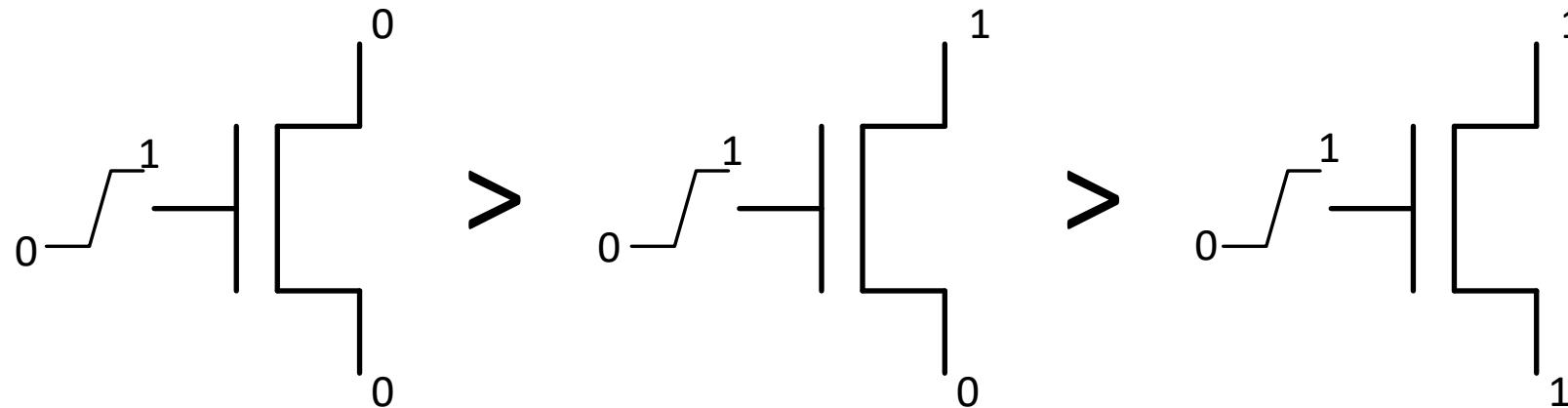


Optional assignment:
Why do I not see the
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