Lecture 3: Basic MOSFET Theory

Based on material prepared by prof. Visvesh S. Sathe

ELECTRICAL & COMPUTER ENGINEERING

Acknowledgements

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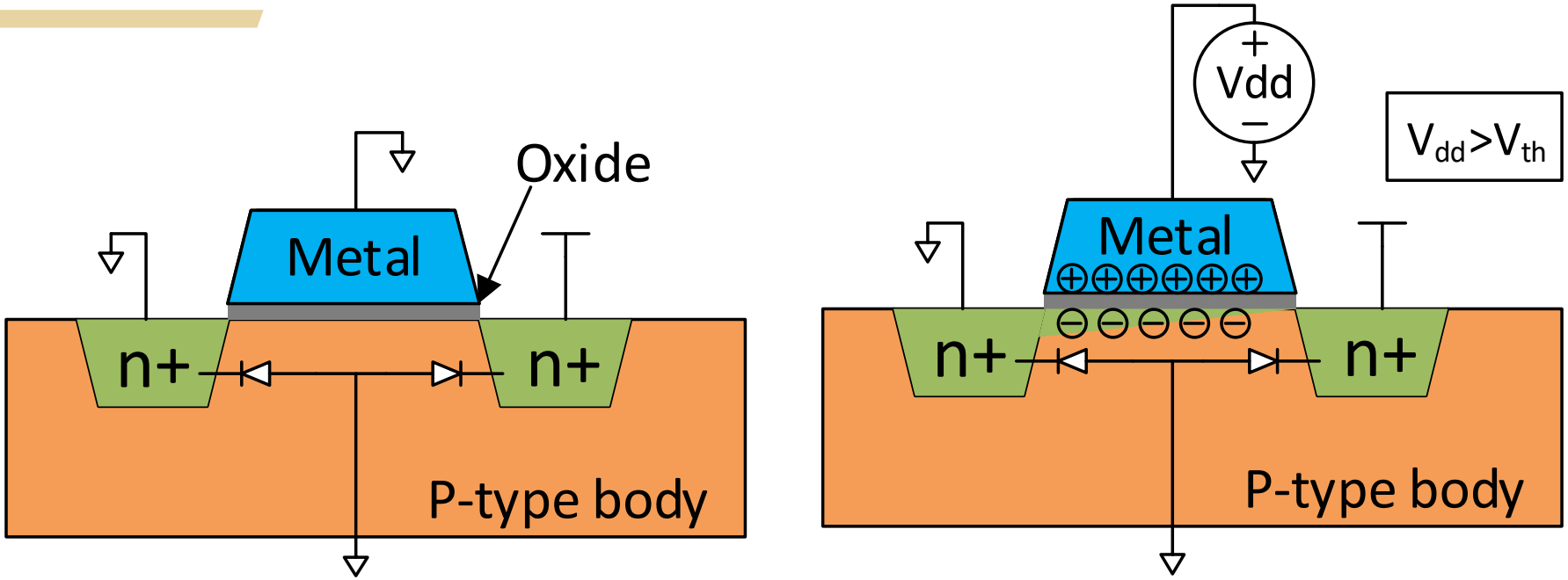
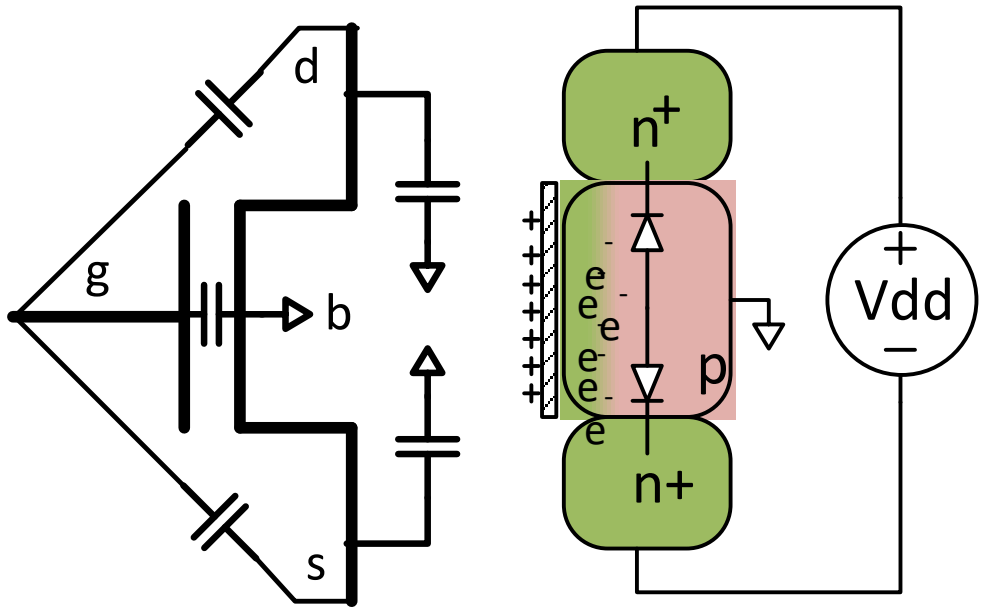
UW (2013-2022)
GaTech (2022-present)

The MOS Structure



- Metal Oxide Semiconductor
  - "Metal" implemented as poly-crystalline silicon (polysilicon) till recently
  - Conductor-insulator-semiconductor "sandwich"
  - Changing the voltage across Metal-Semiconductor varies the properties of the semiconductor

Quick Detour: Parasitic Capacitance



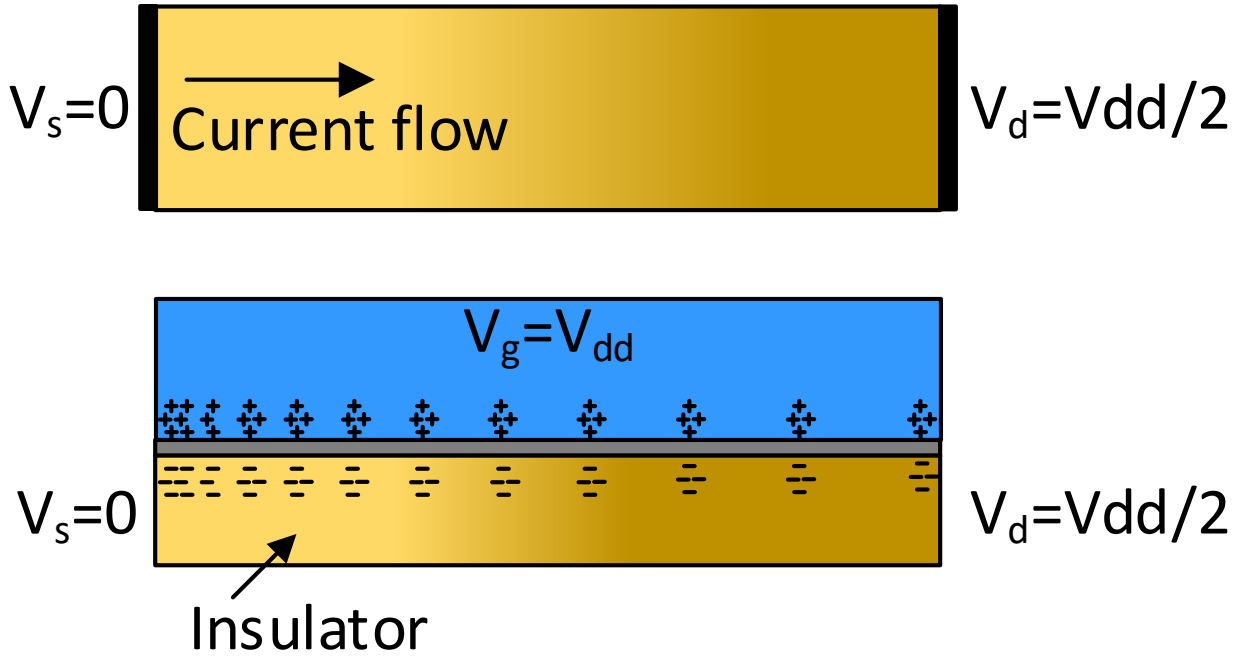
Impact

- Circuit Speed (Digital)
- Power (Digital)
- Bandwidth (Analog)
- Stability (Digital, Analog)

- What is capacitance exactly?
  - So what's so bad about it?
    - V-driven, not Q-driven
    - Low C → Lower Q, faster, lower energy
    - Smaller is faster (Dennard's law)
  - Major Parasitic contributors
    - MOSFET gates, MOSFET source/drains, wire

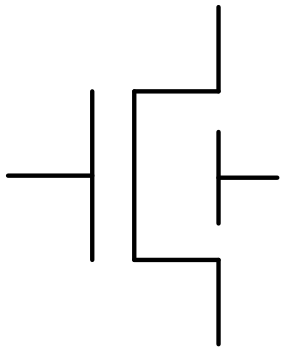
Calculate the per-unit length capacitance of an infinitely long cylindrical wire, diameter d in free space

MOS Transistor – A 10K foot view

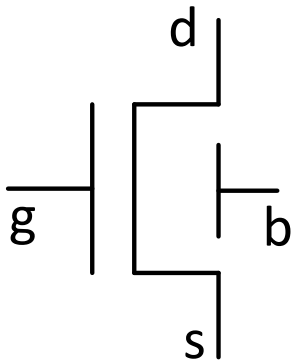


- Capacitor charge buildup allows for a “channel” to form
- Charge density not uniform ➔ ? Impact on R. ? Impact on V(x)
- How can I reduce the resistance of this device further?

MOS Transistor – A Strictly Intuitive View

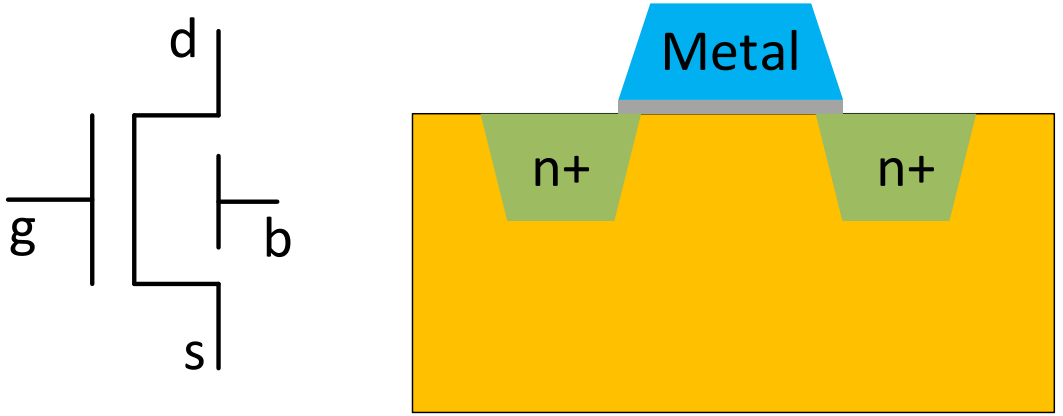


MOS Transistor – A Strictly Intuitive View

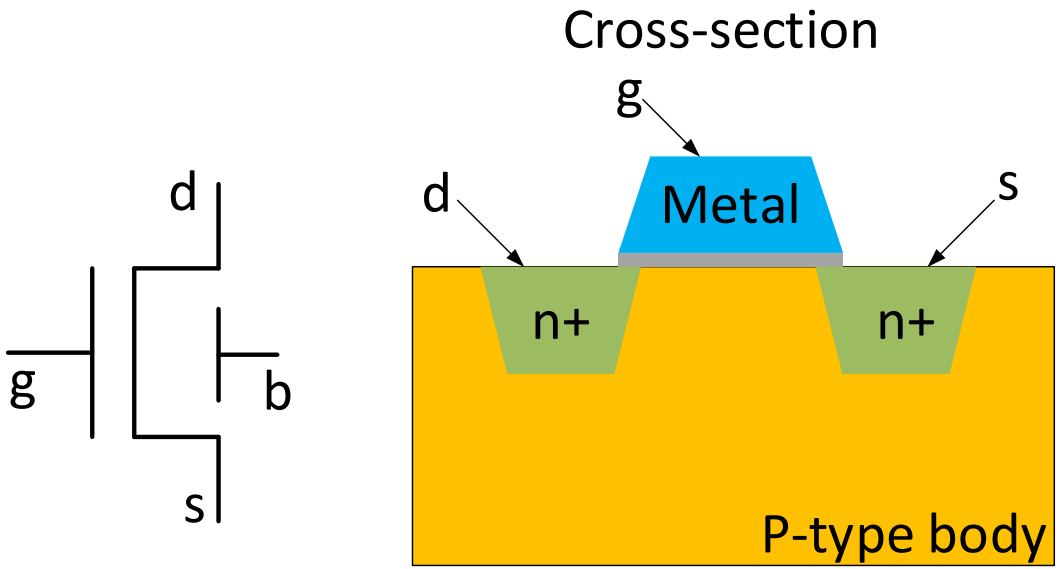


MOS Transistor – A Strictly Intuitive View

Cross-section



MOS Transistor – A Strictly Intuitive View



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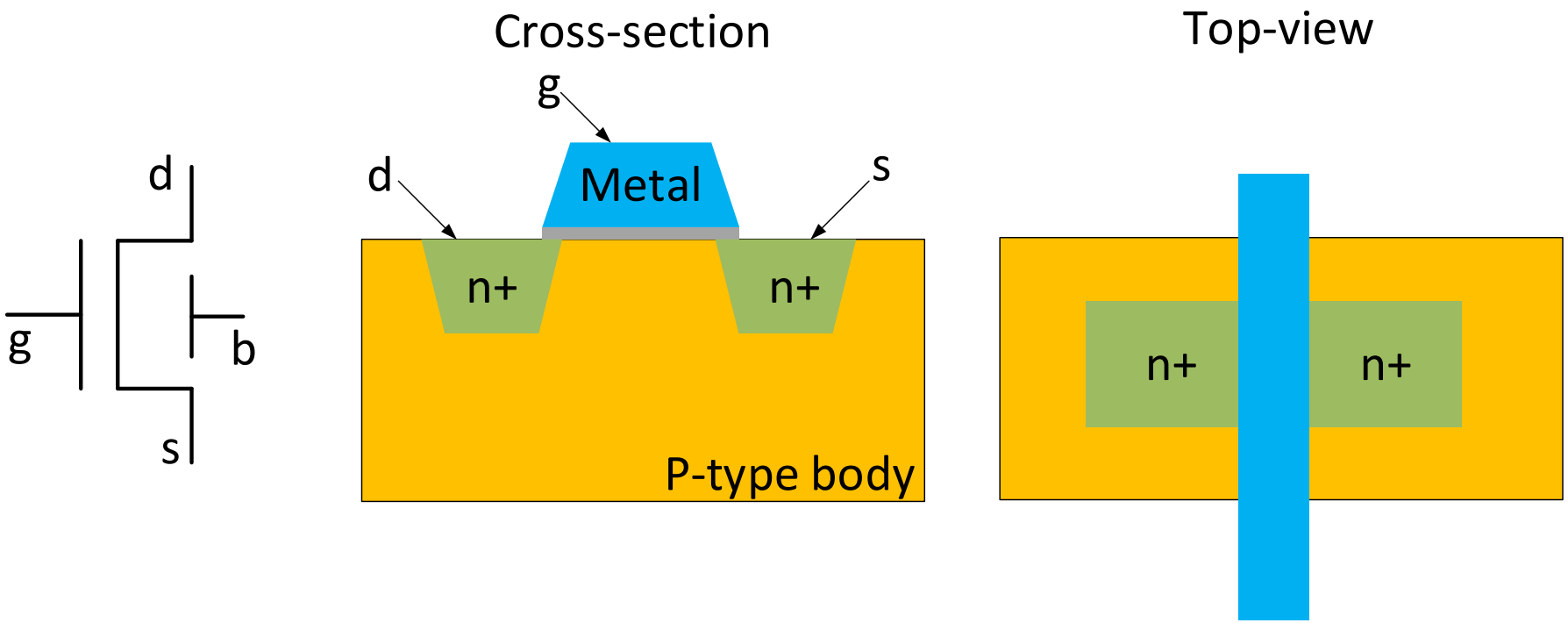

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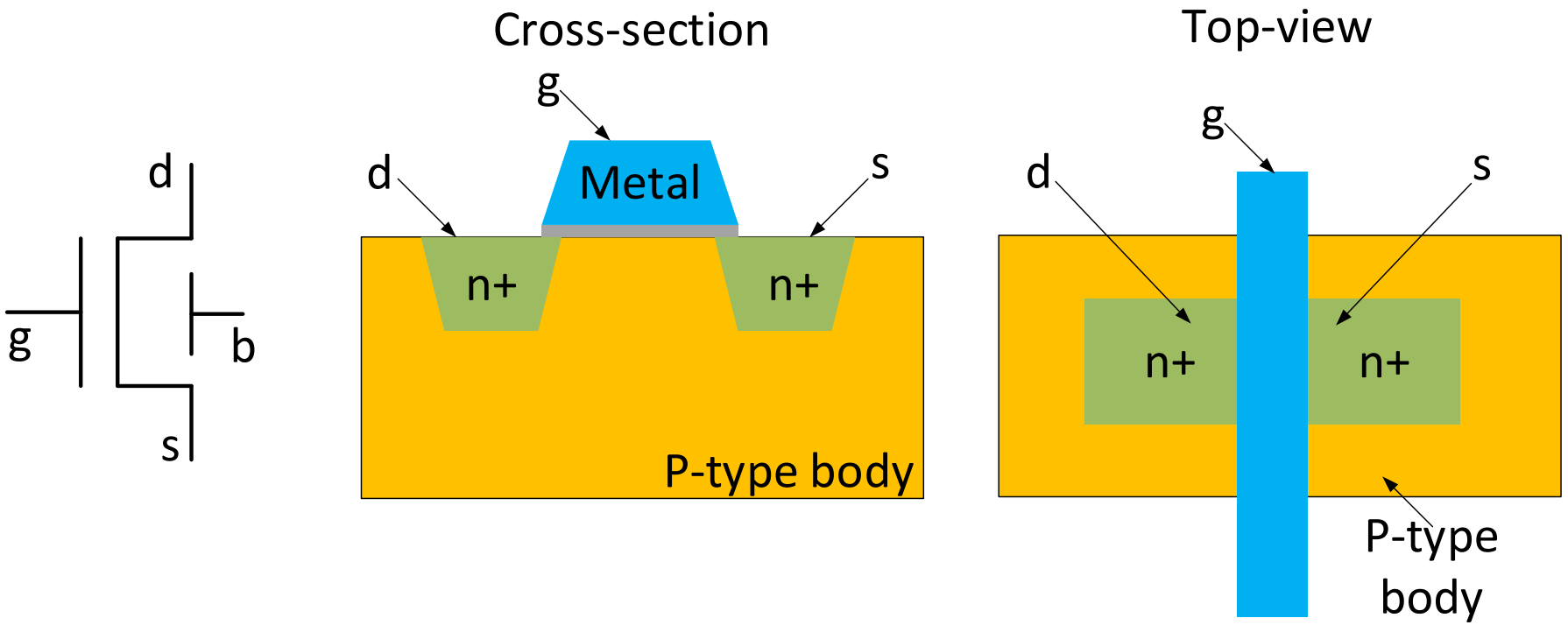

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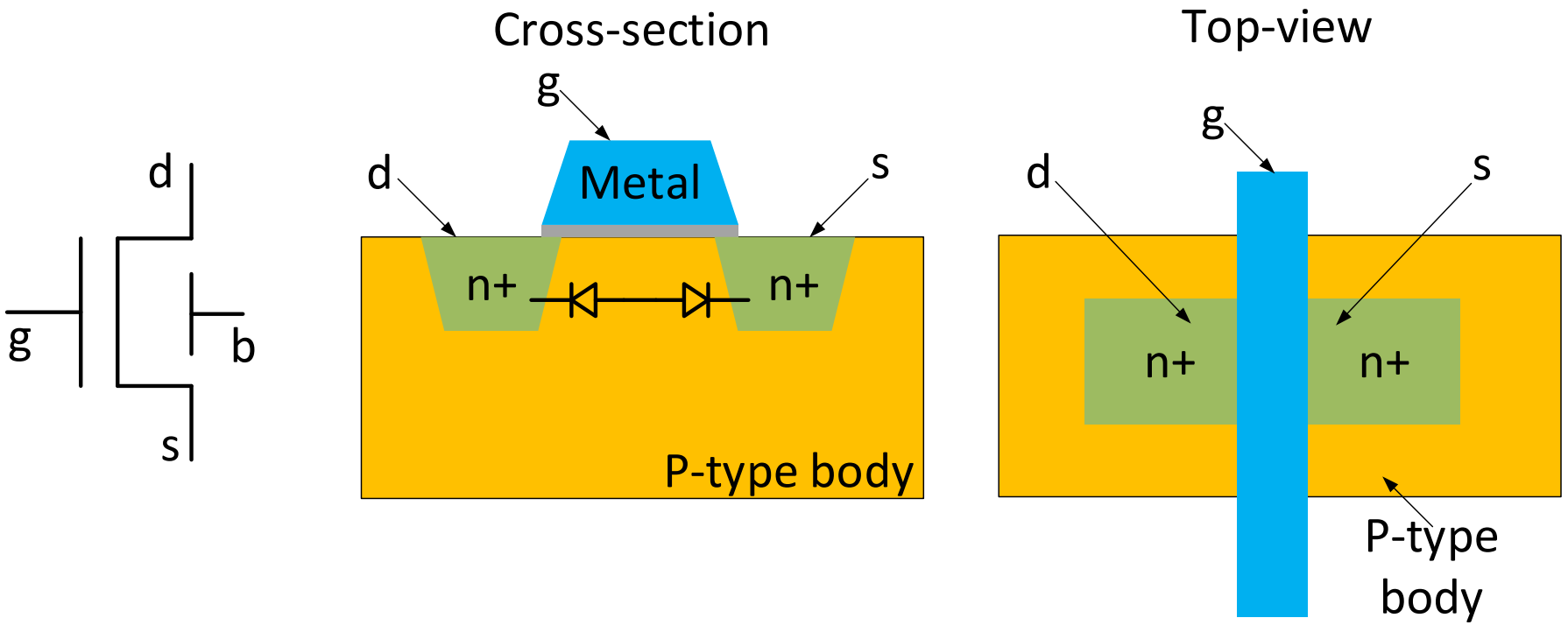

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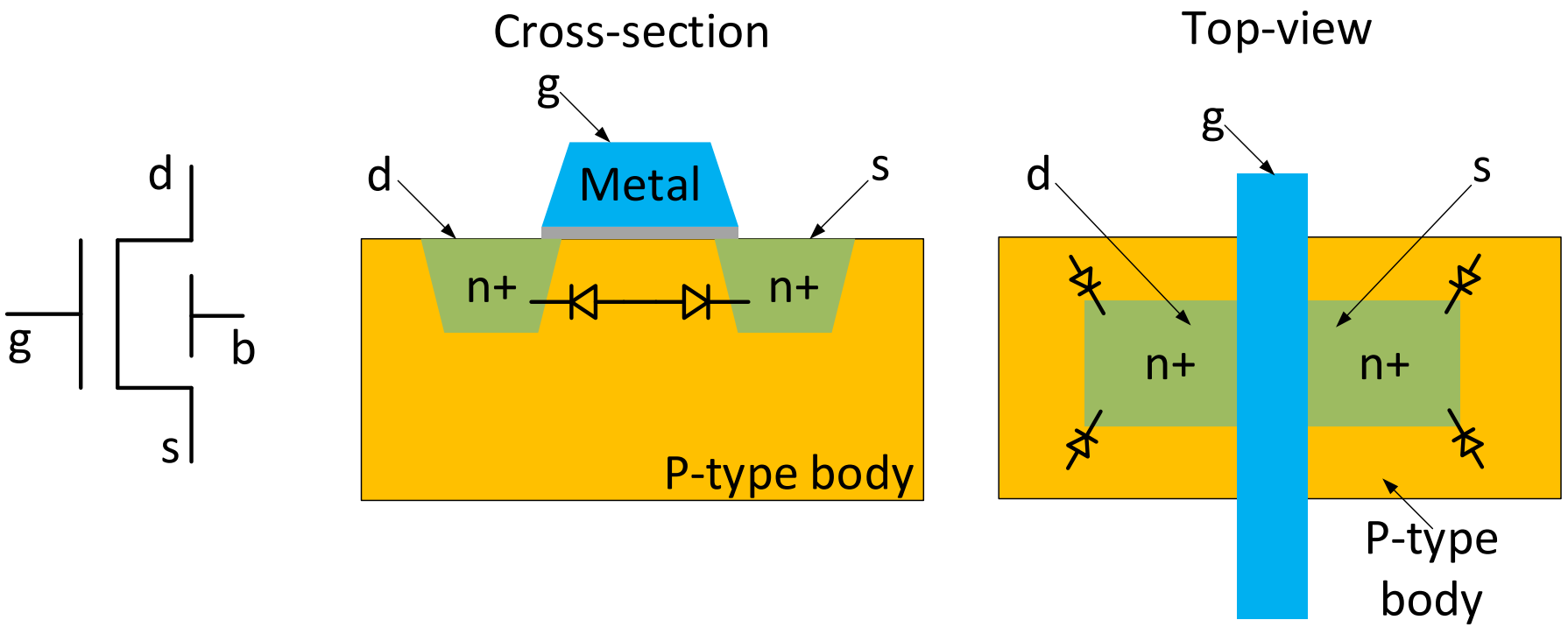
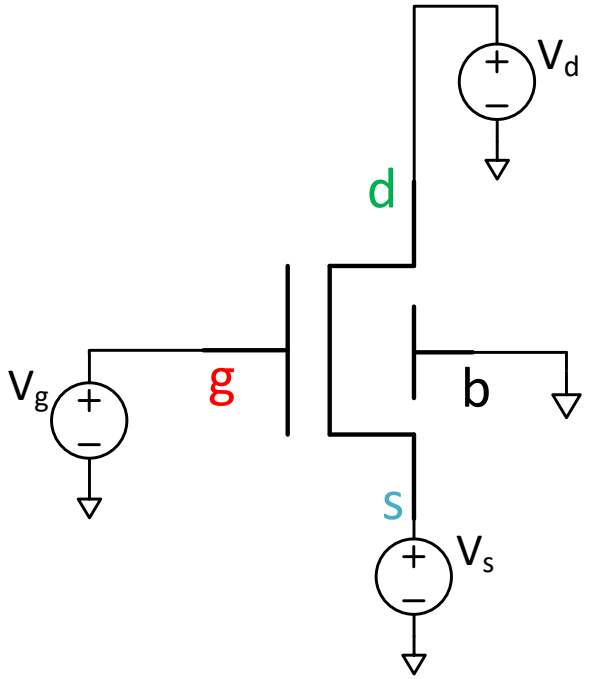
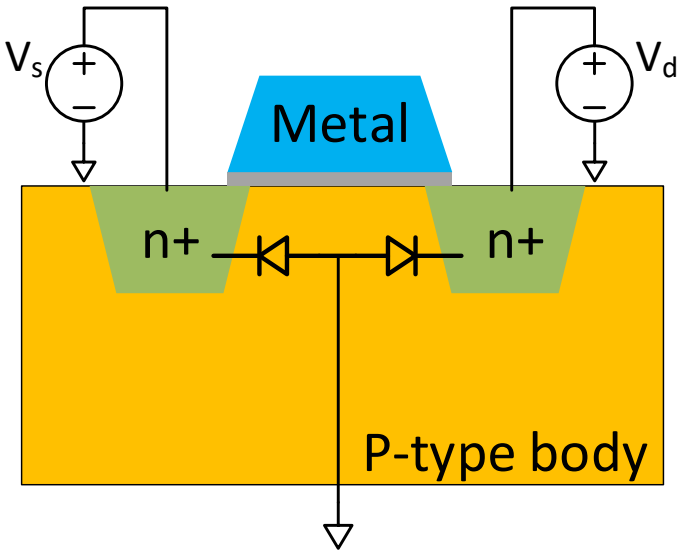


MOS Transistor – A Strictly Intuitive View

- For this course
  - Body of an **nmos** device is always tied to **ground**
  - Body of a **pmos** device is always tied to **Vdd**





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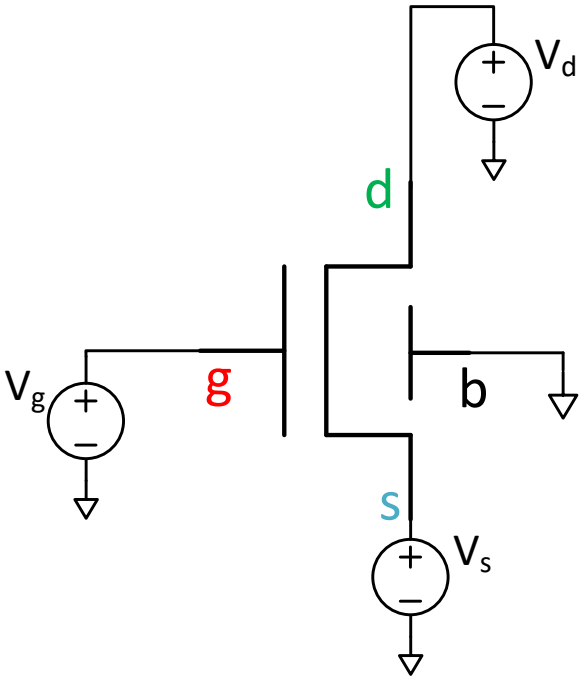
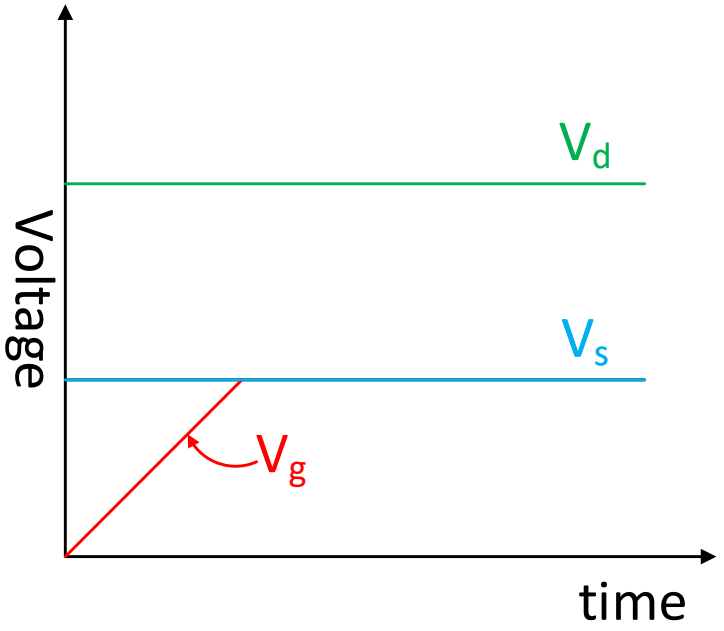
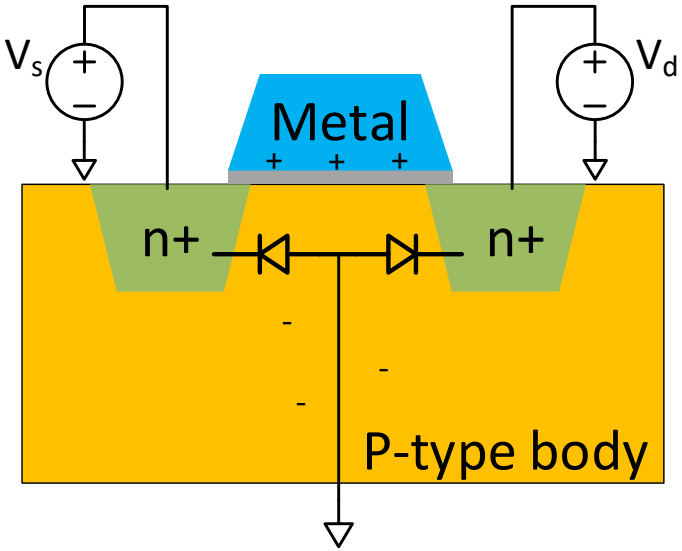
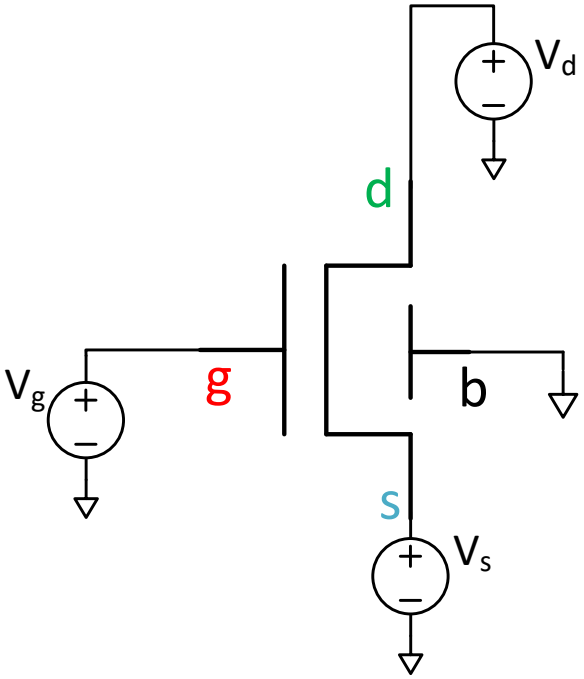


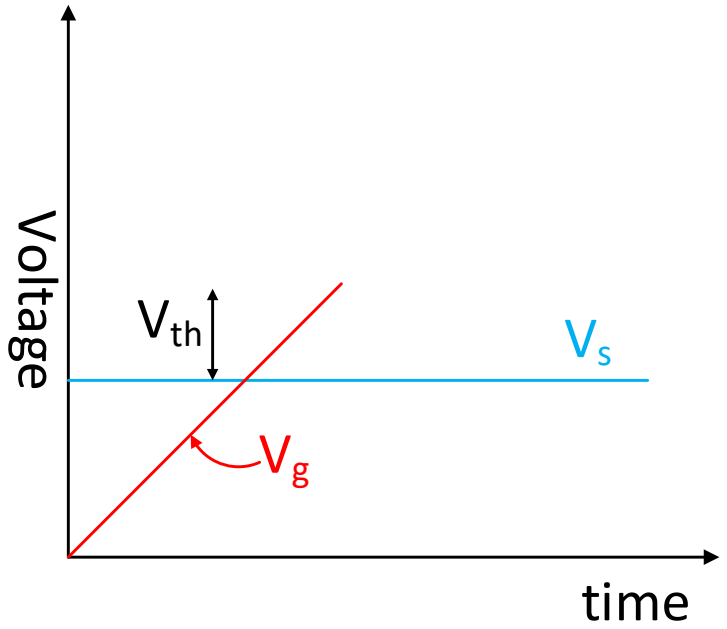


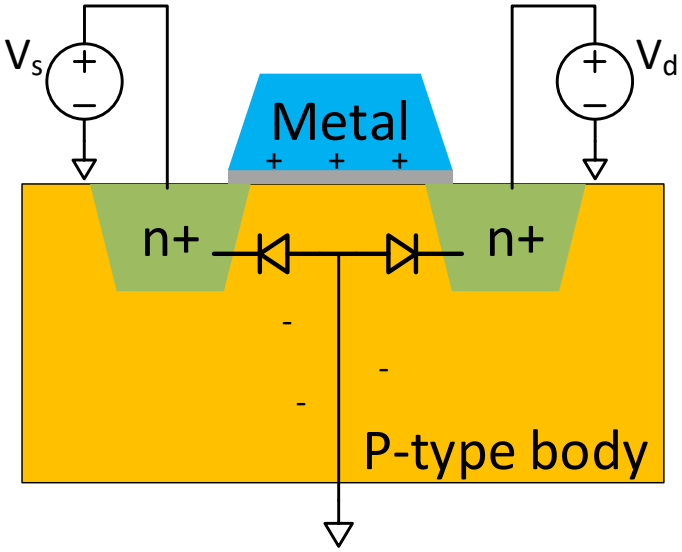


- Initially Vg<Vs
- No channel formed

MOS Transistor – A Strictly Intuitive View

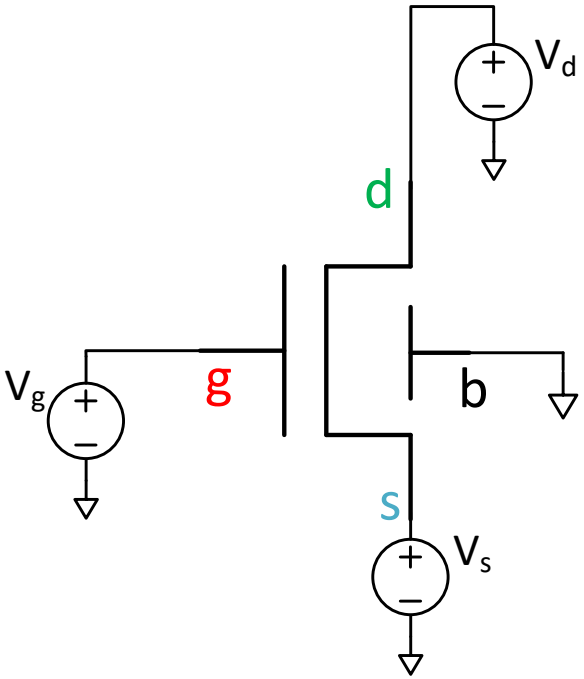


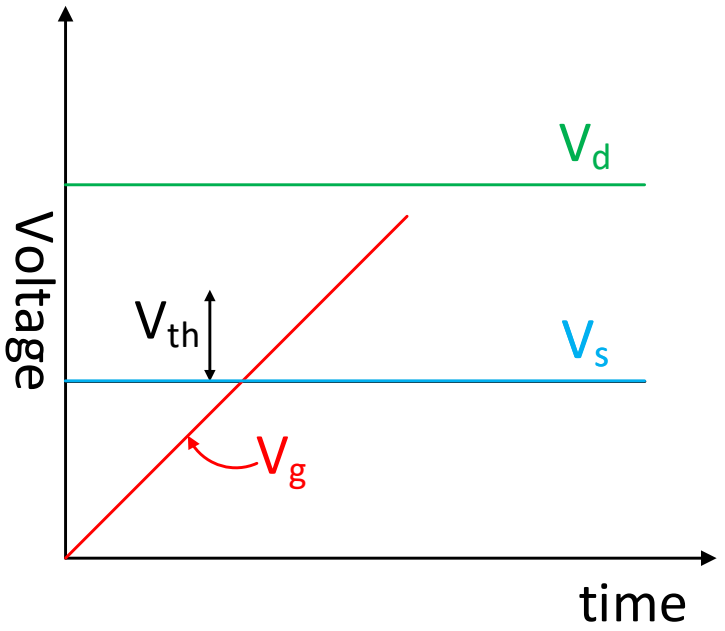


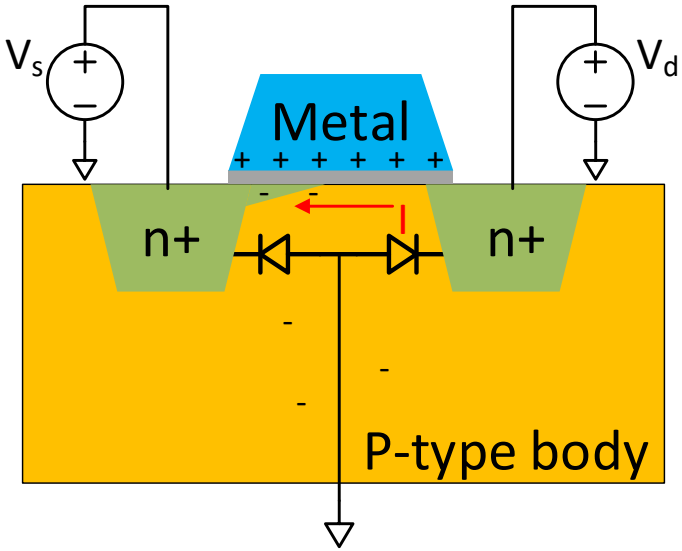


- Initially Vg>Vs
- But Vg – Vs < Vth → No channel formed
- V_g-V_s ➔ V_{gs}
- $V_{gs} – V_{th} = V_{gs}'$ (Also called gate overdrive)

MOS Transistor – A Strictly Intuitive View

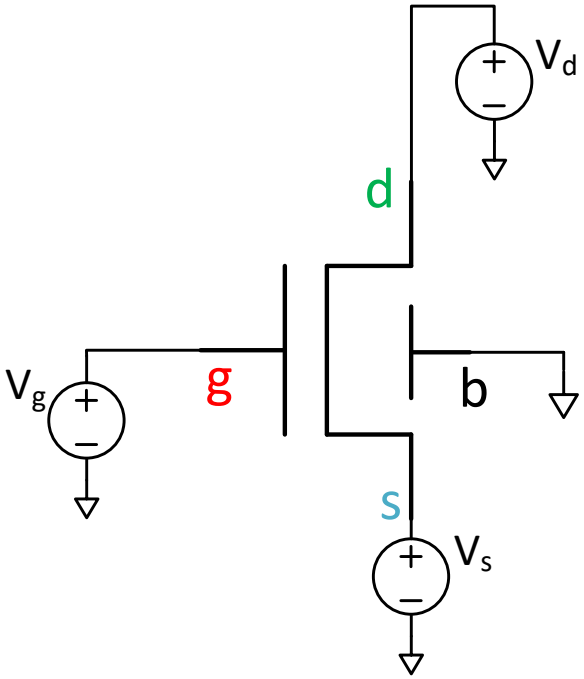


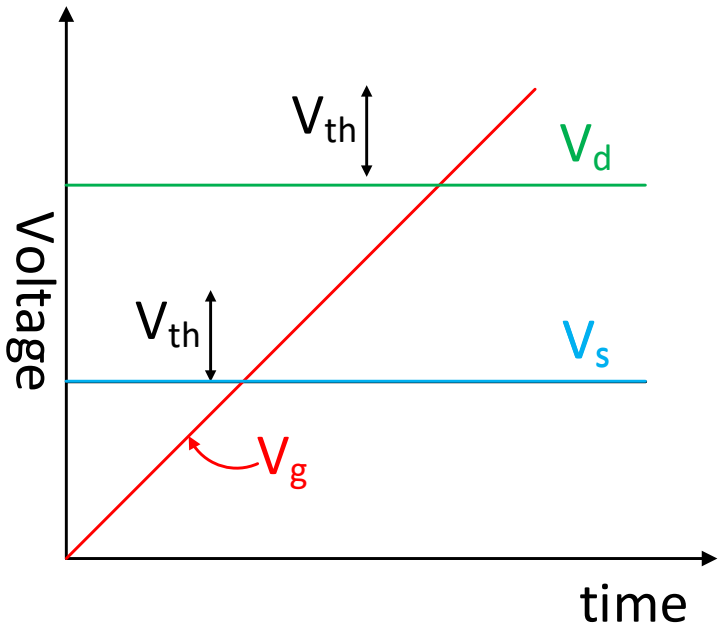


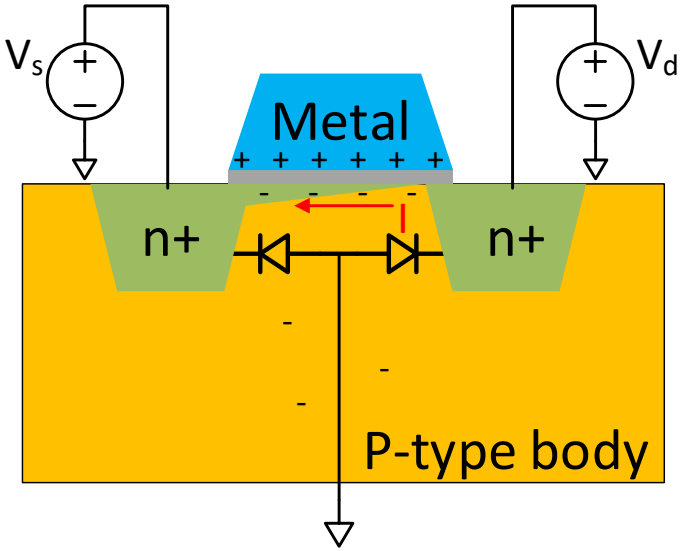


- Channel begins forming as
  $Vg - Vs > Vth \equiv V'_{gs} > 0$ (+gate overdrive)
- Channel still does not extend to L
- Channel not very thick

MOS Transistor – A Strictly Intuitive View

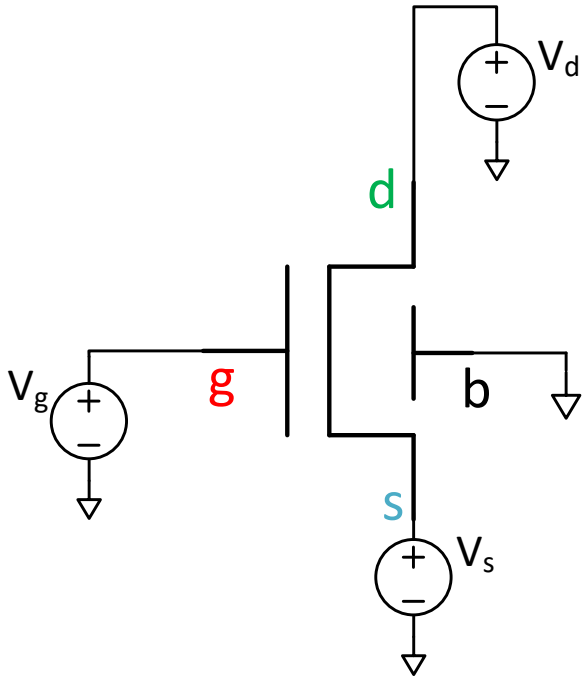


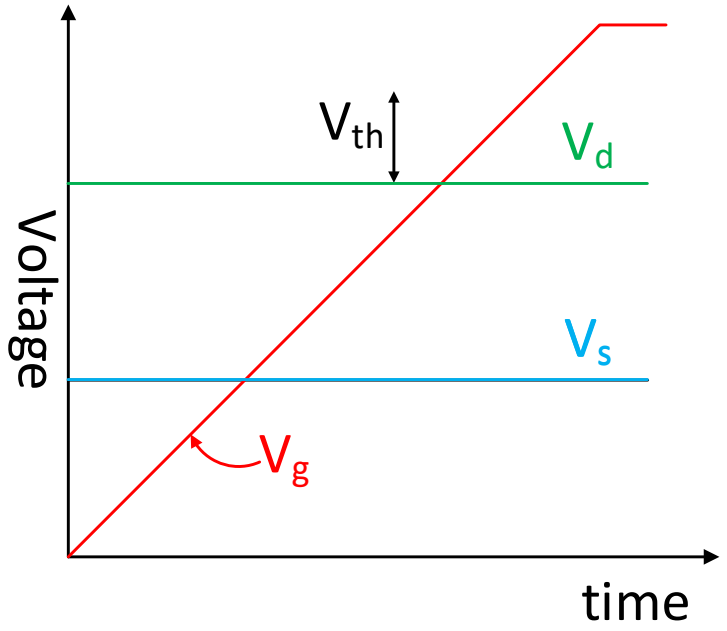


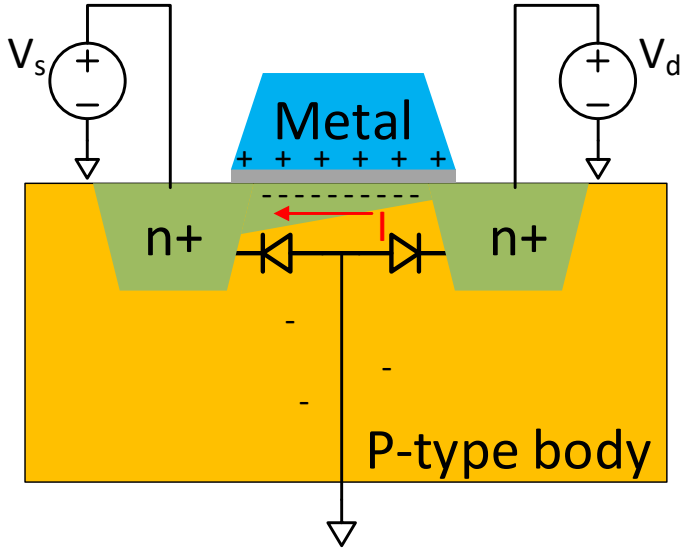


- Channel begins to form as
  Vg – Vs > Vth
- Channel still does not extend to L
- Channel thickness increasing

MOS Transistor – A Strictly Intuitive View

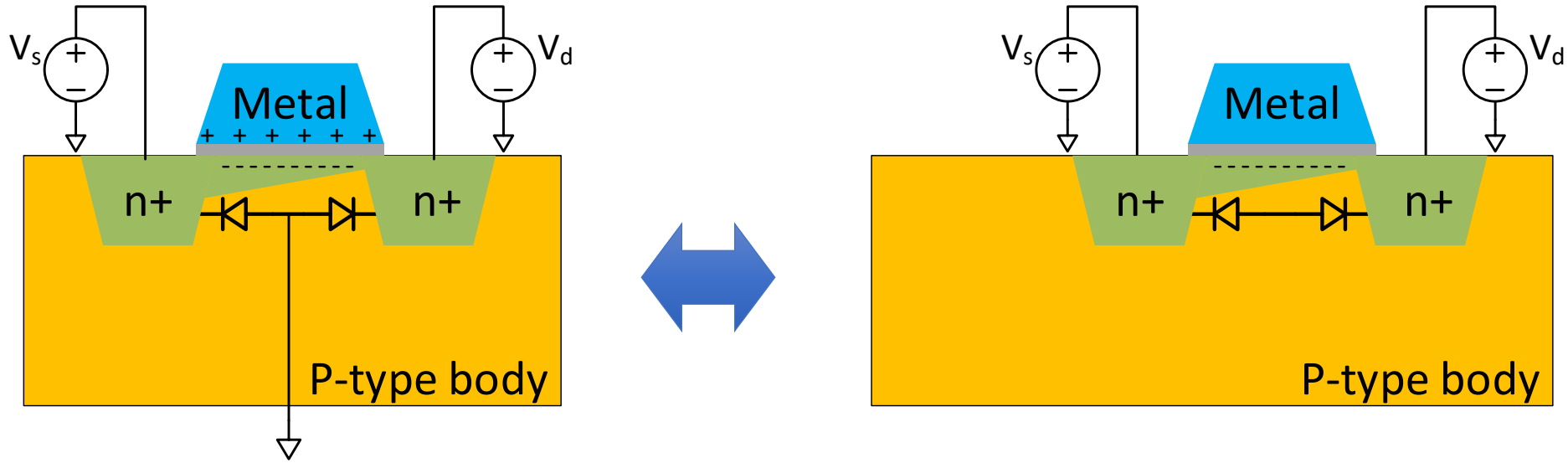






- Channel extends to L as Vg – Vd > Vth
- Channel thicker now → ↓resistance
- Thickness varies along channel!

The Substrate Contact



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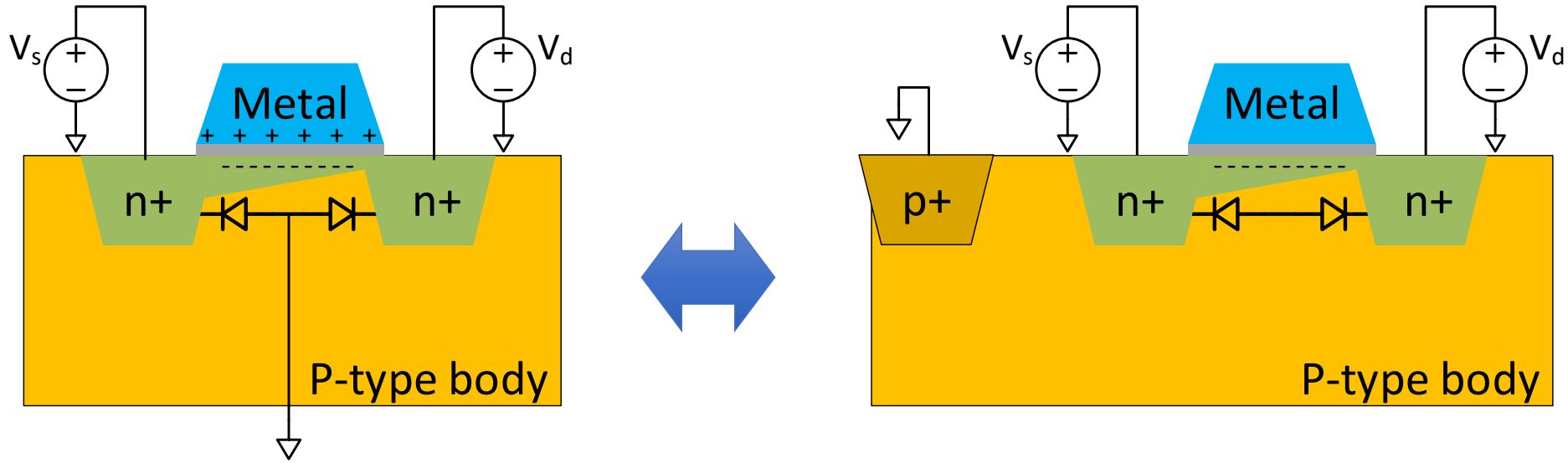
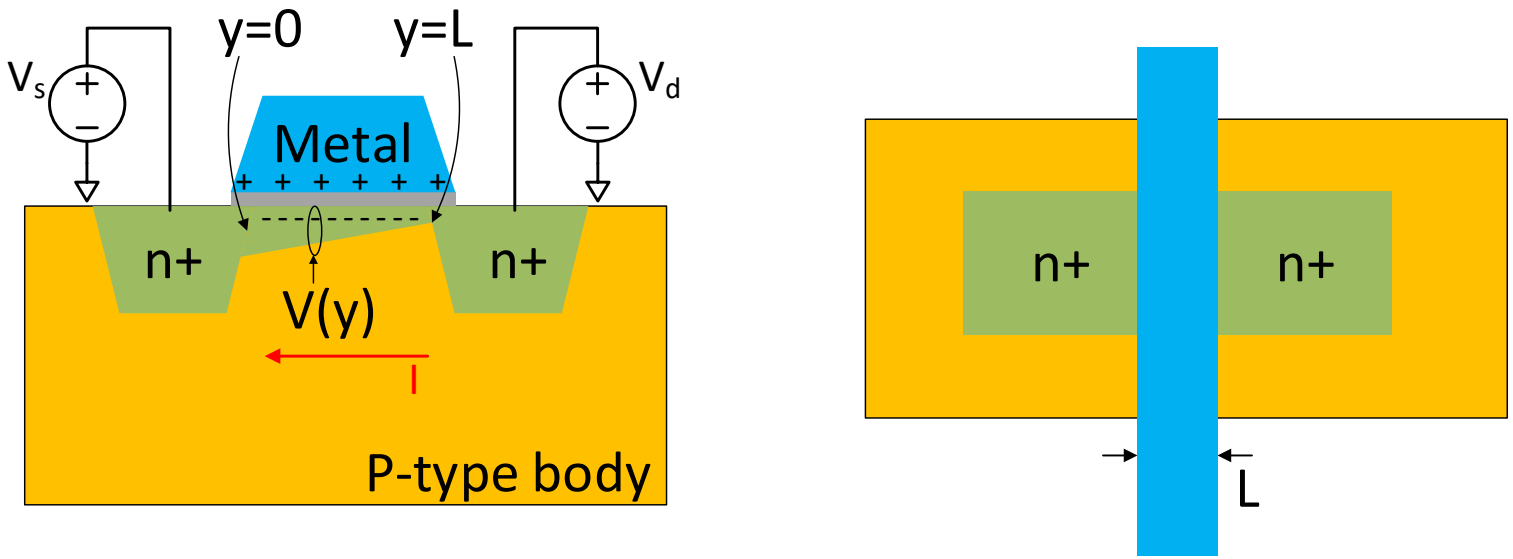


The Ideal Shockley MOSFET model



- Analyze the MOS device in the linear region: V_{gs}-V_{th} = V_{gs}' > V_{ds}
- Recall that channel is fully formed
- Steady-state → Current is the same at any point y along the channel

MOSFET Current Flow

$$I =$$

MOSFET Current Flow

$$I = W$$

MOSFET Current Flow

$$I = W \cdot Q_d$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$
$$= W \cdot C_{ox}$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$
$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right)$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$
$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y) \right) \cdot \mu E_y$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$
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$$= W \cdot C_{ox}\left(V_{gs} - V_{th} - V(y)\right) \cdot \mu \frac{\partial V}{\partial y}$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$
$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y)\right) \cdot \mu E_y$$
$$= W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y)\right) \cdot \mu \frac{\partial V}{\partial y}$$
$$I\, dy = W \cdot C_{ox} \left(V_{gs} - V_{th} - V(y)\right) \cdot \mu\, dV$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$
$$= W \cdot C_{ox}\left(V_{gs} - V_{th} - V(y)\right) \cdot \mu E_y$$
$$= W \cdot C_{ox}\left(V_{gs} - V_{th} - V(y)\right) \cdot \mu \frac{\partial V}{\partial y}$$
$$I\, dy = W \cdot C_{ox}\left(V_{gs} - V_{th} - V(y)\right) \cdot \mu\, dV$$
$$Integrating\ both\ sides\ gives\ \ldots$$
$$\int_0^L I\ dy =$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$
$$= W \cdot C_{ox}\left(V_{gs} - V_{th} - V(y)\right) \cdot \mu E_y$$
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$$\int_0^L I\ dy = \int_0^{V_{ds}} W \cdot C_{ox}\left(V_{gs} - V_{th} - V(y)\right) \cdot \mu\, dV$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$
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$$\int_0^L I\ dy = \int_0^{V_{ds}} W \cdot C_{ox}\left(V_{gs} - V_{th} - V(y)\right) \cdot \mu\, dV$$
$$IL = \mu C_{ox} W\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

MOSFET Current Flow

$$I = W \cdot Q_d \cdot v$$
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$$I = \mu C_{ox}\frac{W}{L}\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

MOSFET Current Flow

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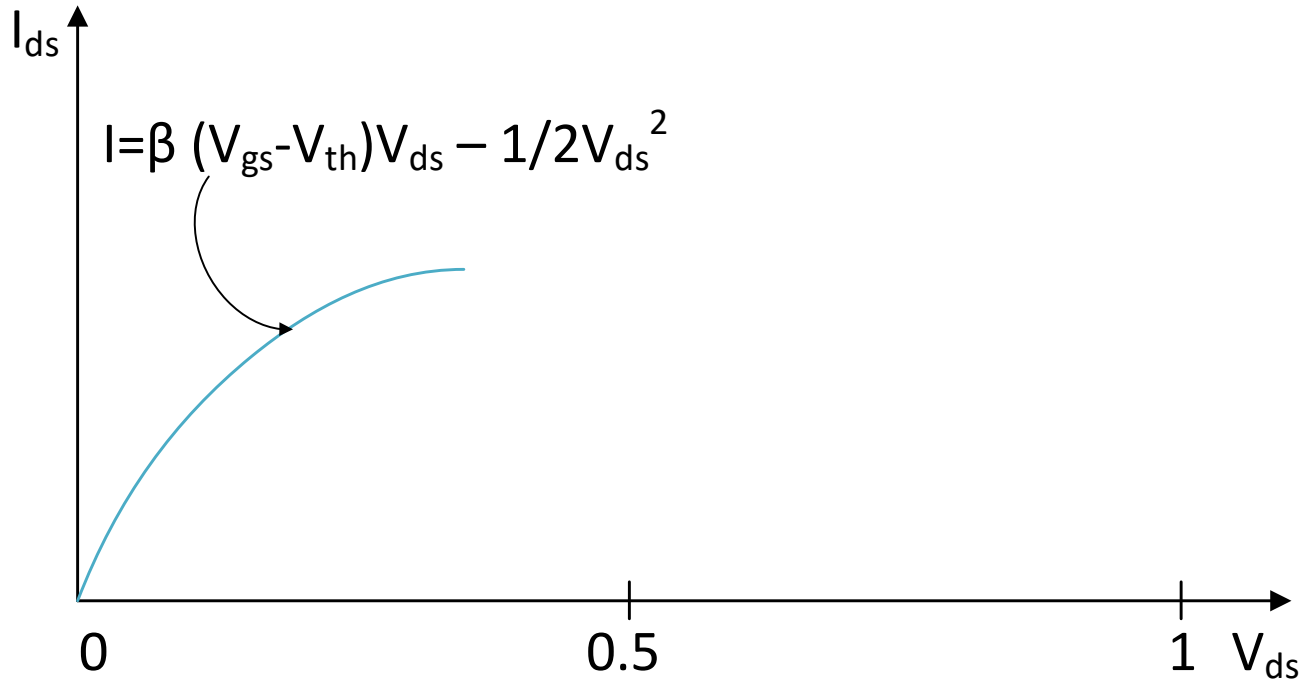
$$I = \mu C_{ox}\frac{W}{L}\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right], \qquad Letting\ \beta = \mu C_{ox}\frac{W}{L}$$
$$I = \beta\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

MOSFET Operation: Triode region

- Equation corresponds to device in Linear (or Triode) region
  - Channel is continuous from source to drain
- Question: Plot I_{ds} vs. V_{ds} for a fixed V_{gs}



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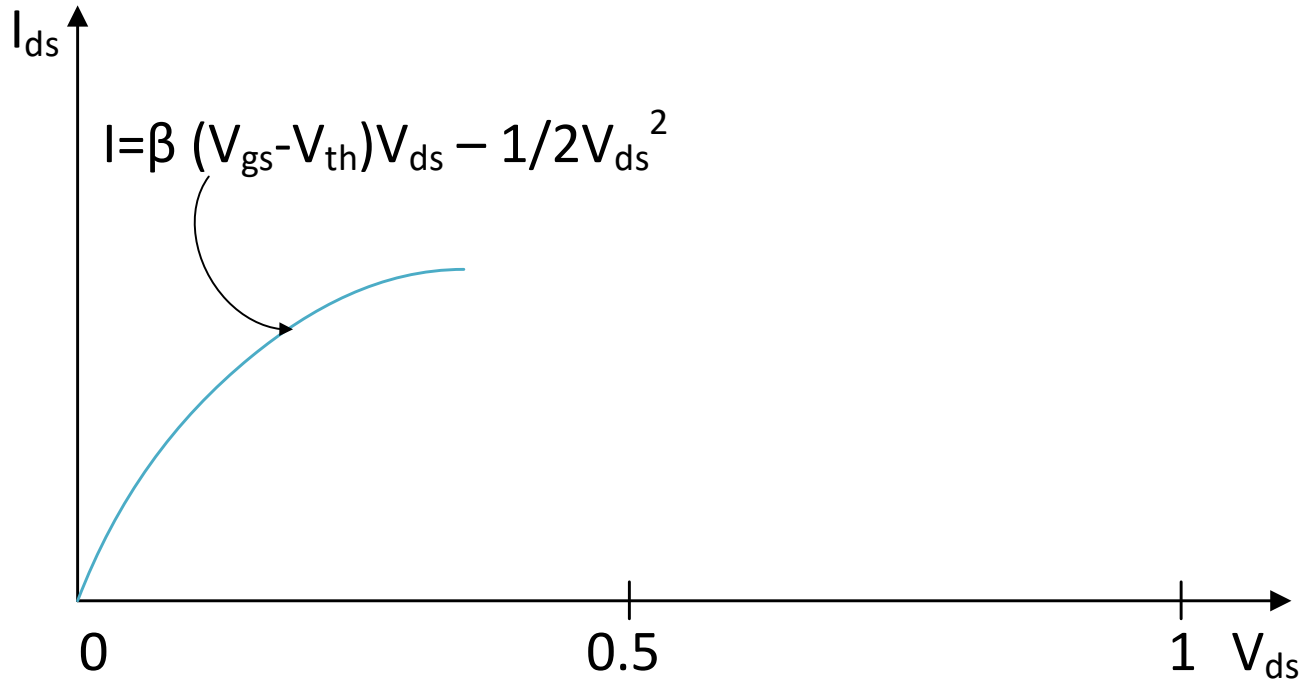
- What happens for $V_{ds}>V_{gs}- V_{th}$?



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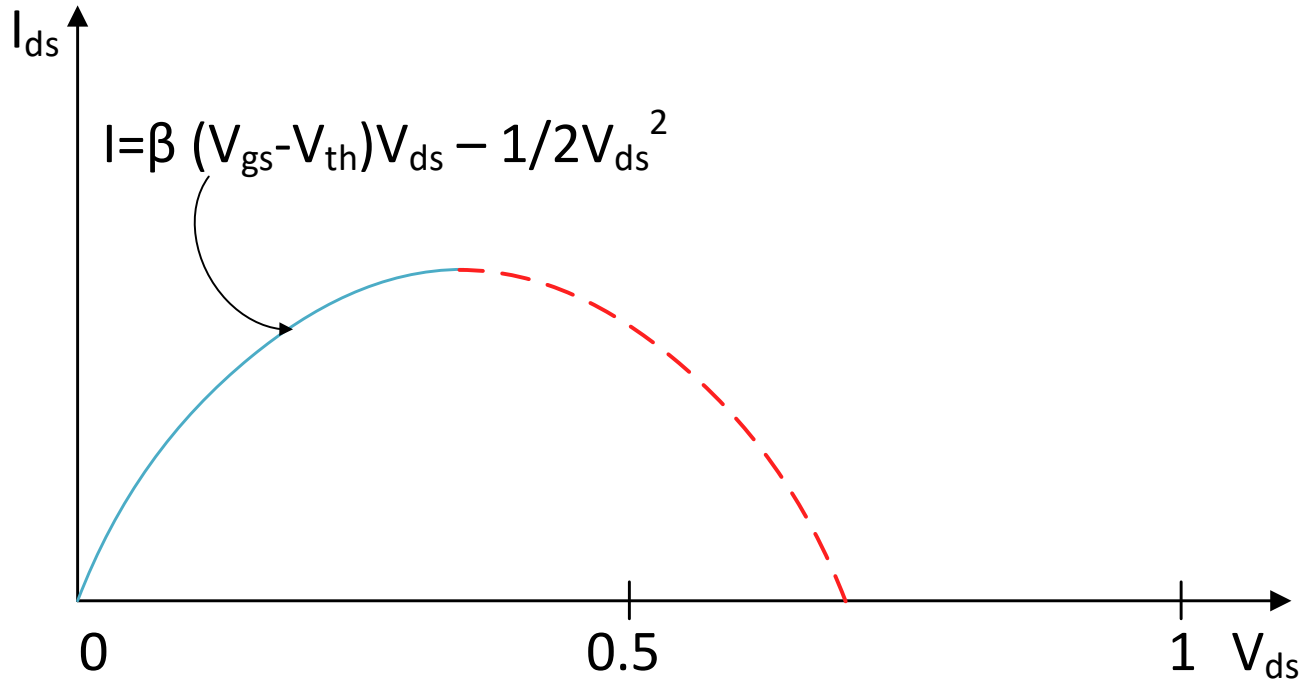

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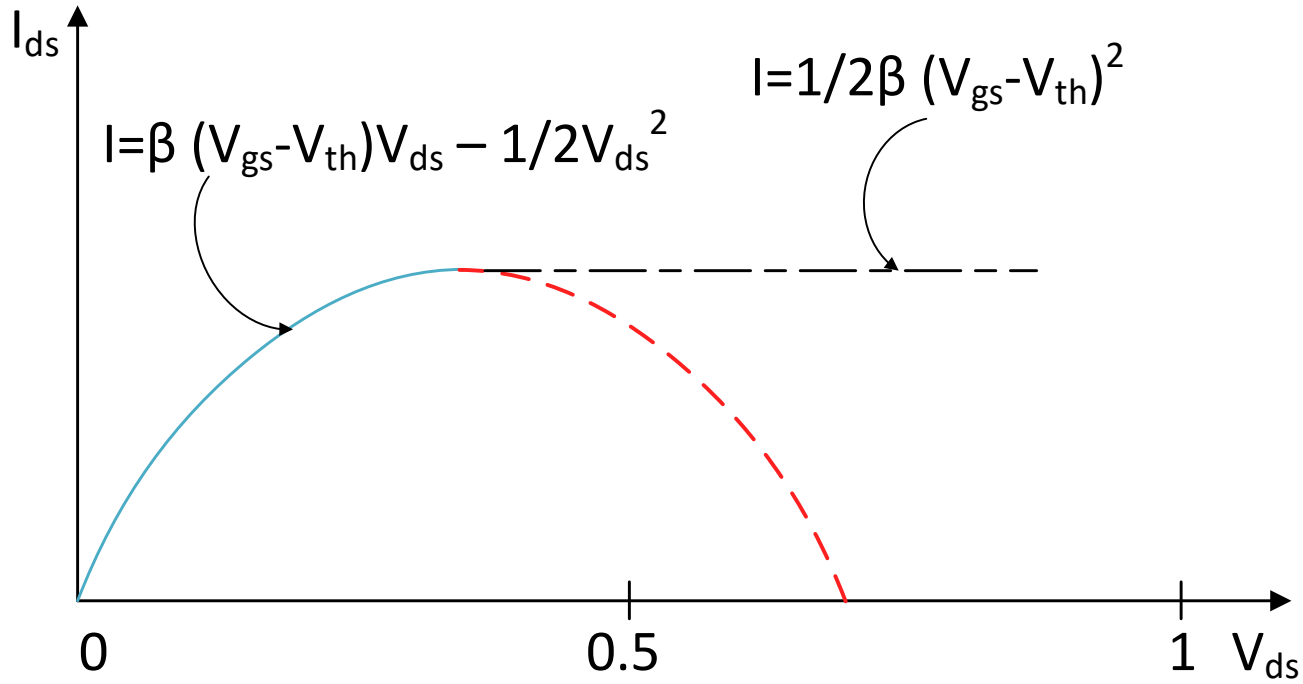
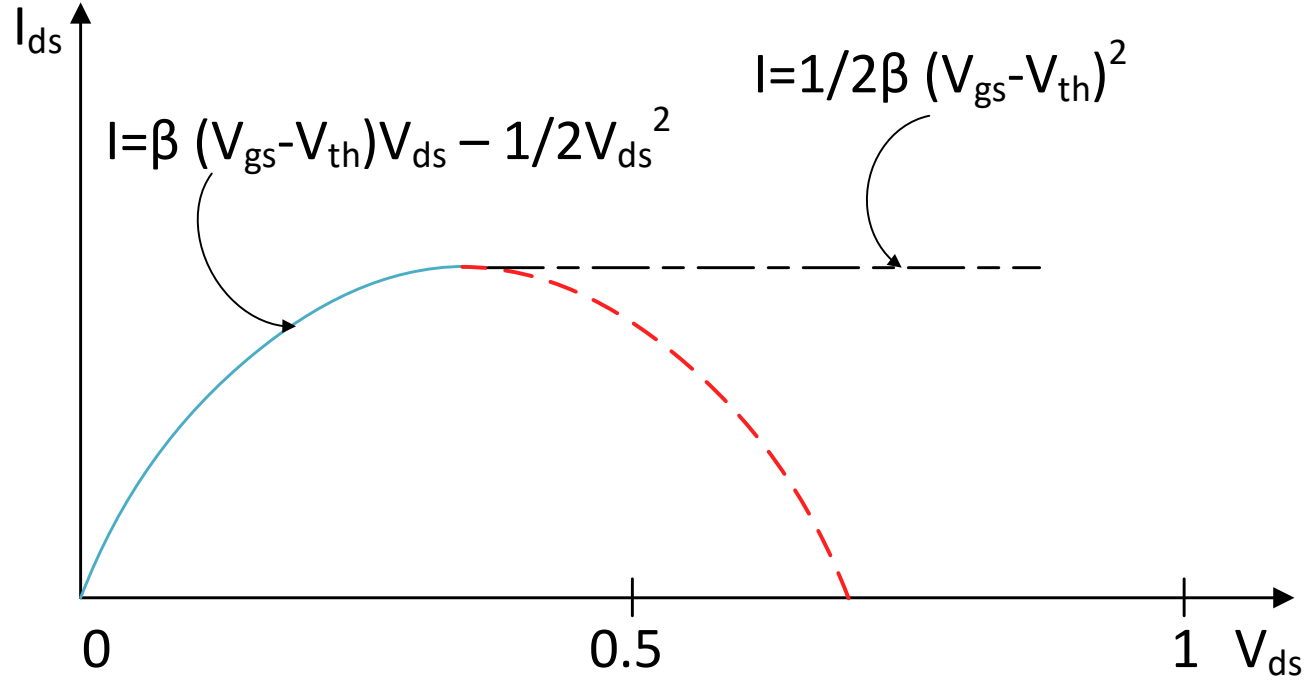
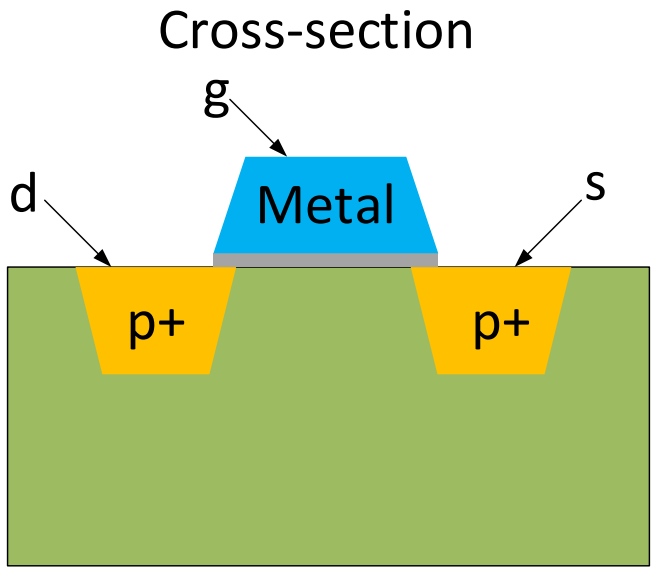


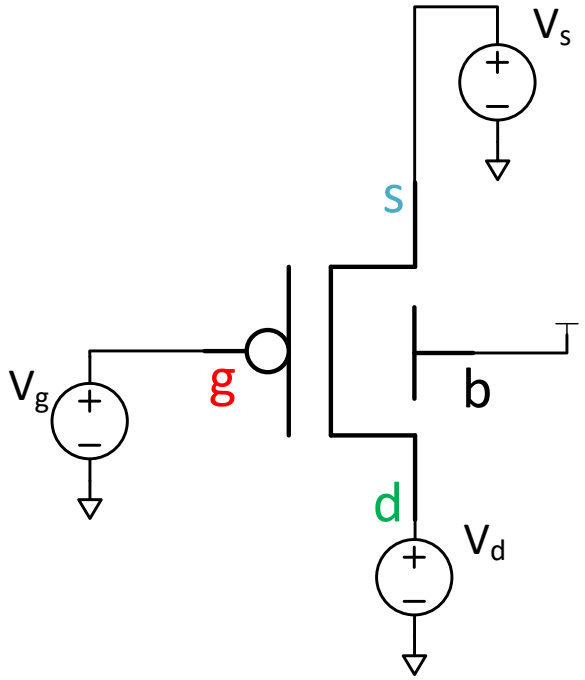
MOSFET Operation: Triode region

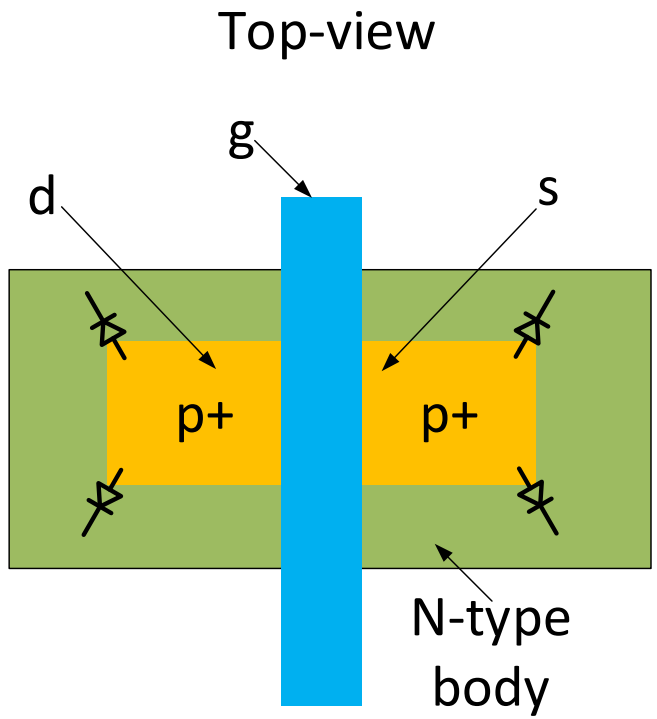
- Equation corresponds to device in Linear (or Triode) region
  - Channel is continuous from source to drain
- Question: Plot I_{ds} vs. V_{ds} for a fixed V_{gs}
- What happens for $V_{ds}>V_{gs}-V_{th}$?
  - Device enters saturation
  - The channel “pinches-off” (More on this shortly)



Break-out session: Figure out the PMOS…



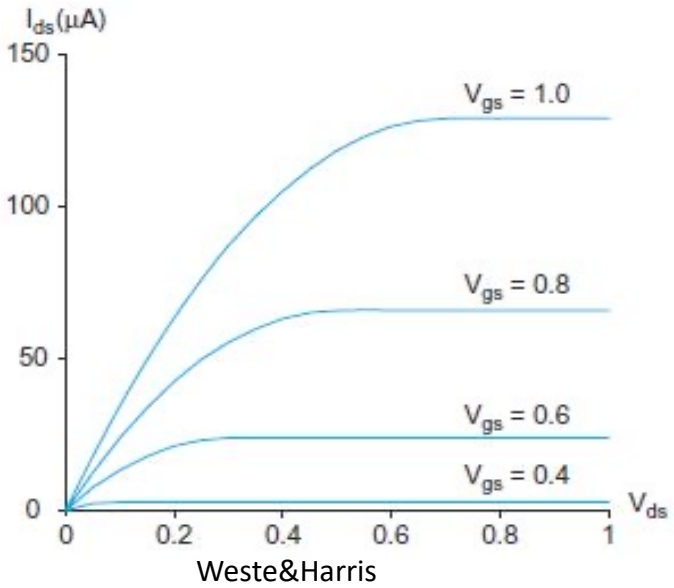




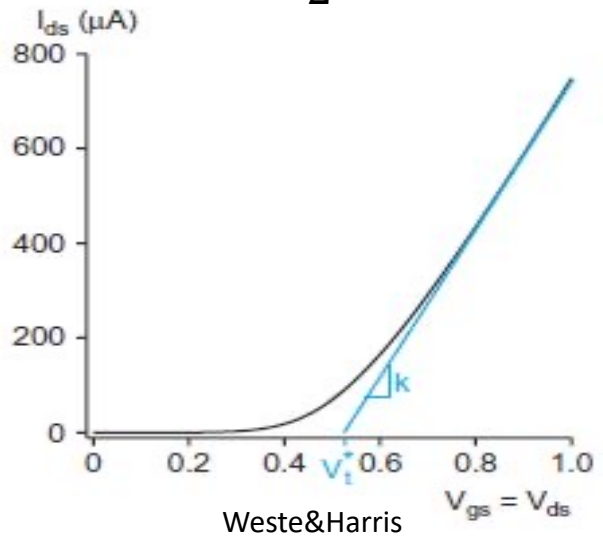
MOSFET Operation: Saturation

- Saturation condition: $V_{gs} - V_{th} \leq V_{ds}$
  - $V_{gs} - V_{th}$ (also denoted as V_{gs}') , the gate overdrive is less than the on-voltage
- Current "levels-off"
  - I_d no longer a function of V_{ds} (to the first order. More on this later)
  - Depends only on V_{gs} and V_{th}

$$I_{ds} = \frac{1}{2}\beta(V_{gs} - V_{th})^2 \;\; if \;\; 0 < V_{gs} - V_{th} < V_{ds}$$



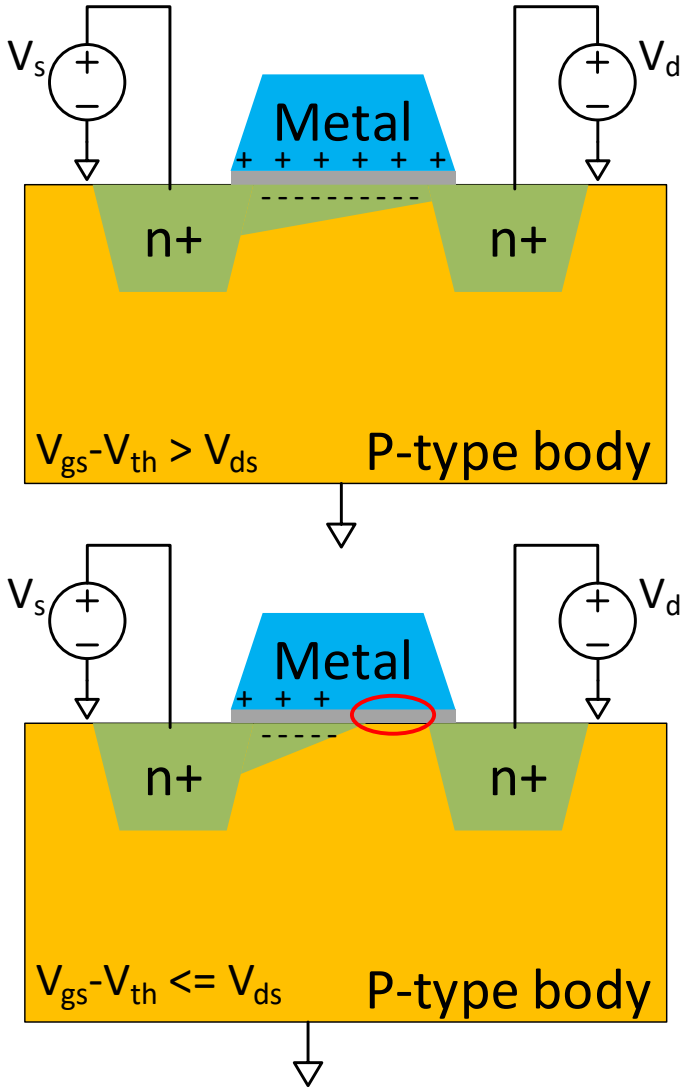
Weste&Harris



Weste&Harris

ELECTRICAL & COMPUTER ENGINEERING

Channel Length Modulation



- In reality, I_{ds} is not constant as V_{ds} increases
- Depletion region forms beyond a “pinch-off” region

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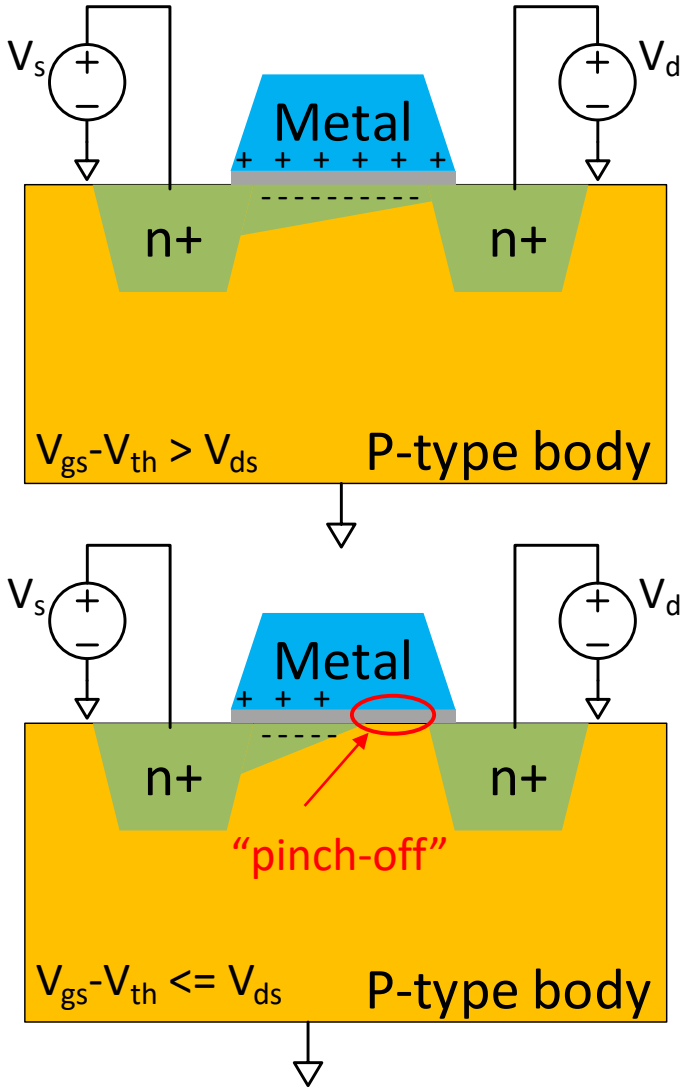

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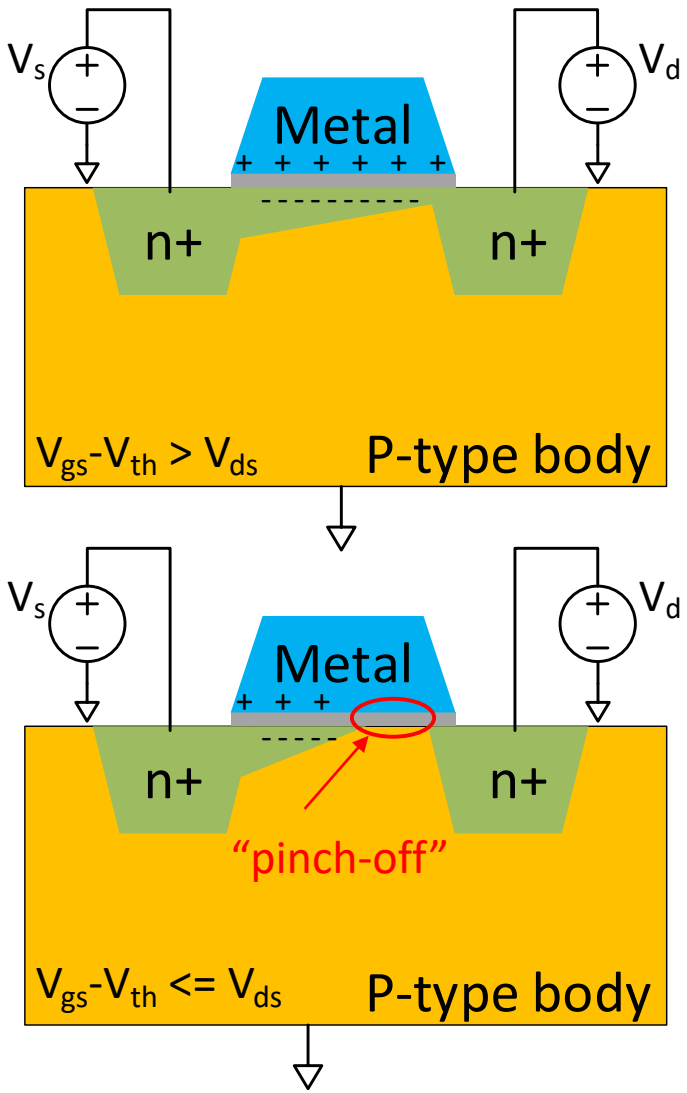

But if there is no channel, how do e^- get over to the drain?

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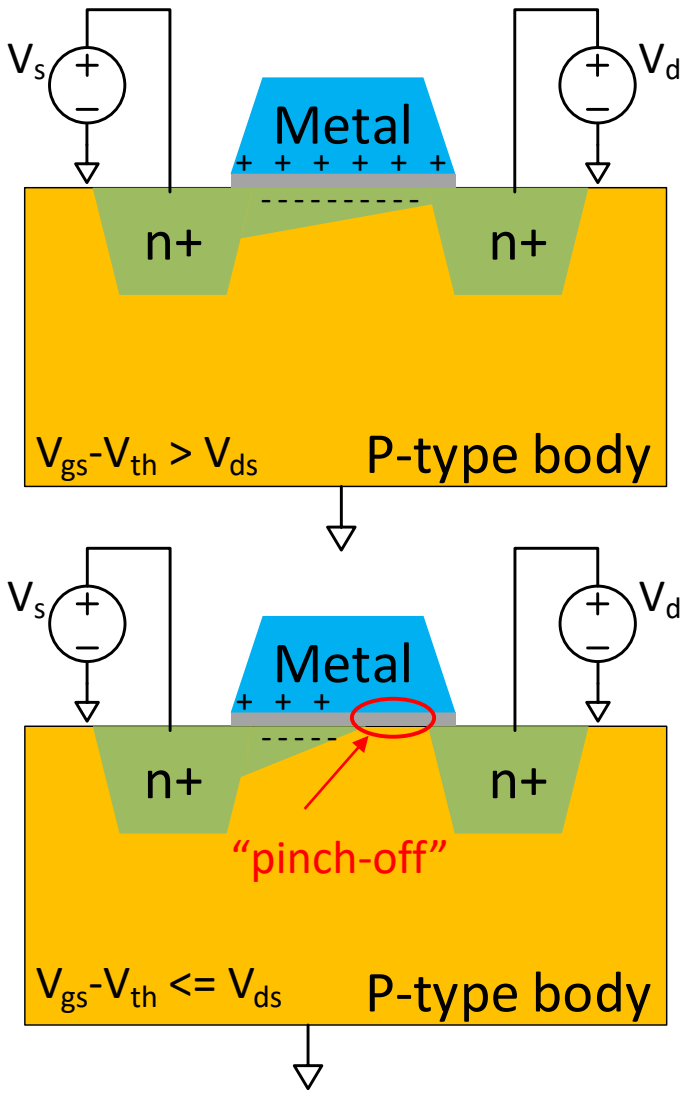

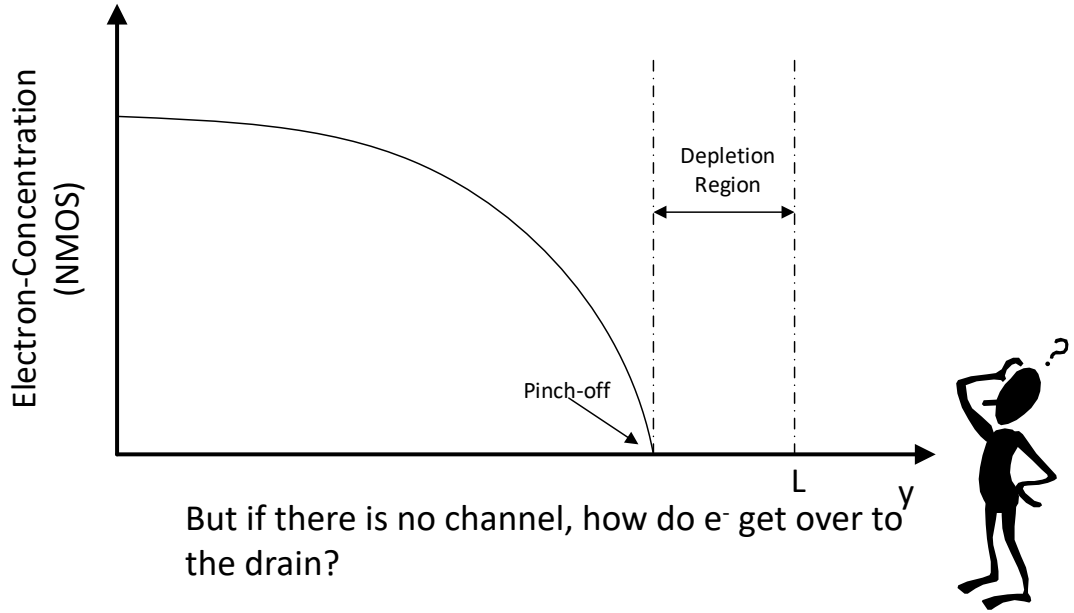

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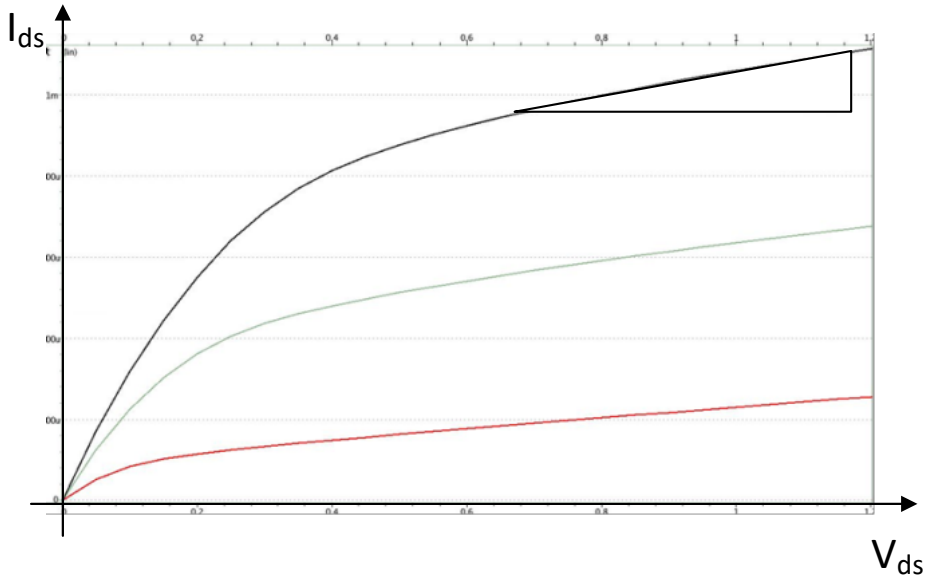
Channel Length Modulation

- Simplifying assumption:
  - Fractional change in channel length is proportional to V_{DS}
  - If ΔL is the depletion width, Let $\frac{\Delta L}{L} = \lambda V_{ds}$



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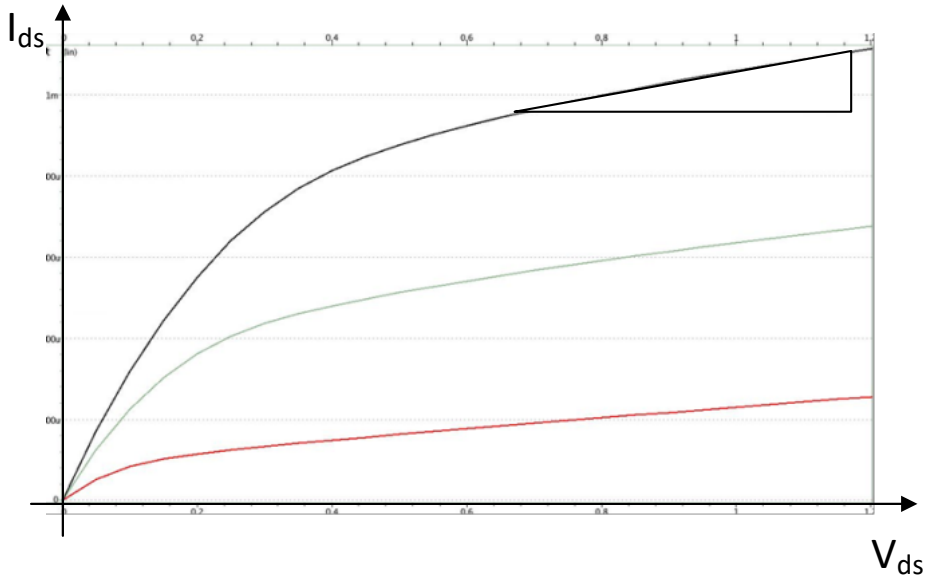

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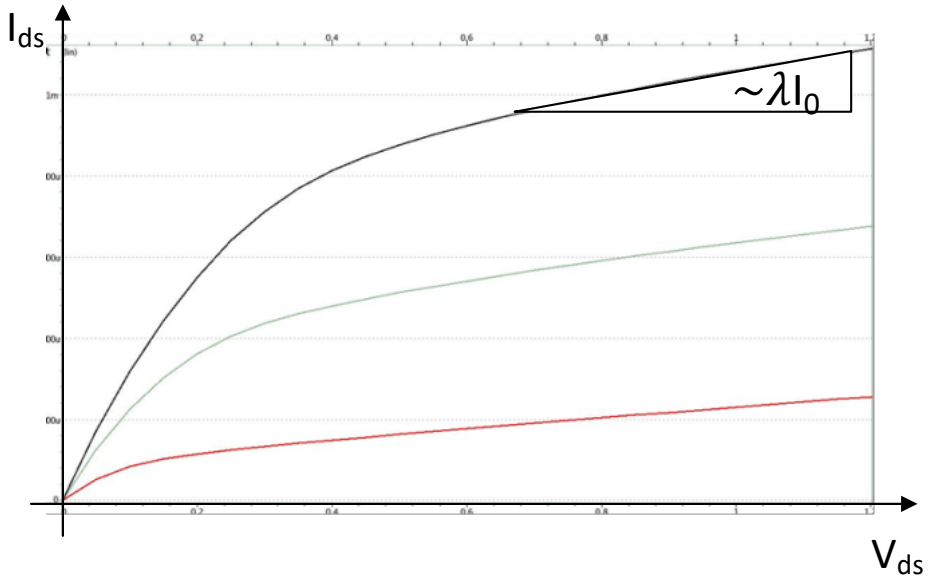

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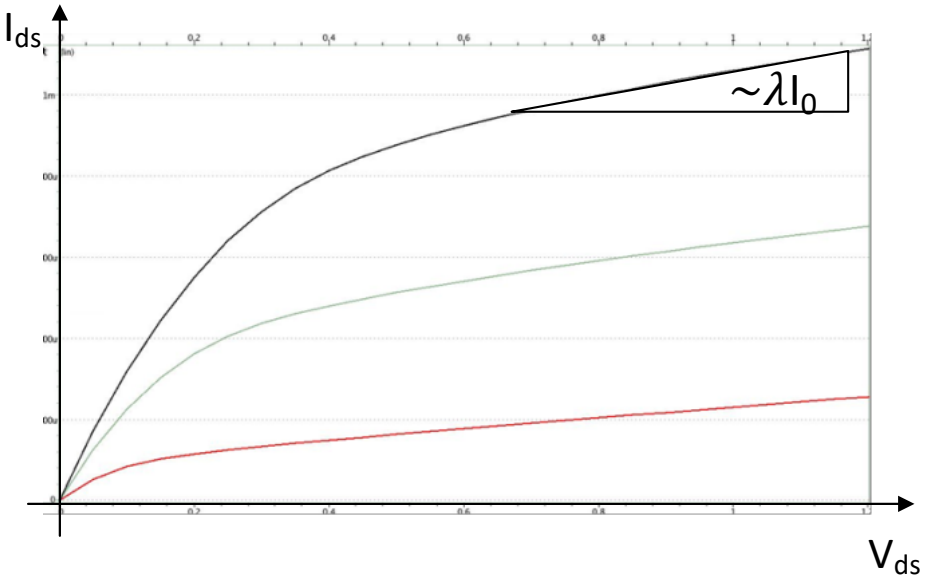

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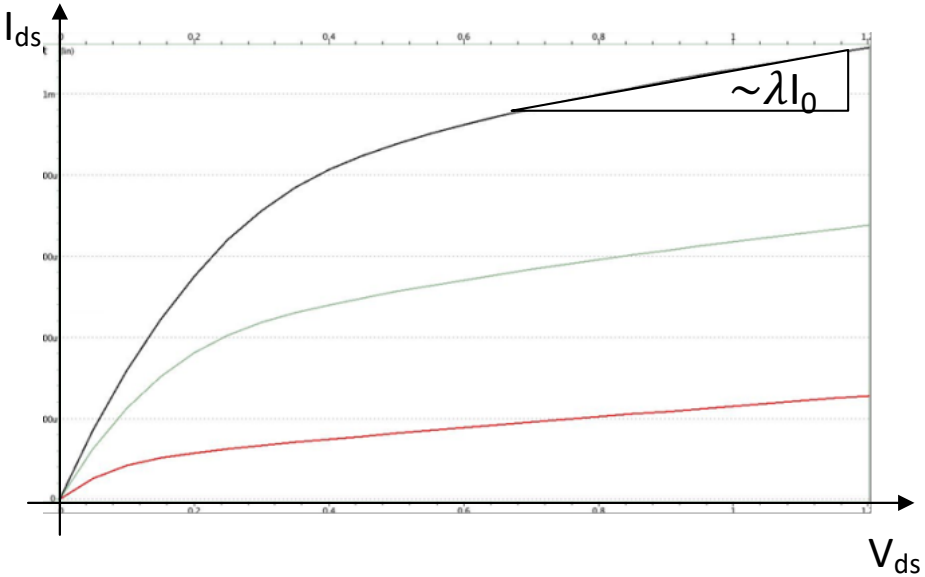

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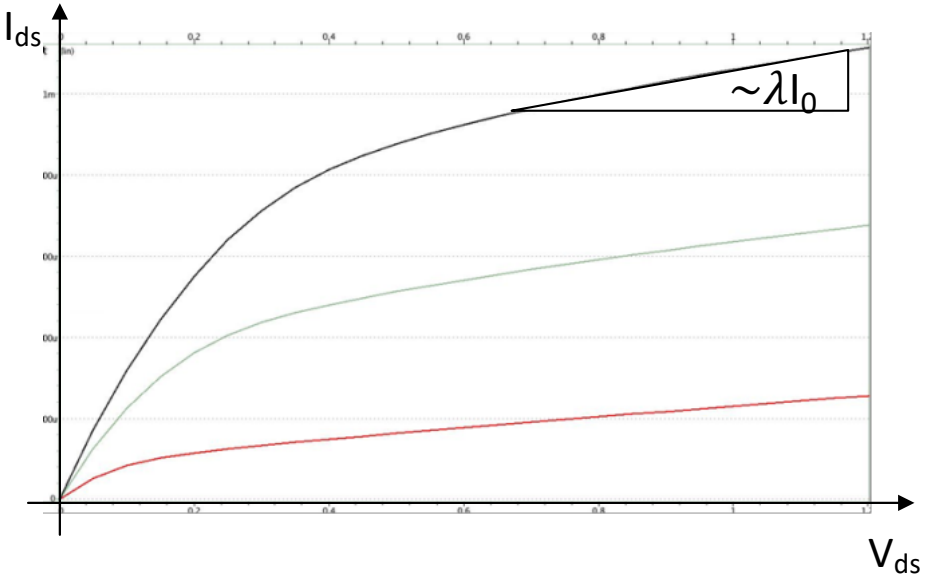

PMOS Operation

- Essentially a dual of the NMOS device operation
- For conduction: Vg – Vs < -Vth → Vs – Vg > Vth → Vsg > Vth
  - Gate overdrive continues to have to exceed Vth
- A lot more convenient to work with Vsg, Vsd and always work with positive Vth values (convention adopted in this class)

- Exercise: Derive the current equation of the PMOS device
- Note: PMOS carrier μ_p is lower than NMOS μ_n → ↓ current drive for the same gate overdrive.

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How can I fix that if I want equal drive strength?

MOSFET Gate Capacitance

- Zeroth order, Cap = W*L*C_{ox}
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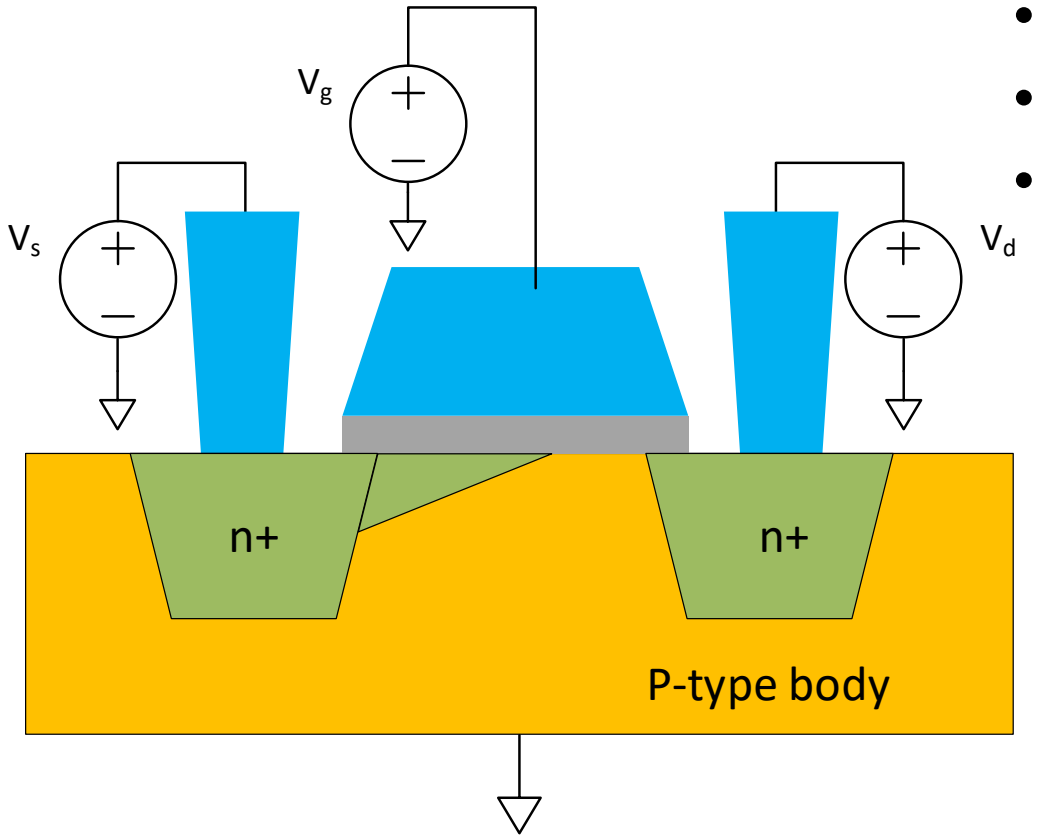

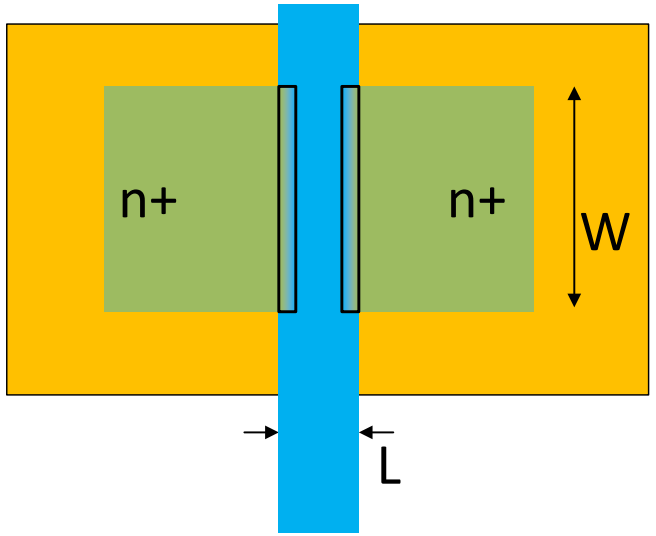

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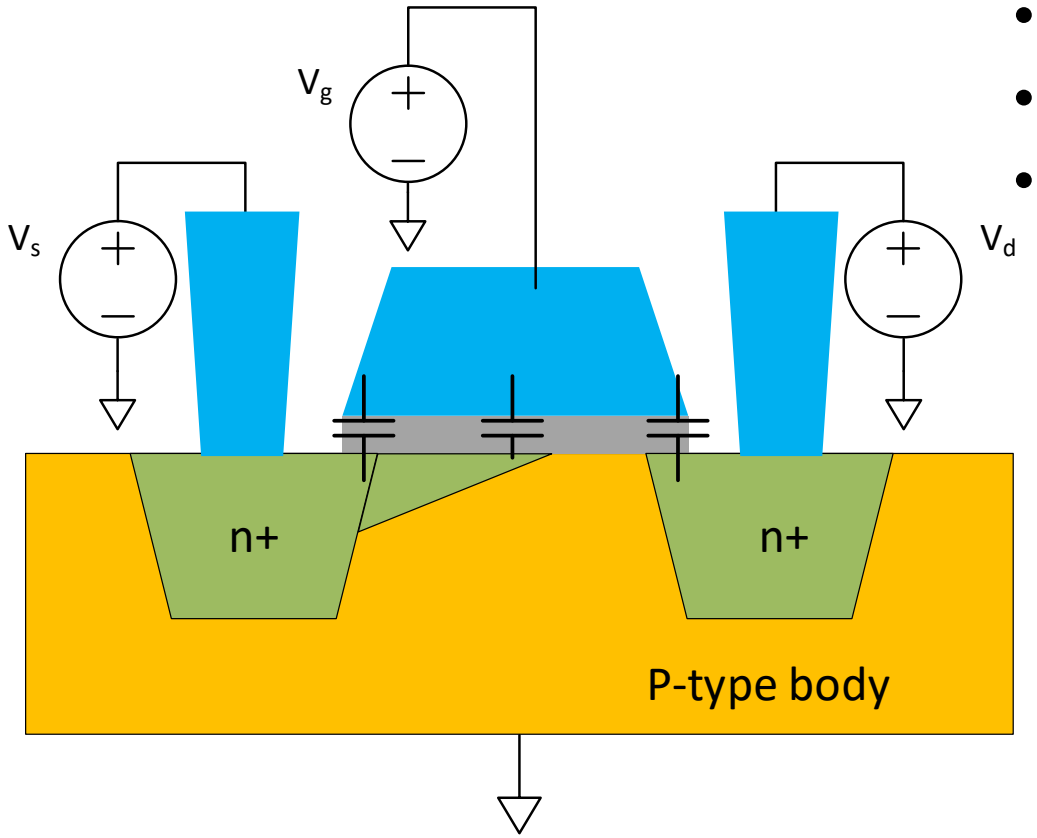

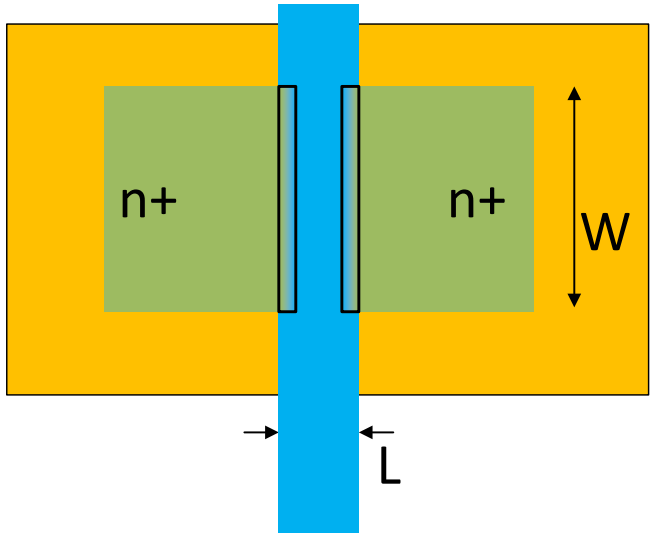

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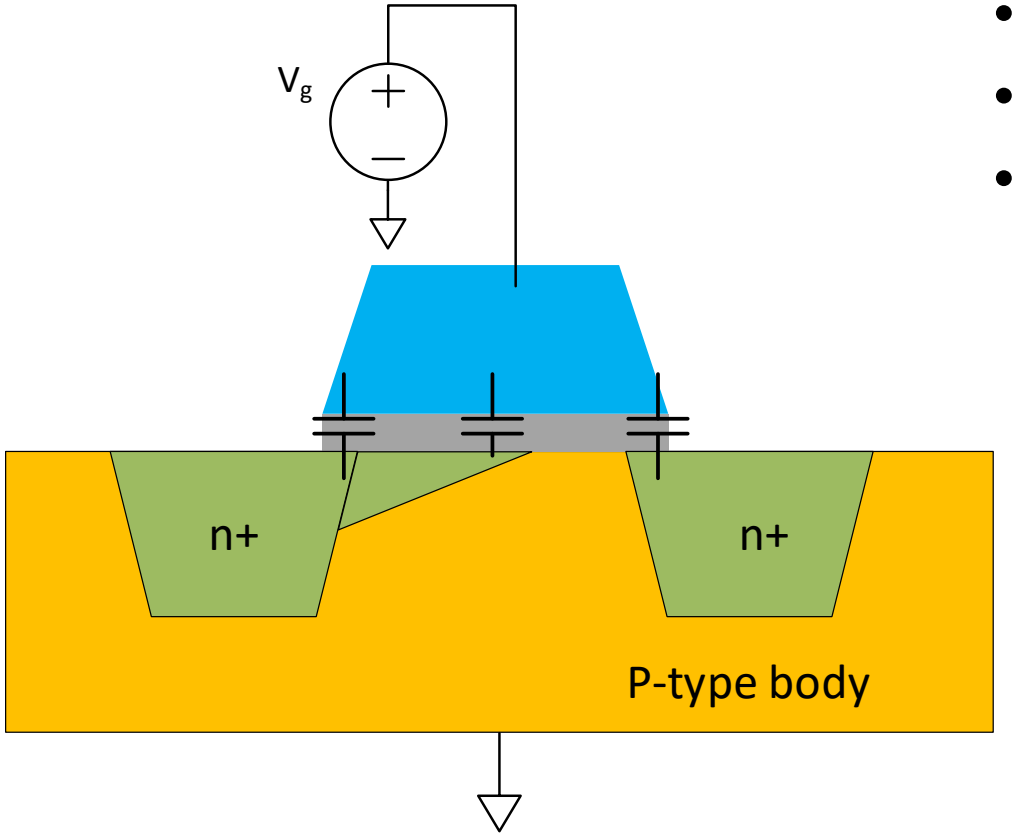

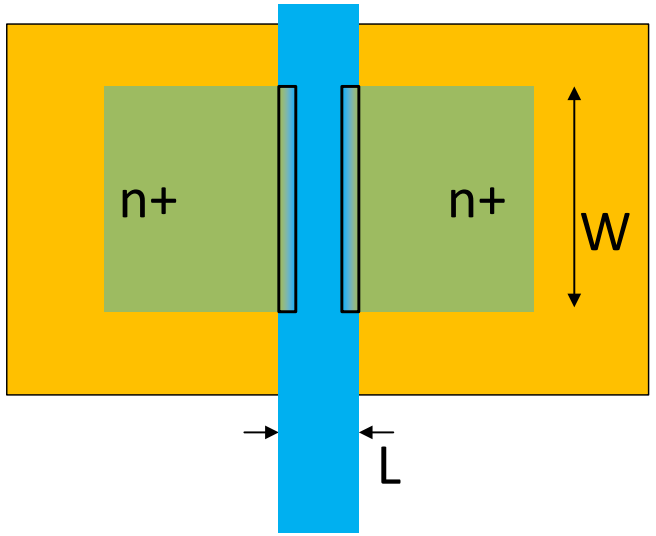

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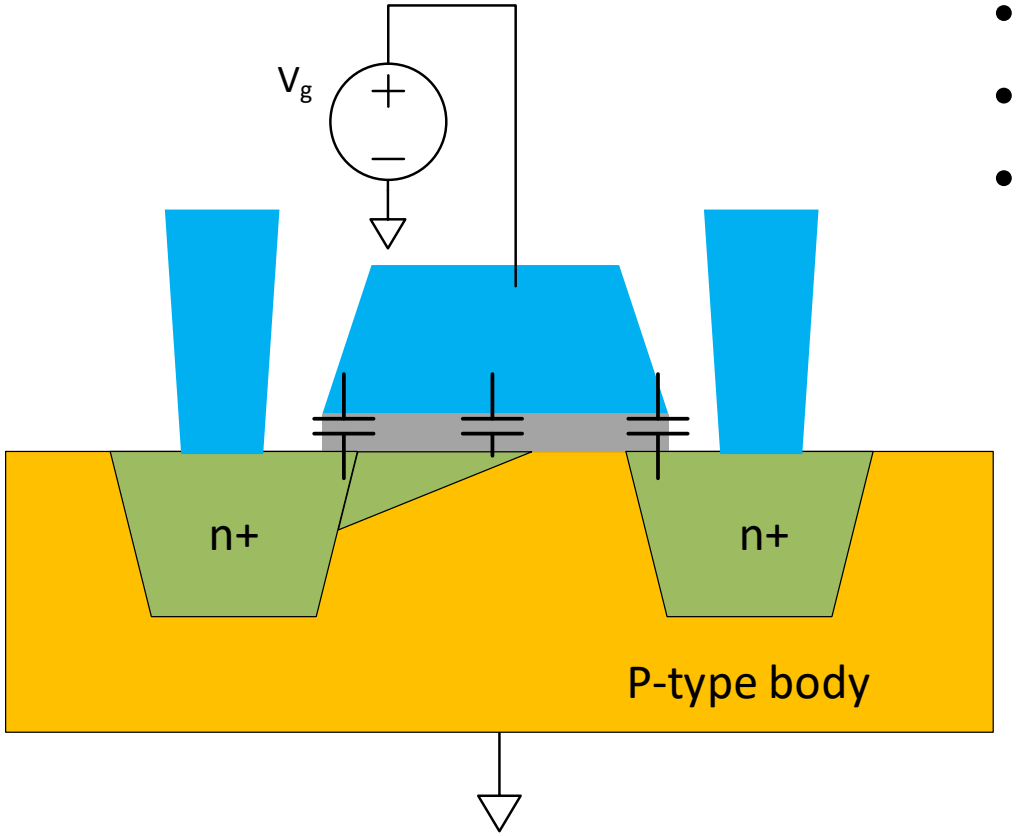

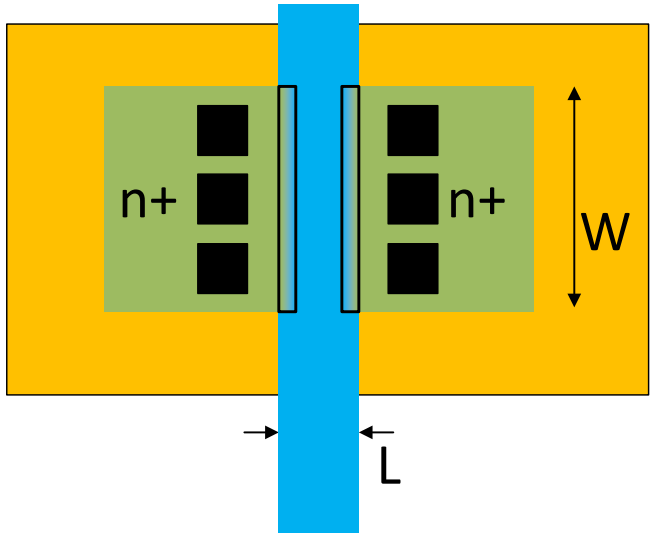

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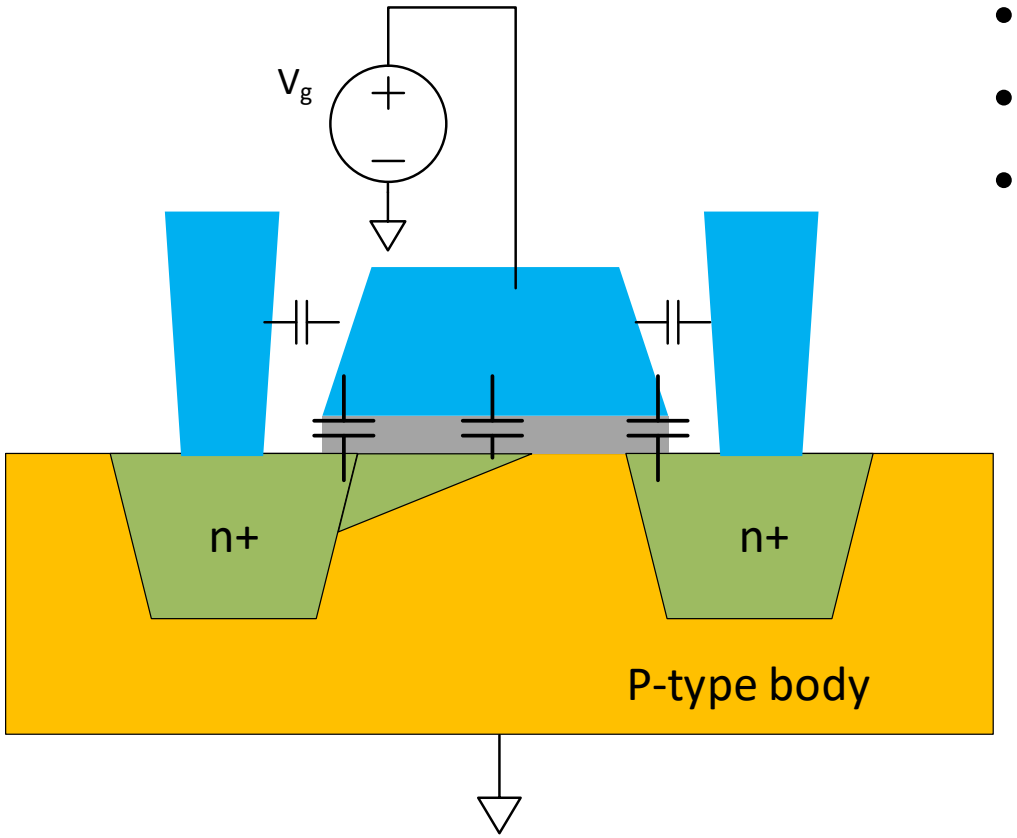

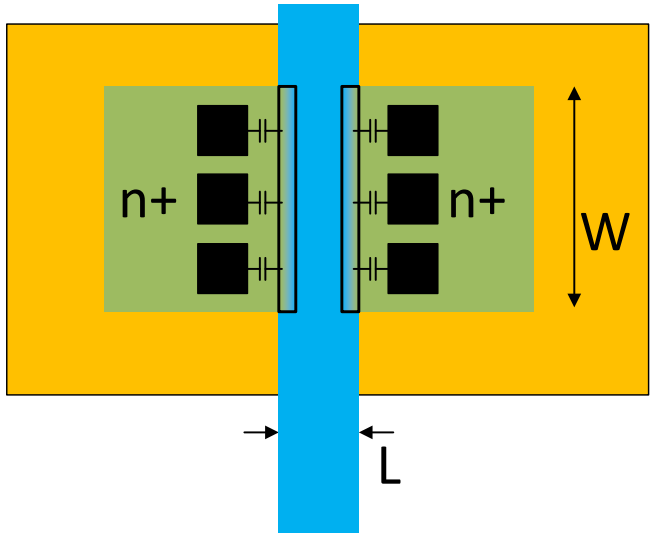

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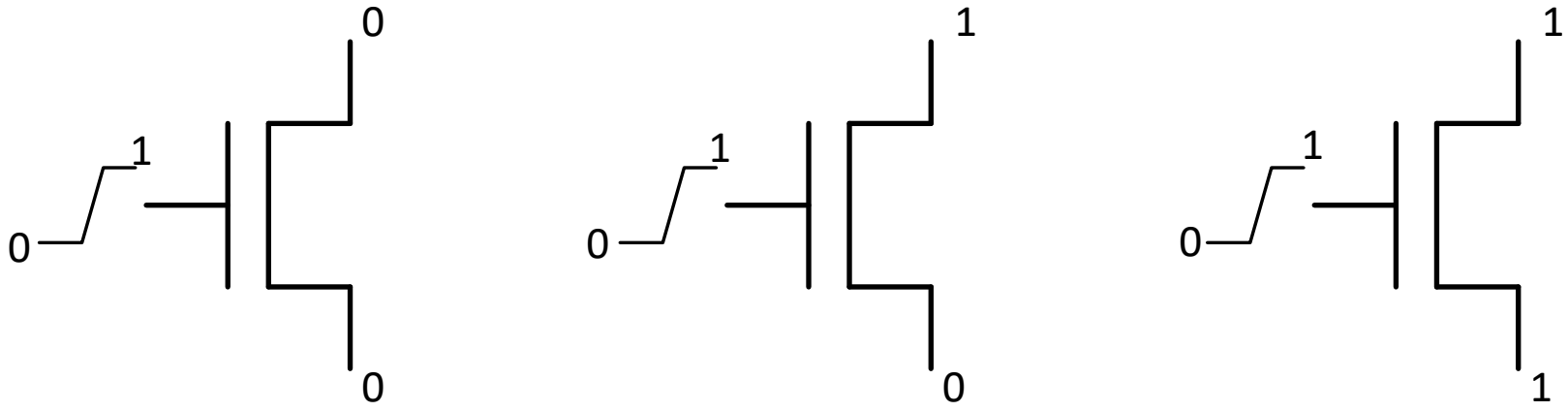

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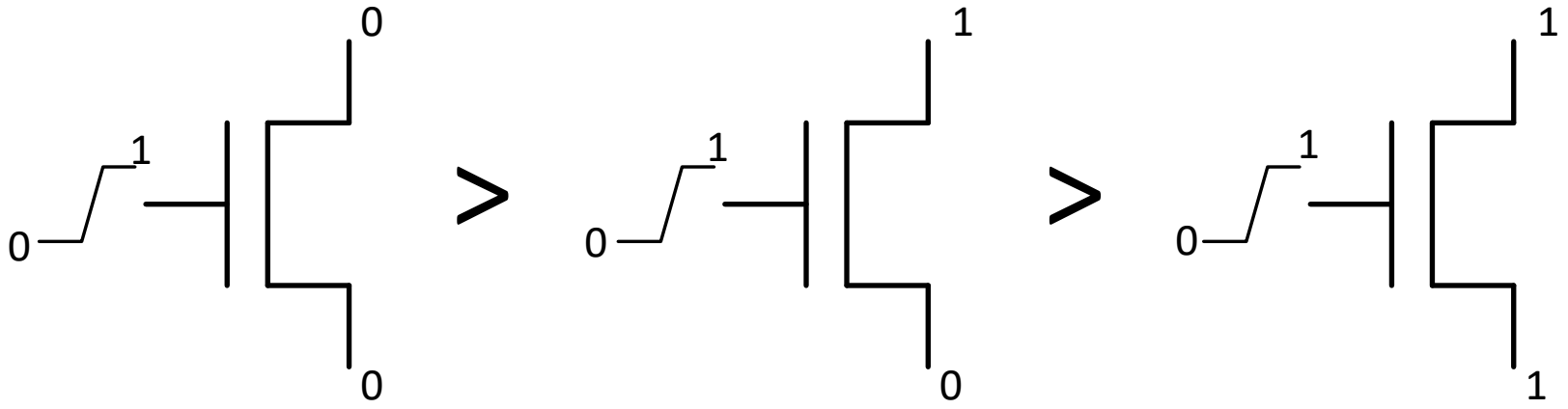

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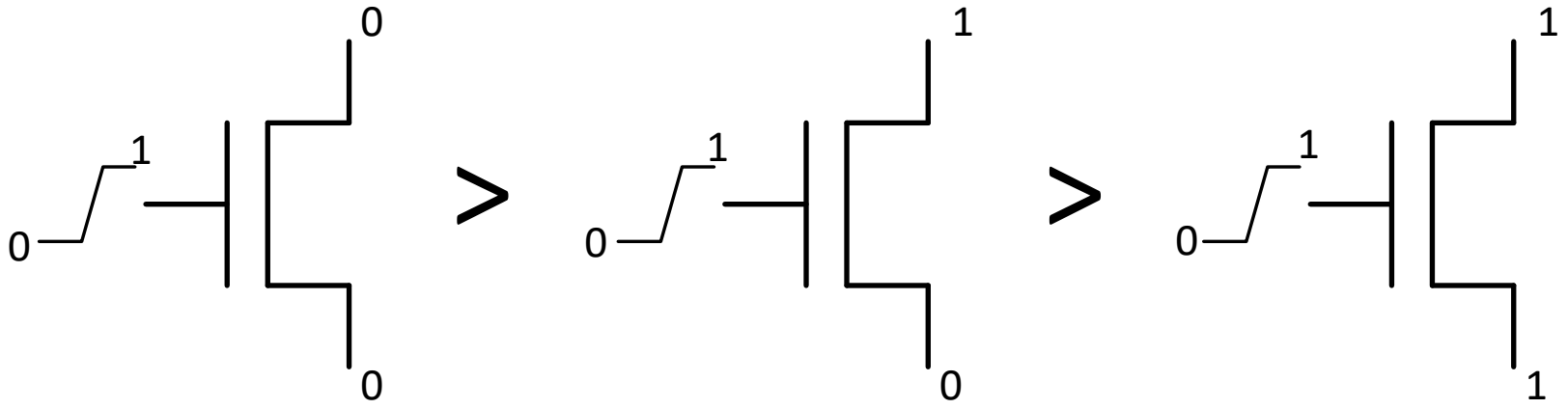

Optional assignment: Why do I not see the accumulation cap in the 11 case?

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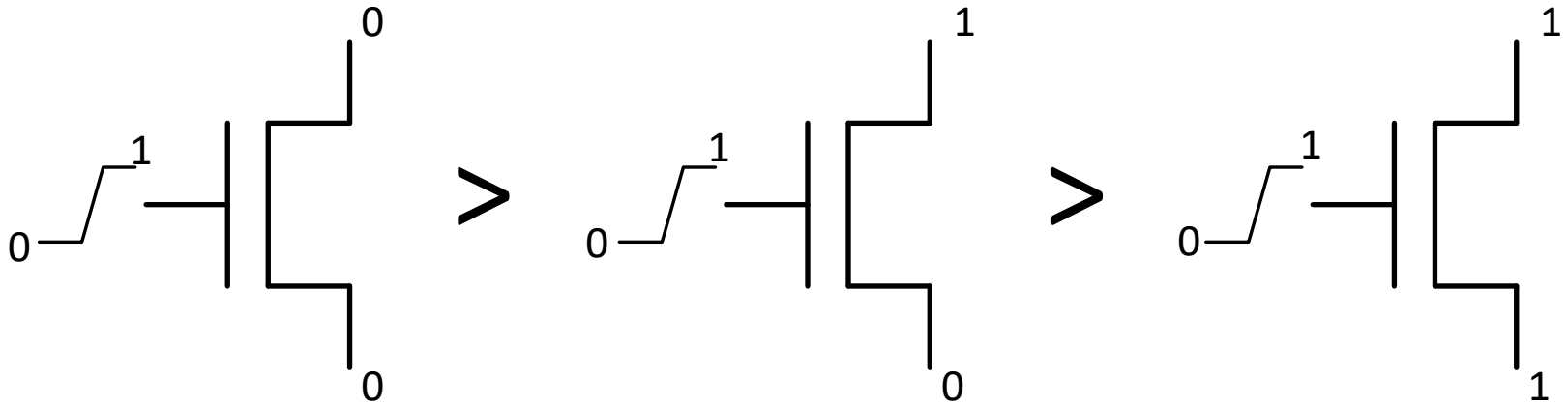

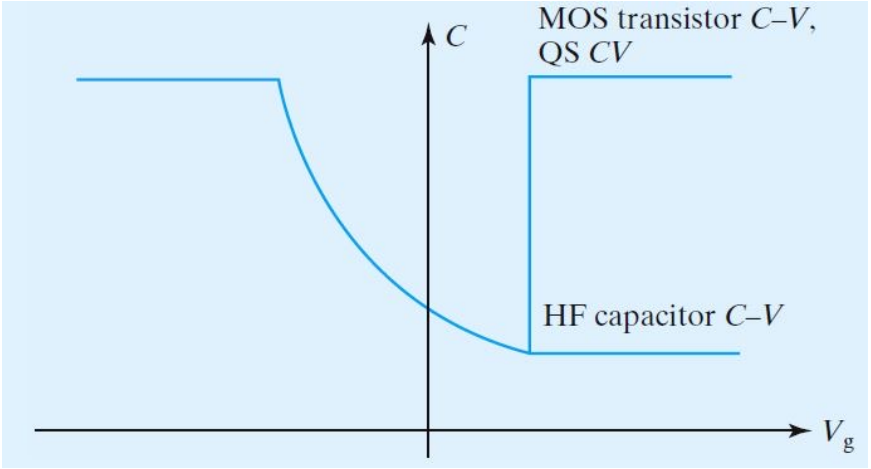

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Junction Capacitance

- Capacitance of the depletion region
  - Area, Perimeter terms
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- Junction capacitance is significant and needs to be controlled
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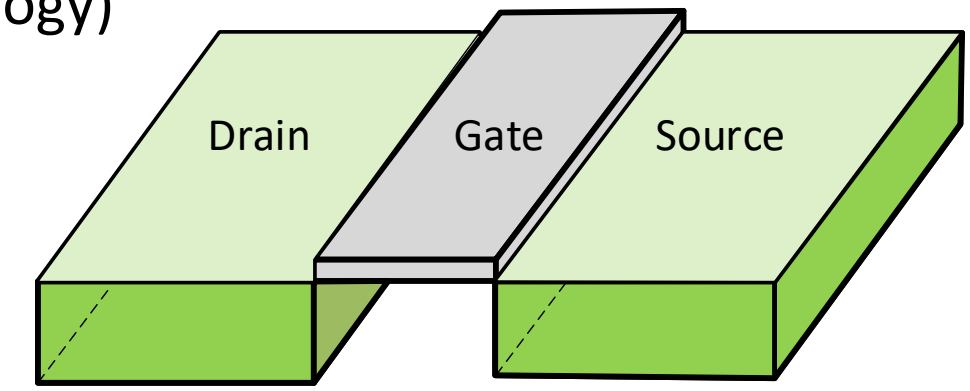

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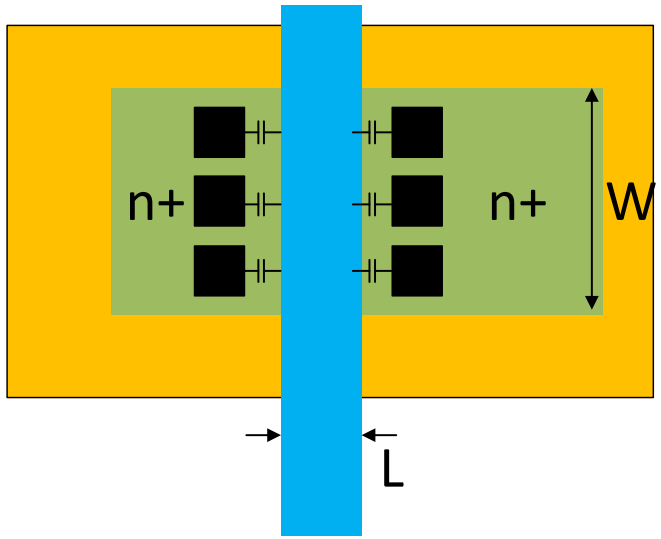

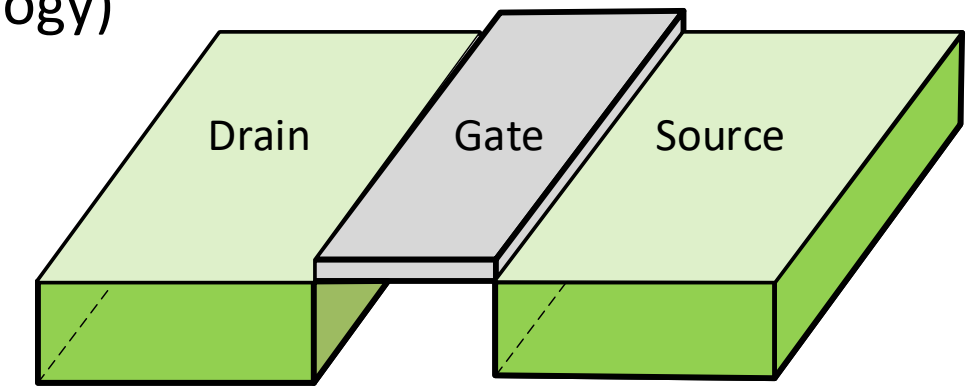

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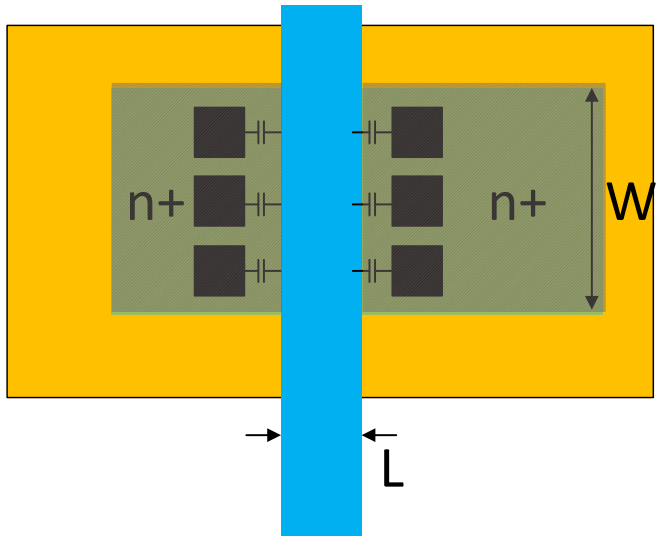

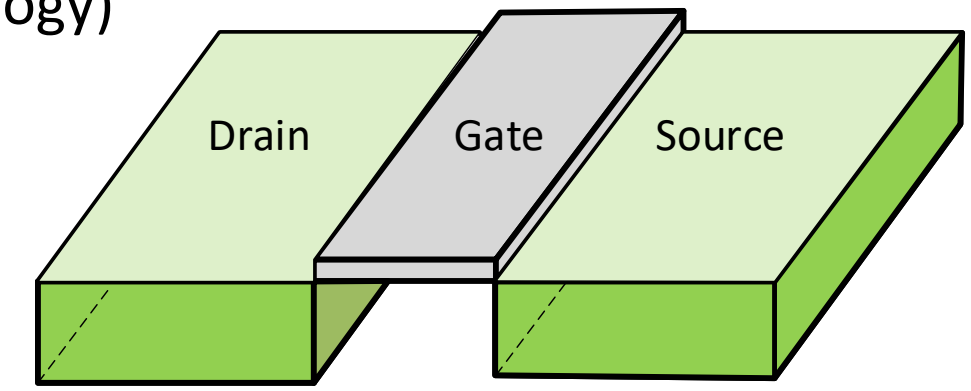

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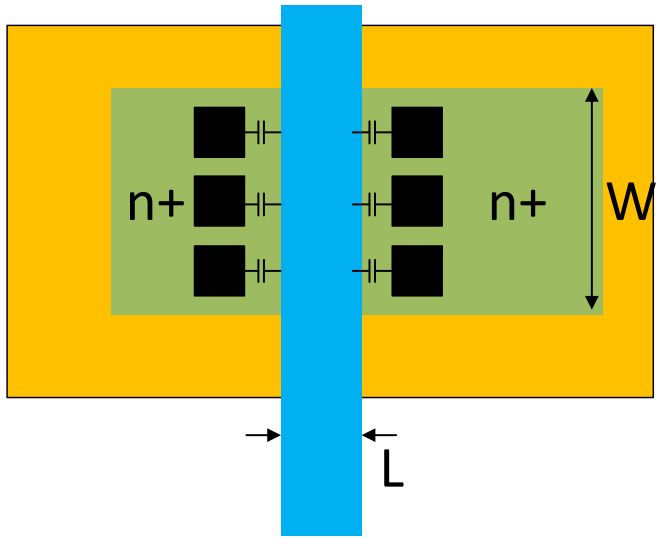

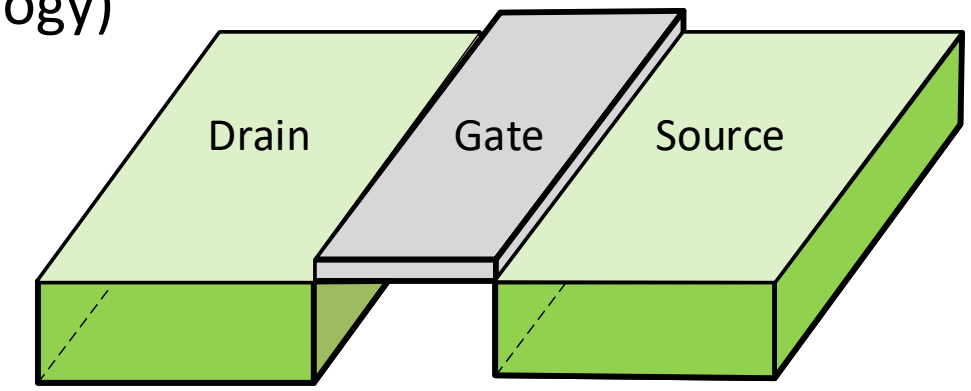

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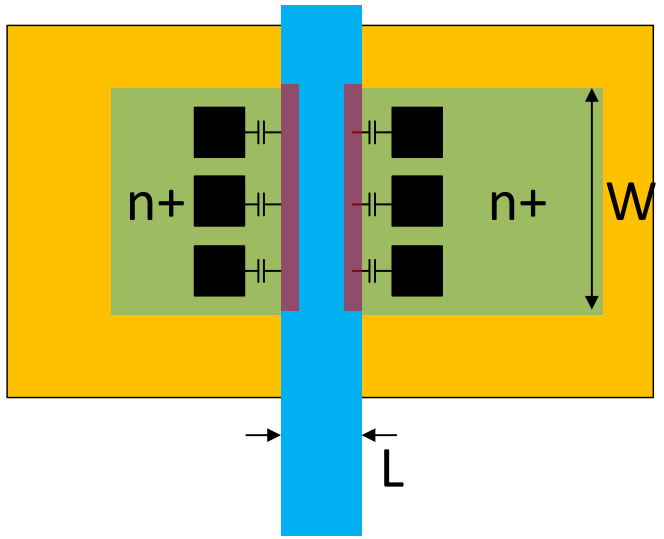

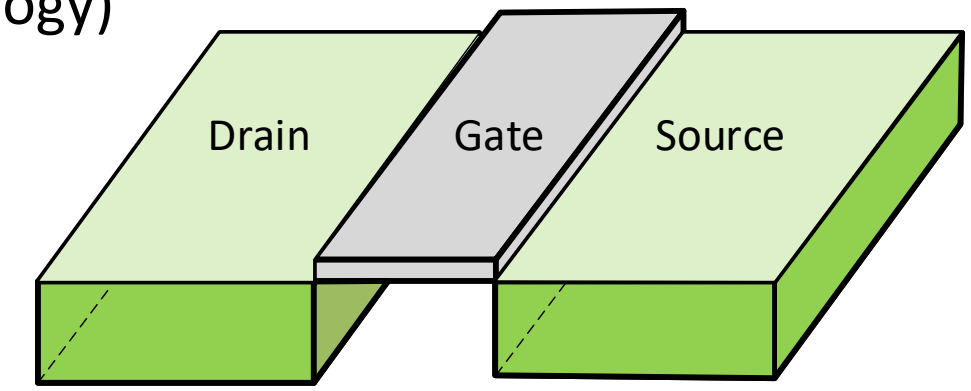

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- Capacitance of the depletion region
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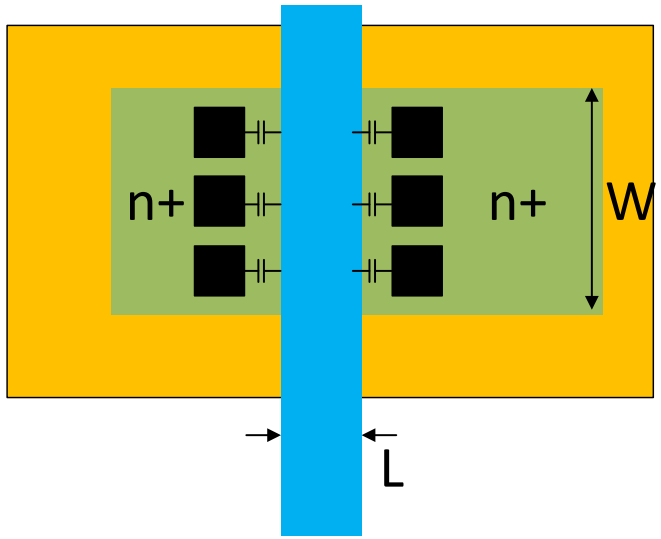

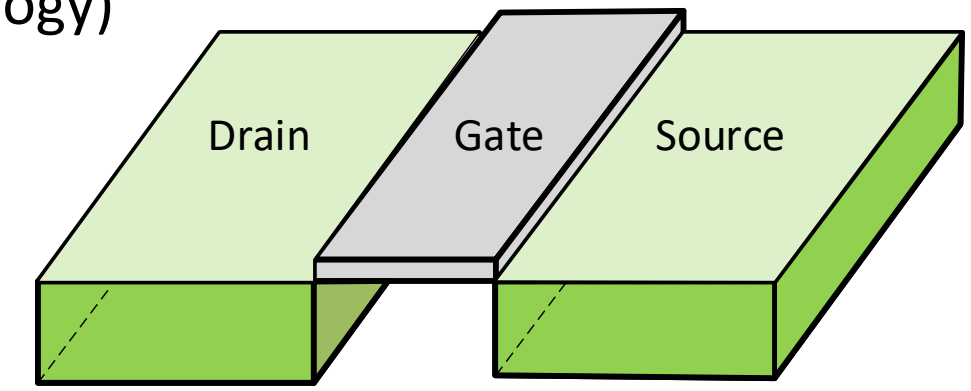

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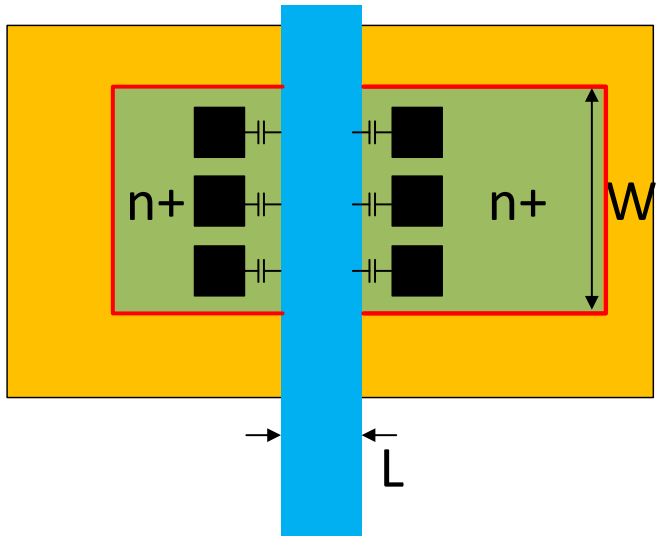

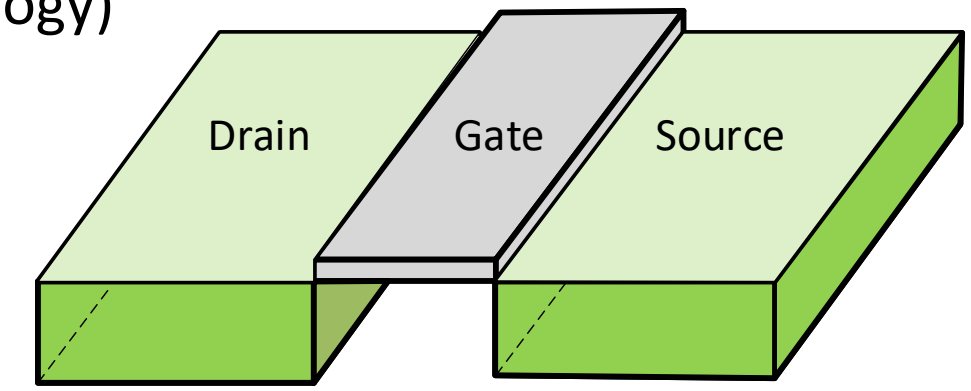

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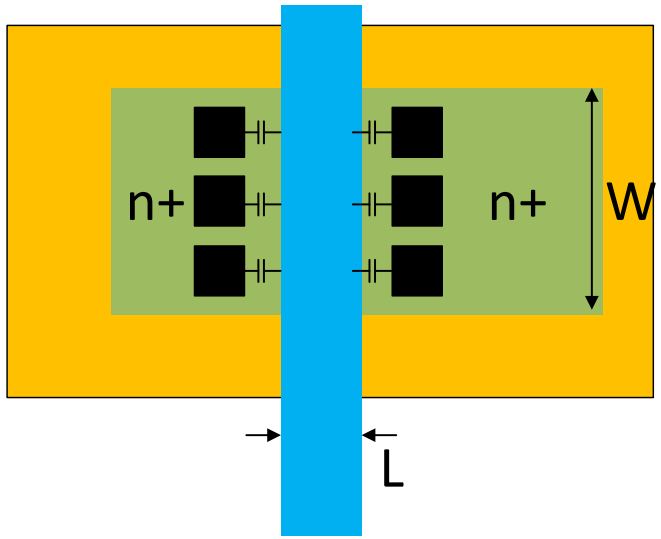

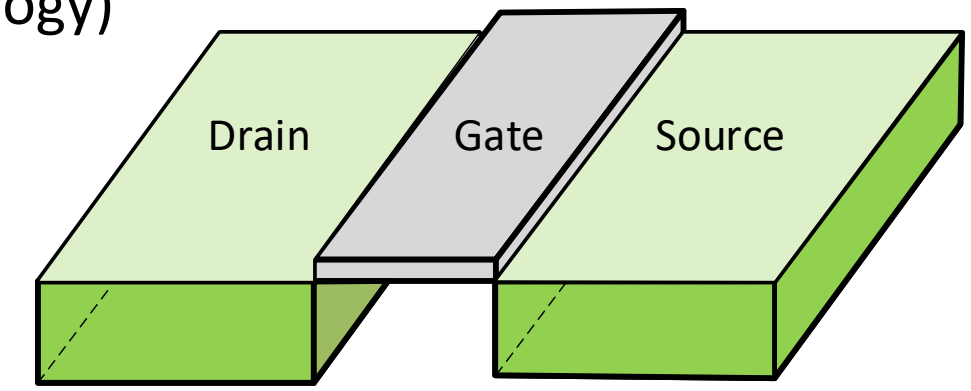

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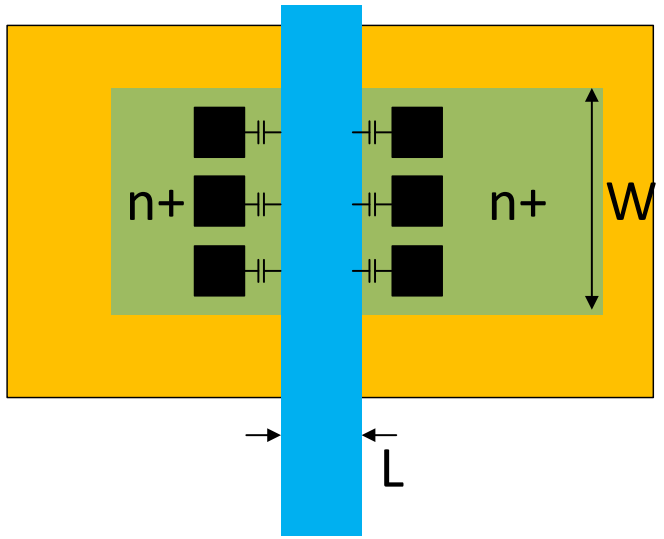
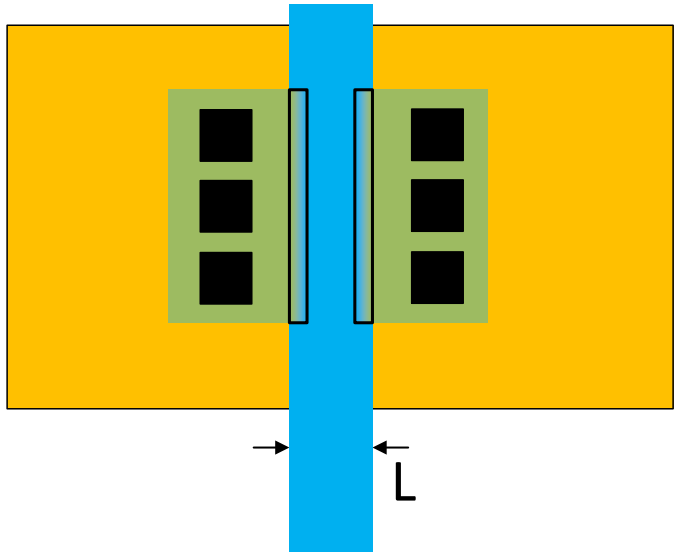
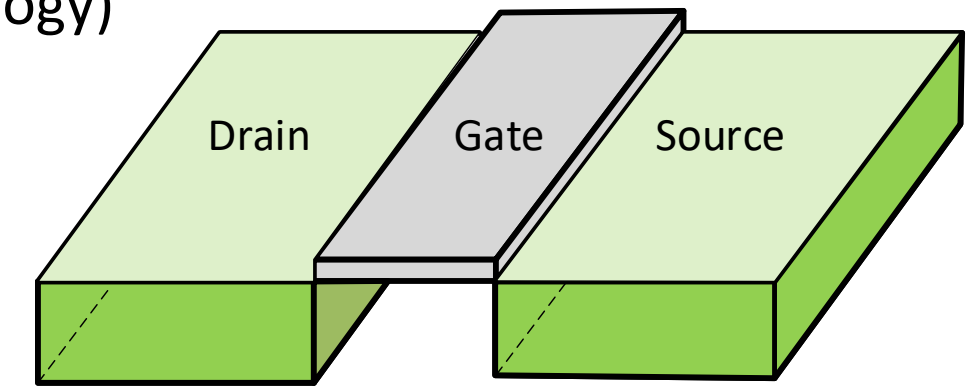
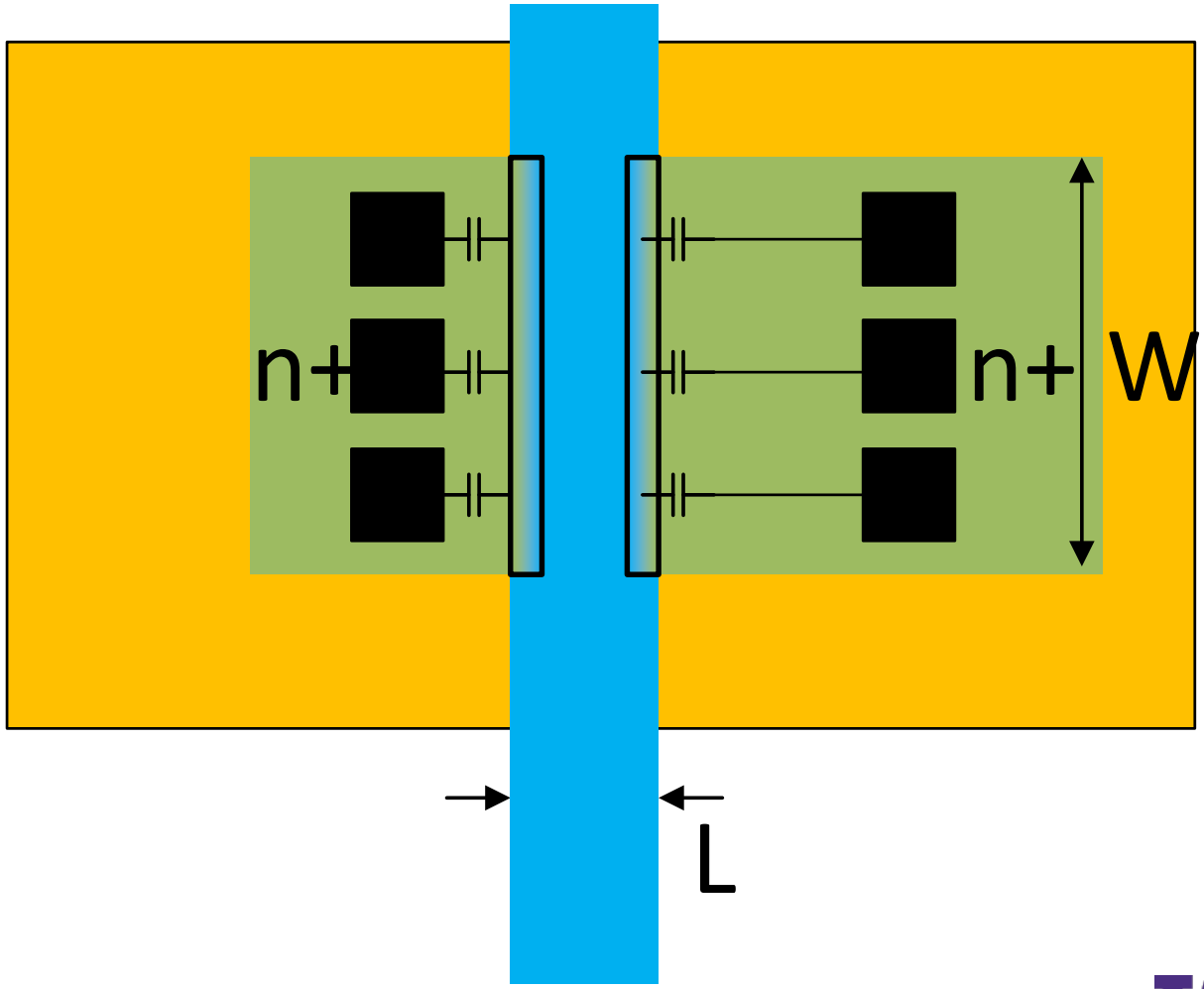




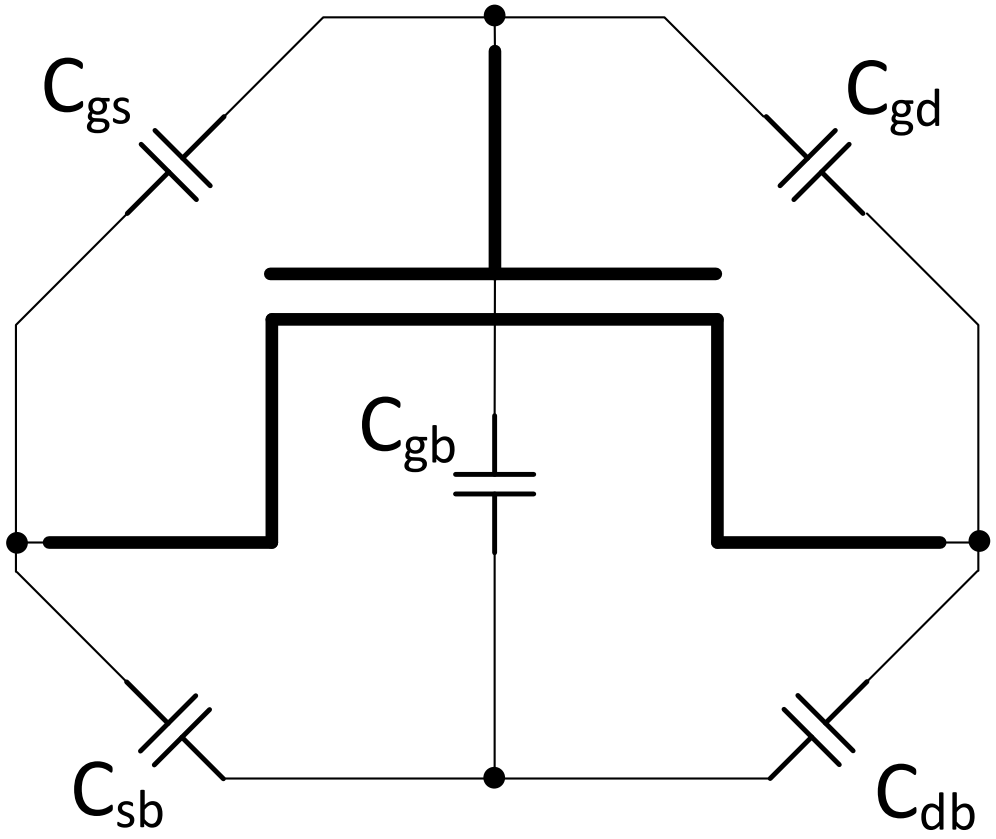


Is This a Good Idea?

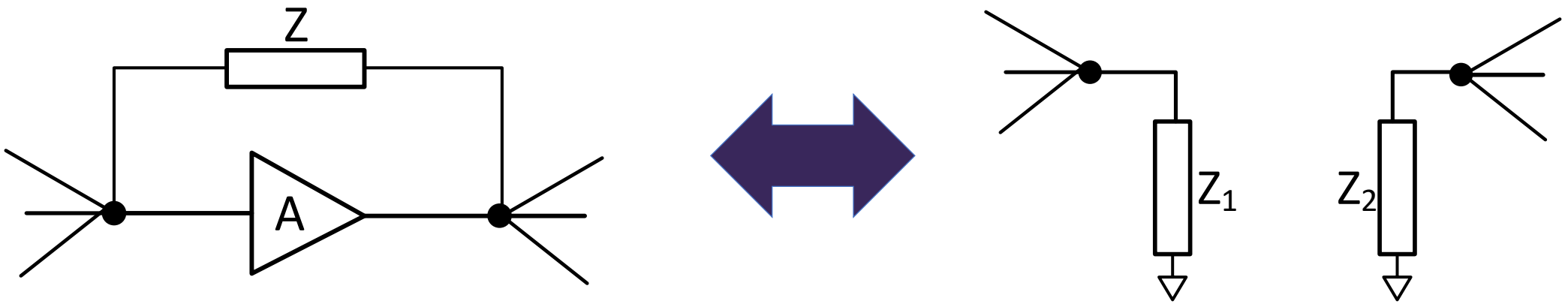


Capacitance of a MOS transistor

- $C_{gate} = W*L*C_{ox}$
- $C_{source} = C_j\,(W) + C_{gs}(W)$
- $C_{drain} = C_j\,(W) + C_{gd}\,(W)$

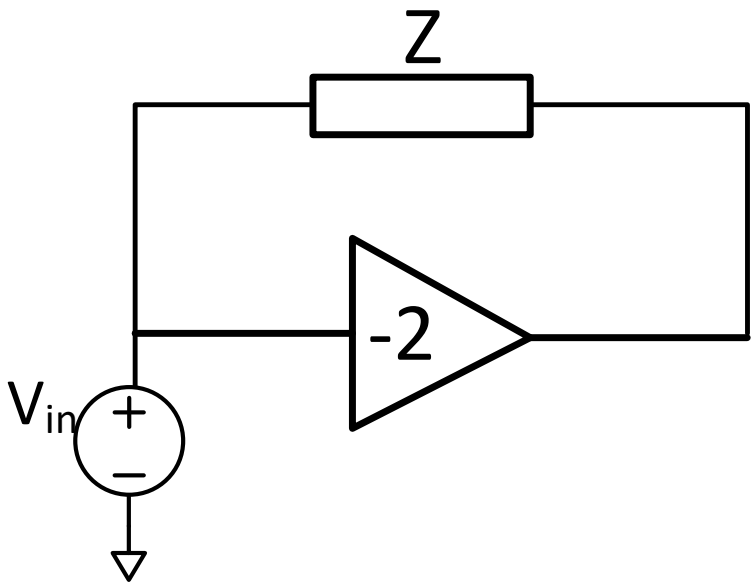


Detour: Miller impedance



- $Z_1 = Z/(1-A)$,
- $Z_2 = Z/(1-A^{-1})$
- Specifically, if A=-1
  - $Z_1 = Z_2 = Z/2$
  - If Z is a capacitance, Capacitance doubles

Quick Example



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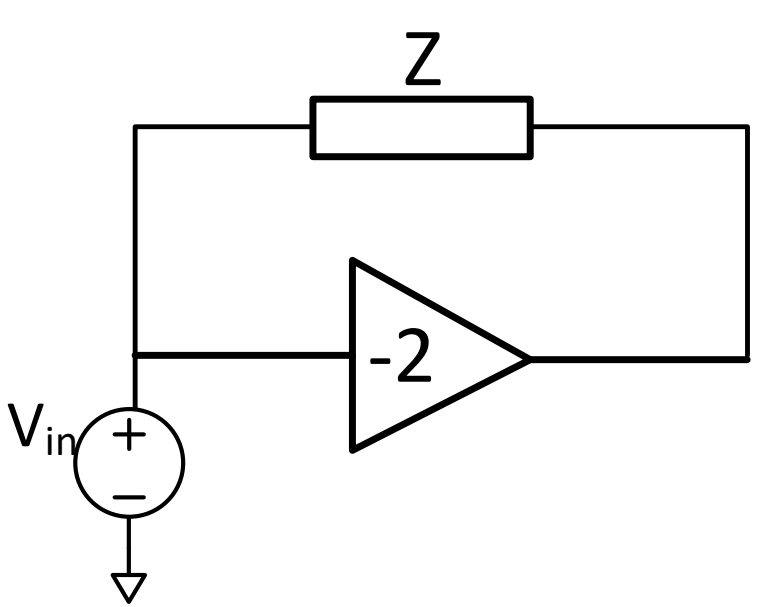
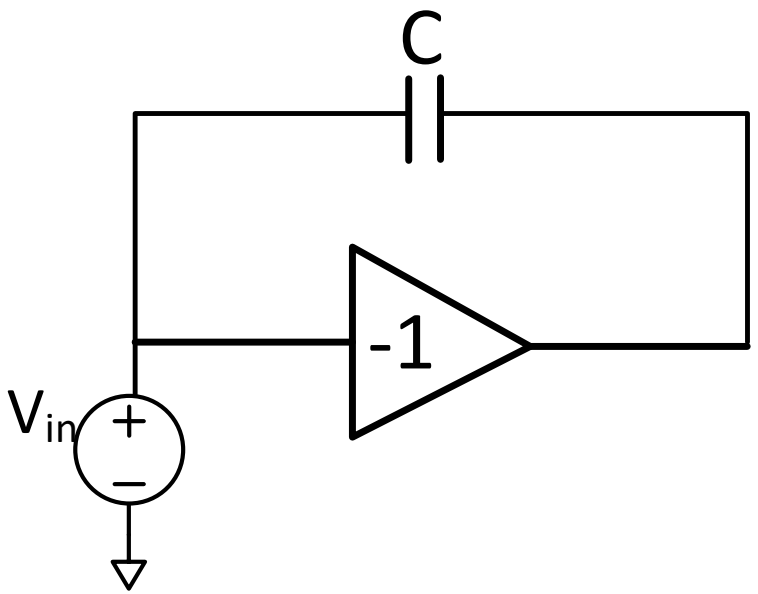
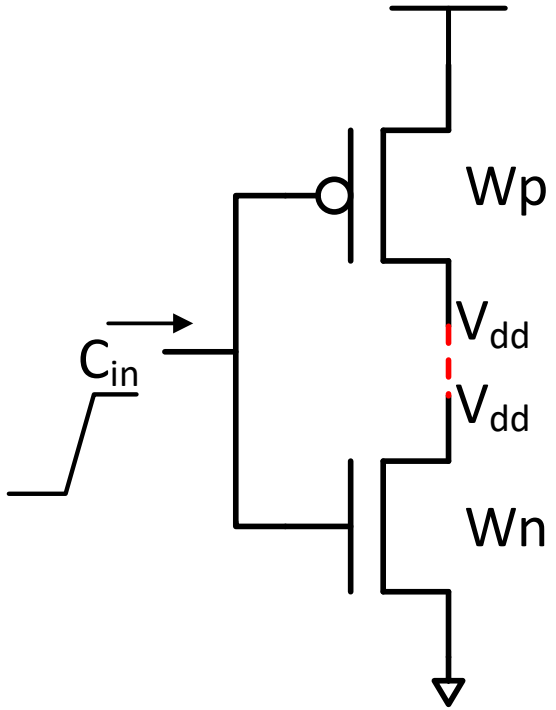




Miller Capacitance in Inverters

- Write down C_{in} in terms of C_{gs},C_{gd} (Drain voltages held constant)
- C_{in} in terms of Cg* for an inverter:
- Source, Drain voltage transitions result of Gate voltage transition
  - Affects delay and power **differently**



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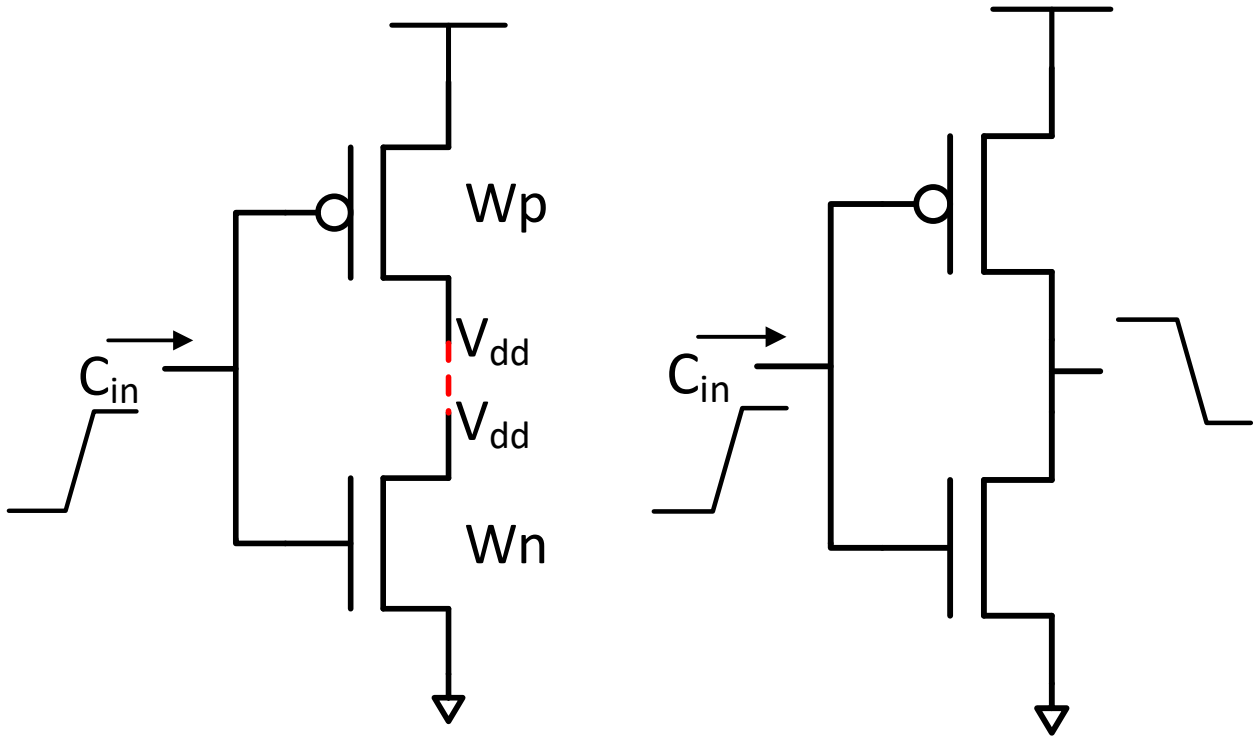

Miller Capacitance in Inverters (contd.)

- Perceived capacitance different for power and delay
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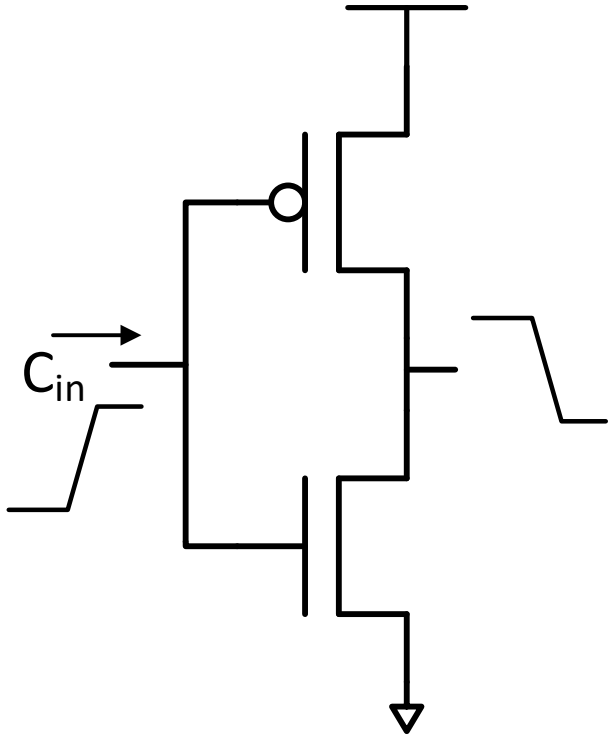

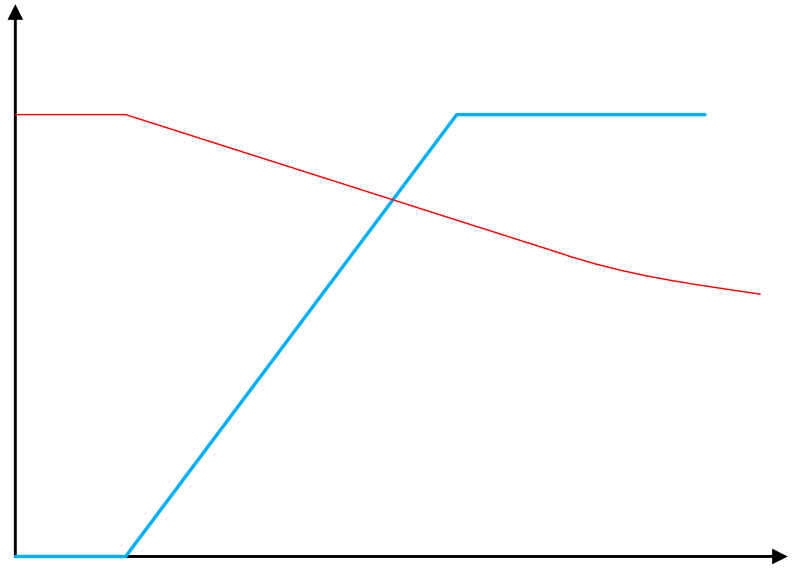

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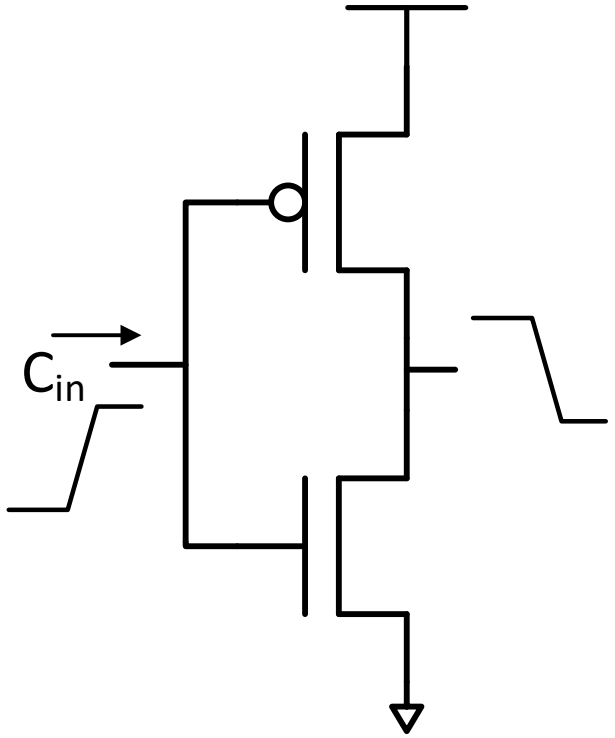

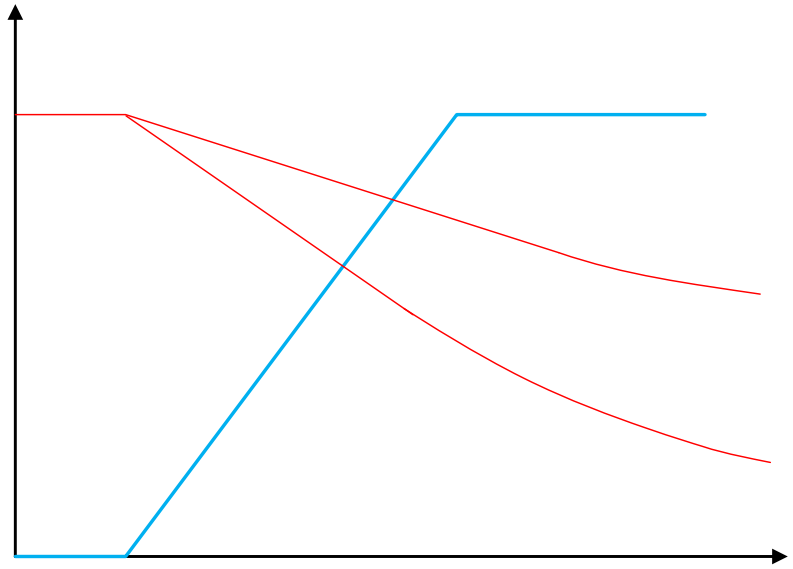

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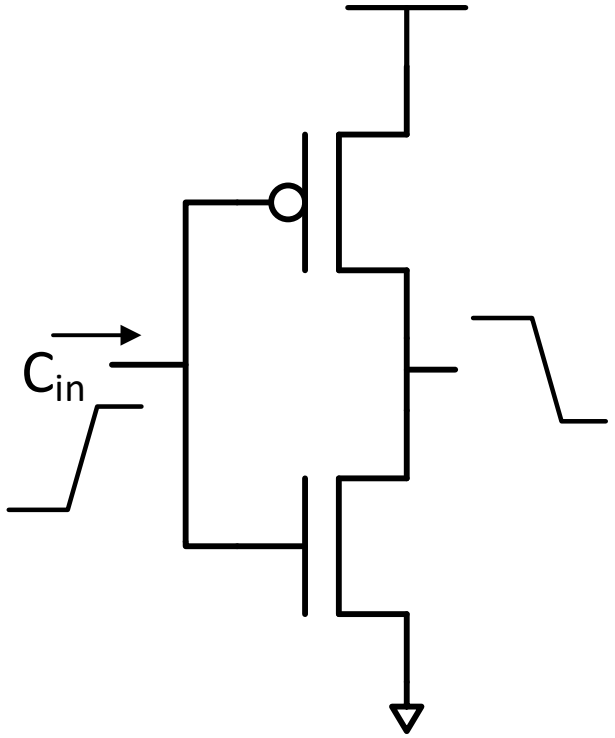

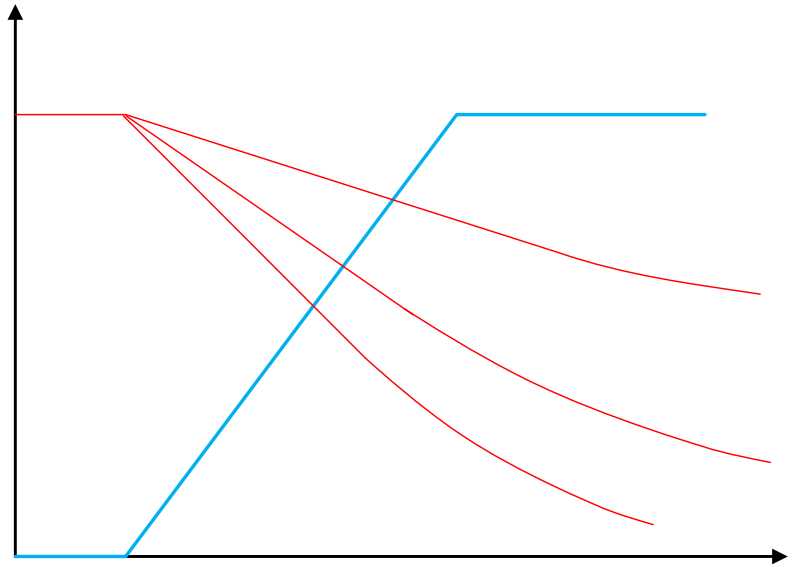

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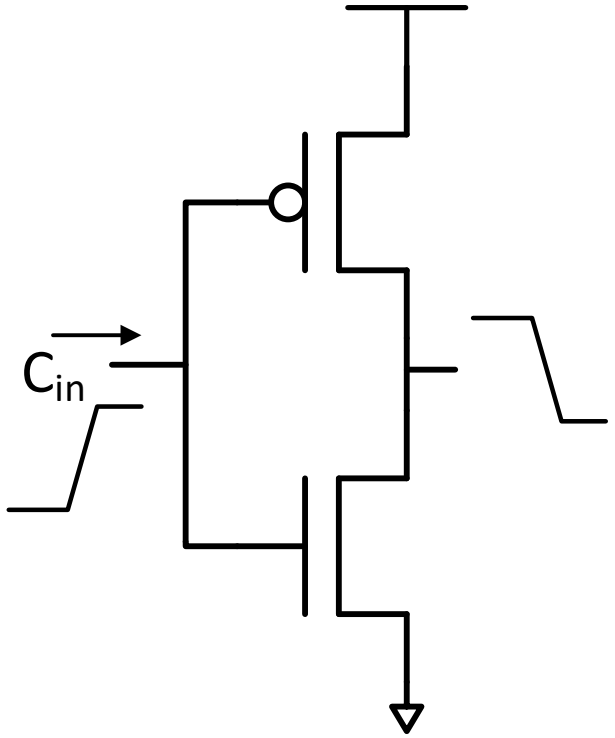

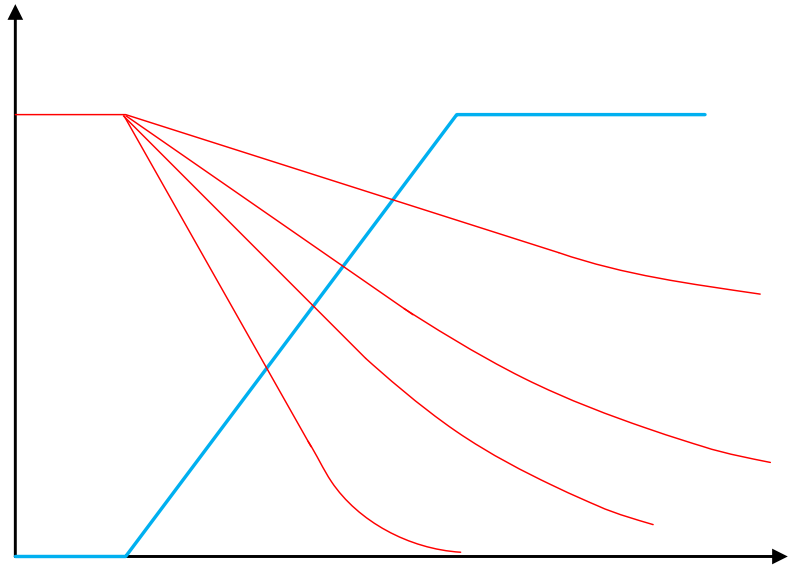

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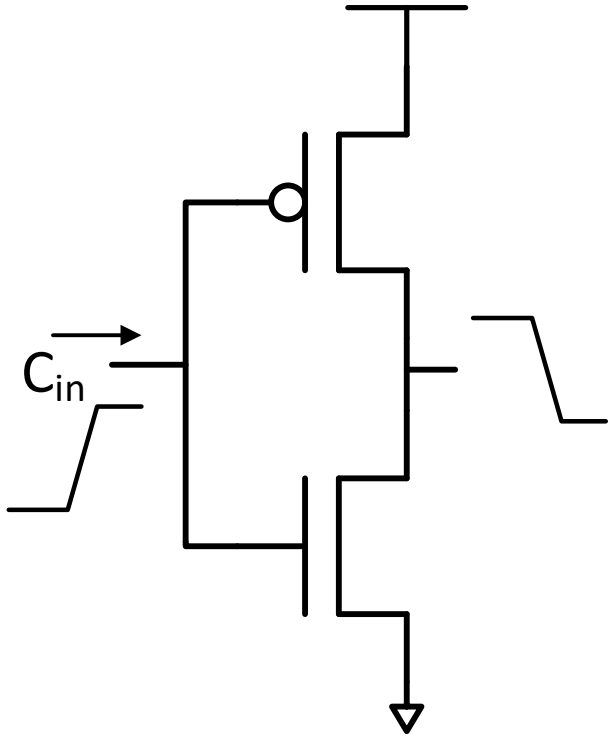

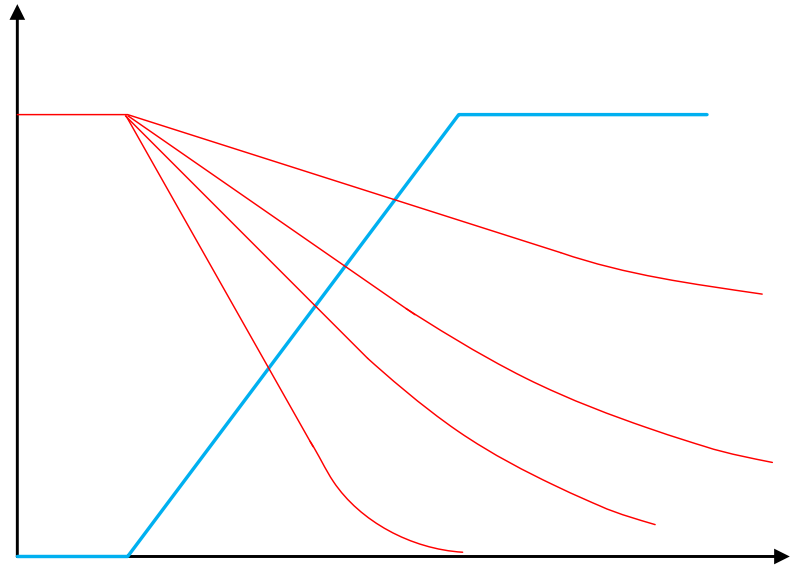

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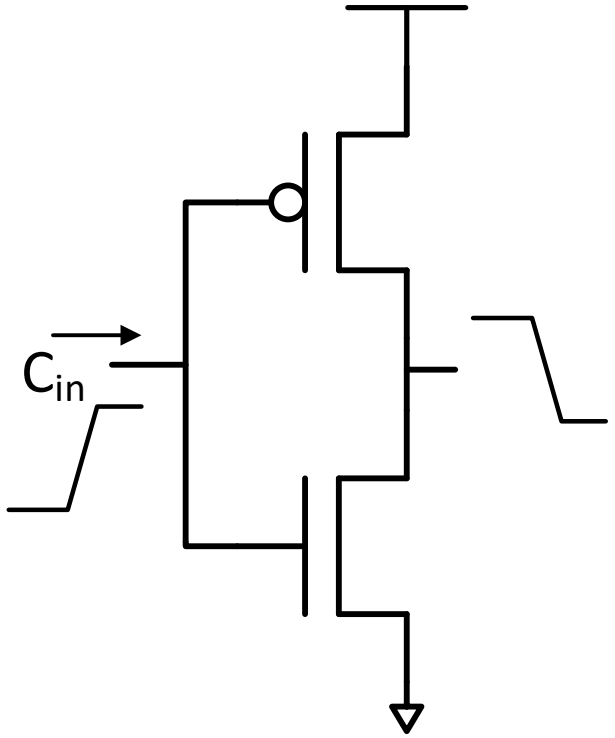
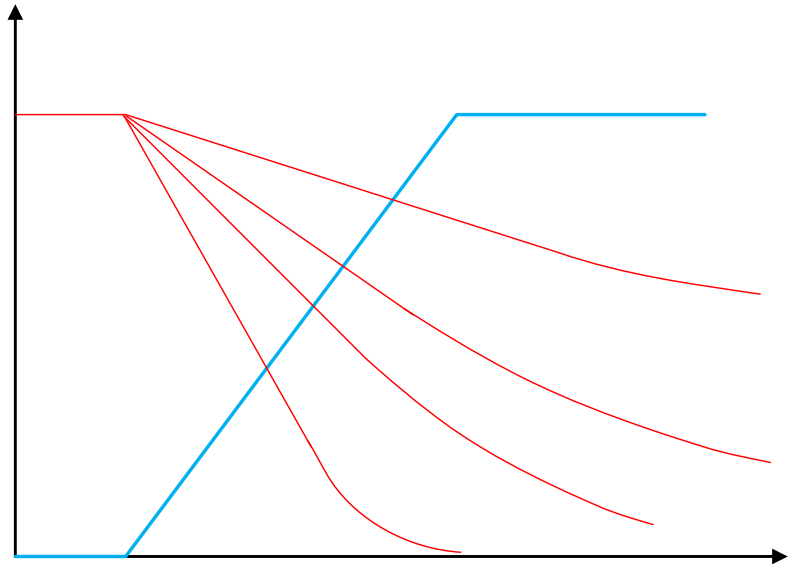
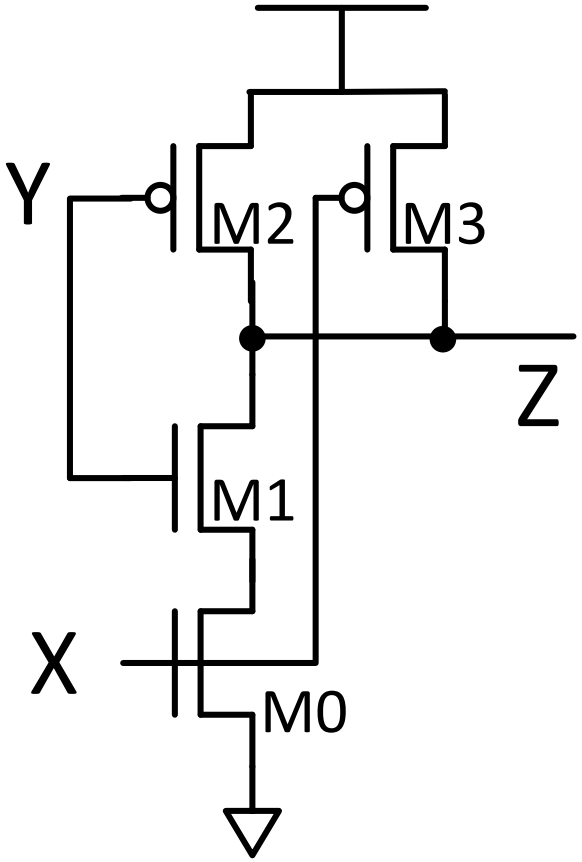
- Miller cap affects both input and output





Miller Capacitance in CMOS gates

- Breakout: What signal transitions result in the worst case input cap for M1?



Reading Assignments

- Required:
  - From sand to a wafer: http://www.youtube.com/watch?v=i8kxymmjdoM
  - Nice video of simplified process fabrication step at : http://www.youtube.com/watch?v=OBiu2agne_U
  - Slightly more up-to-date overview of process fabrication http://www.youtube.com/watch?v=-GQmtITMdas&list=PL17EE400FD24FFE20&index=7

- Recommended :
  - Section 1.5
  - Weste&Harris , Chapter 2-2.2

- Optional
  - Weste & Harris , Chapter 2-2.4

Reading assignment

- Section 1.5

- Optional Reading
  - Read up on body effect
  - Velocity saturation and the short channel transistor model