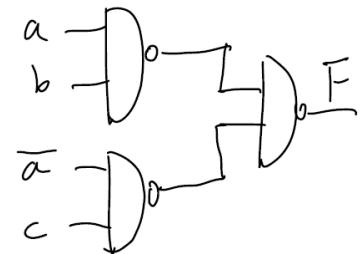
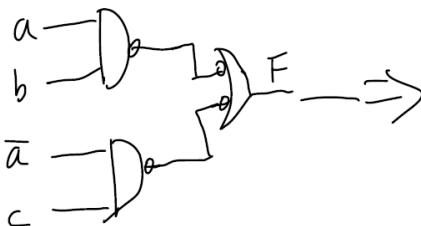


1. [5 points] Write down the CMOS implementation of the following Boolean function in as few gates as possible. Assume you get inverted input signals for free, and **you can use only nand and nor gates**:

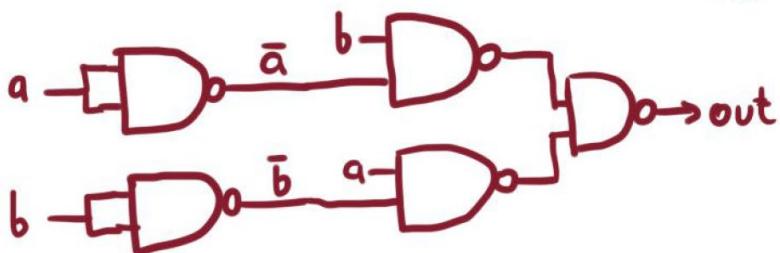
a	b	c	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$$F = ab + \bar{a}c + bc$$



2. [5 points] Construct a 2-input XOR gate using 2-input NAND gates **and NAND gates only**.

$$\text{xor} = a\bar{b} + \bar{a}b$$



Note: Multiple approaches available for question 2.

3. [3+3+3=9 points] Consider the figures shown below.

- a. For the circuit in Fig. 1a what is the delay associated with a step transition (one rising and one falling) as shown in the figure. Assume that output resistance of the inverters is $1k\Omega$

Both the transitions occur at the same time
 $\Rightarrow A = -1$ (since the transitions are opposite)

$$\text{Miller factor } \alpha = 1 - A \Rightarrow \boxed{\alpha = 2}$$

$$\tau = RC = R(C_a + \alpha C_c) = 1k(100f + 200f) = 300 \text{ ps}$$

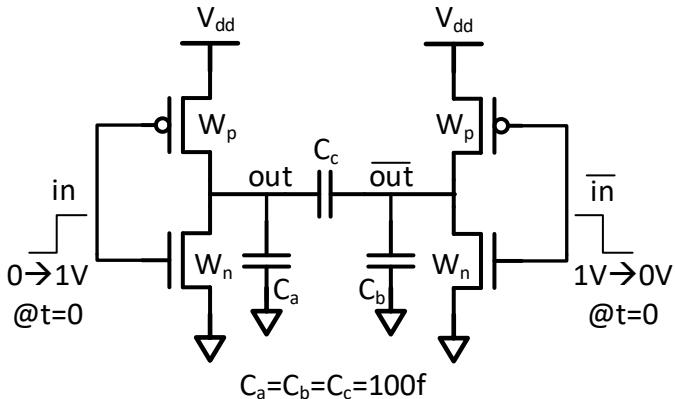


Figure 1a

- b. Consider Fig. 1b below: Assume that output resistance of the inverters is driving za are $1\text{k}\Omega$. Assume worst case conditions for the circuit driving zb so that the delay between za and zb is as high as possible. What is the worst case delay for the $a \rightarrow za$ transition.
- c. Consider Fig. 1b below: Assume that output resistance of the inverters is driving za are $1\text{k}\Omega$. Assume best case conditions for the circuit driving zb so that the delay between za and zb is as low as possible. What is the best case delay for the $a \rightarrow za$ transition.

C) analogy to b), the best case has $A = 2$. So the delay becomes 0ps!

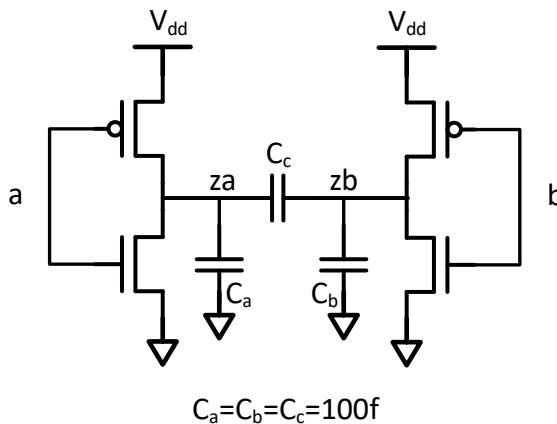


Figure 1b

b) For the worst case scenario, zb is transitioning at a slow rate twice that of za in the opposite direction
 $A = -2$ (Looking in through za)

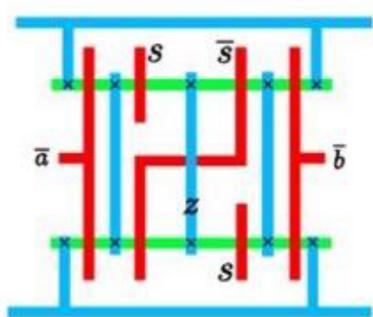
$$\alpha = (1 - A) = 3$$

$$\tau = RC = R(C_a + \alpha C_c) = 1k(100f + 300f) = 400 \text{ ps}$$

4. [3+1 = 4 points] Consider the stick diagram in figure 2.

a. Write down the boolean equation describing the gate

b. What is the functionality of the gate. Don't give us a formula, just describe the function?



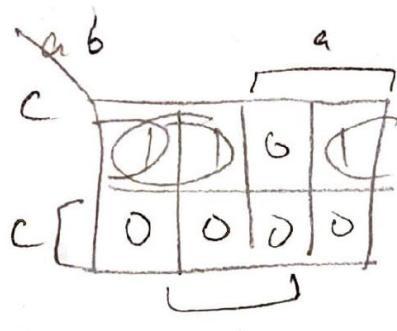
a. $Z = \bar{s}a + sb$

b. This is a 2:1 inverting MUX.
Since the input is \bar{a}, \bar{b} .

Figure 2

5.

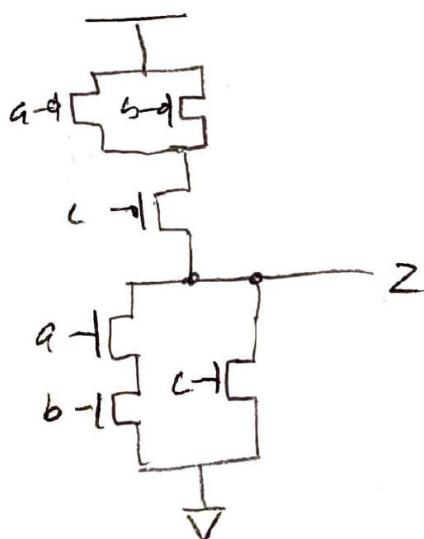
a	b	c	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0



$$Z = \bar{b}\bar{c} + \bar{c}\bar{a} = \bar{c}(\bar{b} + \bar{a})$$

$$= \bar{c}(\bar{b}\bar{a})$$

$$= \frac{\bar{c}}{\bar{c} + \bar{b}\bar{a}}$$



6. [5+5=10points]

- a. Consider the inverter shown in Figure 4a. Draw the transfer function of the inverter
 - b. Consider the inverter shown in Figure 4b. Overlay the transfer function of this inverter over your solution from 6a above.

DRAW YOUR FINAL ANSWERS OVERLEAF ON THE PROVIDED AXES. Be sure to label key points of the transfer function such as transitions from linear/cutoff/saturation etc.

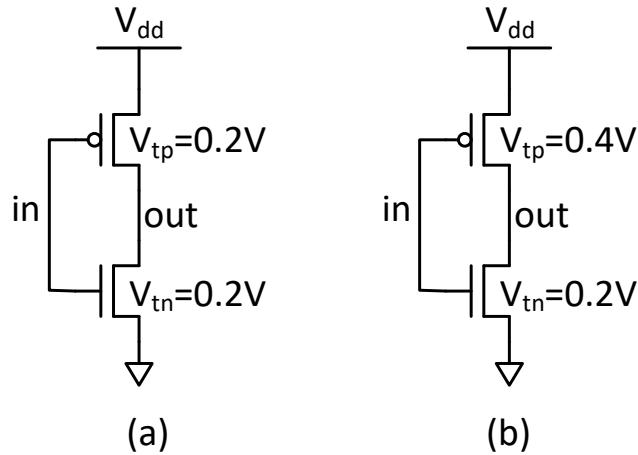
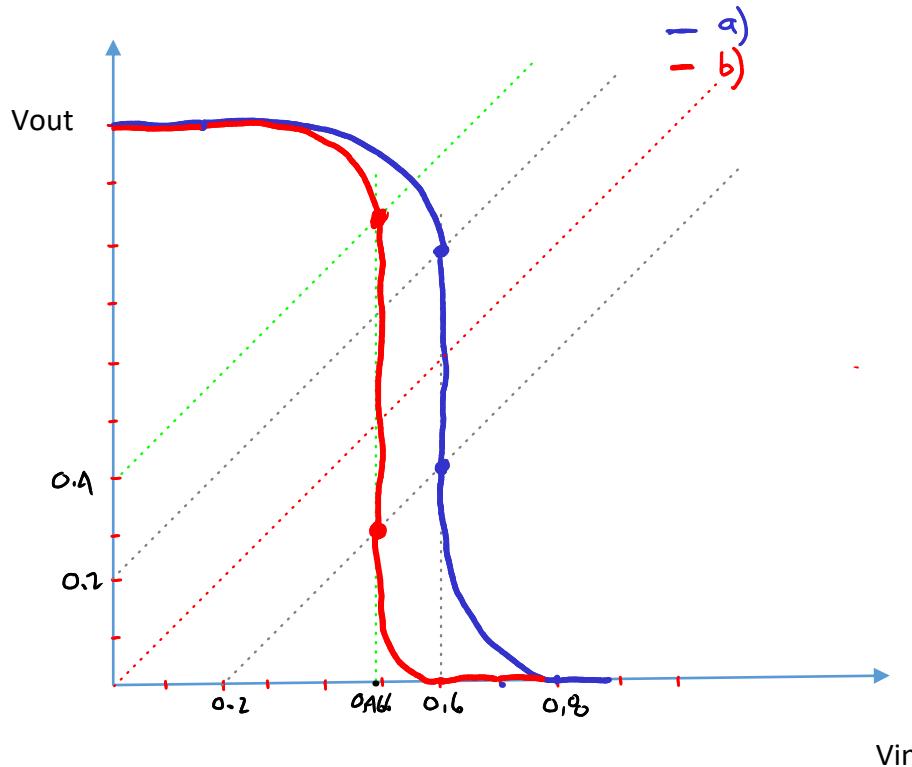


Figure 4



NMOS

- $V_{in} > V_{th} \text{ ON}$
- $V_{out} \geq V_{in} - V_{th} \text{ SAT}$
- $V_{out} \leq V_{in} - V_{th} \text{ LIN}$
- $V_{inv} = \frac{V_{dd} - V_{thp} + V_{thn} \cdot \beta_r}{1 + \beta_r}$
- where β_r is the β ratio
- $V_{inv,a} = 0,16$
- $V_{inv,b} = 0,466$

Question 7

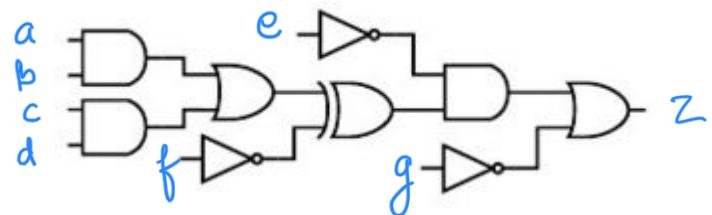


Figure 5

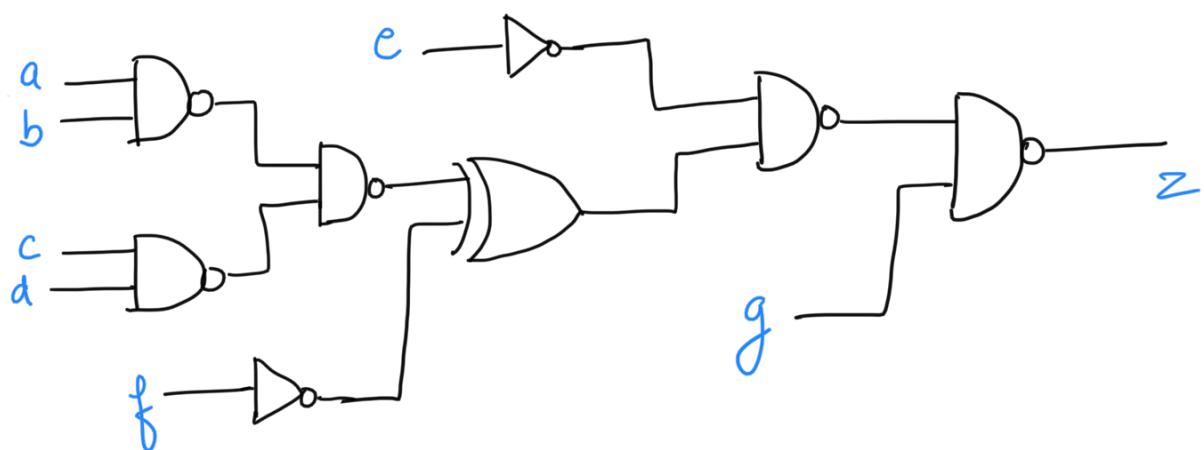
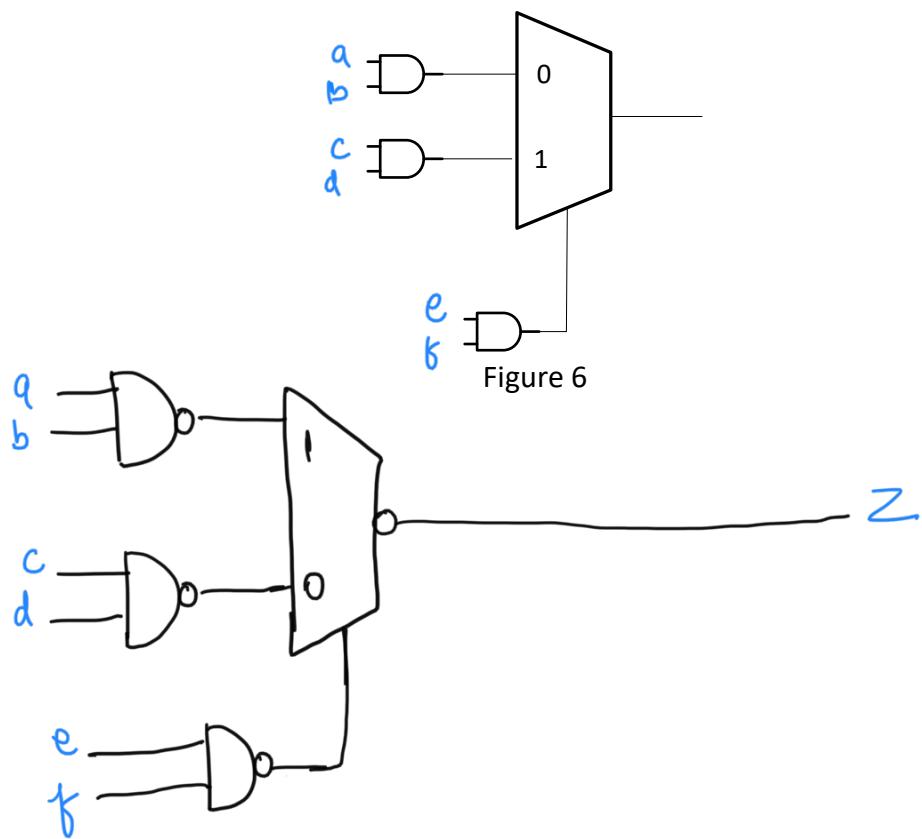
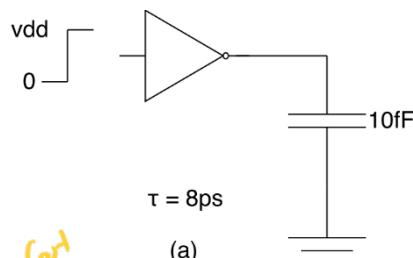


Figure 6



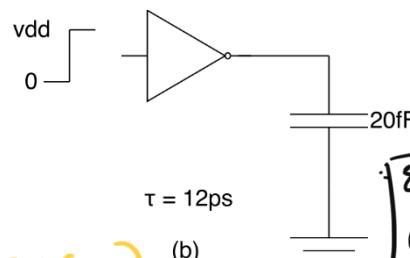
$$f = 10^{-15} \text{ F}$$

8. [3 + 3 + 3 = 9 points] Note the delay for a unit step input for the loaded inverters in Figure 7 (a) and (b).

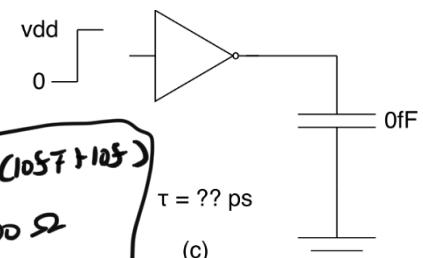


$$h = \frac{C_L}{C_{in}}$$

(a)



(b)



(c)

$$\tau = R_c (C_L + C_{SL})$$

Figure 7

a. What is the delay for (c)?

$$\tau_1 = R_c (10fF + C_{SL}) \Rightarrow 8ps = R_c (10fF + C_{SL})$$

$$\tau_2 = R_c (20fF + C_{SL}) \Rightarrow 12ps = R_c (20fF + C_{SL})$$

b. What is the effective resistance of the inverter?

$$R_c = 400\Omega$$

c. Estimate the resistance of this inverter at Vdd = 0.6V, Vth = 0.3V (Note that the delays reported above were for Vdd = 1V, Vth = 0.2V)

$$\tau_{above} = \frac{Q}{I} = \frac{VC(VDD)}{\frac{1}{2}\beta(VDD - Vth)^2} = \frac{VC(1)}{\frac{1}{2}\beta(1-0.2)^2} = 3.125 \frac{C}{\beta}$$

$$R = \frac{VDD}{\frac{1}{2}\beta(VDD - Vth)^2}$$

$$R_o = \frac{0.6}{\frac{1}{2}\beta(0.6 - 0.3)^2}$$

$$= \frac{0.6}{\frac{1}{2}(7.81)(0.3)^2}$$

$$R_o = 1.7 k\Omega$$

$$0.4k\Omega \quad \frac{(VDD)}{\frac{1}{2}\beta(VDD - Vth)^2}$$

$$0.1k\Omega \quad \frac{(1)}{\frac{1}{2}\beta(1-0.2)^2}$$

$$\beta = 7.81$$

9. [12 points] Consider the inverter cascade in Fig. 8. Use the delay formulation of $\tau = R_i C_{i+1}$ to figure out inverter input capacitance assignments for x and y that will minimize the delay through the chain from **in** to **out**. Note that the standard geometric formula does not apply because the wire loading on the inverters is too large to be ignored. (Hint: Formulate the problem using first principles and then use the same maximization/minimization approach. If you really must, or have a deep aversion for evaluating derivatives, you're welcome to use python/perl/Excel-solver/Matlab or pretty much any solver mechanism to figure out your answer as well).

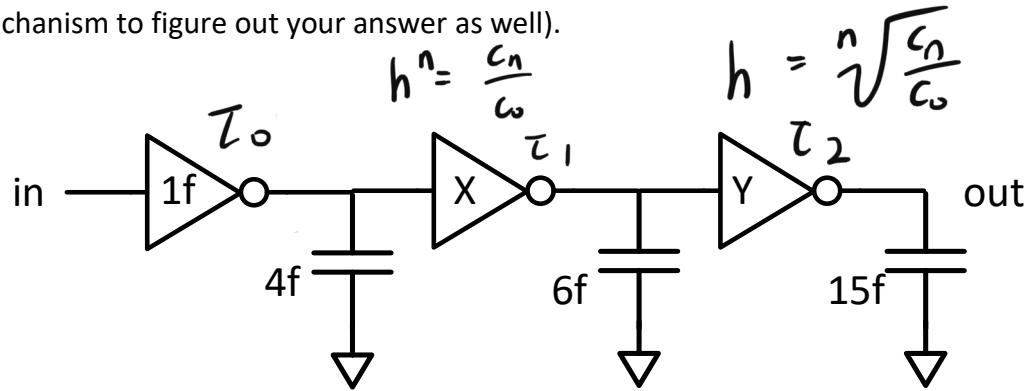


Figure 8

$$\tau = R_o C_L$$

$$\tau = \frac{k}{C_i} (C_\omega + C_L)$$

$$\tau_0 = k \left(\frac{y+x}{1} \right)$$

$$\tau_1 = k \left(\frac{6+y}{x} \right)$$

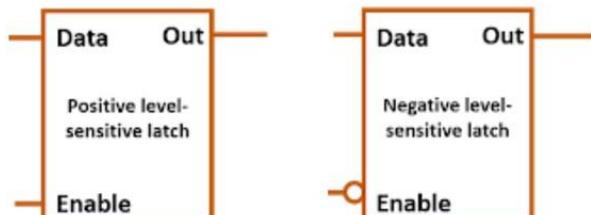
$$\tau_2 = k \left(\frac{15}{y} \right)$$

$$\tau = k \left[4+x + \left(\frac{6+y}{x} \right) + \frac{15}{y} \right]$$

↓ take partial deriv,
find min

$$\begin{cases} x = 3.662^2 \\ y = 7.41168 \end{cases}$$

10. [9+3+4 = 17 points] For this problem, consider the standard cells that are constructed from the sub-blocks below:



$T_{\text{setup}} = 100\text{p}$
 $T_{\text{hold}} = -30\text{p}$
 $T_{\text{dq}} = 140\text{p}$
 $T_{\text{cq}} = 120\text{p}$

$T_{\text{setup}} = 100\text{p}$
 $T_{\text{hold}} = -30\text{p}$
 $T_{\text{dq}} = 140\text{p}$
 $T_{\text{cq}} = 120\text{p}$

Figure 9

- a. Consider the standard cell constructed in Fig. 10 below
- Is this structure a timing element? Yes
 - Does it sample data on an “edge” or level? Edge
 - What level or edge is data sampled on? Posedge
 - Is data released on Q on an edge or a level? Edge
 - What level or edge is the data produced on Q? Negedge
 - What is your best estimate for its setup time? 100 ps
 - What is your best estimate for the clk-Q delay of the structure? 1120 ps
 - What is the pipelining overhead of this flip-flop? 1220 ps
 - What is the hold-immunity of this structure? 1150 ps

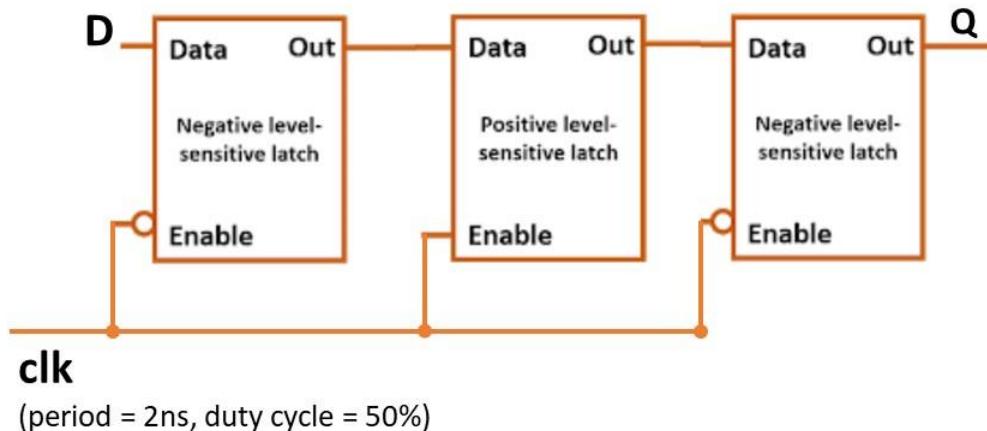


Figure 10.

b. Consider the flip-flop constructed in Fig. 11.

- What is your best estimate of setup time for this flip-flop? 100 ps
- What is your best estimate of hold time for this flip-flop? -30 ps
- Are there any other timing concerns with this flip-flop?

Data arrives exactly at the latching edge of the A-latch potentially causing setup/hold violations

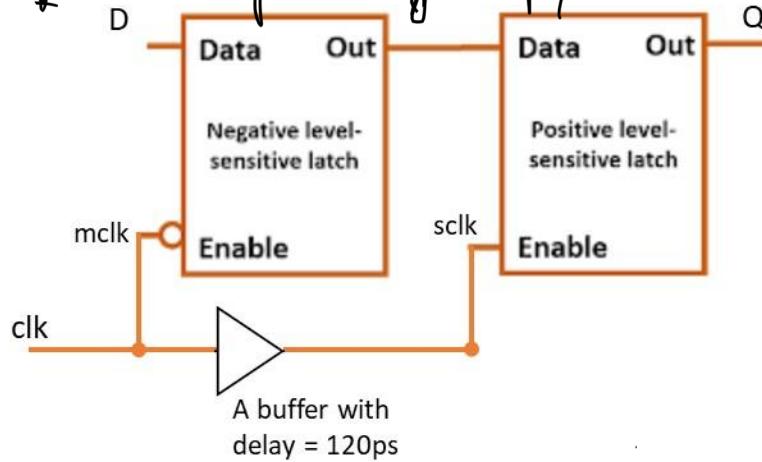


Fig. 11

c. Finally, consider the standard cell construction of Fig. 13

- What is your best estimate of setup time for this flip-flop? 110 ps
- What is your best estimate of hold time for this flip-flop? -40 ps
- What is your best estimate of T_{CQ} for this flip-flop? 240 ps
- What is the race immunity of this flop? 280 ps
- What is the pipelining overhead of this flop? 350 ps

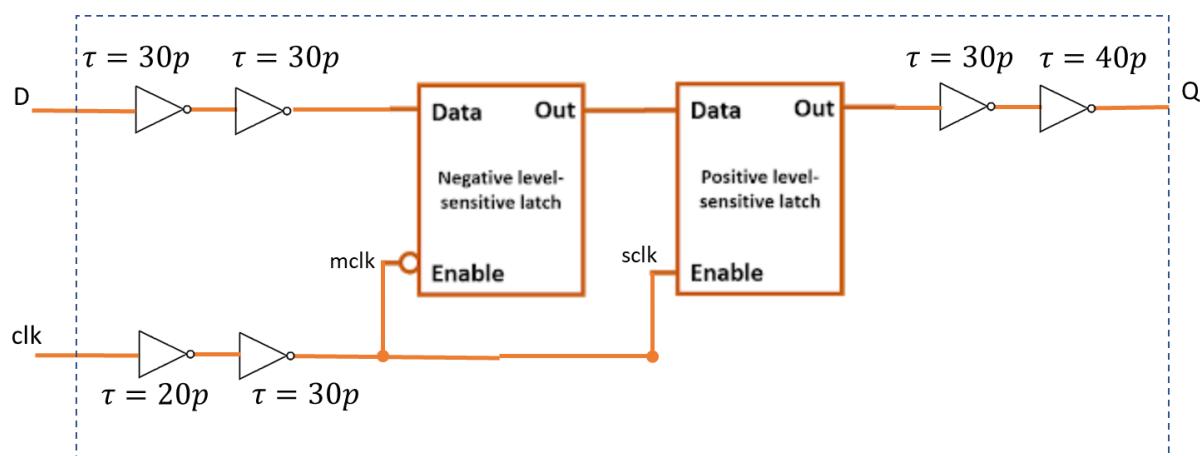


Fig. 13