Lecture 4: CMOS Inverter Fabrication (and Layout)

Based on material prepared by prof. Visvesh S. Sathe

Acknowledgements

All class materials (lectures, assignments, etc.) based on material prepared by Prof. Visvesh S. Sathe, and reproduced with his permission


Visvesh S. Sathe
Associate Professor
Georgia Institute of Technology
https://psylab.ece.uw.edu

UW (2013-2022)
GaTech (2022-present)

The Design Process

- High-level design → Schematic → **Layout → Fabrication**

- Layout (or Mask layout) is the exchange format to specify exactly how you want each transistor in your design to look

- CMOS inverter layout (step by step) , and how it determines the fabrication process

- **D**esign **R**ule **C**hecks (DRCs) and their importance
  - Metal-metal
  - Via enclosure
  - Poly past active
  - Active within nwell, away from nwell
  - Min width rules/Min area rules
  - Minimum overlap

- Some aspects of modern fabrication process tech.

ELECTRICAL & COMPUTER ENGINEERING
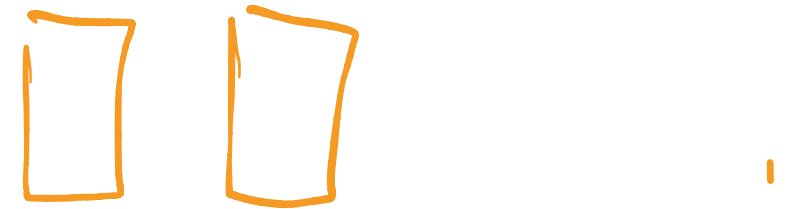
CMOS Inverter: Logic to Silicon View

- Schematic is converted to "mask-layout" for fabrication
    - Actual 2D geometrical description of how the inverter is to be fabricated
    - Polygons of different "layers" describe construction of the inverter
    - "Mask" term due to use of these shapes as masks during photolithography (and eventually etch) to define the target shapes in each layer
- Starting point: Clean silicon wafer with an epitaxially-grown doped, P-type substrate
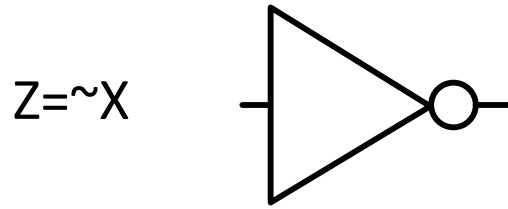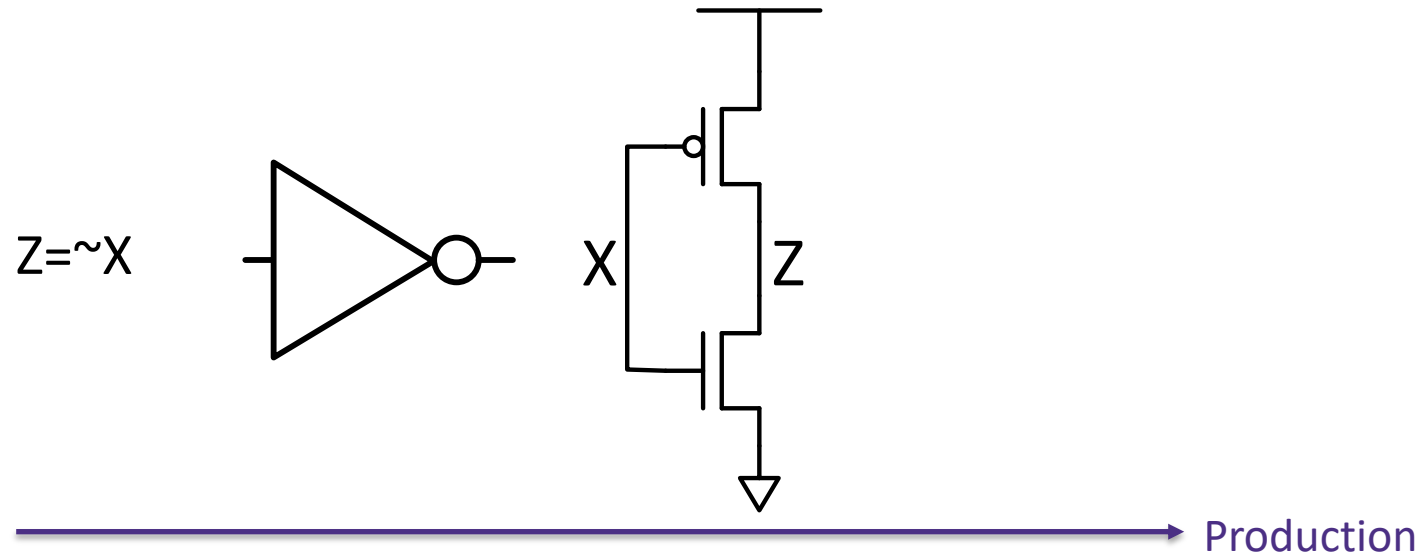
W ELECTRICAL & COMPUTER ENGINEERING

CMOS Inverter: Logic to Silicon View

Z=~X

- Schematic is converted to "mask-layout" for fabrication
    - Actual 2D geometrical description of how the inverter is to be fabricated
    - Polygons of different "layers" describe construction of the inverter
    - "Mask" term due to use of these shapes as masks during photolithography (and eventually etch) to define the target shapes in each layer
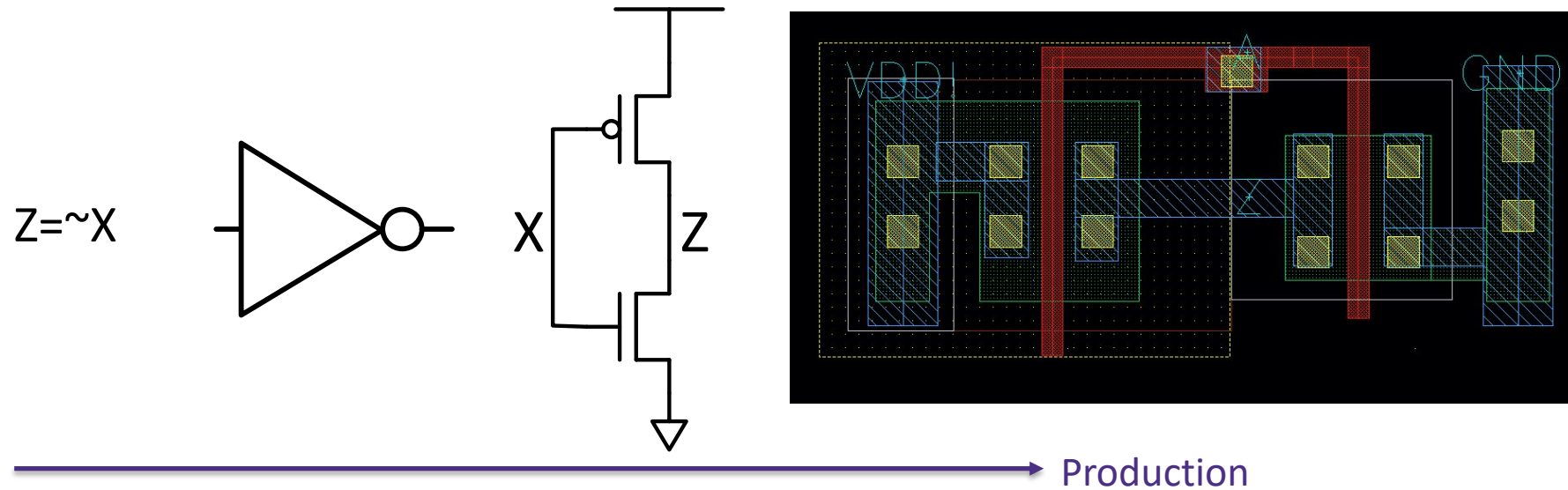- Starting point: Clean silicon wafer with an epitaxially-grown doped, P-type substrate

CMOS Inverter: Logic to Silicon View

Z=~X

→ Production

- Schematic is converted to "mask-layout" for fabrication
  - Actual 2D geometrical description of how the inverter is to be fabricated
  - Polygons of different "layers" describe construction of the inverter
  - "Mask" term due to use of these shapes as masks during photolithography (and eventually etch) to define the target shapes in each layer
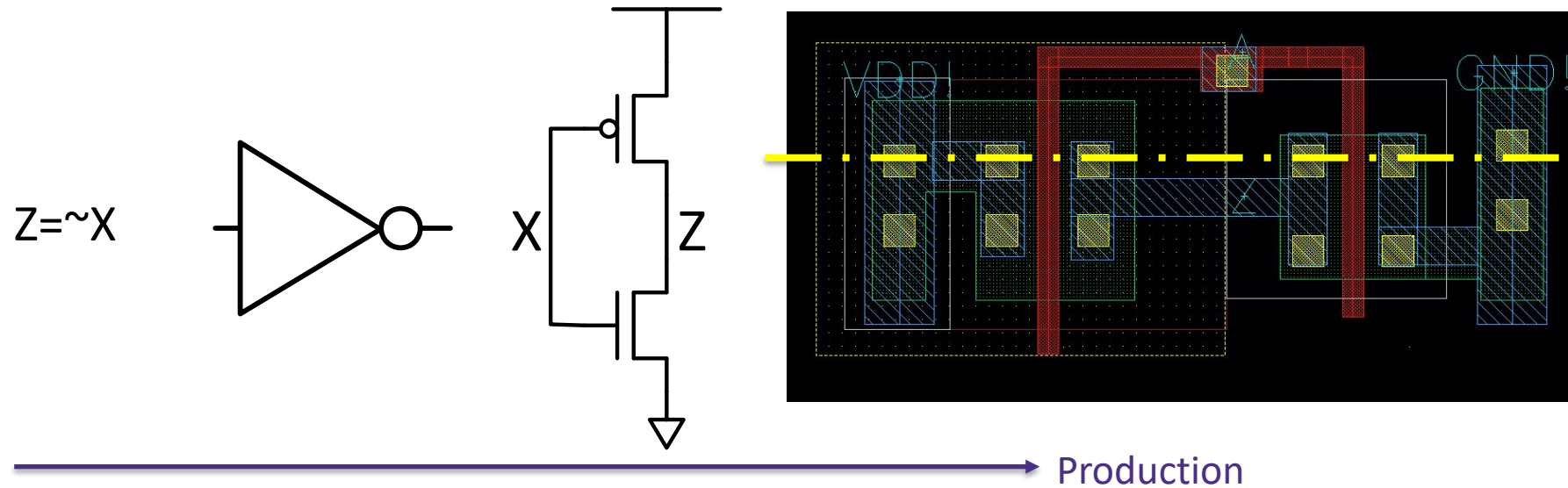- Starting point: Clean silicon wafer with an epitaxially-grown doped, P-type substrate

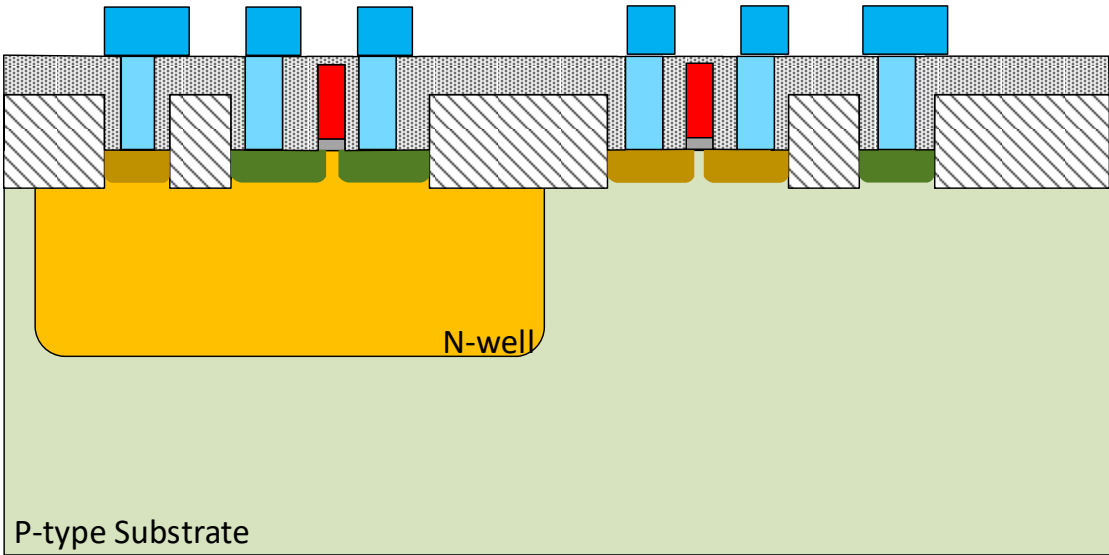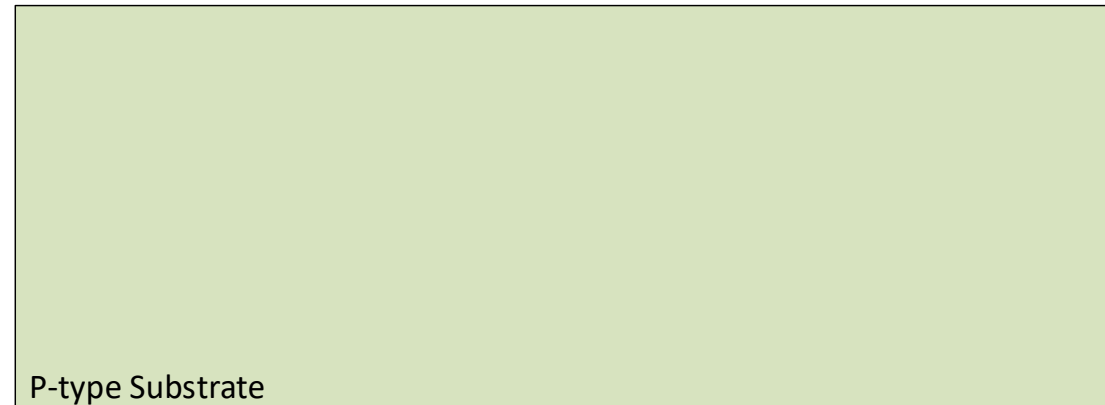# CMOS Inverter: Logic to Silicon View

Z=~X

→ Production

- Schematic is converted to "mask-layout" for fabrication
    - Actual 2D geometrical description of how the inverter is to be fabricated
    - Polygons of different "layers" describe construction of the inverter
    - "Mask" term due to use of these shapes as masks during photolithography (and eventually etch) to define the target shapes in each layer
- Starting point: Clean silicon wafer with an epitaxially-grown doped, P-type substrate

W ELECTRICAL & COMPUTER ENGINEERING
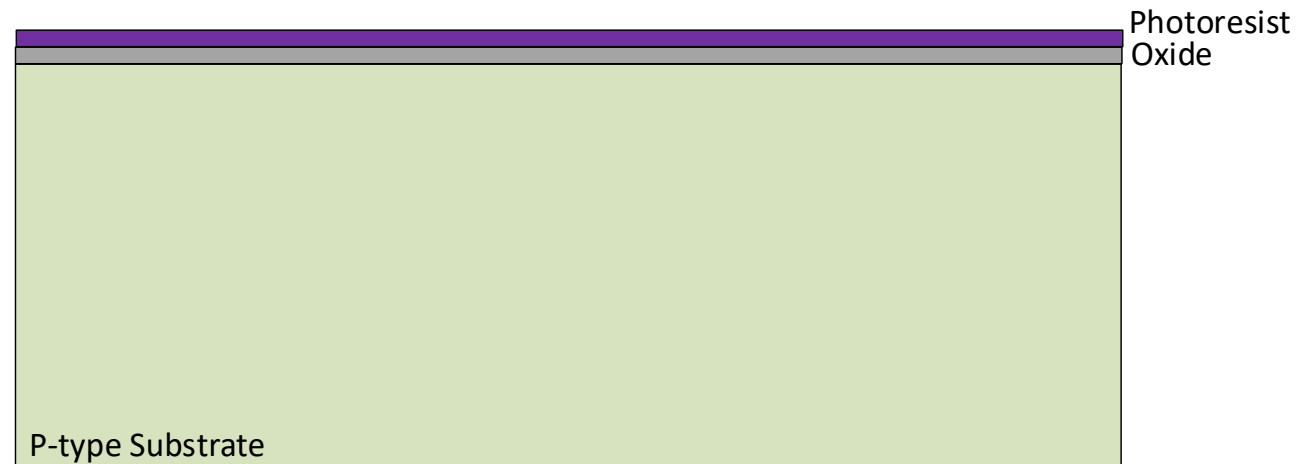
CMOS Inverter: Logic to Silicon View

Z=~X   X   Z   → Production

- Schematic is converted to "mask-layout" for fabrication
  - Actual 2D geometrical description of how the inverter is to be fabricated
  - Polygons of different "layers" describe construction of the inverter
  - "Mask" term due to use of these shapes as masks during photolithography (and eventually etch) to define the target shapes in each layer
- Starting point: Clean silicon wafer with an epitaxially-grown doped, P-type substrate

W ELECTRICAL & COMPUTER ENGINEERING

CMOS Inverter: Logic to Silicon View

Production

- Schematic is converted to "mask-layout" for fabrication
  - Actual 2D geometrical description of how the inverter is to be fabricated
  - Polygons of different "layers" describe construction of the inverter
  - "Mask" term due to use of these shapes as masks during photolithography (and eventually etch) to define the target shapes in each layer
- Starting point: Clean silicon wafer with an epitaxially-grown doped, P-type substrate

W ELECTRICAL & COMPUTER ENGINEERING

CMOS Inverter: Logic to Silicon View

Production

- Schematic is converted to "mask-layout" for fabrication
  - Actual 2D geometrical description of how the inverter is to be fabricated
  - Polygons of different "layers" describe construction of the inverter
  - "Mask" term due to use of these shapes as masks during photolithography (and eventually etch) to define the target shapes in each layer
- Starting point: Clean silicon wafer with an epitaxially-grown doped, P-type substrate

1: Simplified CMOS Inverter Fabrication

1.1: Create *Nwell* region

P-type Substrate

1.2: Create *Nwell* region

Oxide

P-type Substrate

- Grow oxide-layer to serve as a barrier

1.3: Create *Nwell* region

Photoresist

Oxide

P-type Substrate

- Deposit photoresist

ELECTRICAL & COMPUTER
ENGINEERING

1.4: Create *Nwell* region

UV

Nwell

Photoresist

Oxide

P-type Substrate

- Use N-Well Mask to allow light to selectively soften photoresist

W ELECTRICAL & COMPUTER ENGINEERING

1.5: Create *Nwell* region

Photoresist
Oxide

P-type Substrate

- Wash away softened photoresist

ELECTRICAL & COMPUTER
ENGINEERING

1.6: Create *Nwell* region

Photoresist
Oxide

P-type Substrate

- Etch away SiO$_2$

ELECTRICAL & COMPUTER
ENGINEERING
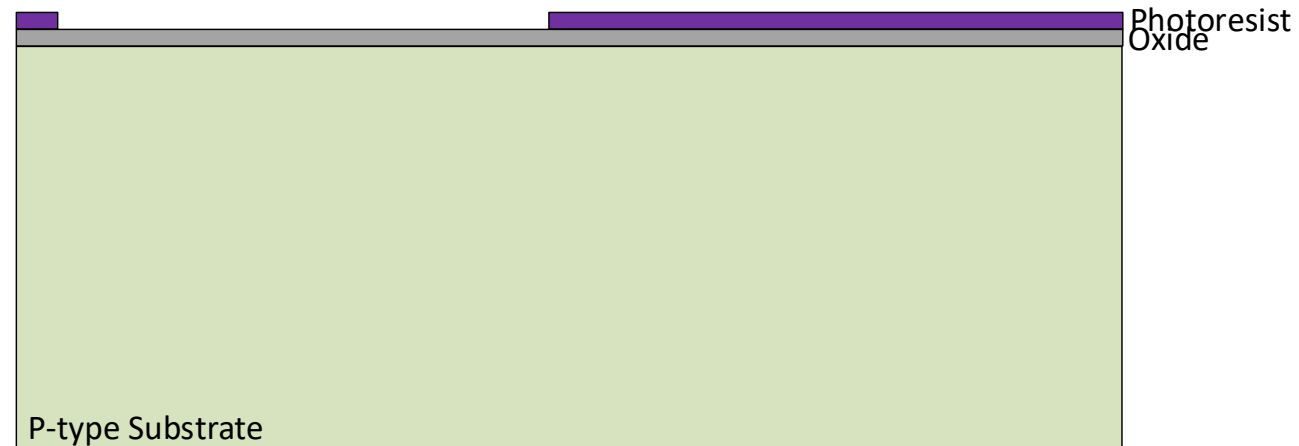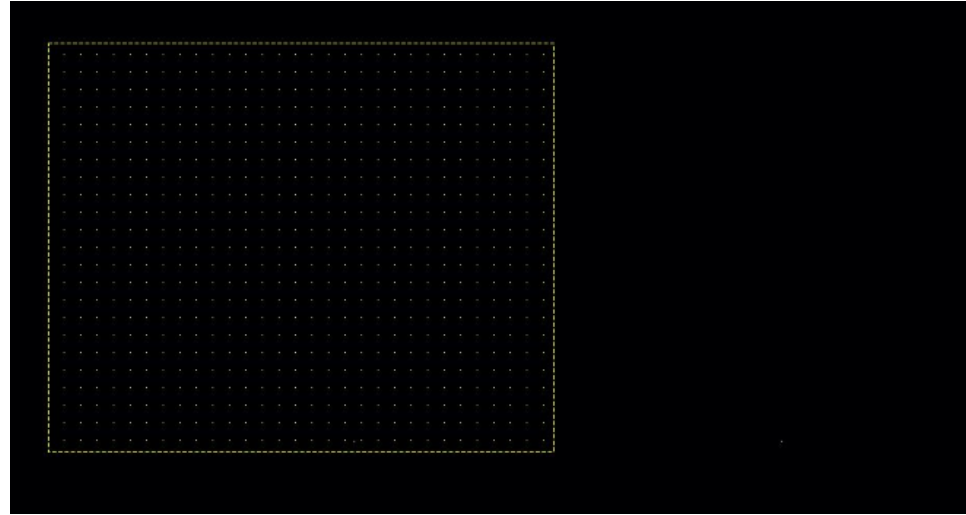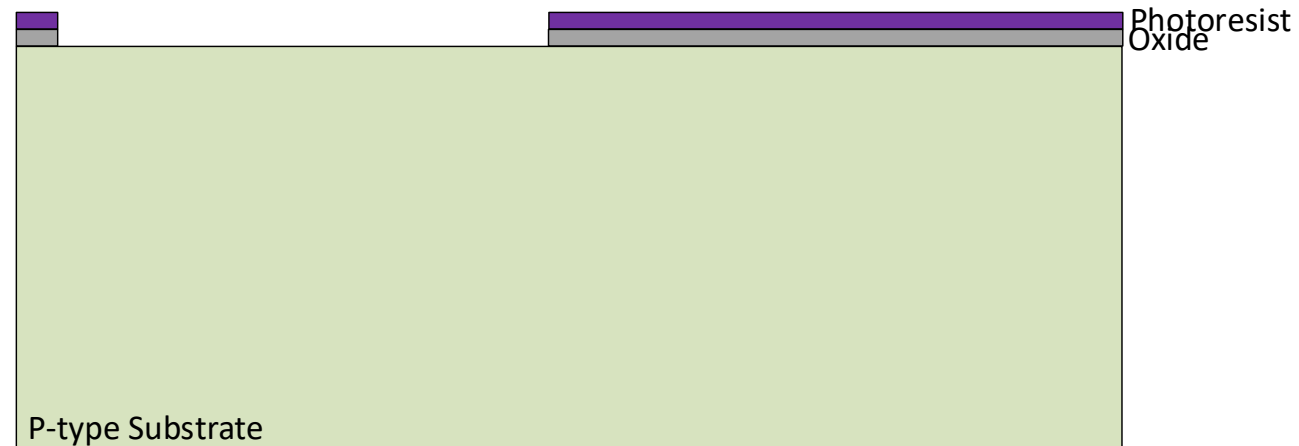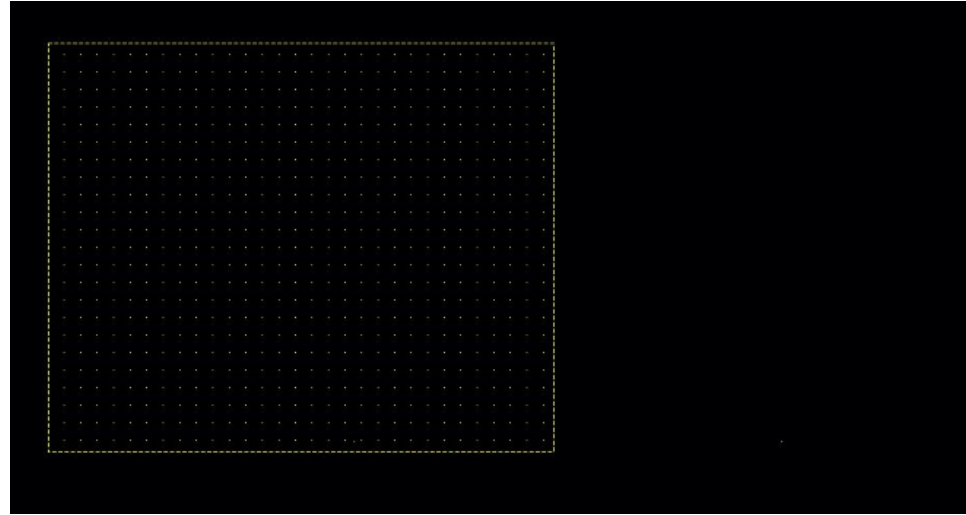
1.7: Create *Nwell* region
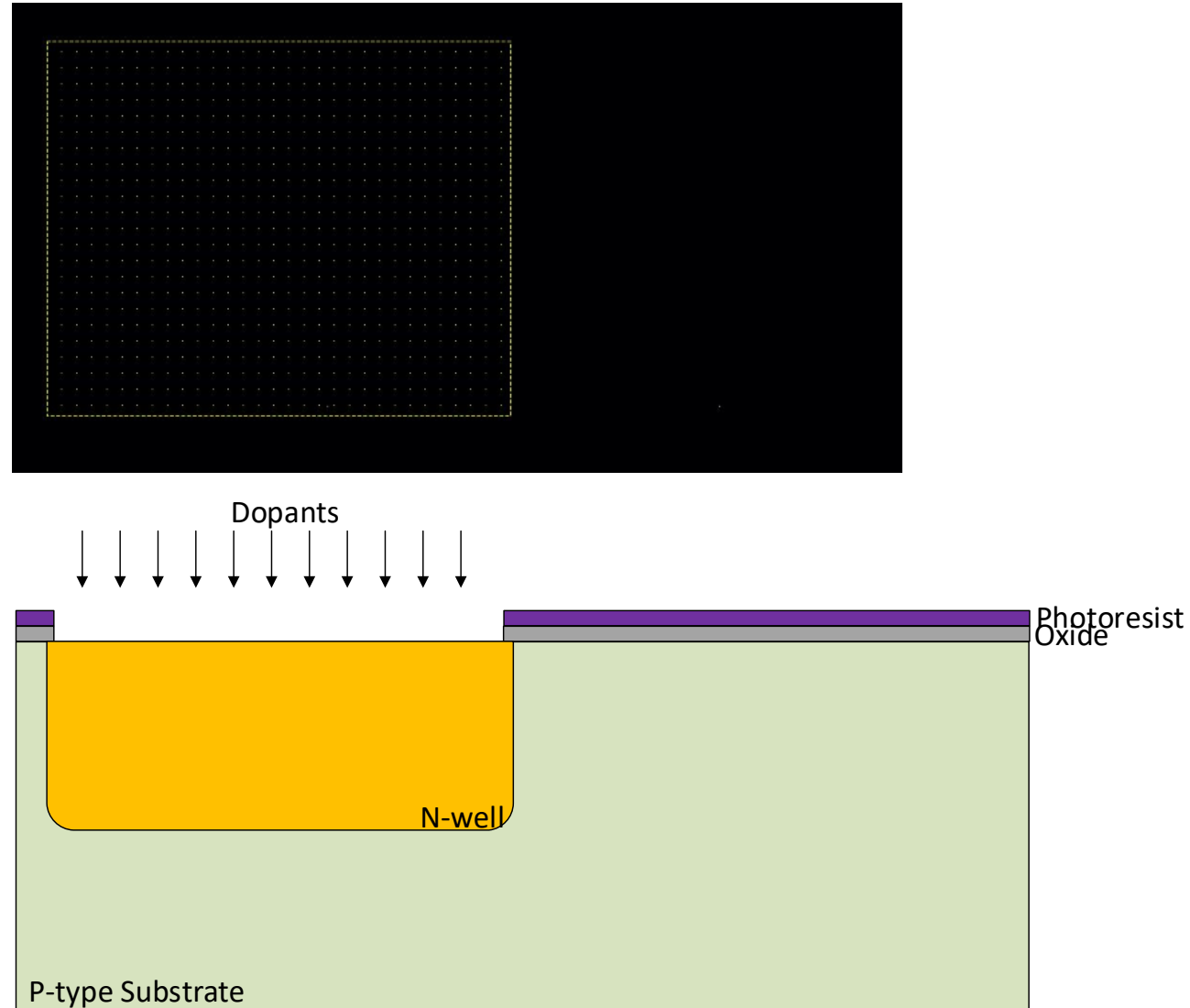
- Deposit N-type dopants and anneal for formation of N-well

2.1: Grow Field Oxide Outside Diffusion

- Grow field-oxide over regions outside transistor and contact areas

Nitride

N-well

P-type Substrate
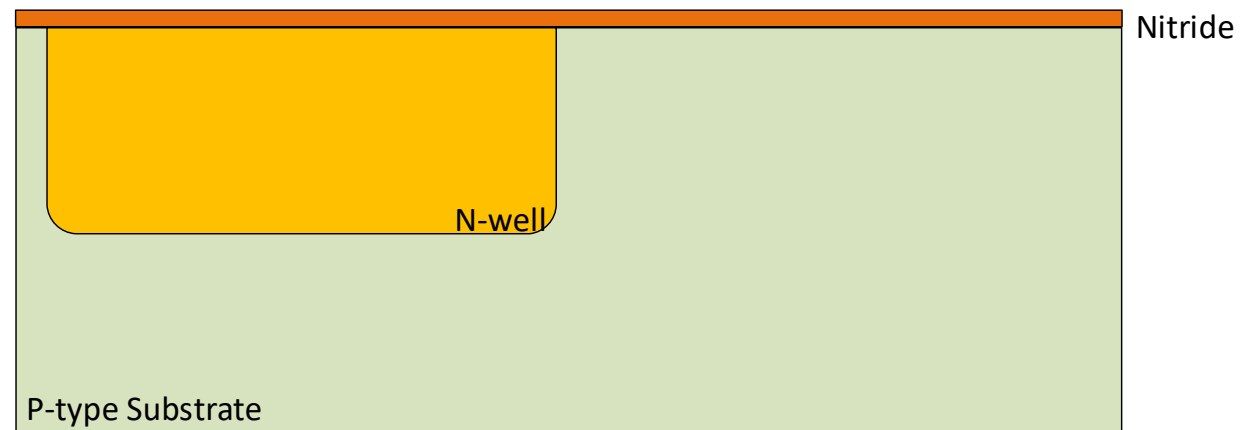
- First form a Si_3N_4 layer over silicon (prevent oxidation)

ELECTRICAL & COMPUTER
ENGINEERING

2.2: Grow Field Oxide Outside Diffusion
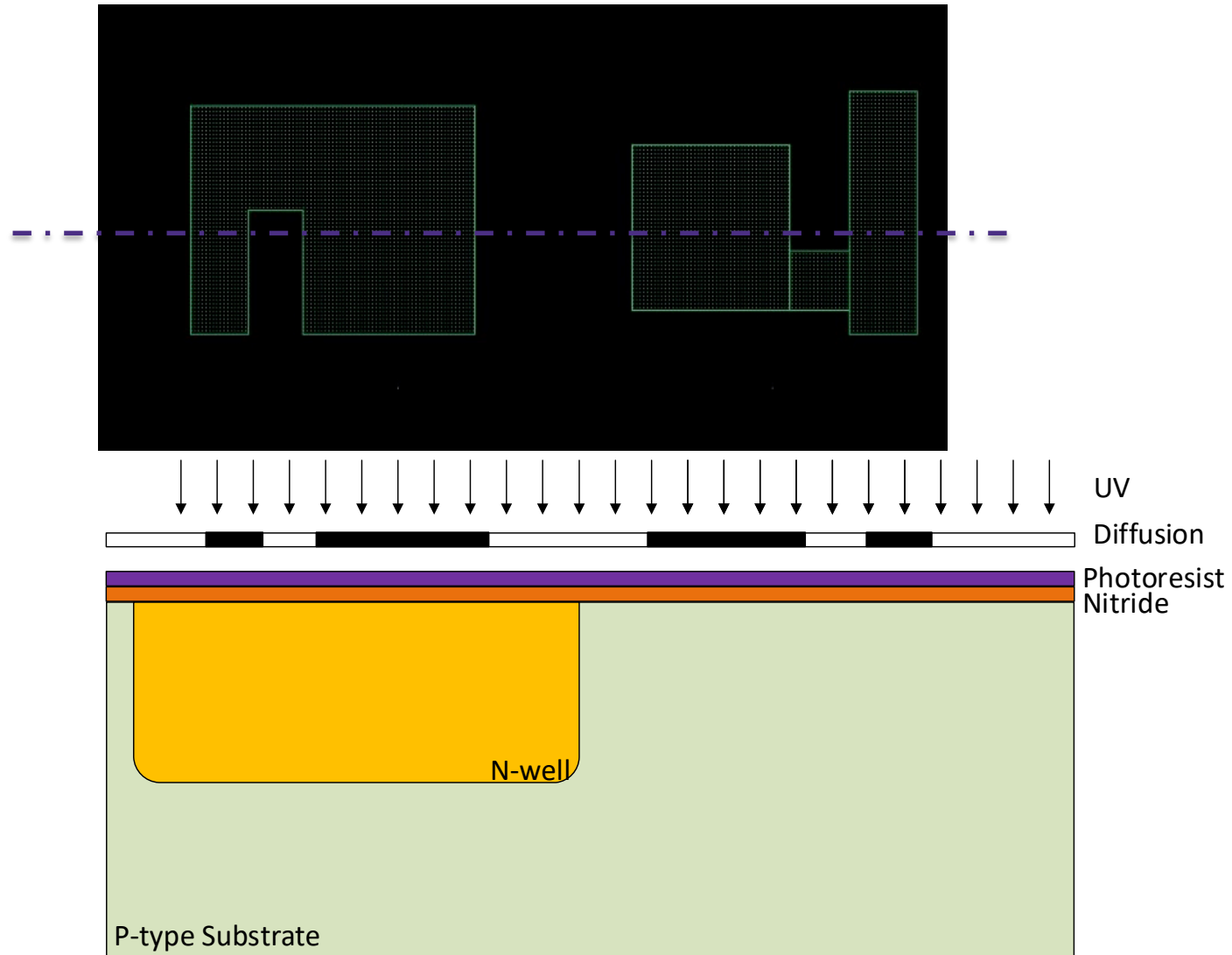
- Use OD* mask to selectively soften deposited photoresist

2.3: Grow Field Oxide Outside Diffusion
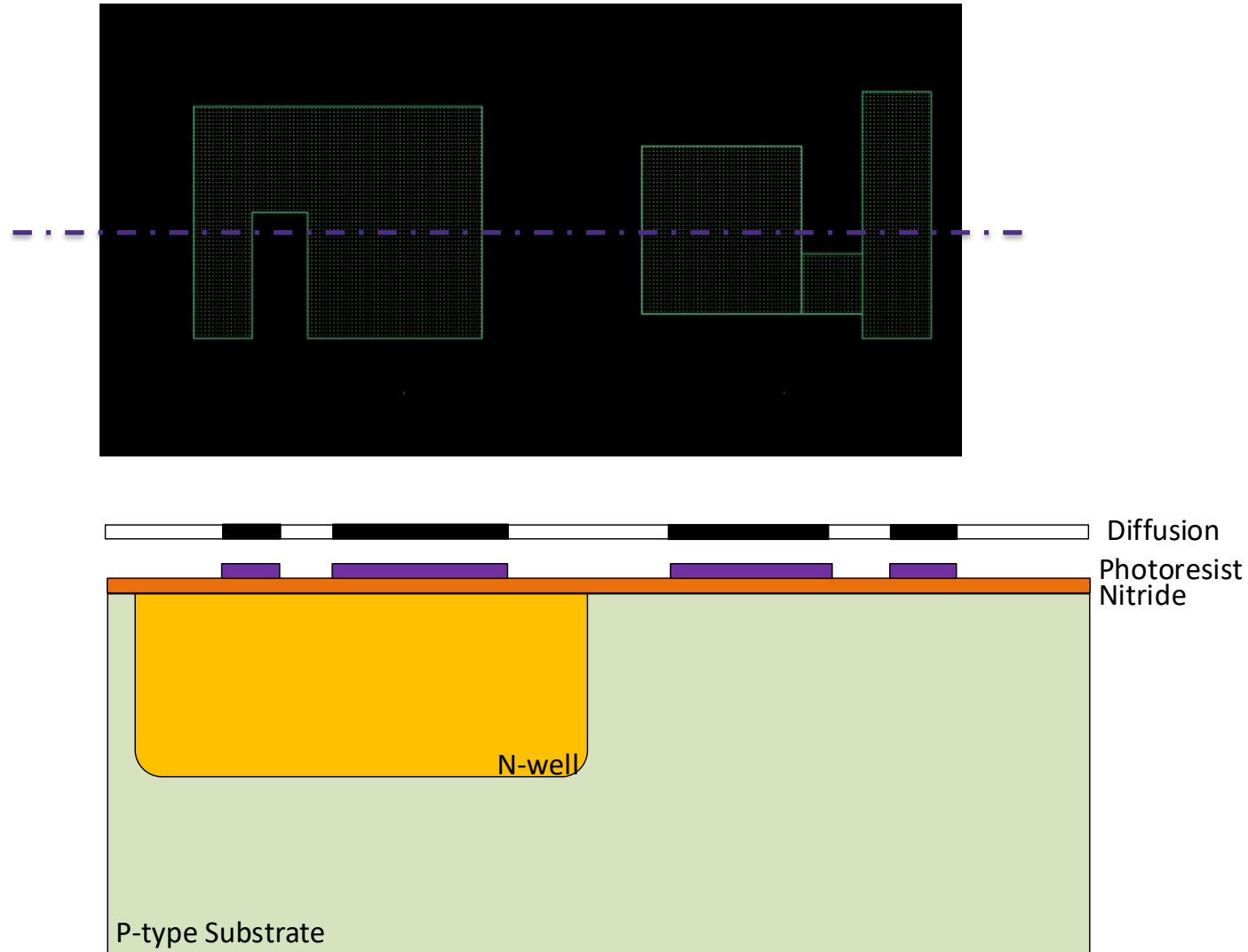
- Wash off softened photoresist

2.4: Grow Field Oxide Outside Diffusion

Nitride

N-well

P-type Substrate
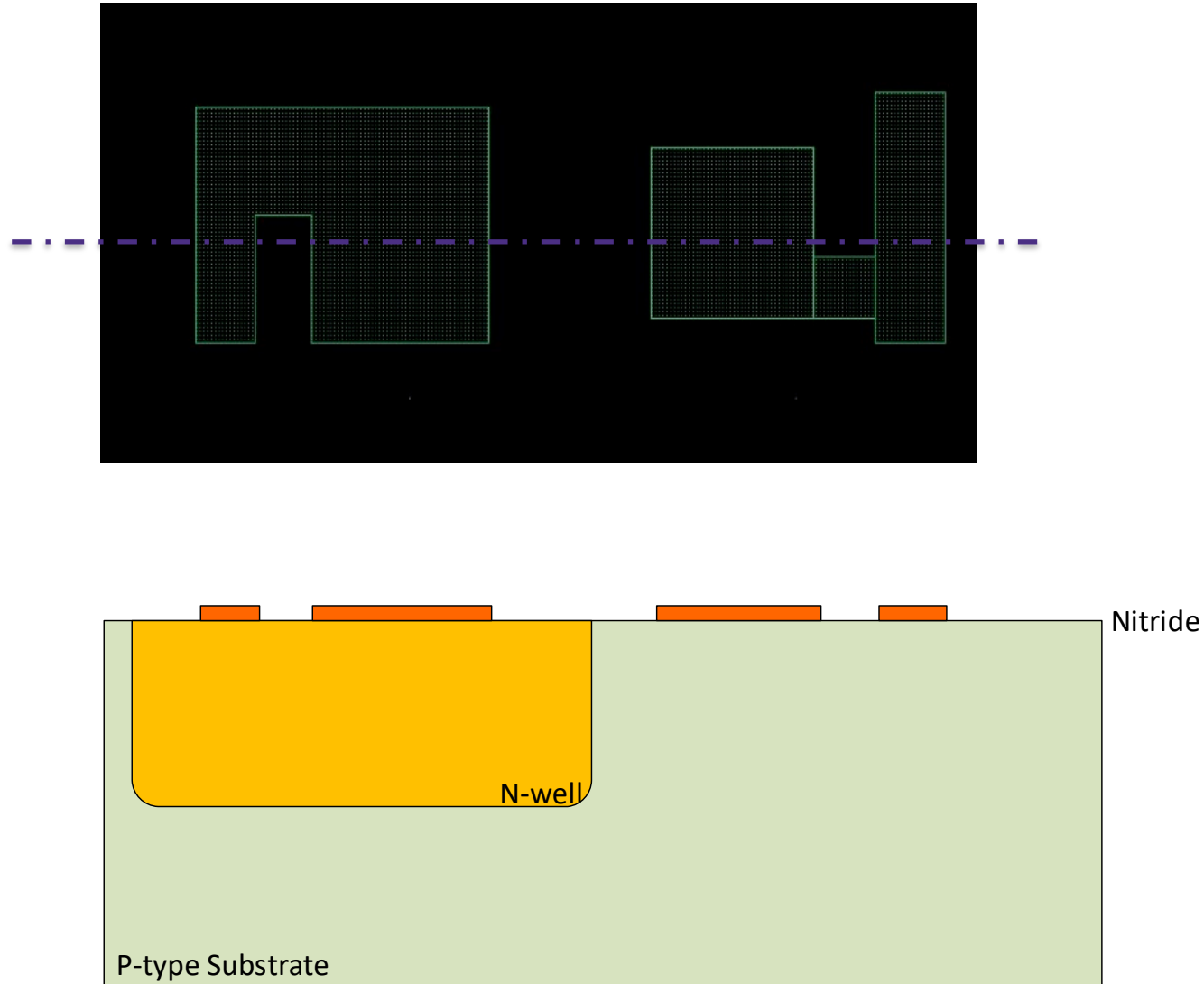
- *Piranha* etch photoresist

ELECTRICAL & COMPUTER
ENGINEERING

2.5: Grow Field Oxide Outside Diffusion

N-well

P-type Substrate
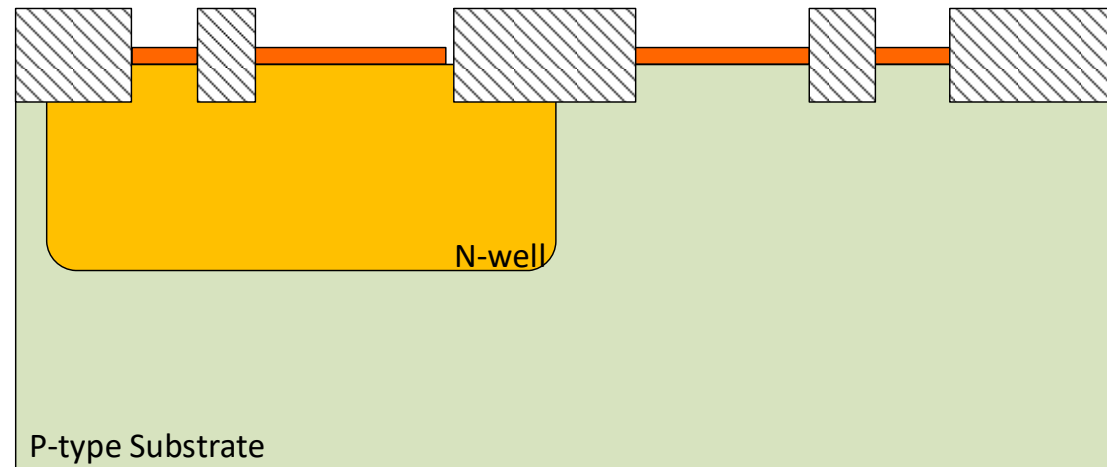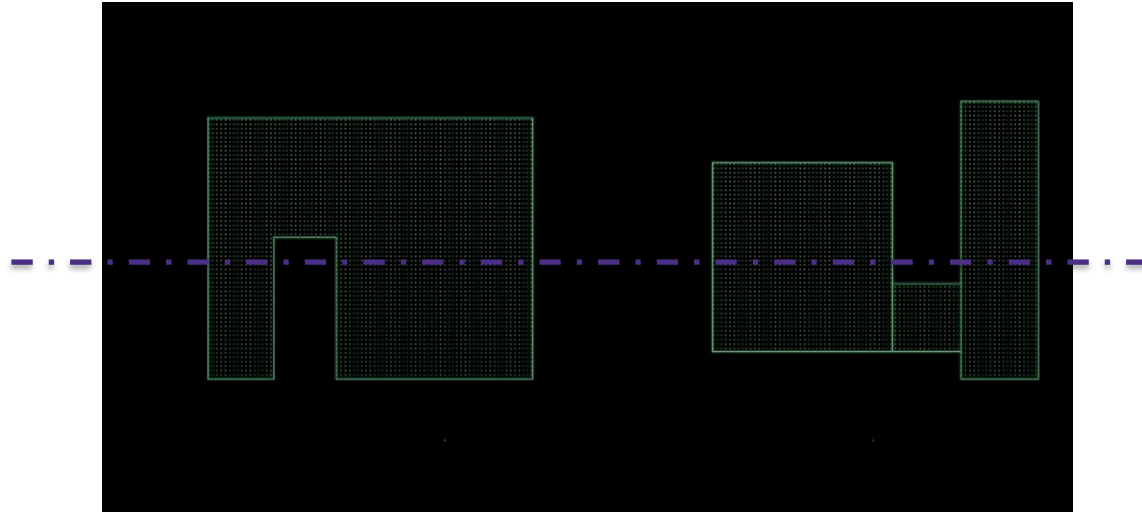
- Grow field-oxide over regions outside transistor and contact areas.

3:Build Polysilicon Gate

- Build the gate using polycrystalline silicon (or Polysilicon, or poly)

N-well

P-type Substrate

ELECTRICAL & COMPUTER ENGINEERING

3.1:Build Polysilicon Gate

Thin Oxide

N-well

P-type Substrate
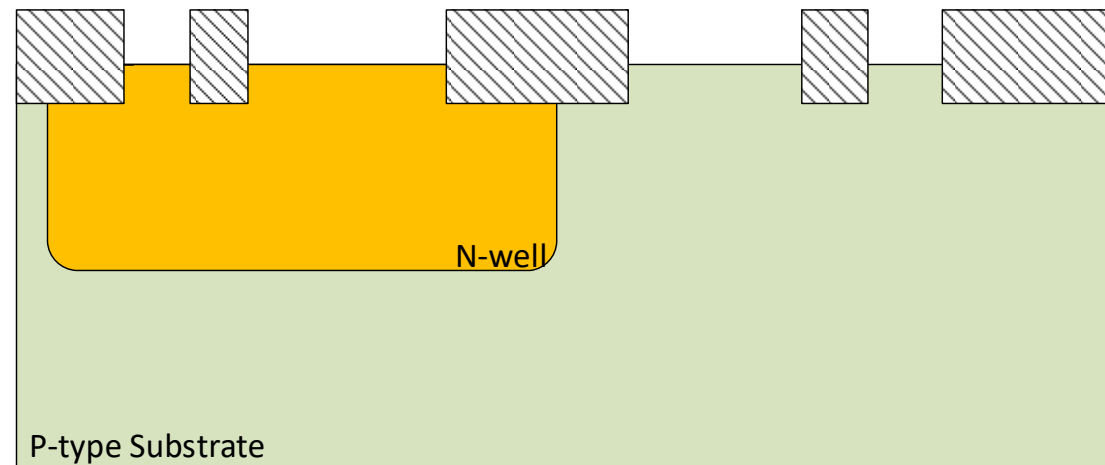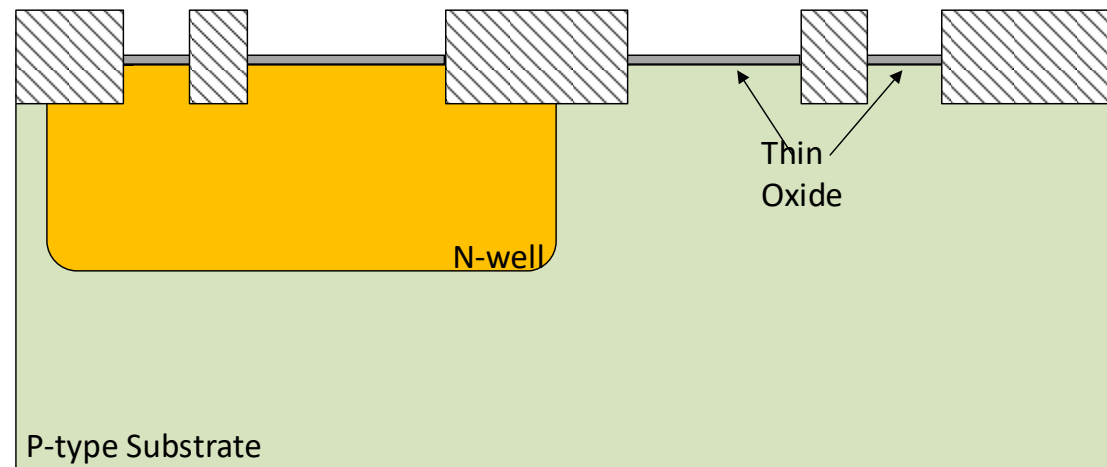
- Grow gate-oxide

3.1:Build Polysilicon Gate

Great, but why do I **need** field oxide in the first place??!

Thin Oxide

N-well

P-type Substrate
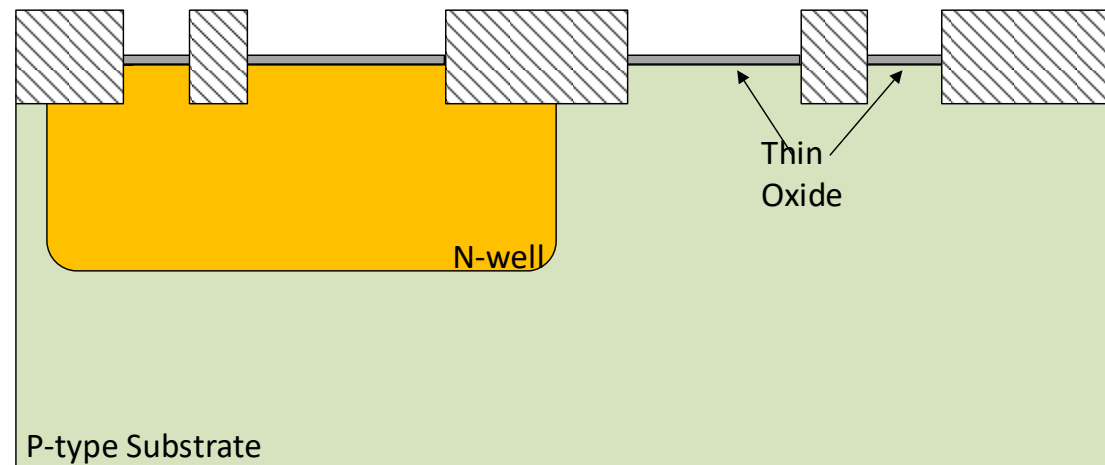
- Grow gate-oxide

3.2: Build Polysilicon Gate

N-well

Thin
Oxide

P-type Substrate
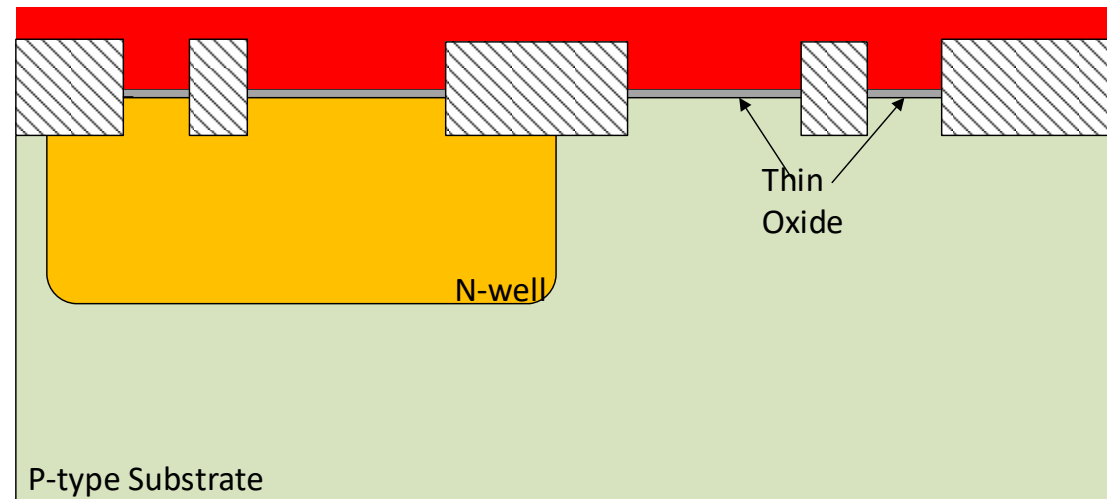
- Deposit Poly

3.3:Build Polysilicon Gate

Thin Oxide

N-well

P-type Substrate
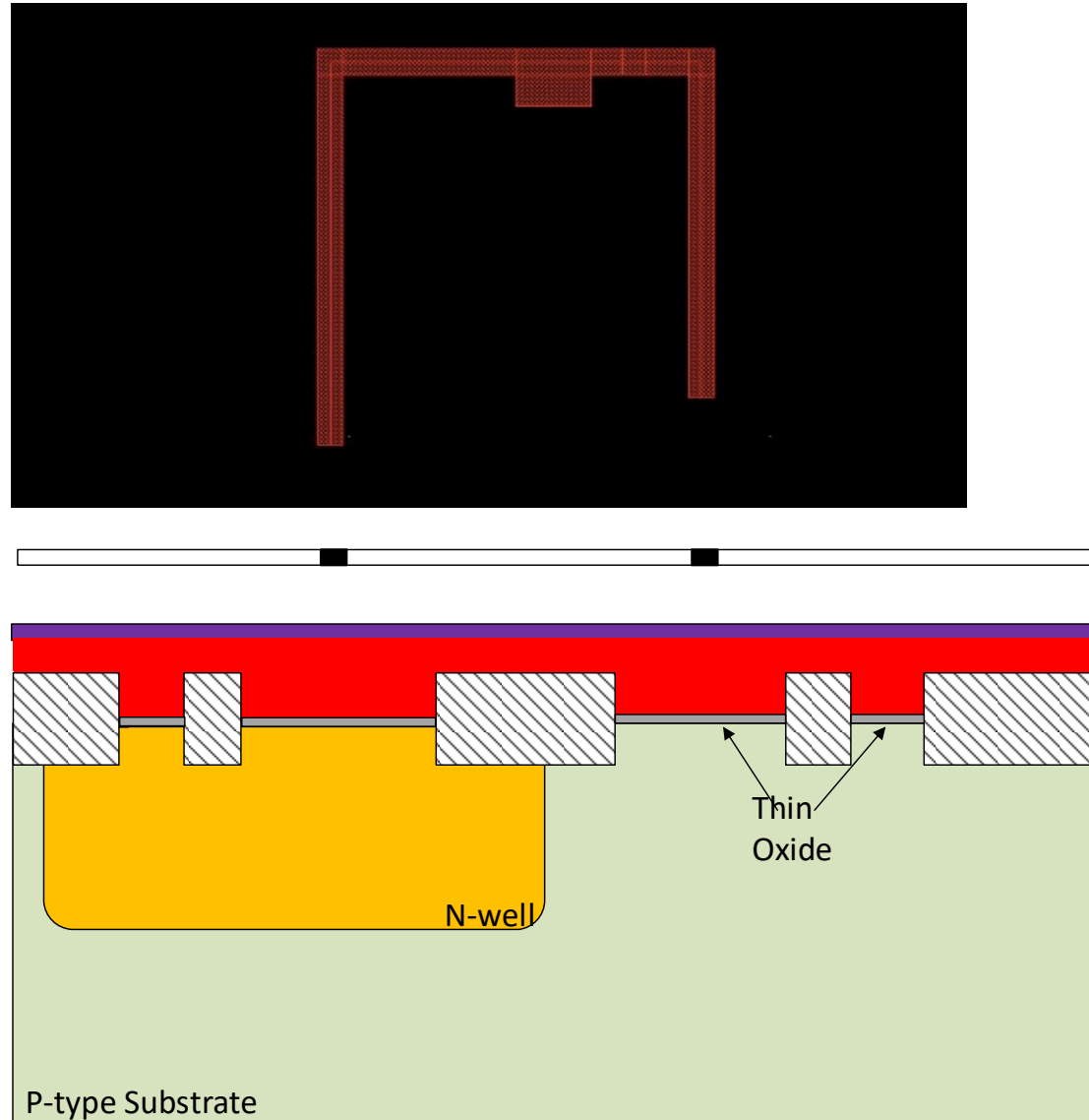
- Develop photoresist using PO mask

ELECTRICAL & COMPUTER ENGINEERING

3.4:Build Polysilicon Gate

Thin
Oxide

N-well

P-type Substrate
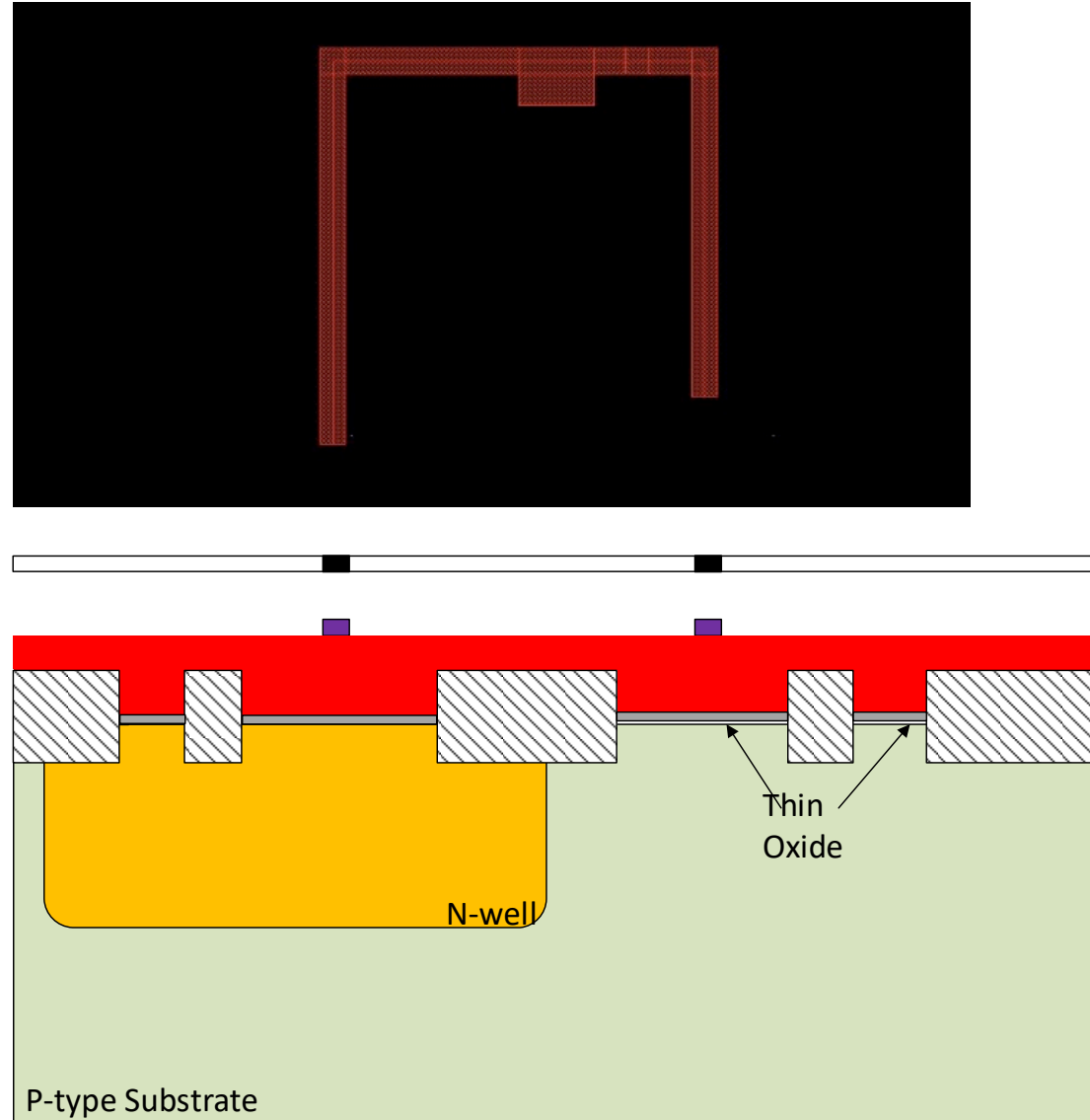
- Etch away softened photoresist

3.5:Build Polysilicon Gate

Thin
Oxide

N-well

P-type Substrate
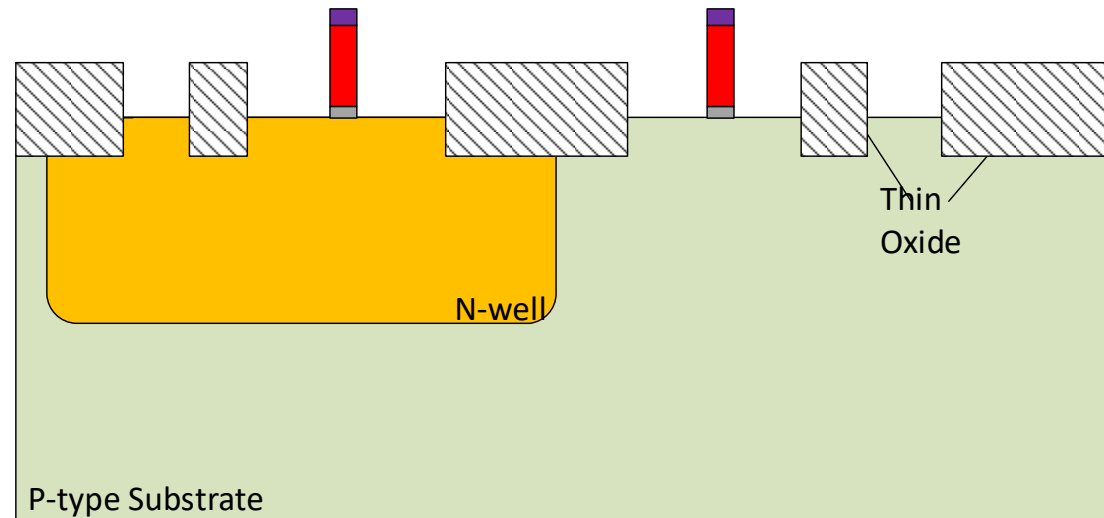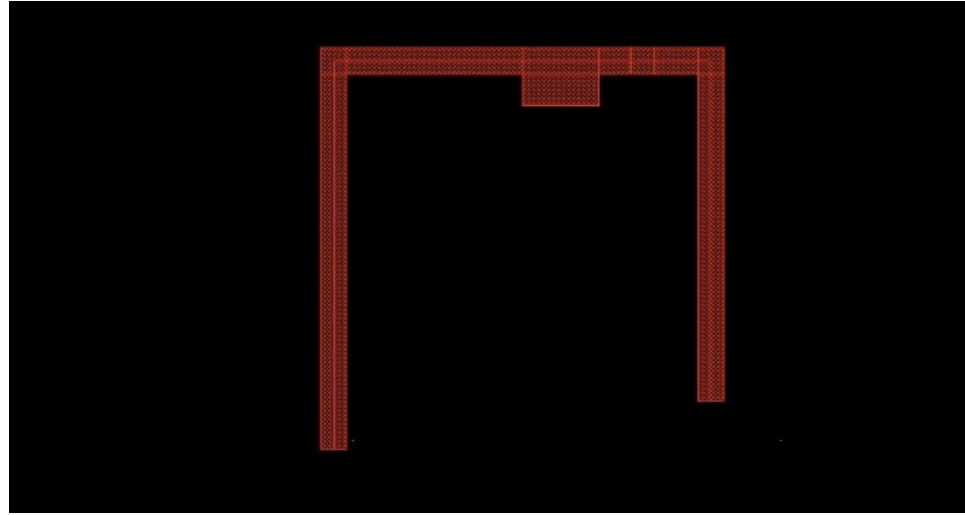
- Etch away softened photoresist

3.6:Build Polysilicon Gate

N-well

P-type Substrate
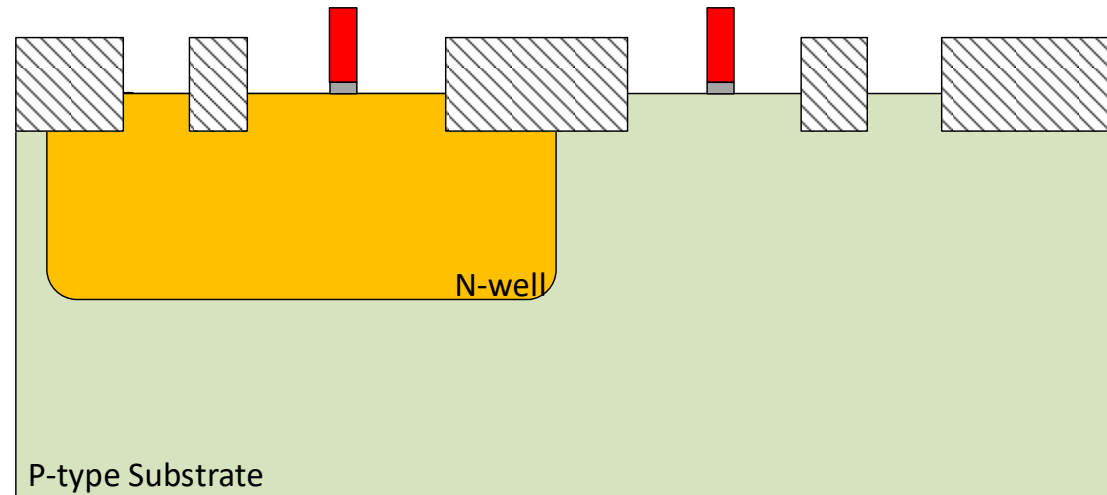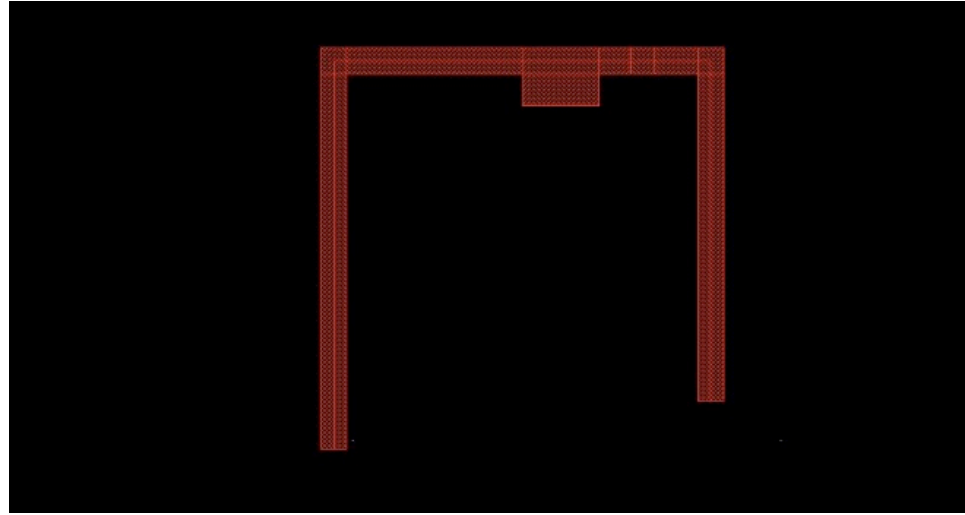
- Etch away exposed polysilicon

ELECTRICAL & COMPUTER ENGINEERING

4:Build PMOS, Substrate Contact

N-well

P-type Substrate
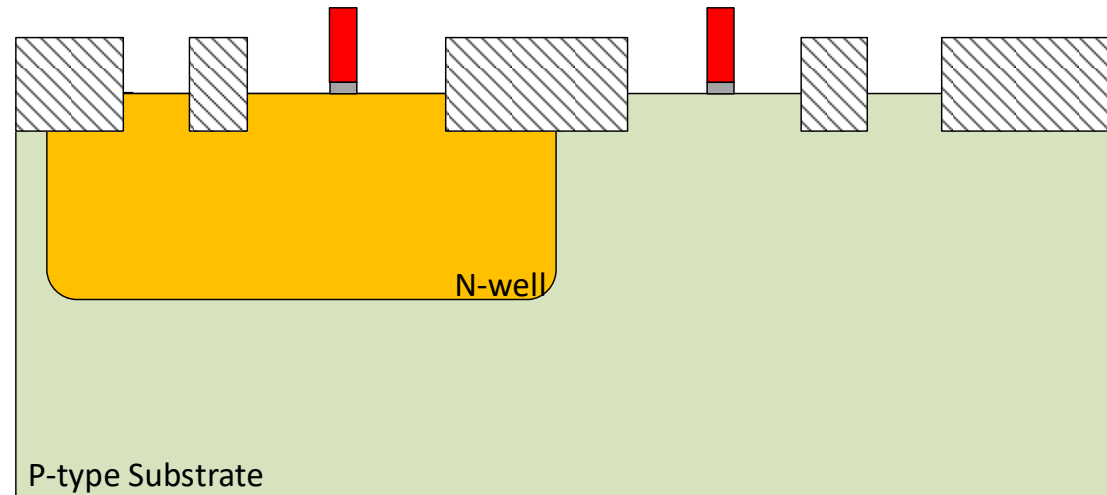
4.1:Build PMOS, Substrate Contact

N-well

P-type Substrate

- Deposit photoresist

4.2:Build PMOS, Substrate Contact
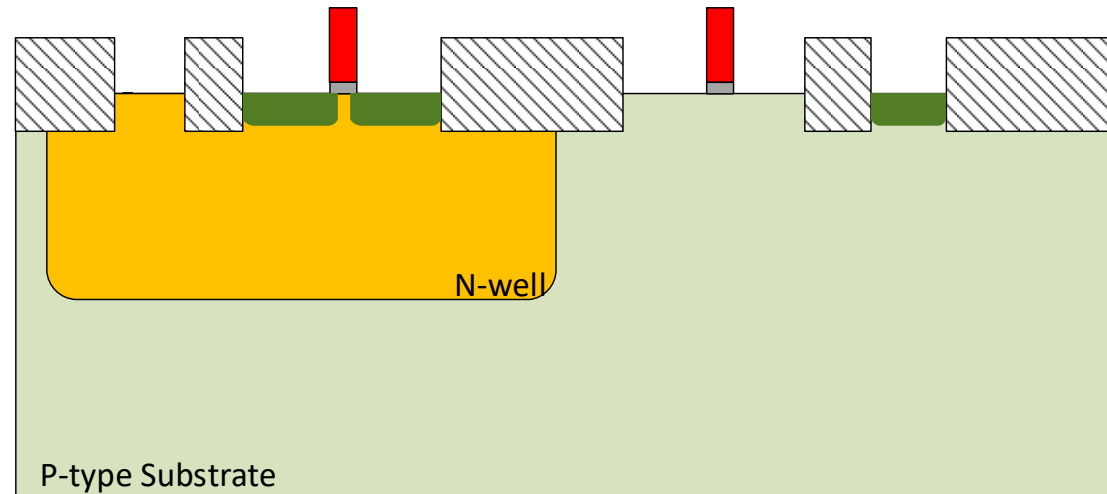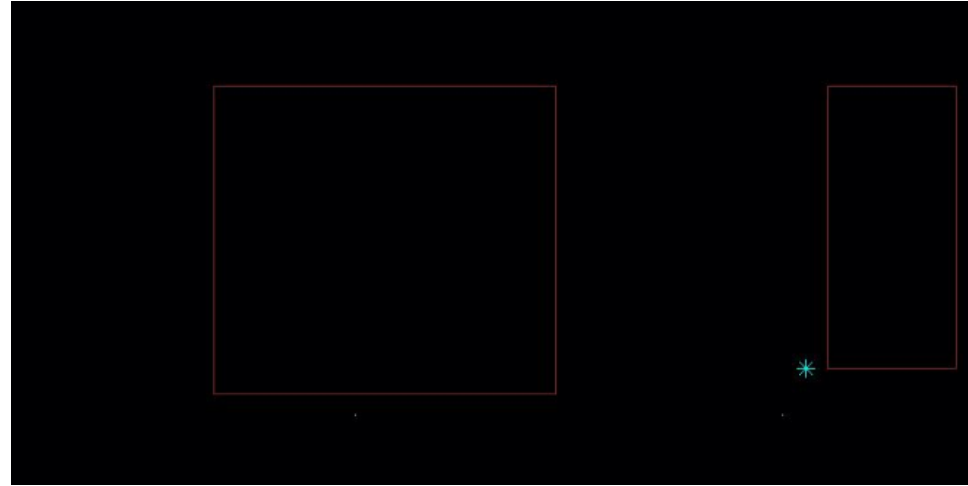

- Use PP mask to develop photoresist

ELECTRICAL & COMPUTER ENGINEERING
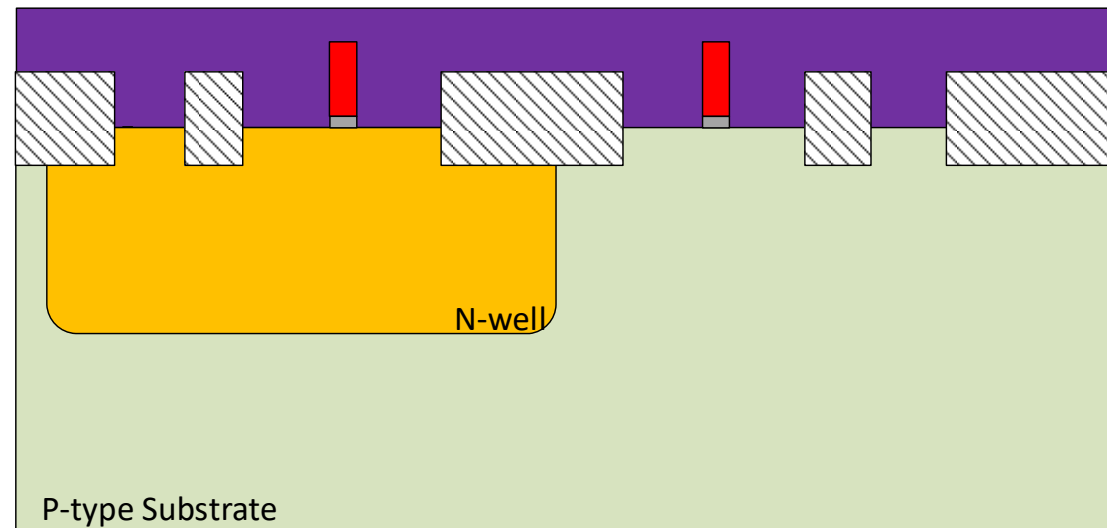
4.2:Build PMOS, Substrate Contact
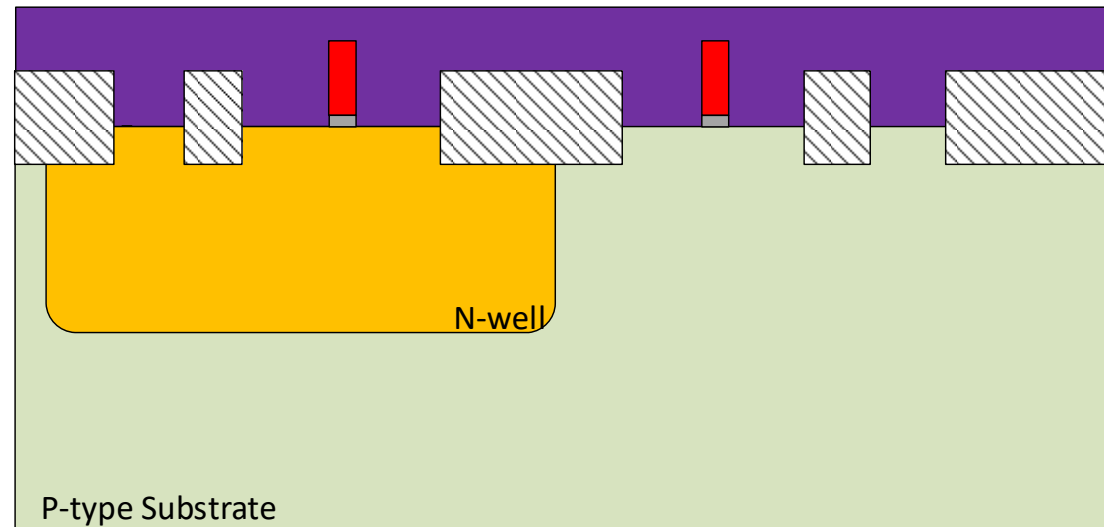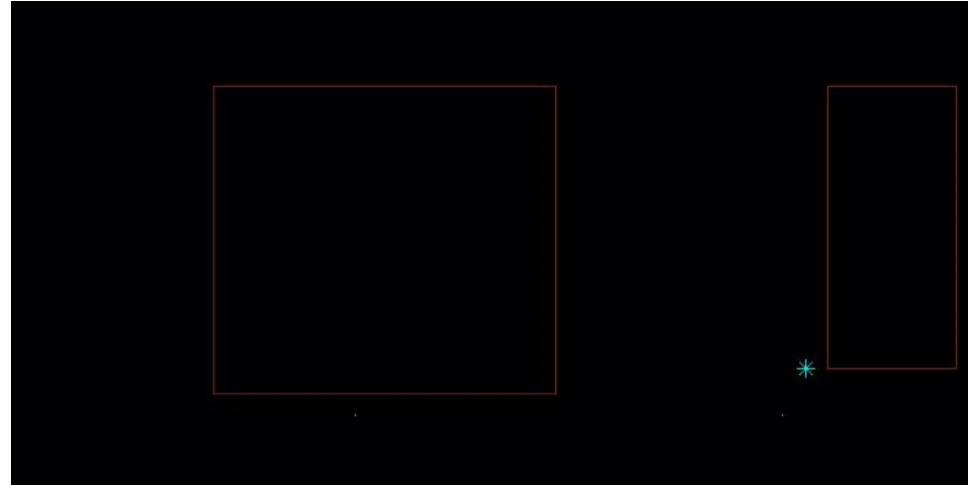
- Use PP mask to develop photoresist

4.2:Build PMOS, Substrate Contact

- Use PP mask to develop photoresist

ELECTRICAL & COMPUTER ENGINEERING
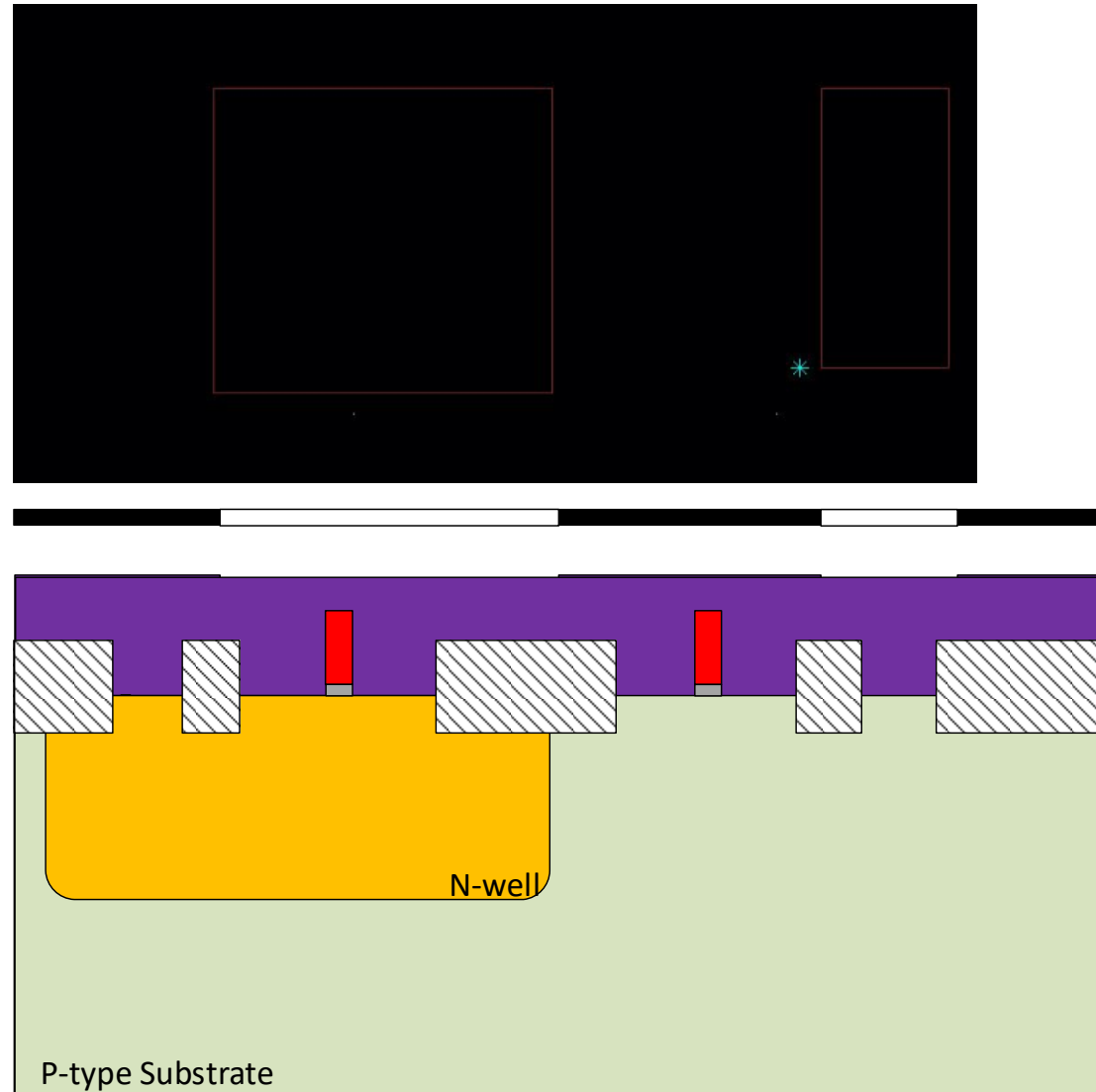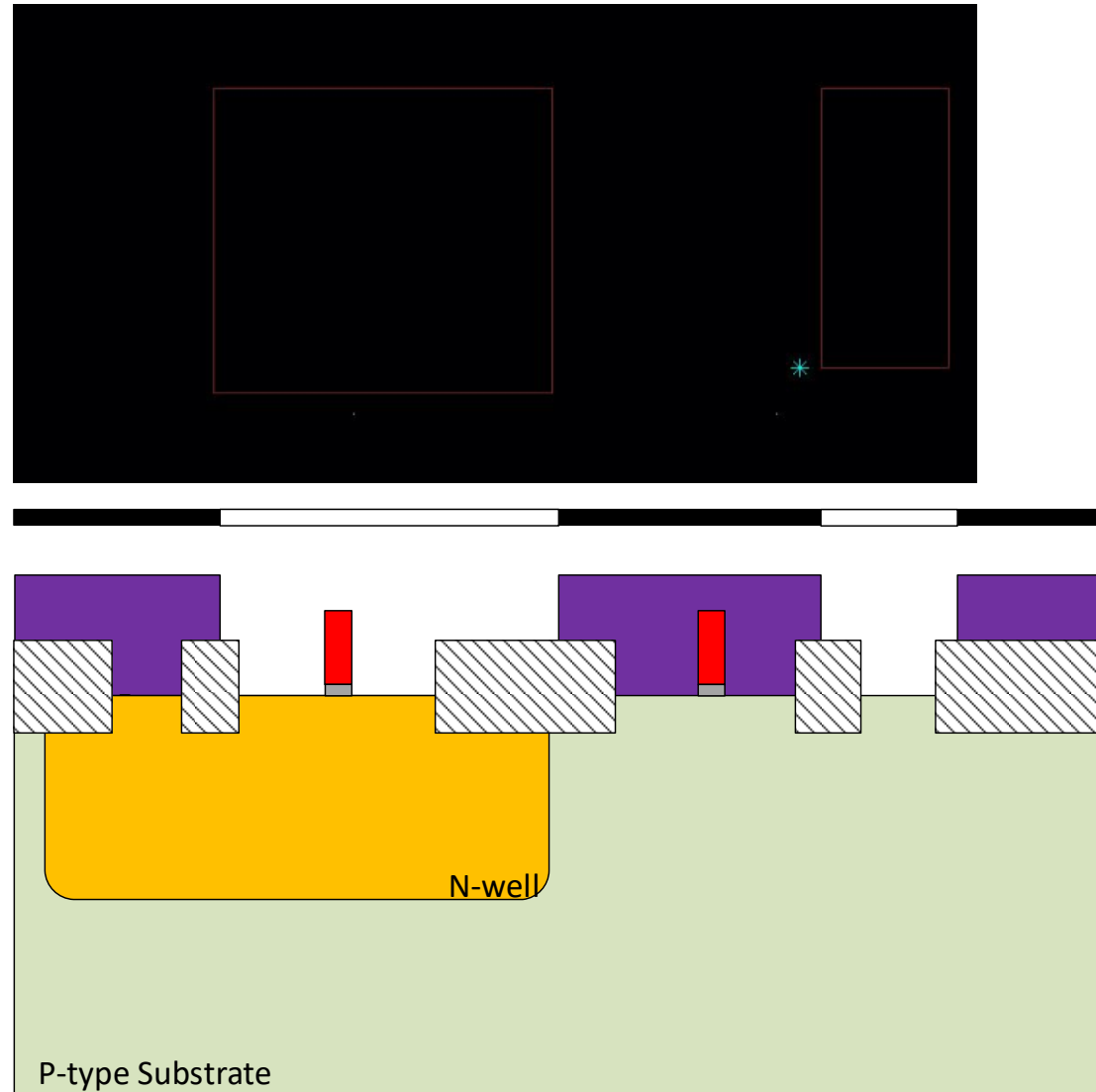
4.3:Build PMOS, Substrate Contact

Self-aligned gate : Implant n+/p+ after gate to automatically form gate exactly where it is needed
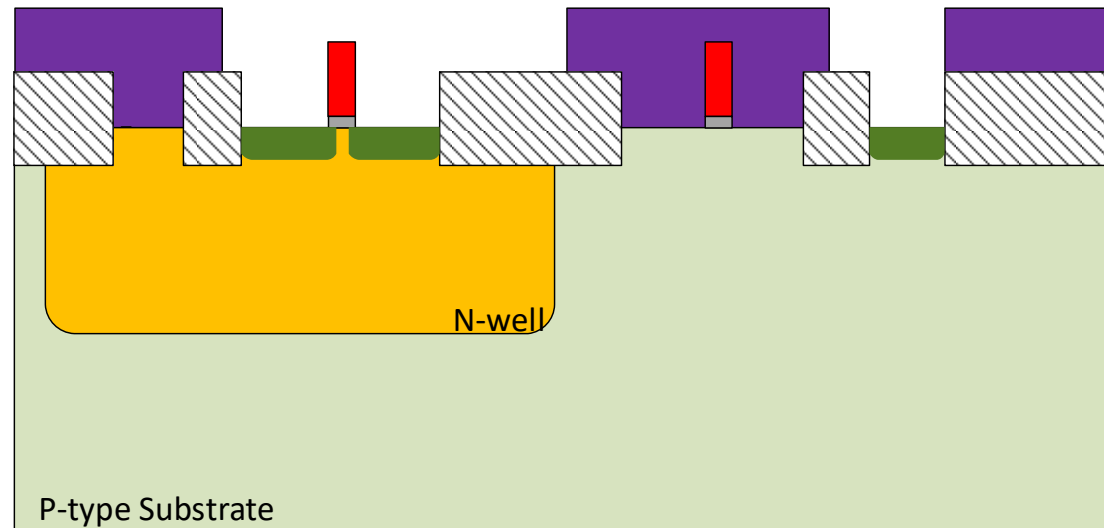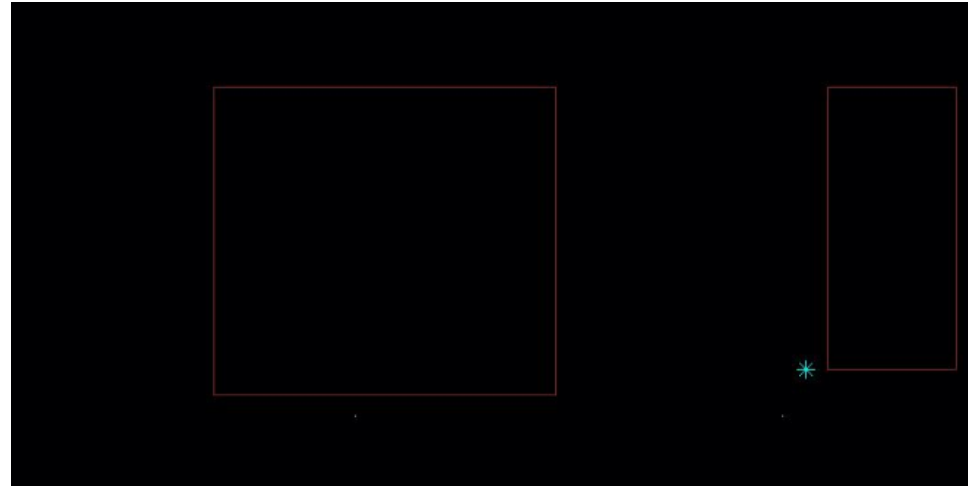
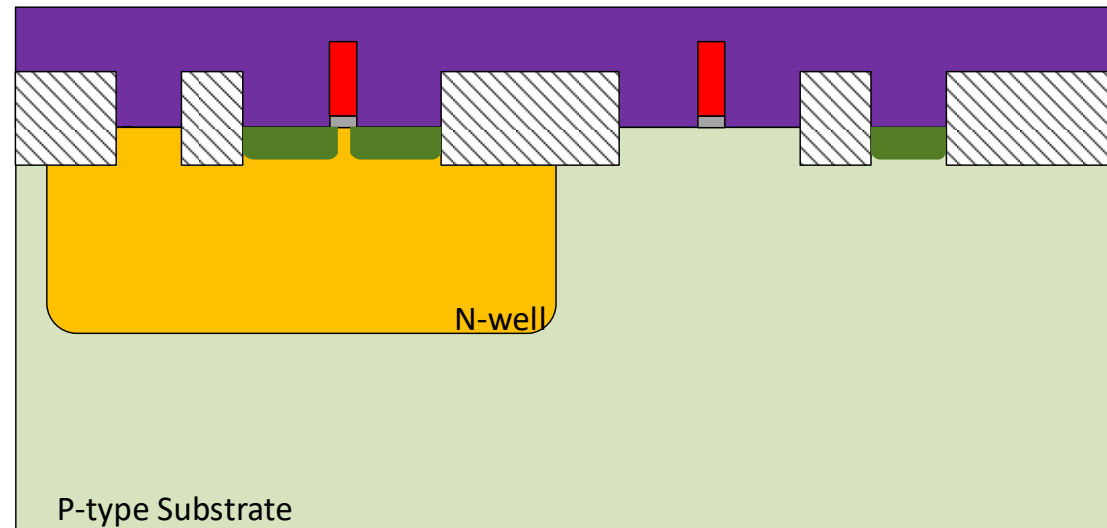- Ion Implantation to create P+ regions for S/D and substrate contact

ELECTRICAL & COMPUTER ENGINEERING

4.4:Build PMOS, Substrate Contact

- Wash off photoresist

5:Build NMOS, Body Contact

N-well

P-type Substrate
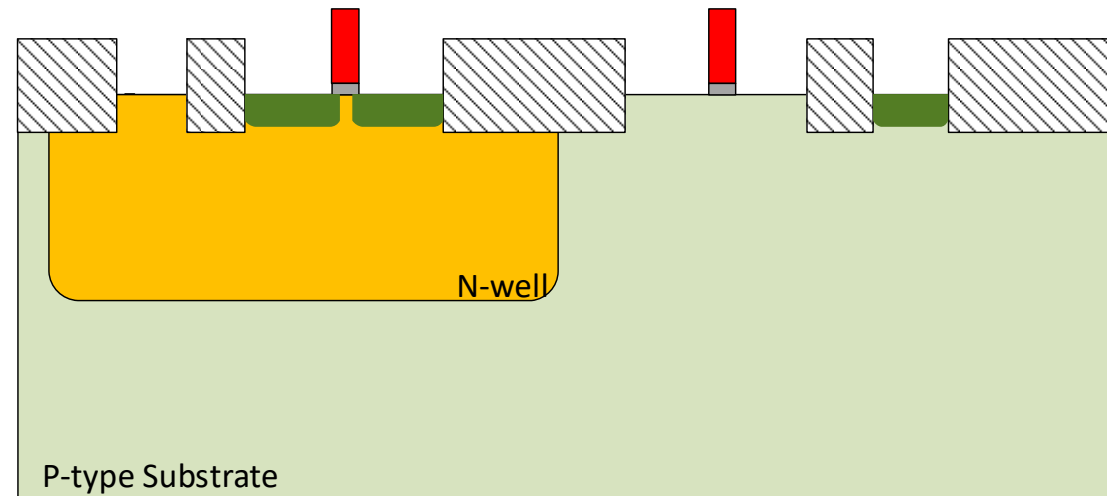
- Next, we deposit N+ to form the Nmos S/D and body contacts

W ELECTRICAL & COMPUTER ENGINEERING

5.1:Build NMOS, Body Contact

N-well

P-type Substrate

- Photoresist

ELECTRICAL & COMPUTER
ENGINEERING

5.2:Build NMOS, Body Contact

- Use NP mask to develop photoresist

ELECTRICAL & COMPUTER
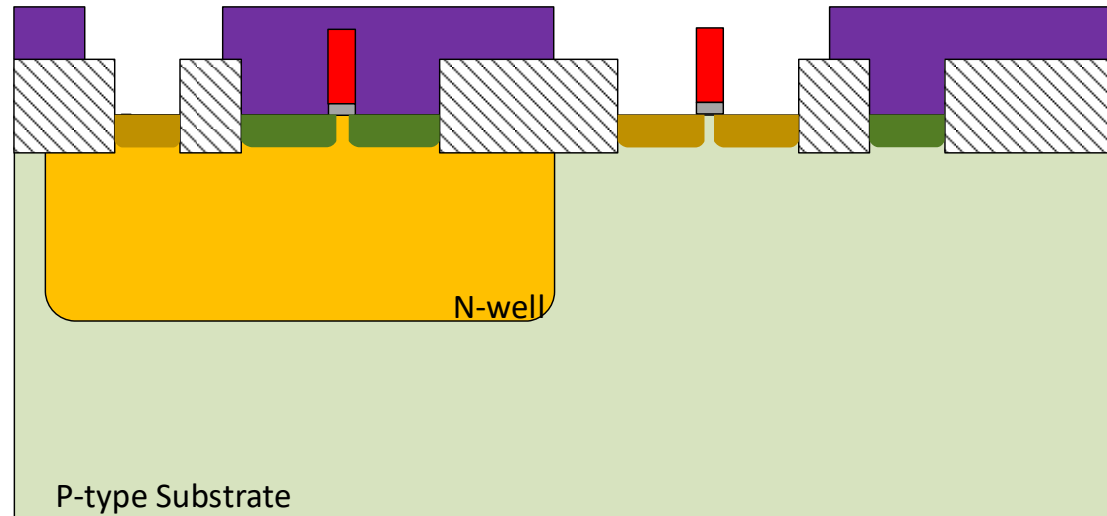ENGINEERING

5.2:Build NMOS, Body Contact
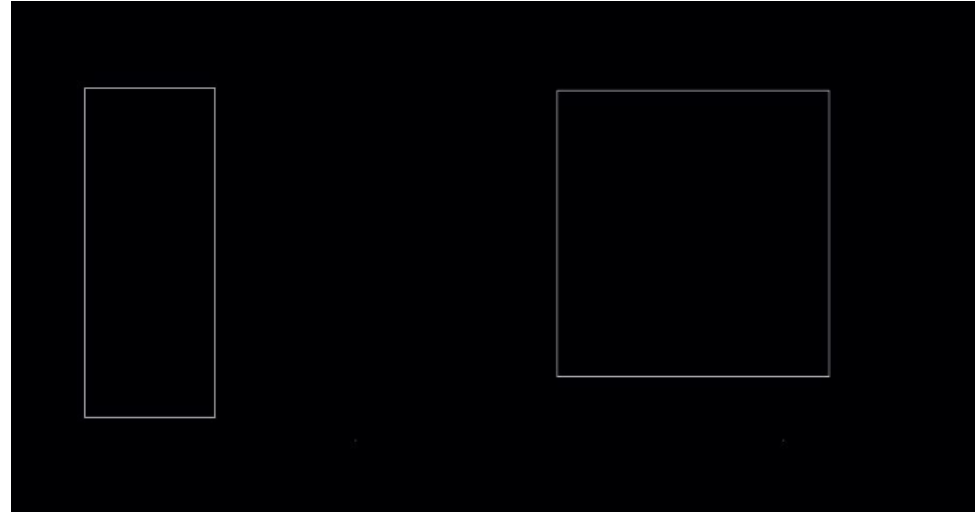

- Use NP mask to develop photoresist

5.2:Build NMOS, Body Contact
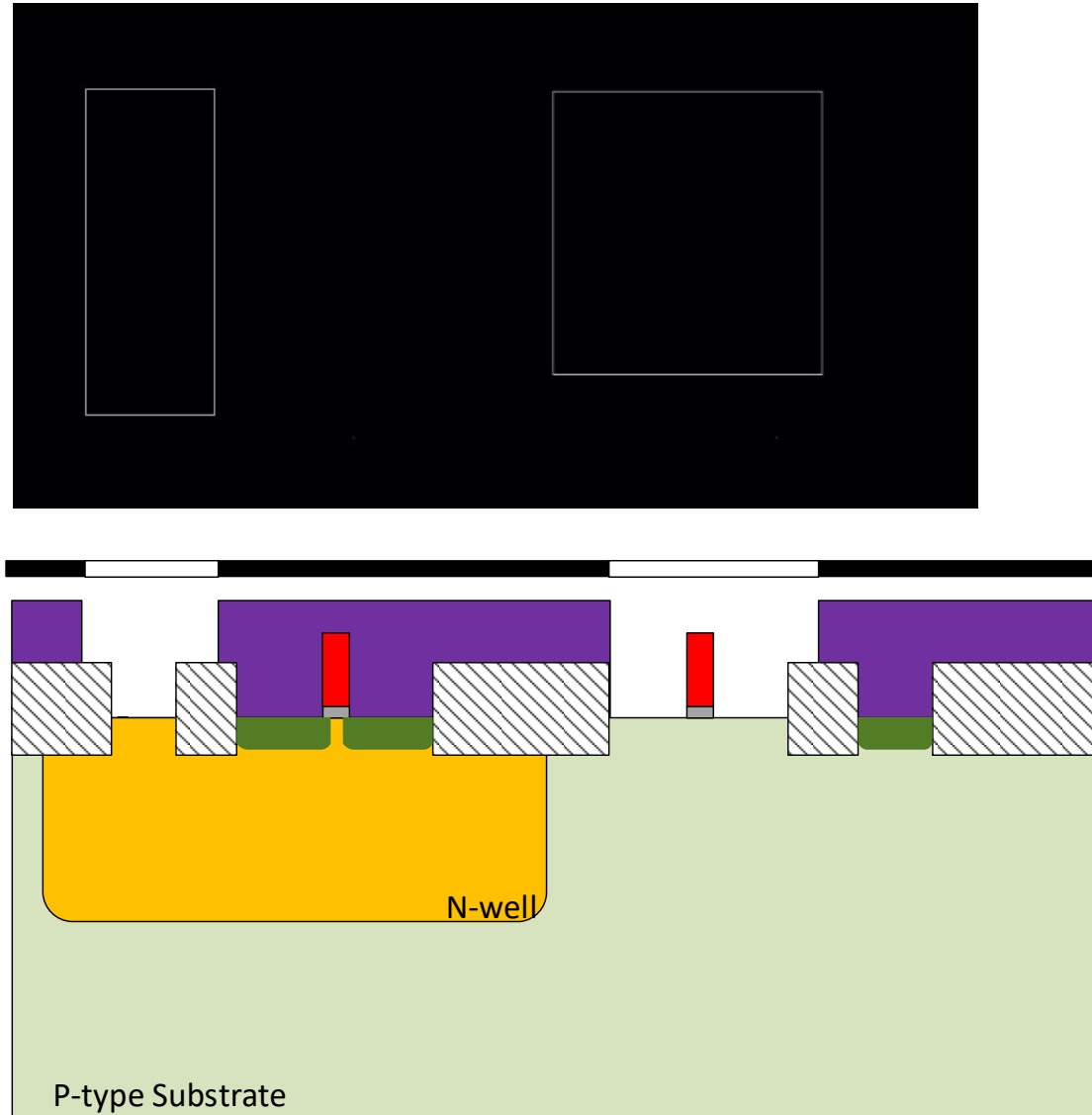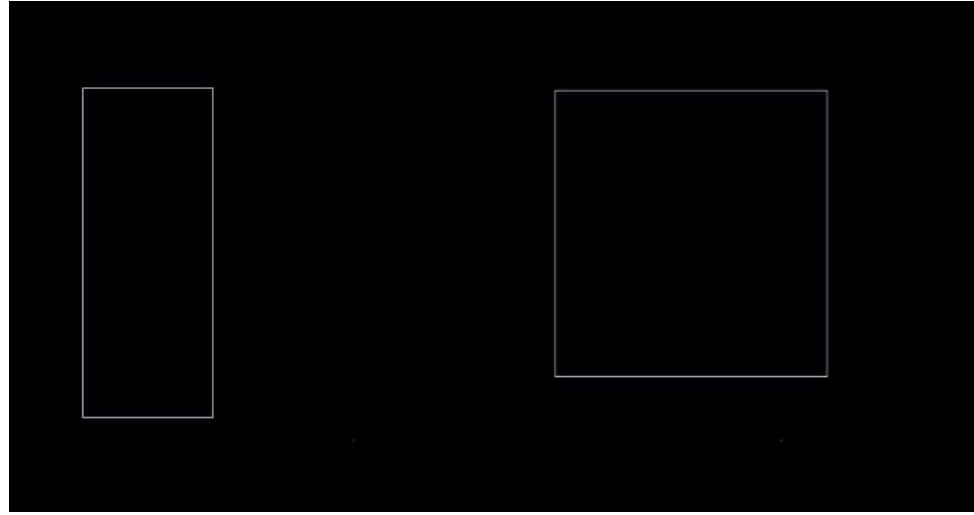

- Use NP mask to develop photoresist

ELECTRICAL & COMPUTER
ENGINEERING

5.3:Build NMOS, Body Contact

N-well

P-type Substrate

- Etch photoresist

ELECTRICAL & COMPUTER ENGINEERING

5.4:Build NMOS, Body Contact

P-type Substrate

N-well
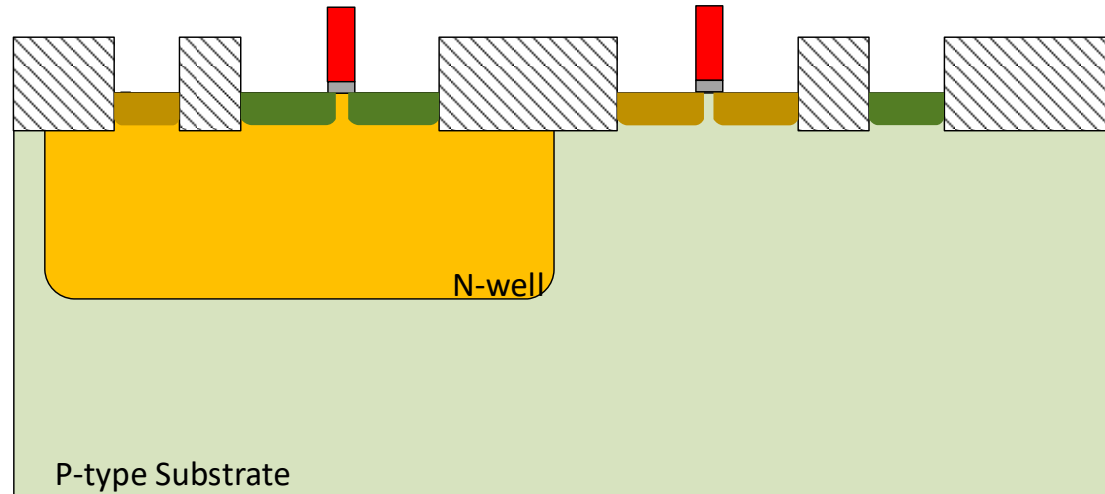
- Deposit N+, wash photoresist

6: Contacts to metal

P-type Substrate

N-well

- Deposit N+, wash photoresist

ELECTRICAL & COMPUTER ENGINEERING
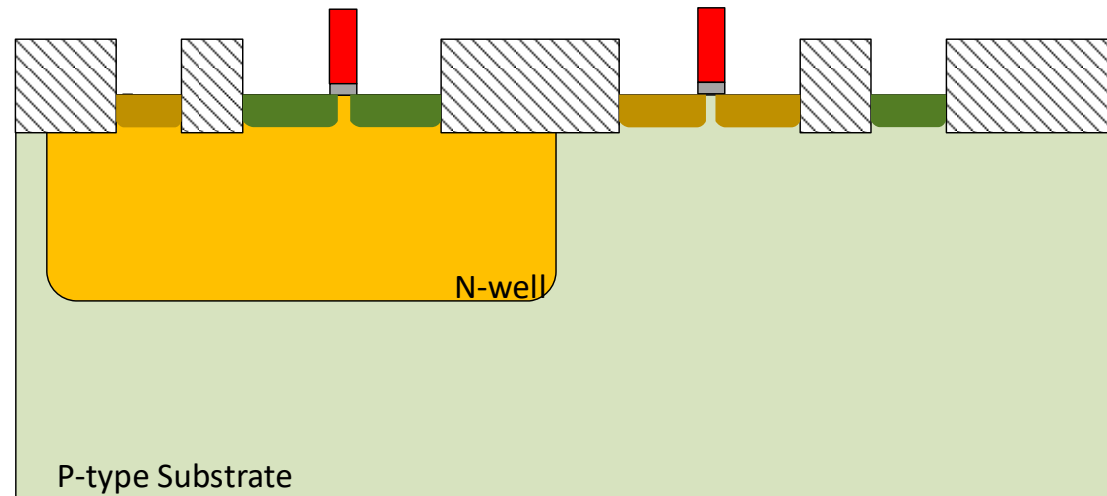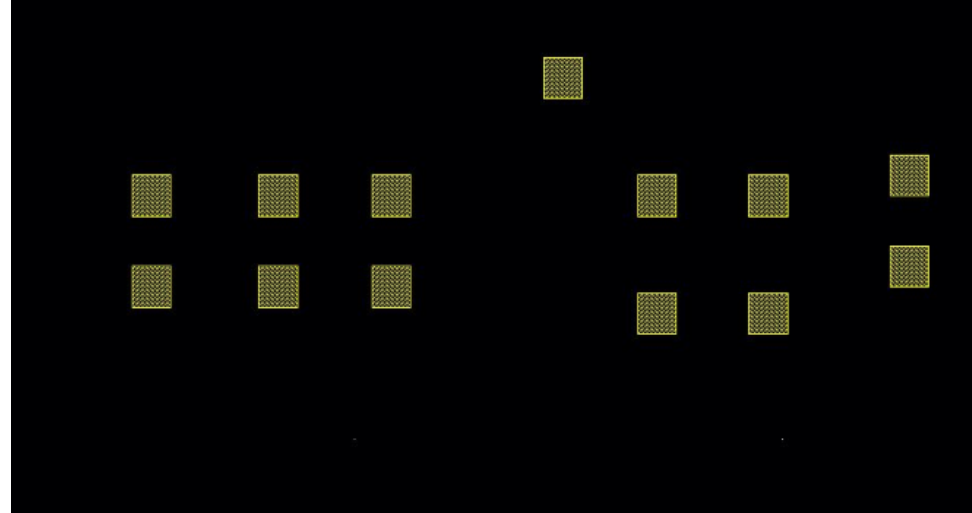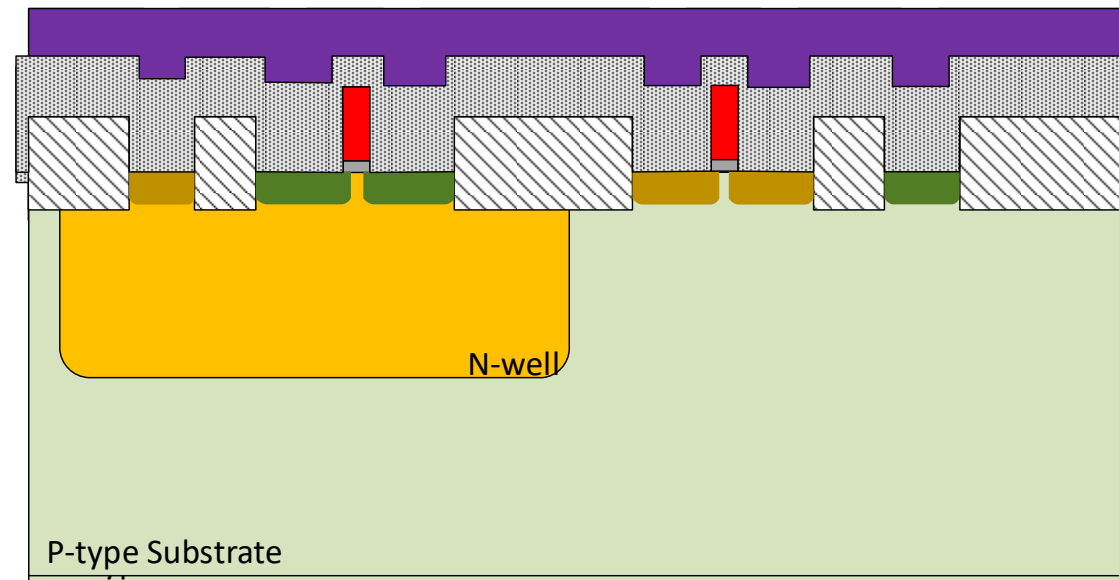
6.1: Contacts to metal
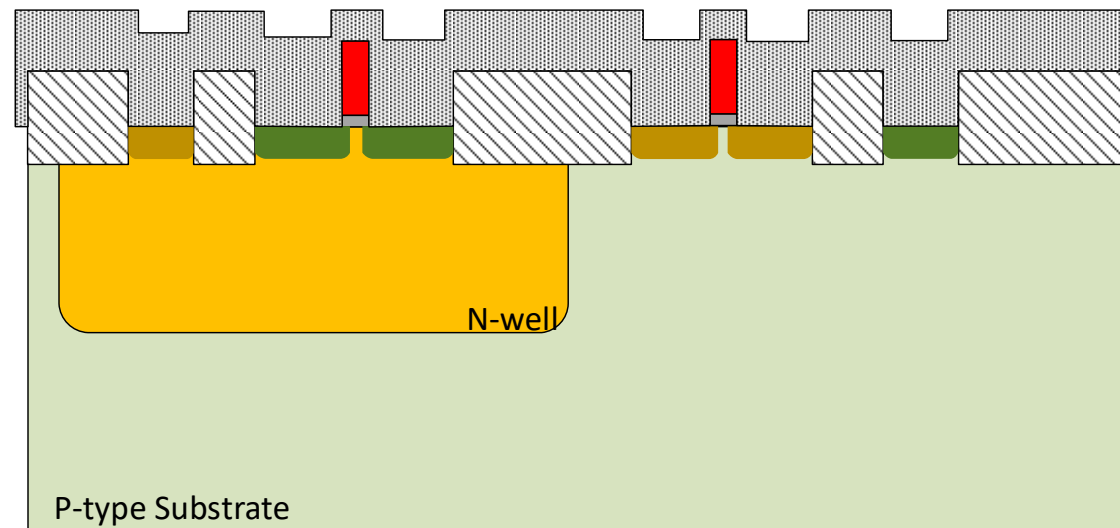
- Deposit oxide layer (metal-oxide-metal-oxide.... from here on)

6.2: Contacts to metal

What happened to PO contact?
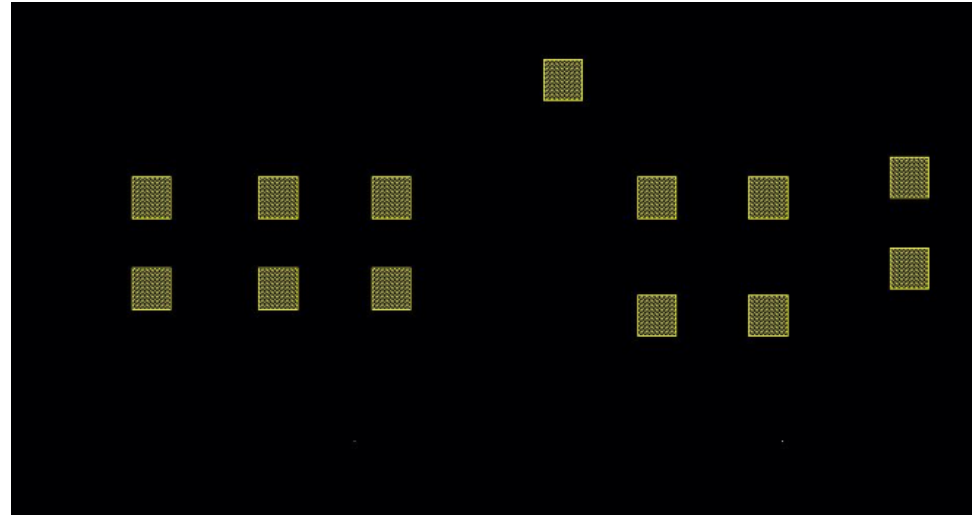
N-well

P-type Substrate

6.2: Contacts to metal

What happened to PO contact?
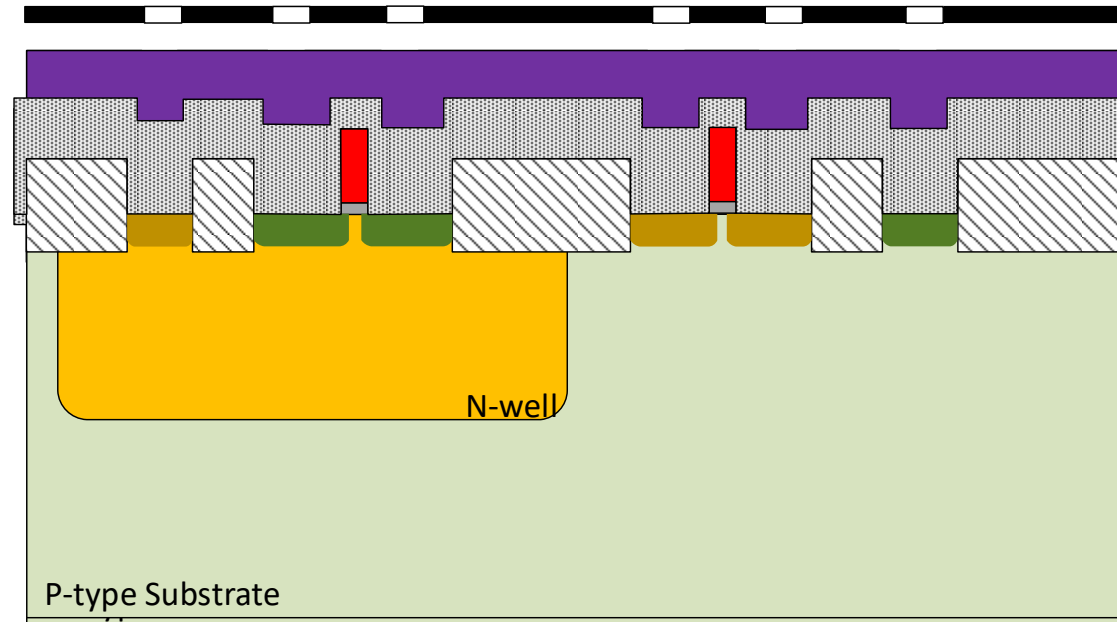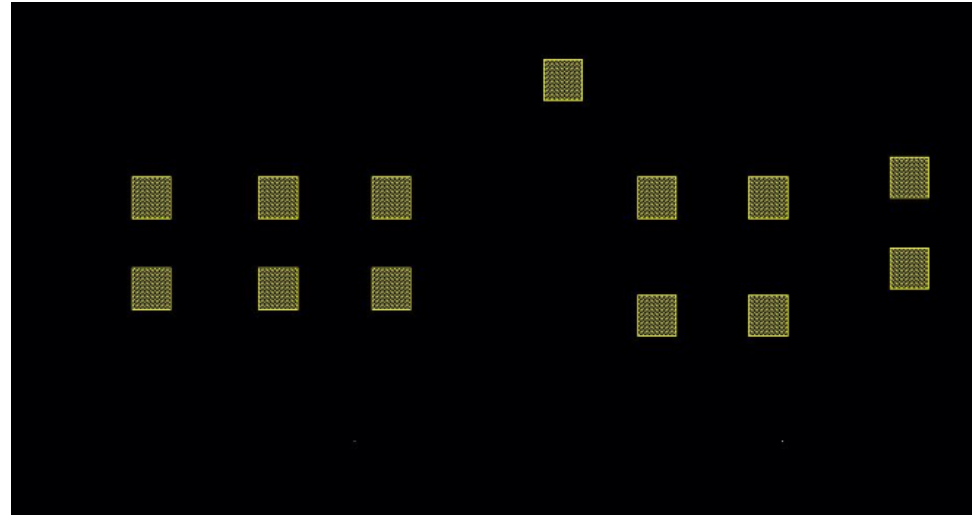
N-well

P-type Substrate
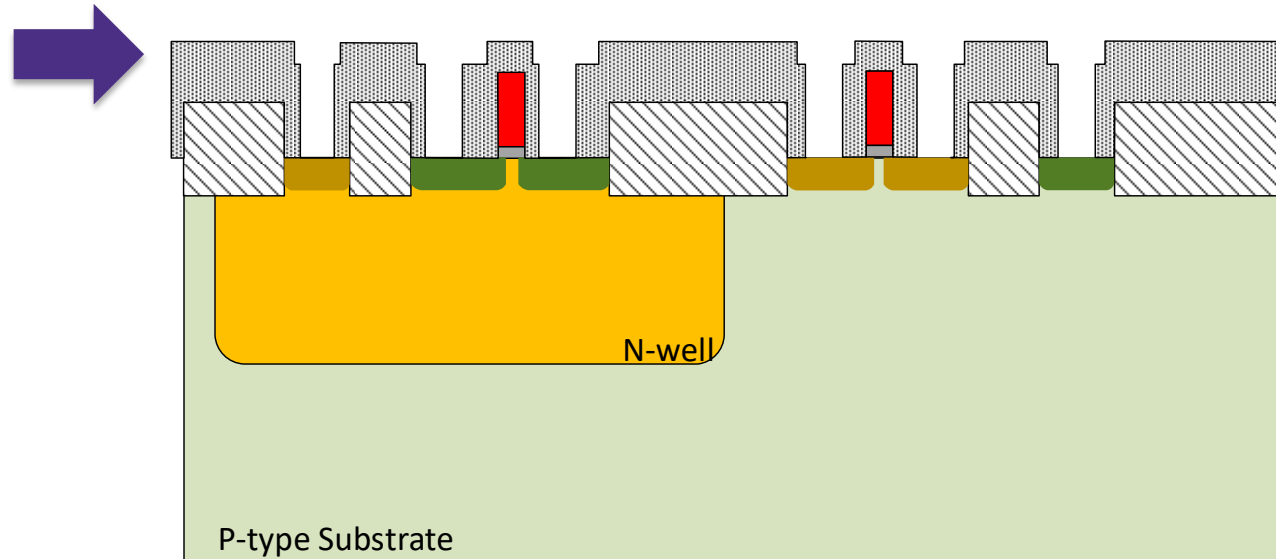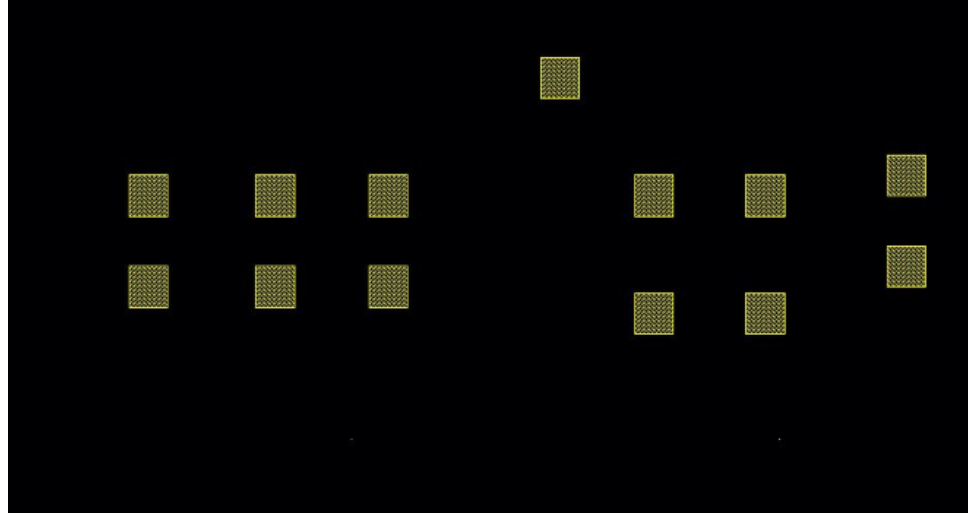
6.2: Contacts to metal

What happened to PO contact?

N-well

P-type Substrate

6.3: Contacts to metal

N-well

P-type Substrate

ELECTRICAL & COMPUTER ENGINEERING
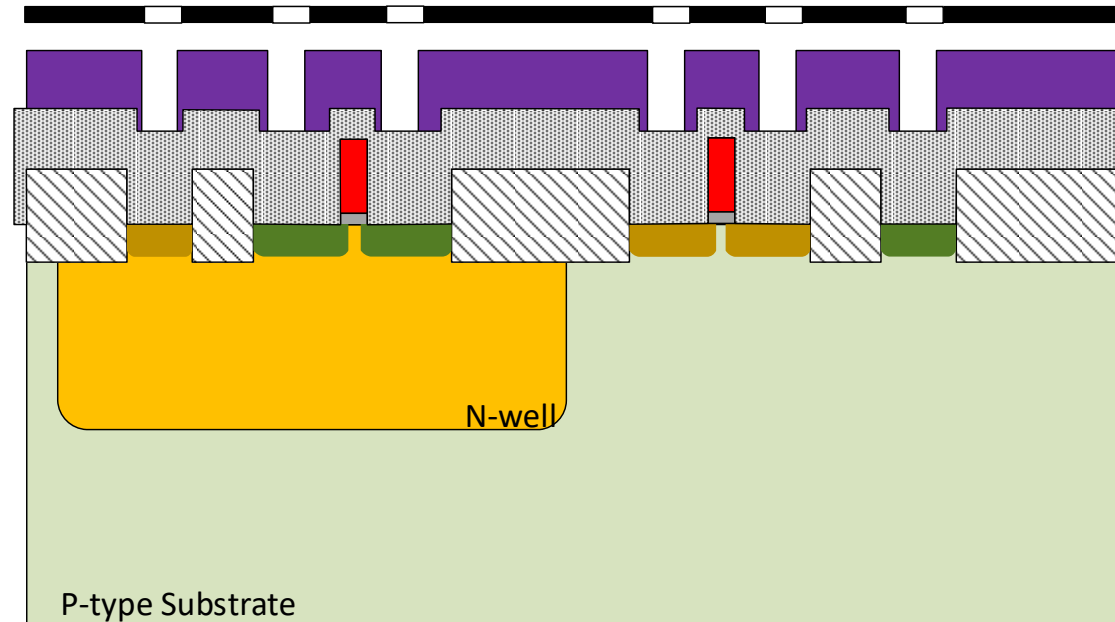
6.4: Contacts to metal
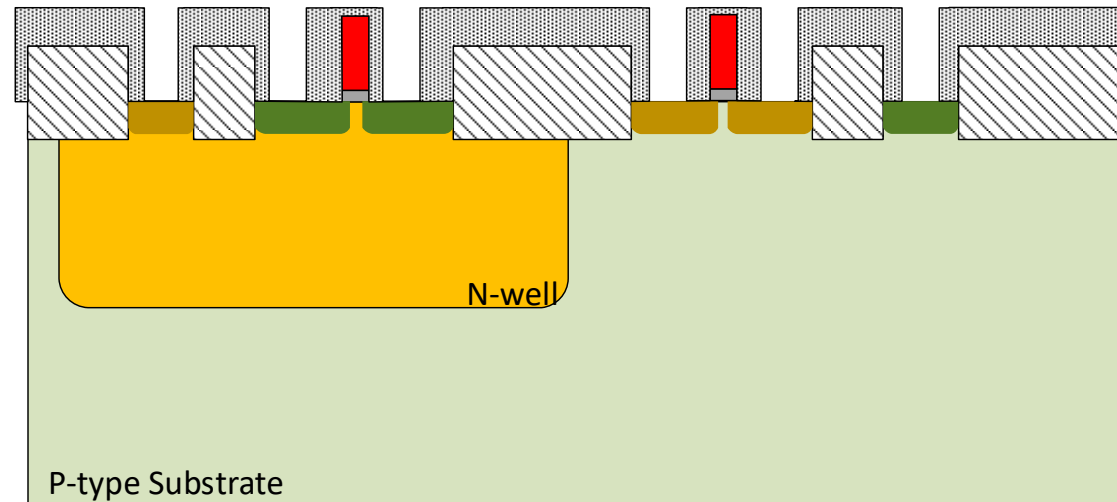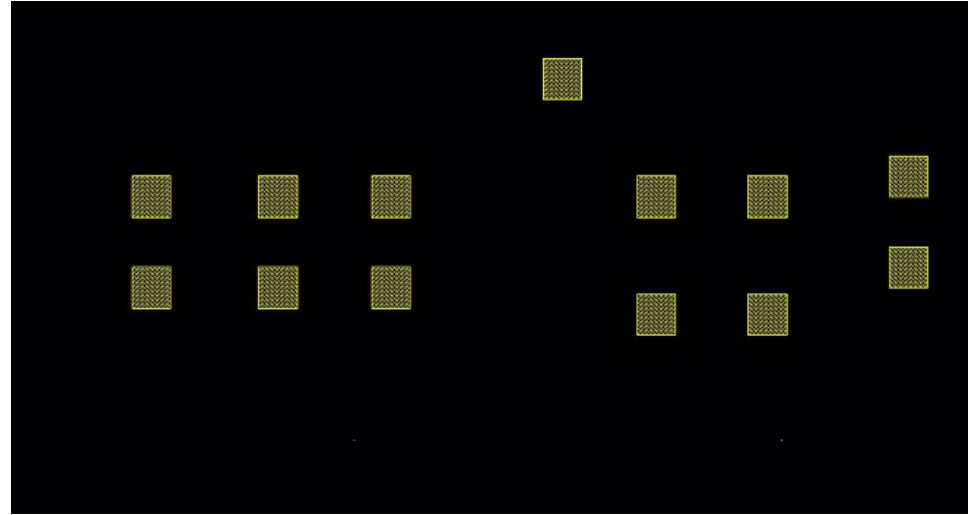
- Polish to even out topography

6.5: Contacts to metal
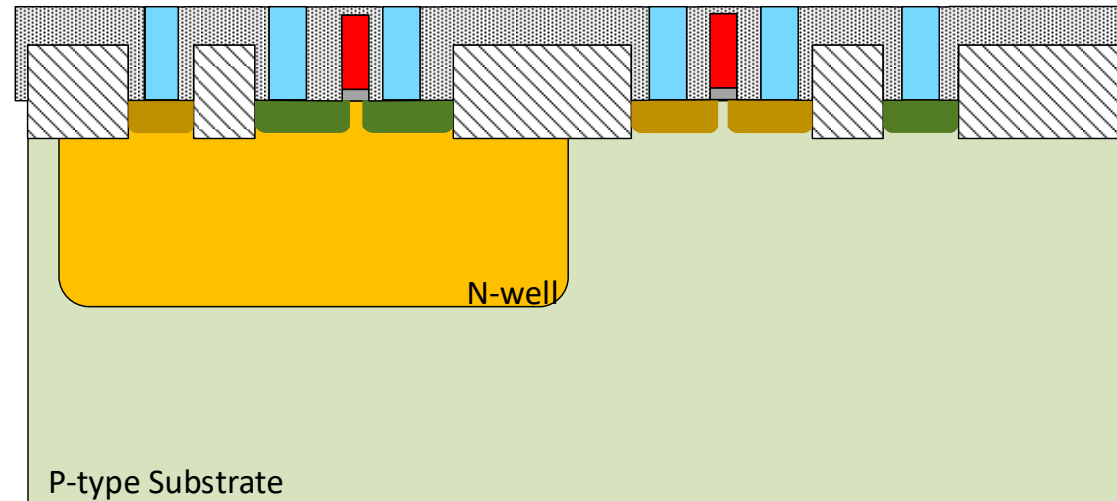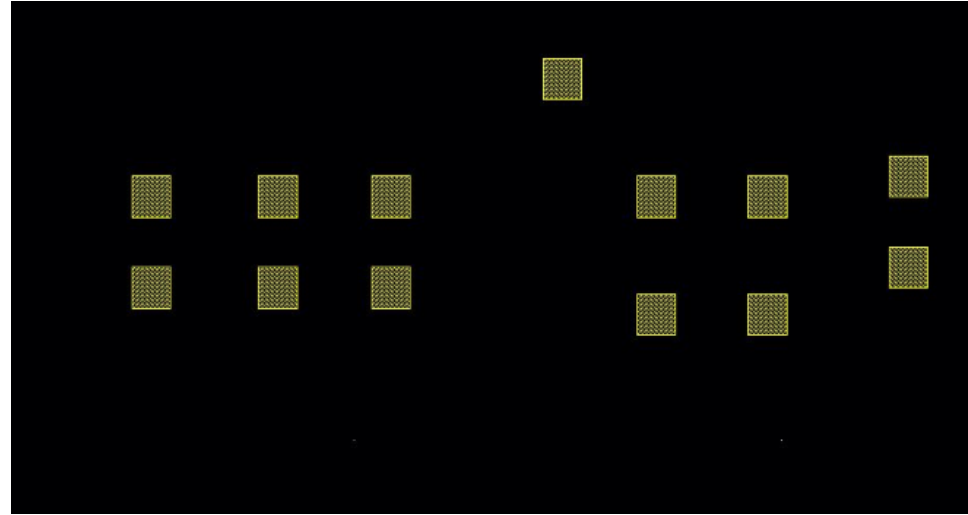
- Deposit contact material

7: Metal

- Fabricate the Metal to connect the transistors (only M1 shown)

ELECTRICAL & COMPUTER ENGINEERING

7.1: Metal

- Fabricate the Metal to connect the transistors (only M1 shown)

7.1: Metal

N-well

P-type Substrate

- Fabricate the Metal to connect the transistors (only M1 shown)

ELECTRICAL & COMPUTER ENGINEERING
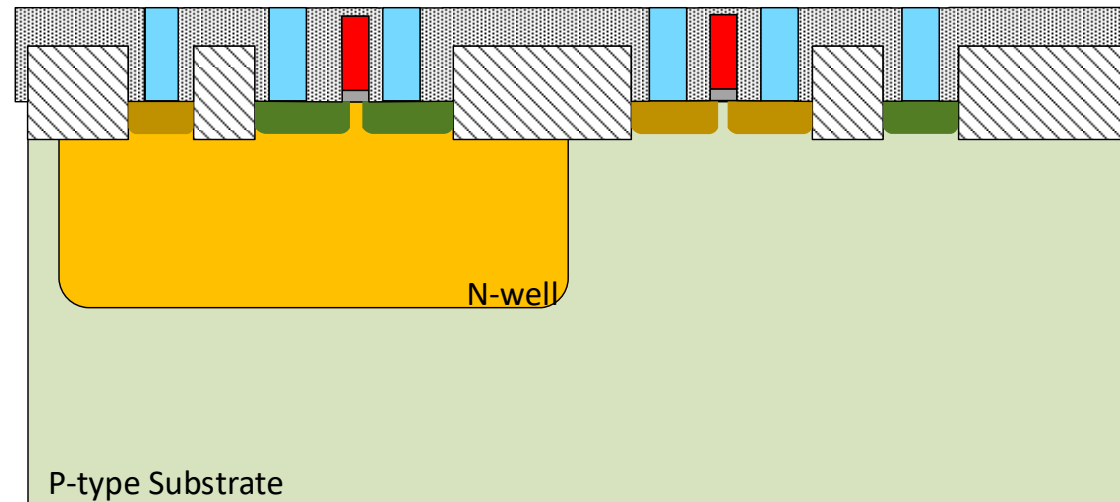
7.1: Metal

- Fabricate the Metal to connect the transistors (only M1 shown)

7.1: Metal

- Fabricate the Metal to connect the transistors (only M1 shown)

ELECTRICAL & COMPUTER ENGINEERING

7.1: Metal

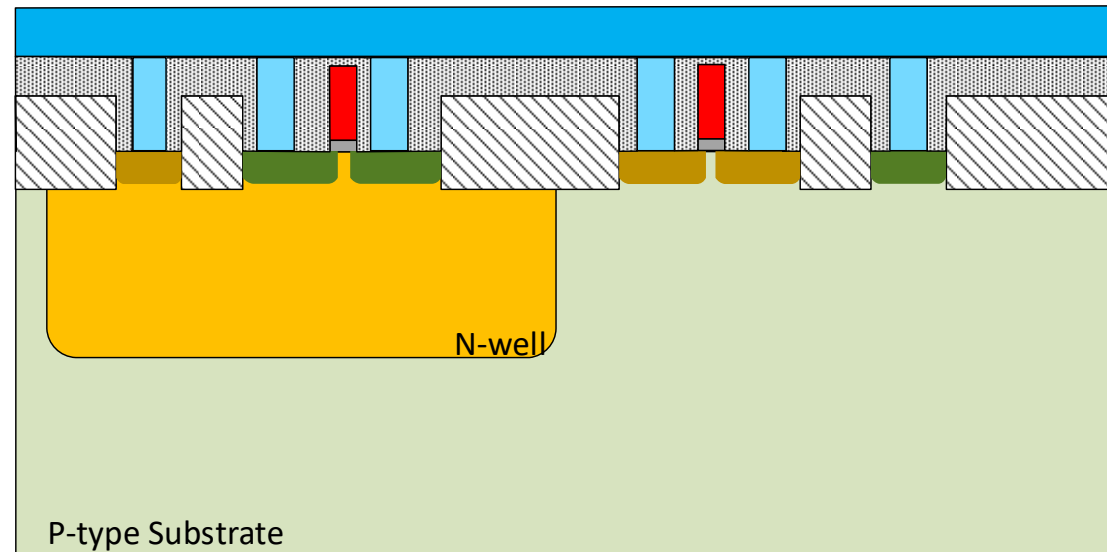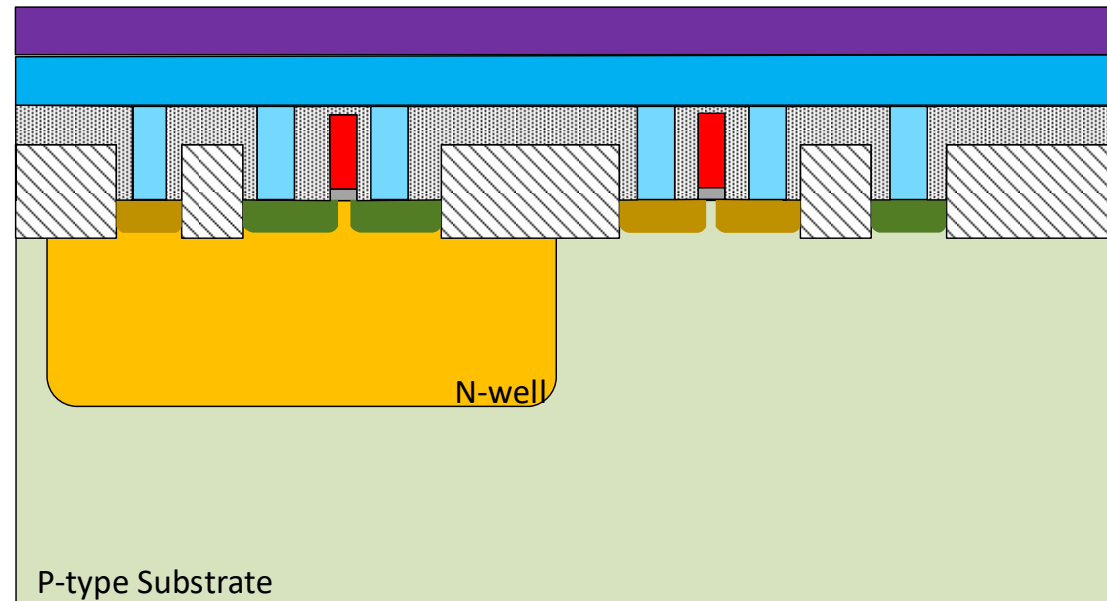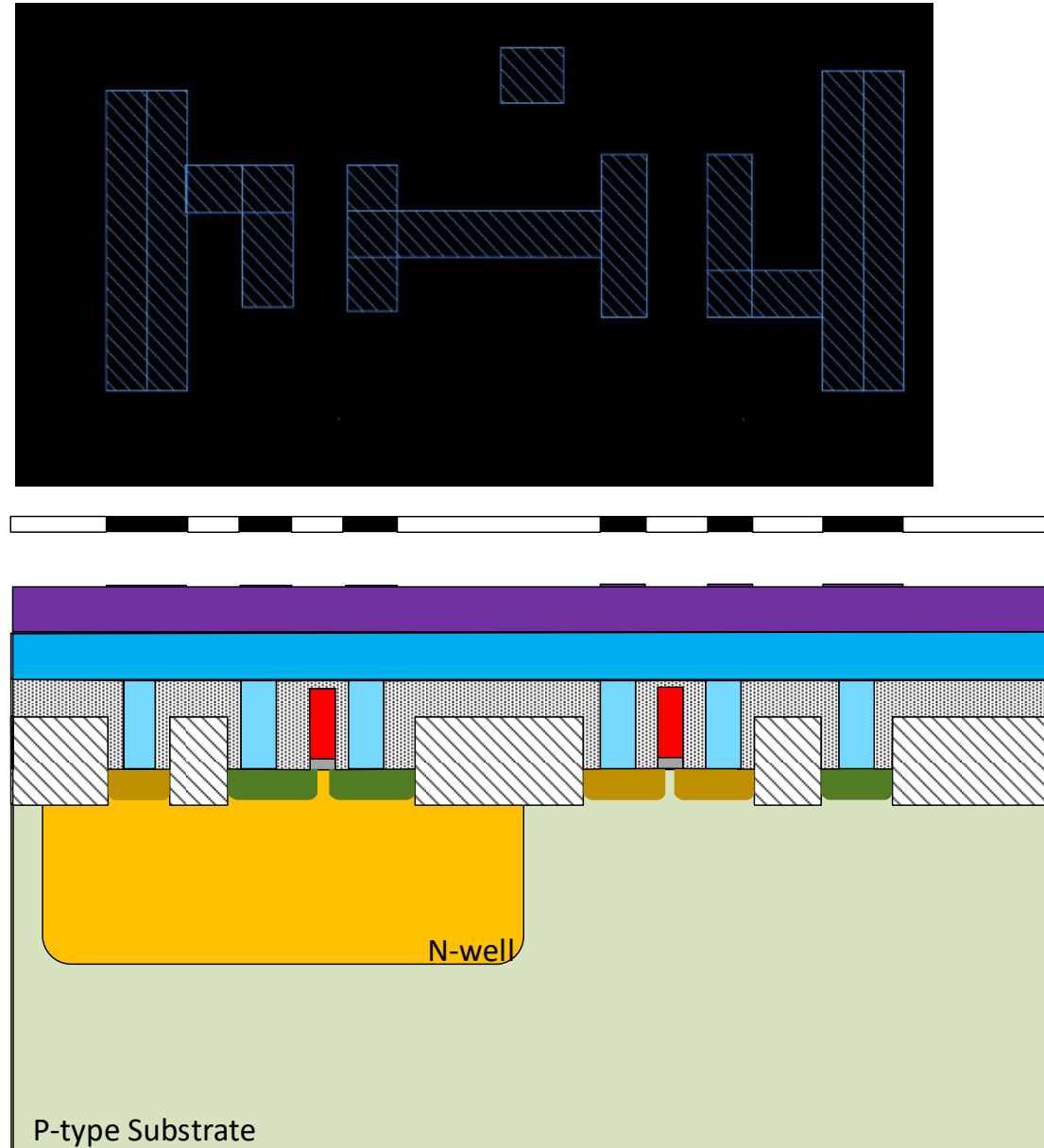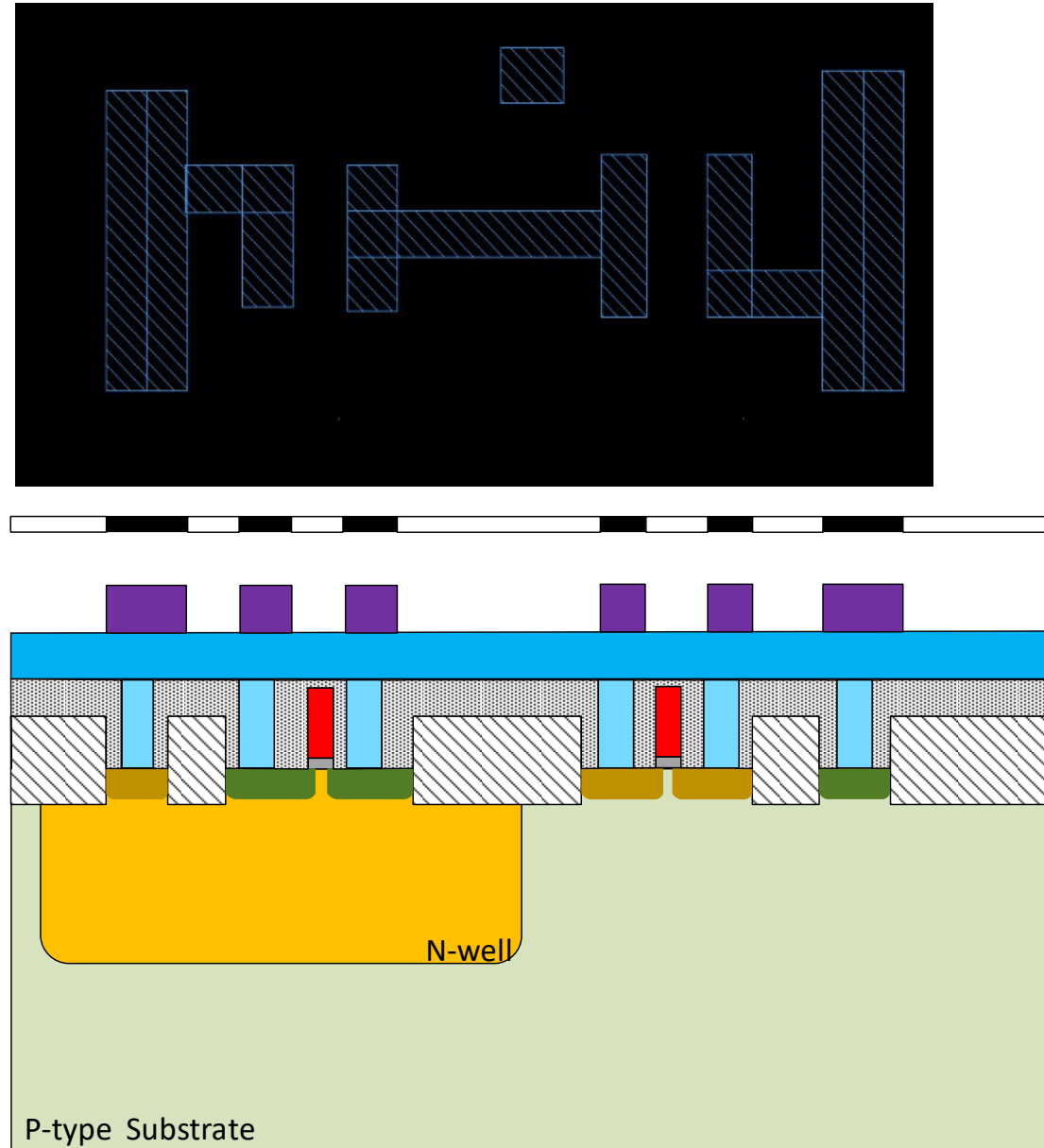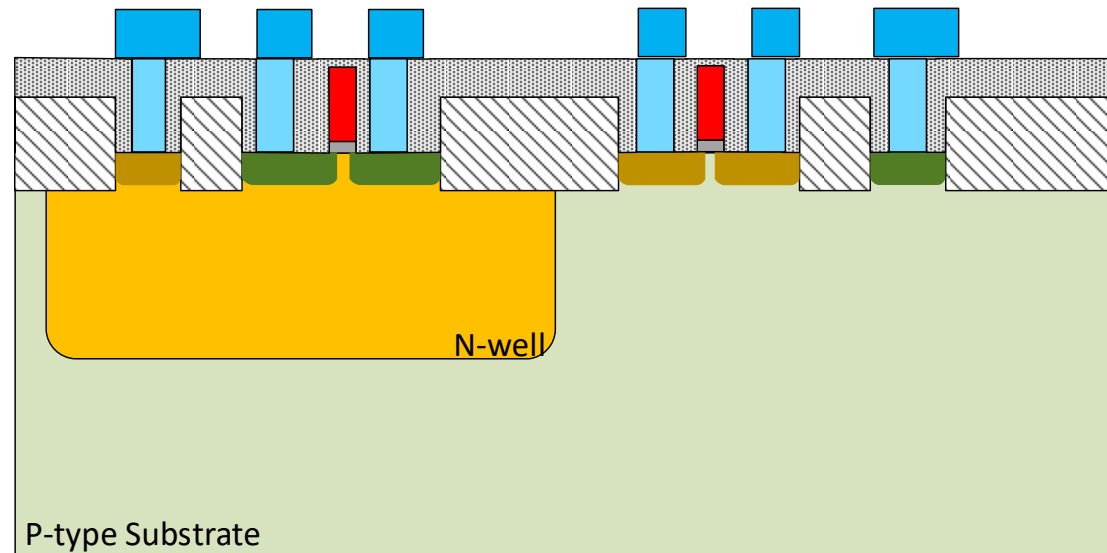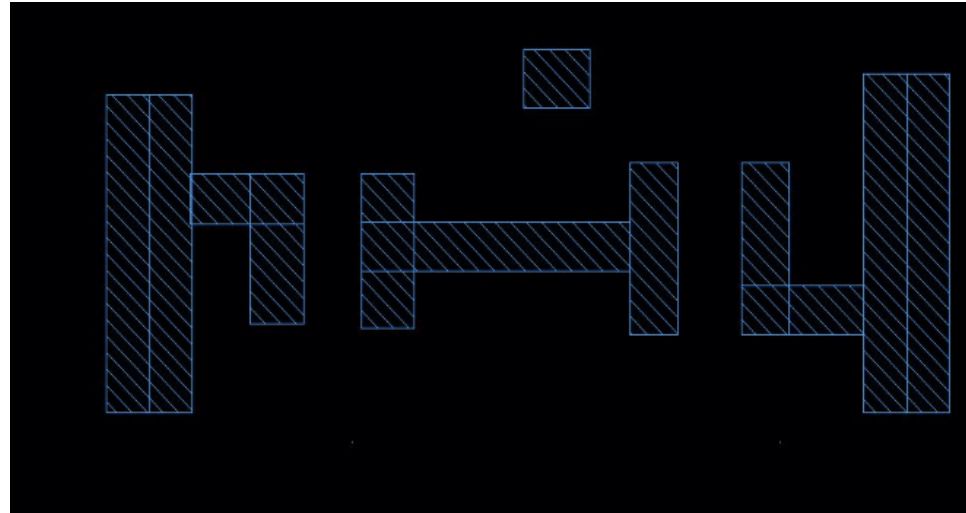- Fabricate the Metal to connect the transistors (only M1 shown)

ELECTRICAL & COMPUTER
ENGINEERING

Key Fabrication Steps

- Depositing material
  - Epitaxial growth (Si)
  - CVD (Chemical-Vapor Deposition), used for via/metals
  - Diffusion/Ion-implantation (For dopants to create N-Well, N+, P+)
  - Reaction
    - SiO_2 : Used for form field-oxide, gate-oxide, barrier for ion-implantation
    - Si_3N_4 : Inert, used as a means to prevent oxidation during formation of field-oxide
- Patterning (Lithography)
  - Apply photoresist
  - Use mask to selectively soften photoresist (for + photoresist)
  - Remove softened photoresist (photoresist, expose->soluble to developer, wash it off)
  - Perform selective deposition/etch step
  - Etch away remainder of the photoresist using a *piranha* etch
- Maintain even topography – Chemical Mechanical Polish (CMP)
- Etching (SiO_2, Si_3N_4, Metal, Photoresist and many more...)

W | ELECTRICAL & COMPUTER ENGINEERING

Additional Notes

- LOCOS no longer used in scaled processes
  - "Birds-beak" requires too much separation, area hit
  - Use Shallow Trench Isolation instead
- "Poly" is now done using Metal Gate
  - Avoid effective oxide thickness increase seen with poly
  - Lower gate resistance
- Oxides
  - Gate oxide is a High-K material*
  - Inter-layer dielectric (ILD), between metals use low-K dielectrics
- Latest CMOS technologies use a tri-gate (finfet) structure. No planar MOSFETs
  - Better short channel effects
  - Restrictive in device widths
- Modern processes use many more masks and stages than shown here

Design Rule Checks (DRCs)

- Modern microprocessors have >4billion transistors
- Every one of them, and their connecting wires needs to work
- Design Rule Checks
  - Enforce constraints that must be met by mask geometries
    - Min-spacing (Avoid shorts, leak-paths)
    - Min-width (Avoid pinch-off)
    - Overlap (Ensure sufficient intersection, enclosure)
    - Density checks (Global and Local)
  - Violation causes shorts, opens, parametric yield loss
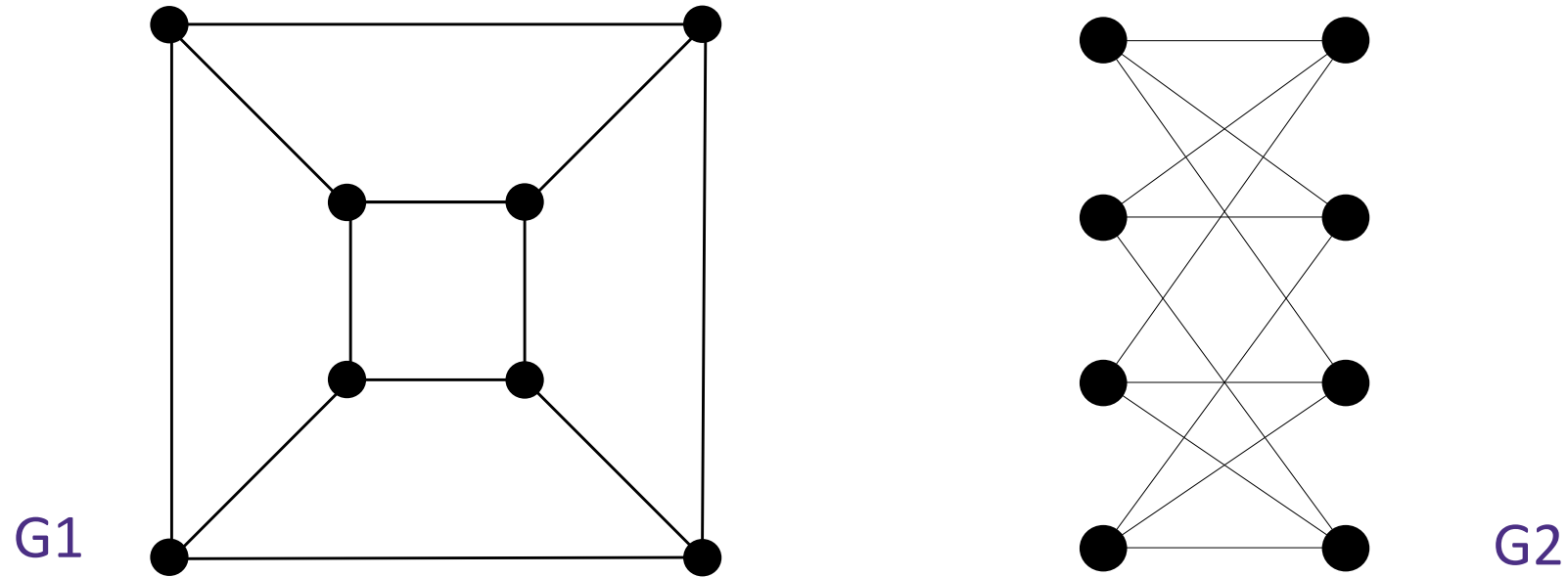
Layout vs. Schematics (LVS)
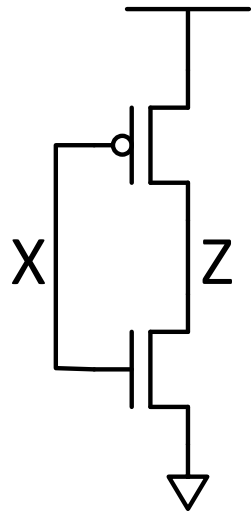
V.S.
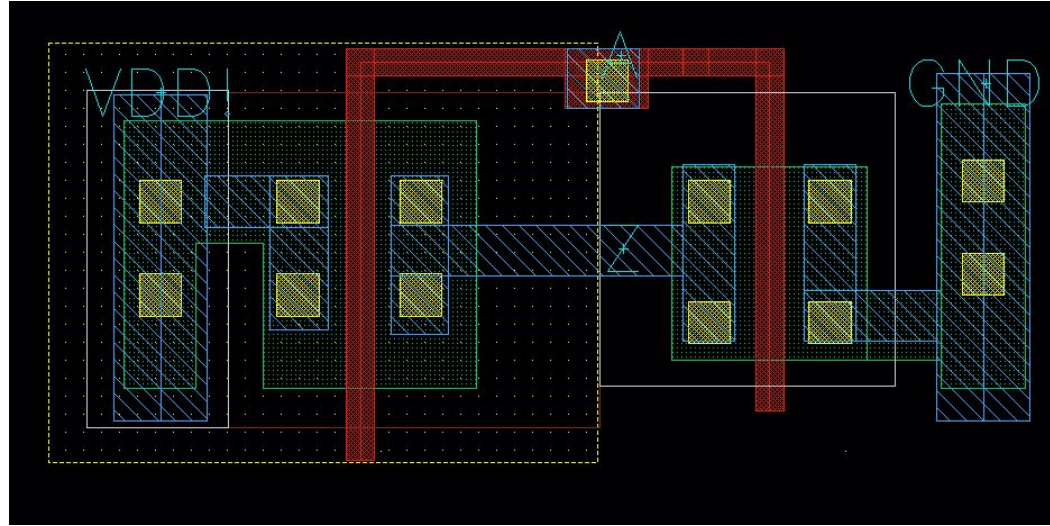
- Complex design environments → Design is entered and evaluated at a higher level of abstraction
  - C/C++
  - HDL
  - At least schematics
- Layout then created. Mask must match required functionality
- Problem of checking whether Layout = Schematic essentially a check for graph isomorphism

W ELECTRICAL & COMPUTER ENGINEERING

Quick de-tour: Graph Isomorphism

G1

G2

- "A one-on-one and onto" mapping between nodes, f
  - f: $V(G_1) \rightarrow V(G_2)$
  - G_1 and G_2 are isomorphic: a,b adjacent in G_1 $\Leftrightarrow$ f(a), f(b) adjacent in G_2
- LVS seeks to determine if there is an isomorphism between the schematic graph and the layout graph.
  - Include edge properties (fetWidth etc.) in addition to just connections

ELECTRICAL & COMPUTER ENGINEERING

Quick de-tour: Graph Isomorphism
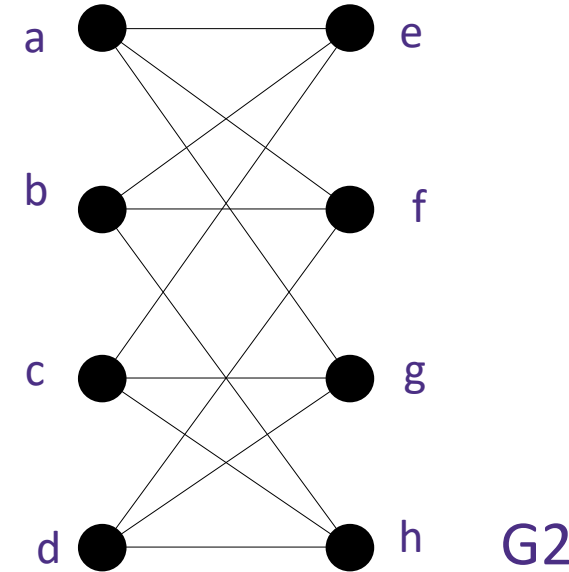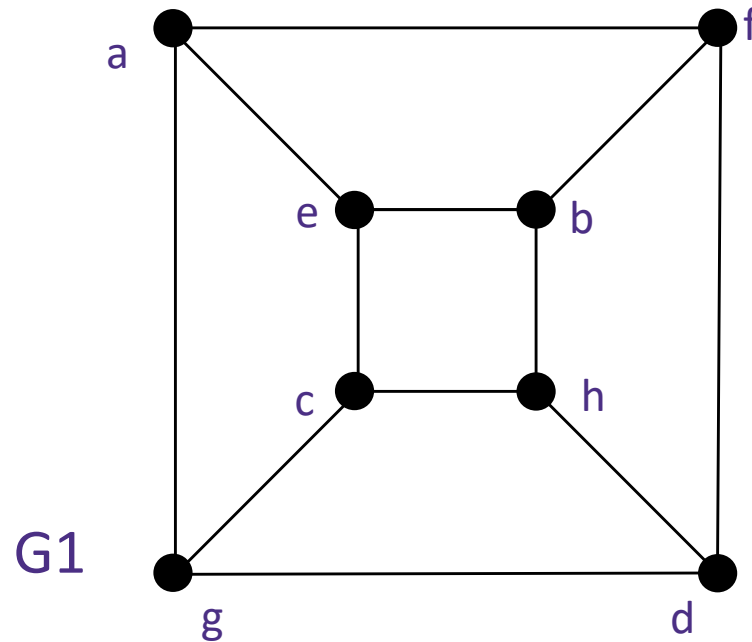
- "A one-on-one and onto" mapping between nodes, f
  - f: $V(G_1) \rightarrow V(G_2)$
  - G_1 and G_2 are isomorphic: a,b adjacent in G_1 $\Leftrightarrow$ f(a), f(b) adjacent in G_2
- LVS seeks to determine if there is an isomorphism between the schematic graph and the layout graph.
 - Include edge properties (fetWidth etc.) in addition to just connections

LVS operation

Source: Ling, IBM

- Read-in schematic netlist
- Generate internal graph representation
- Reduce (if directed) parallel, series components
- Read-in layout netlist (as a gdsII file)
- Use geometry and layer rules (specified in your calibre.lvs file) to generate graph representation
- Reduce if necessary
- Perform equivalence checking between the 2 graphs
- If check fails, report the points of mismatch (careful here!)

W ELECTRICAL & COMPUTER ENGINEERING
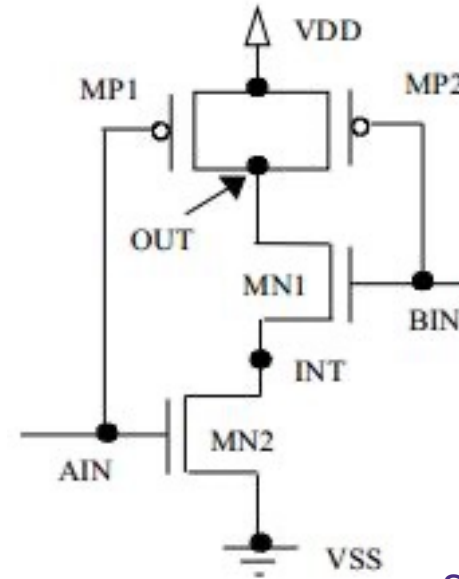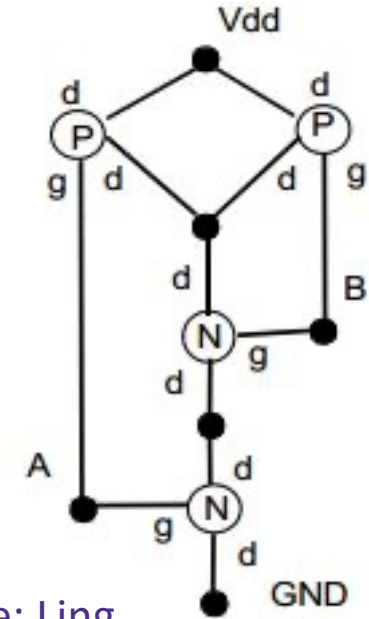
Stick Diagrams: A Quick Introduction

Metal

**Poly**

N/P Diff

Contact
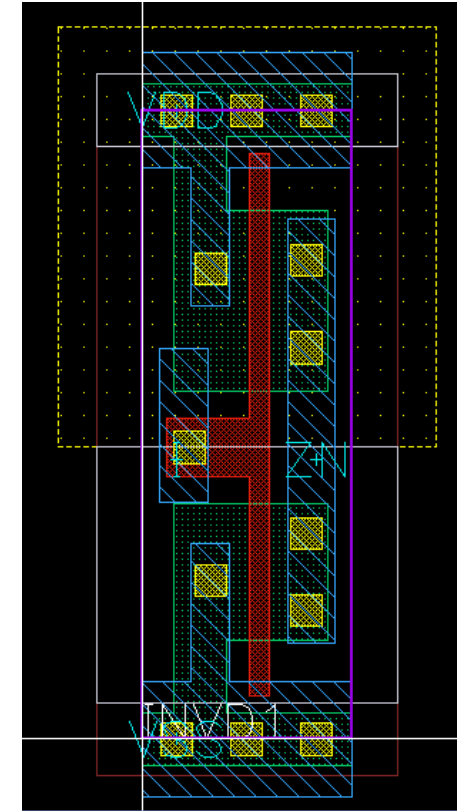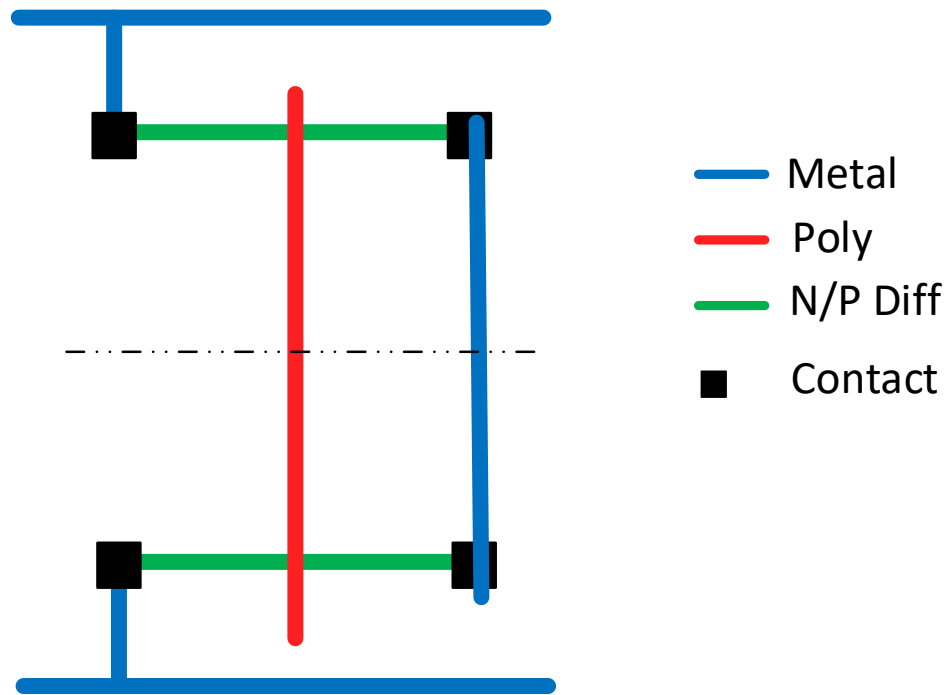
- Moderately complex CMOS gates have non-unique (and other inefficient) ways of being built
- An informal means to sketch out and plan your layout ahead of time
- Part of required reading: W&H Section 1.5.5 (2 pages)

W ELECTRICAL & COMPUTER ENGINEERING

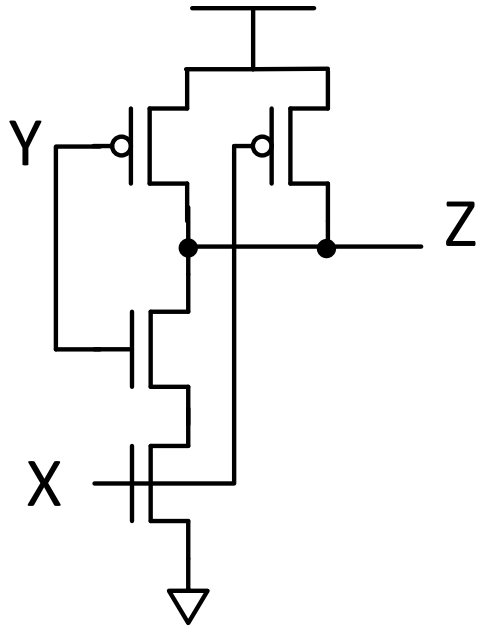# Parting notes on efficient layout: Euler Paths
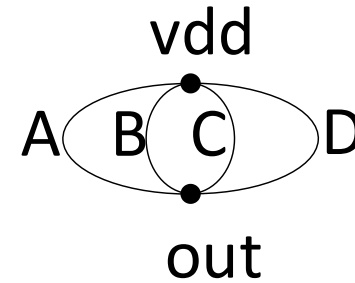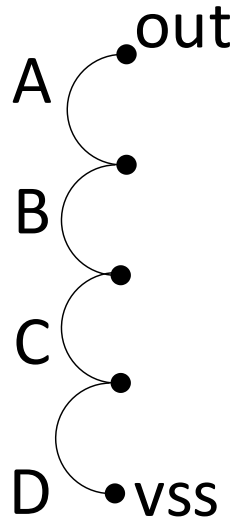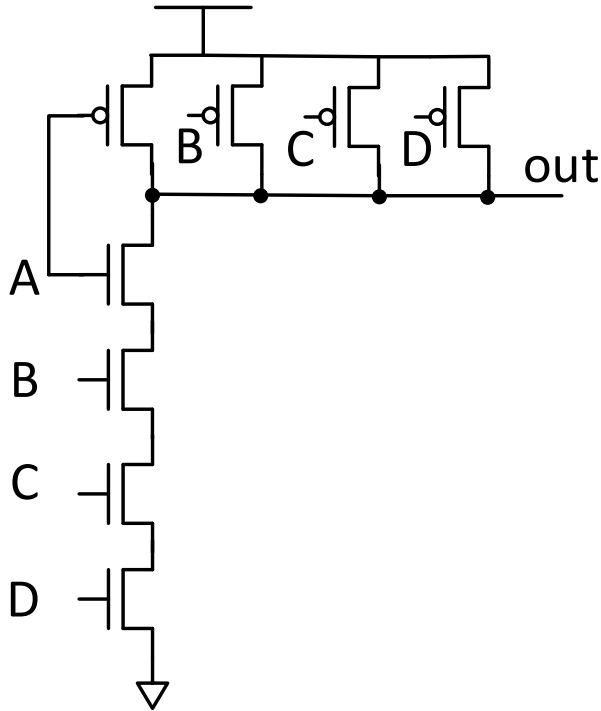
- Euler path: A traversal of a graph which visits **every** edge exactly once
- Draw the pullup/pulldown graph (or sub-graph) and identify an euler path
- Identify whether the dual graph has an euler path with the same path sequence. If yes, gate connections are made a lot simpler
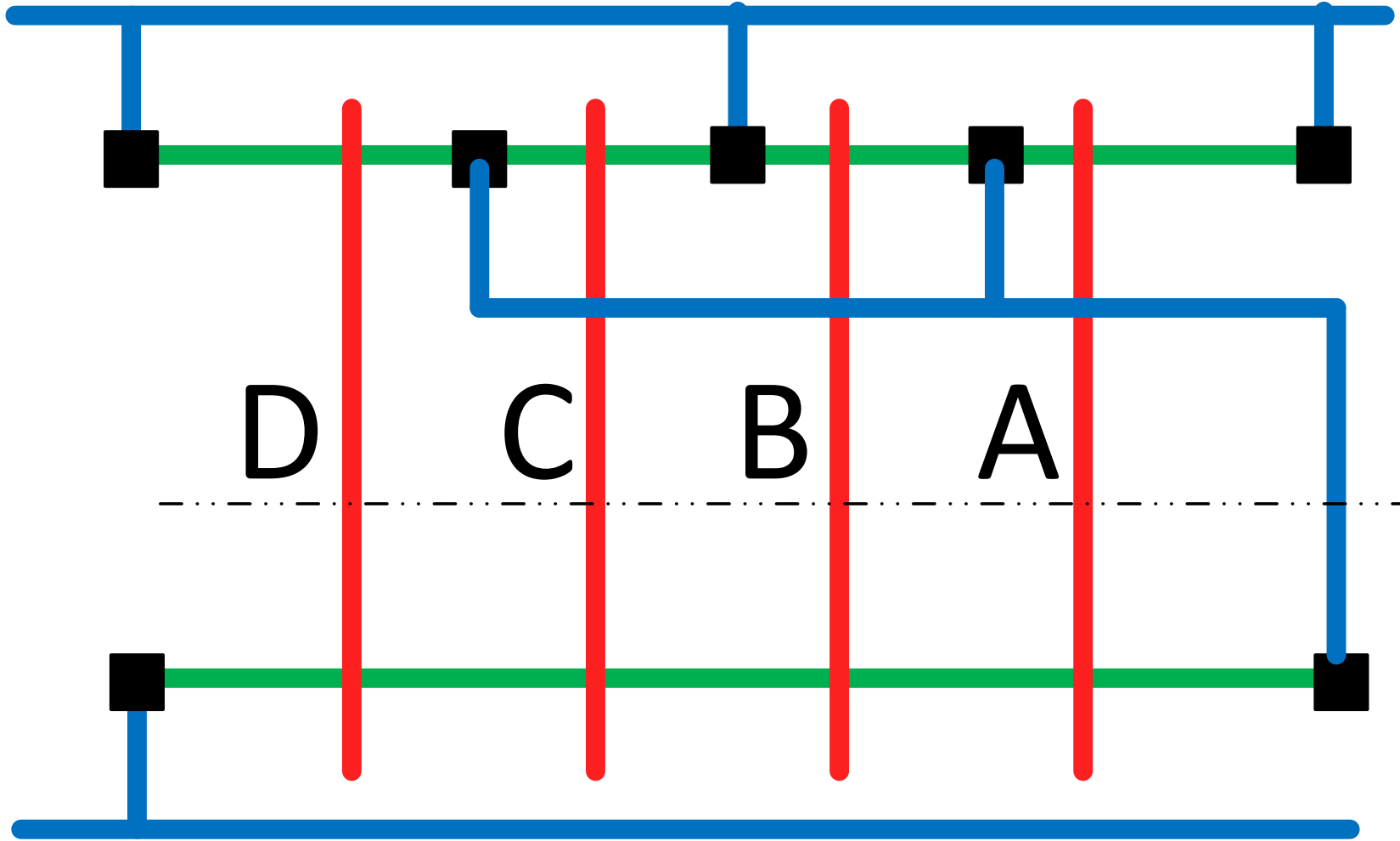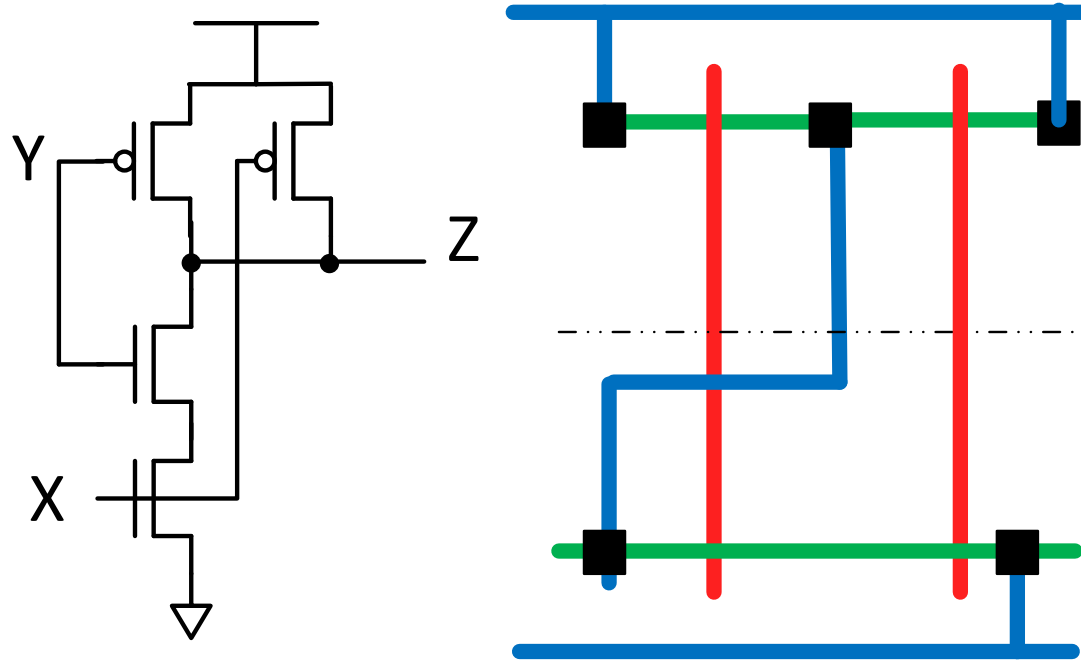
ELECTRICAL & COMPUTER ENGINEERING

Parting notes on efficient layout: Drain Sharing

- Effective means to reduce the parasitic junction, and wiring capacitance
- Use stick diagrams to plan layout accordingly

ELECTRICAL & COMPUTER ENGINEERING

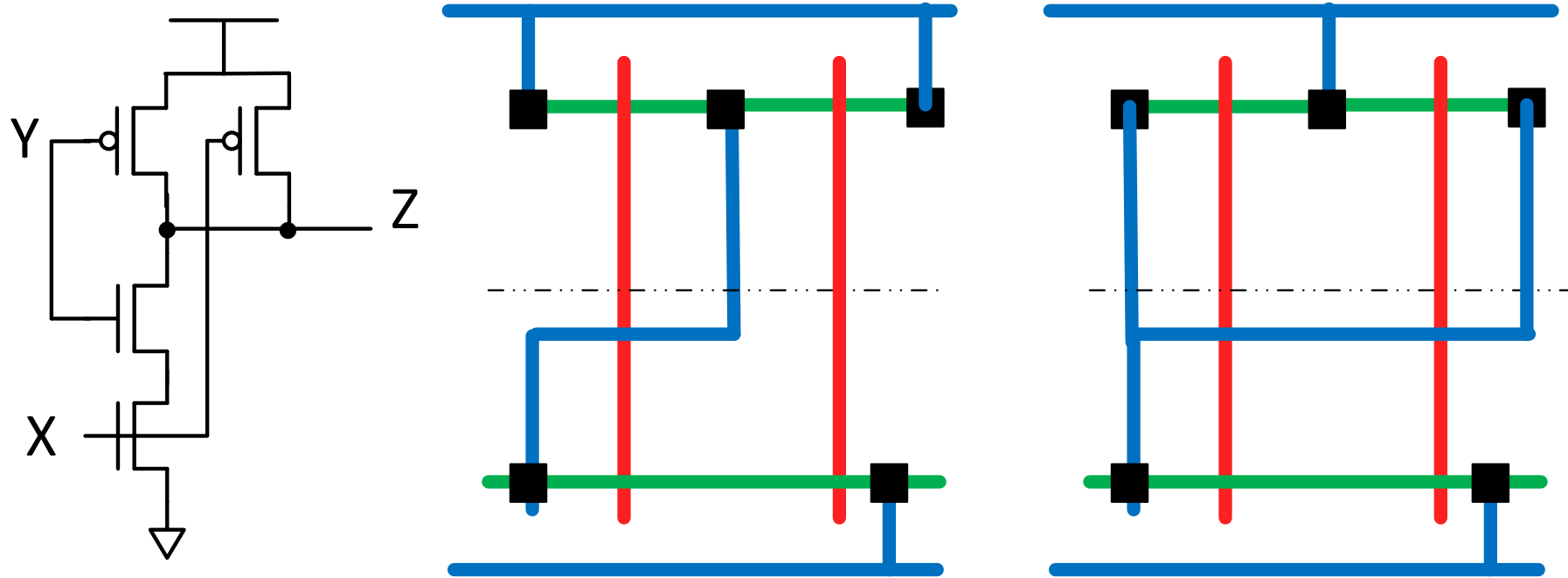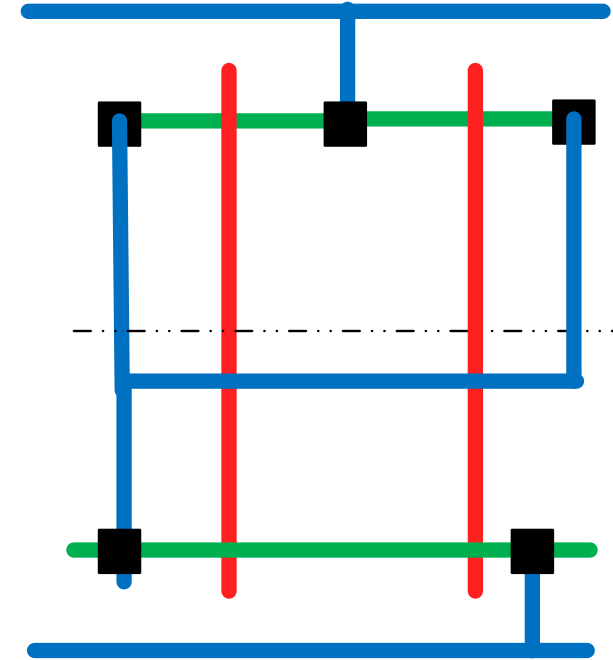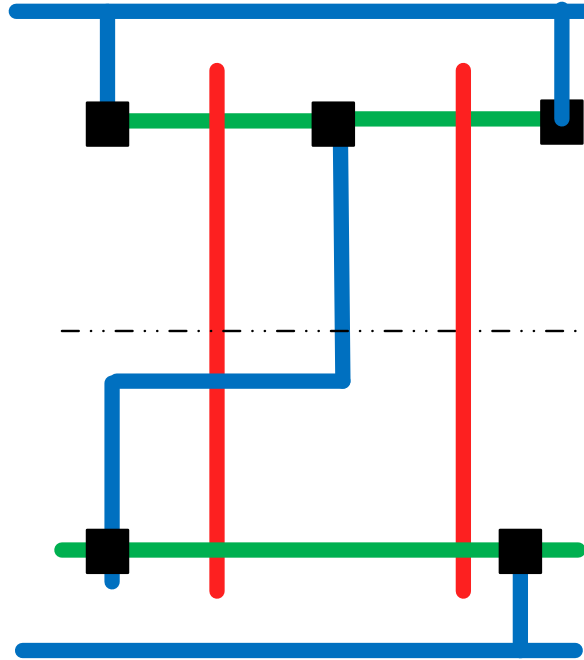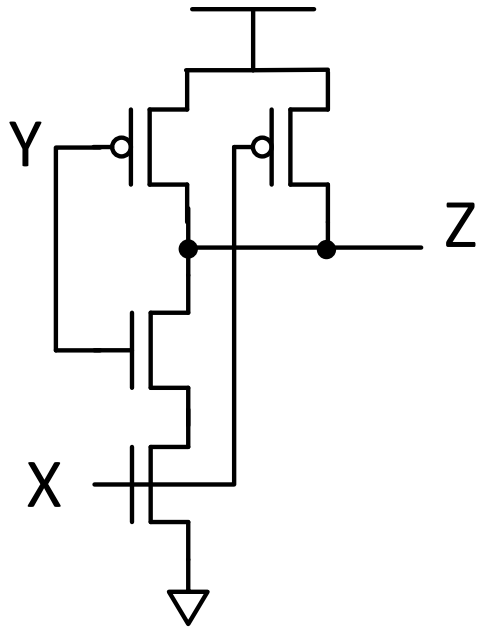# Parting notes on efficient layout: Drain Sharing

- Effective means to reduce the parasitic junction, and wiring capacitance
- Use stick diagrams to plan layout accordingly

Parting notes on efficient layout: Drain Sharing

- Effective means to reduce the parasitic junction, and wiring capacitance
- Use stick diagrams to plan layout accordingly

ELECTRICAL & COMPUTER ENGINEERING

Parting notes on efficient layout: Drain Sharing

OK. Given a choice, which is better layout?

- Effective means to reduce the parasitic junction, and wiring capacitance
- Use stick diagrams to plan layout accordingly

W ELECTRICAL & COMPUTER ENGINEERING

Reading assignment

- Required reading
    - W&H Section 1.5*

- Optional Reading
    - W&H Chapter 3