Lecture 5: The CMOS Inverter

Based on material prepared by prof. Visvesh S. Sathe

Acknowledgements

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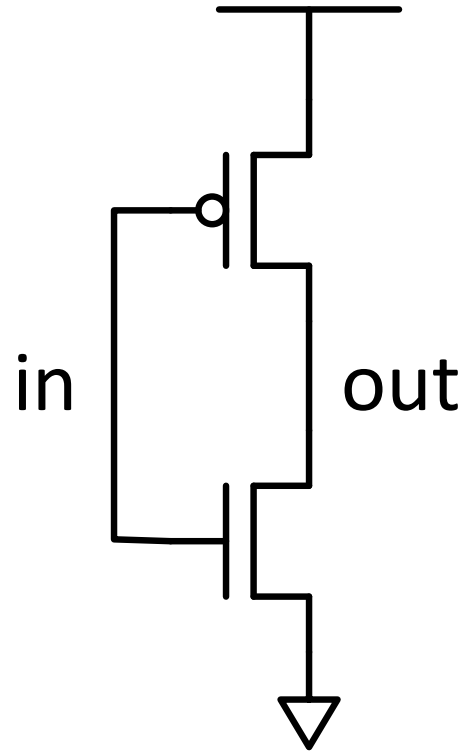
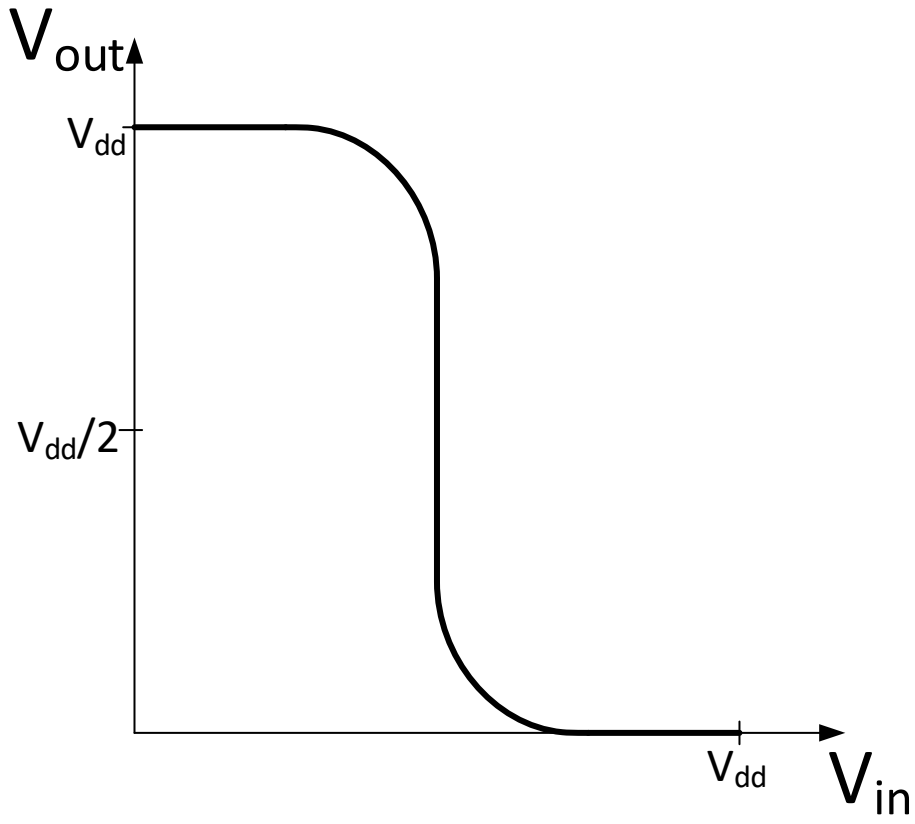
UW (2013-2022)
GaTech (2022-present)

CMOS Gate Design

- Analyze important aspects of CMOS logic
  - Static Operation (Static Noise Margin, Hold resistance)
  - Dynamic operation (Cross-over current, current-drive, delay)
  - Power dissipation
  - Gate sizing basics
  - Effect of voltage scaling
- Use inverter design to understand these various aspects

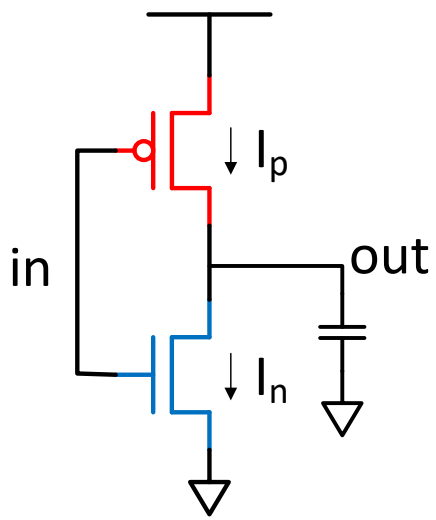
DC Response

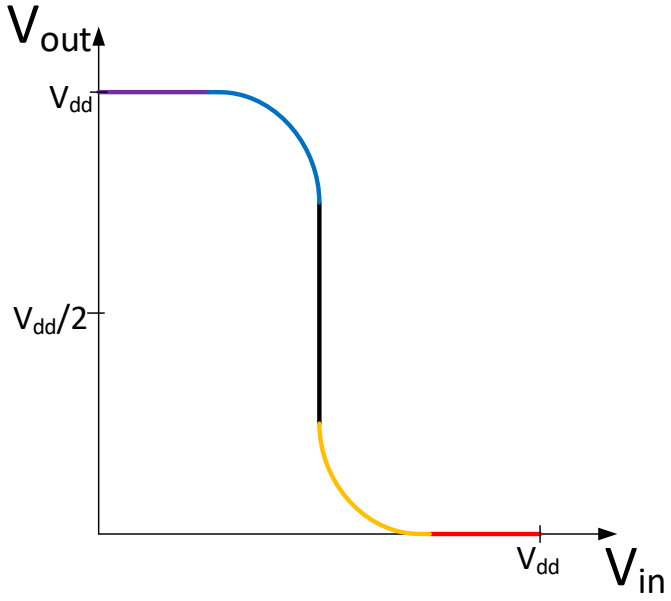




- DC transfer function of a balanced, ideal inverter
  - At each dc value of V_{in}, evaluate V_{out} and record

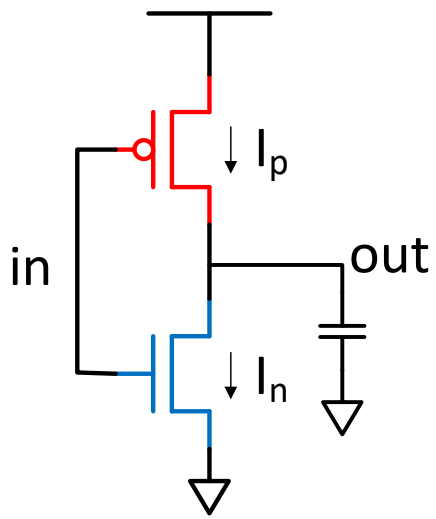
Understanding the DC Transfer Function

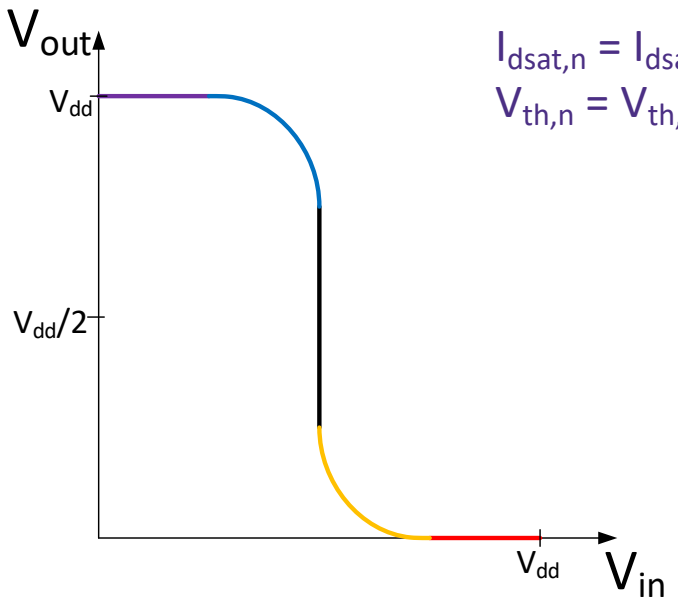




- Static analysis
  - Assumes load is capacitive (No steady-state current draw)
  - Voltages are dc (**Amount of capacitive load is irrelevant**)
- Inverter DC analysis
  - Devices operate over a variety of modes across voltage range
  - Governing equation:
  - Both, equation-based and graphical analysis is valuable
  - Useful in determining robustness to noise (Static Noise Margin/Holding Res)

Understanding the DC Transfer Function





$I_{dsat,n} = I_{dsat,p}$
$V_{th,n} = V_{th,p} = 200mV$

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  - Assumes load is capacitive (No steady-state current draw)
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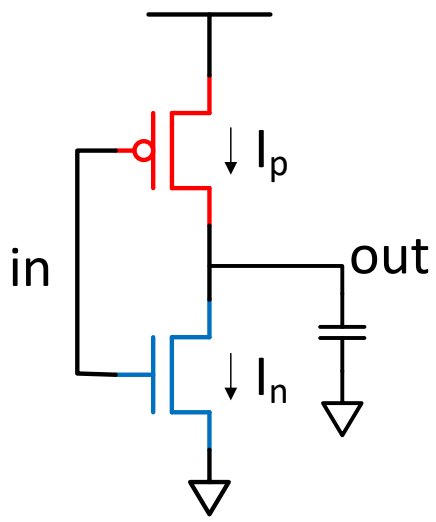
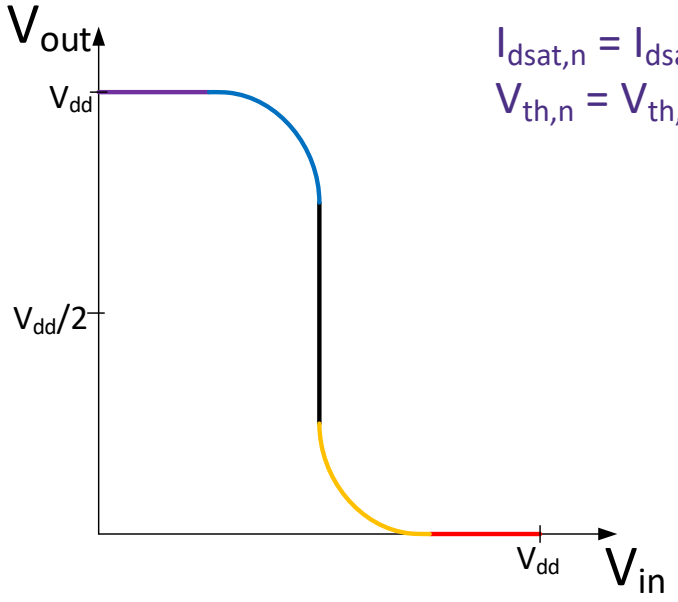
Understanding the DC Transfer Function





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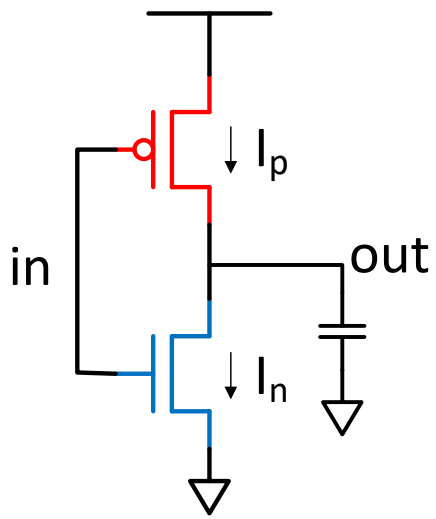

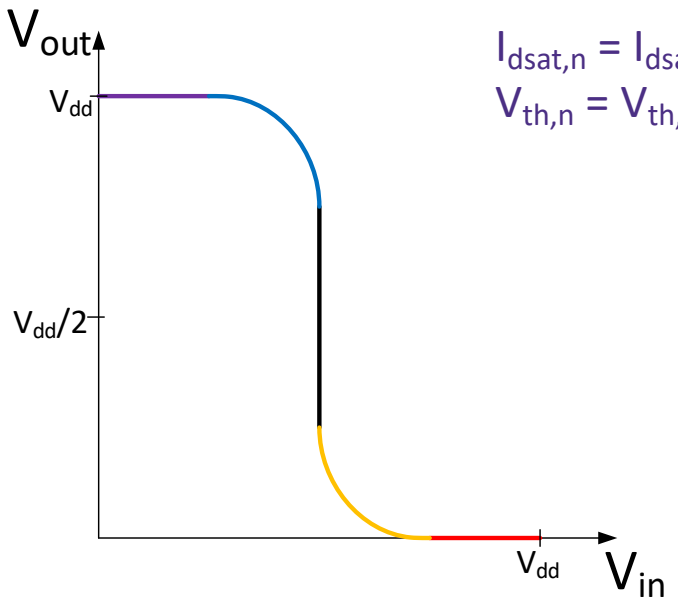

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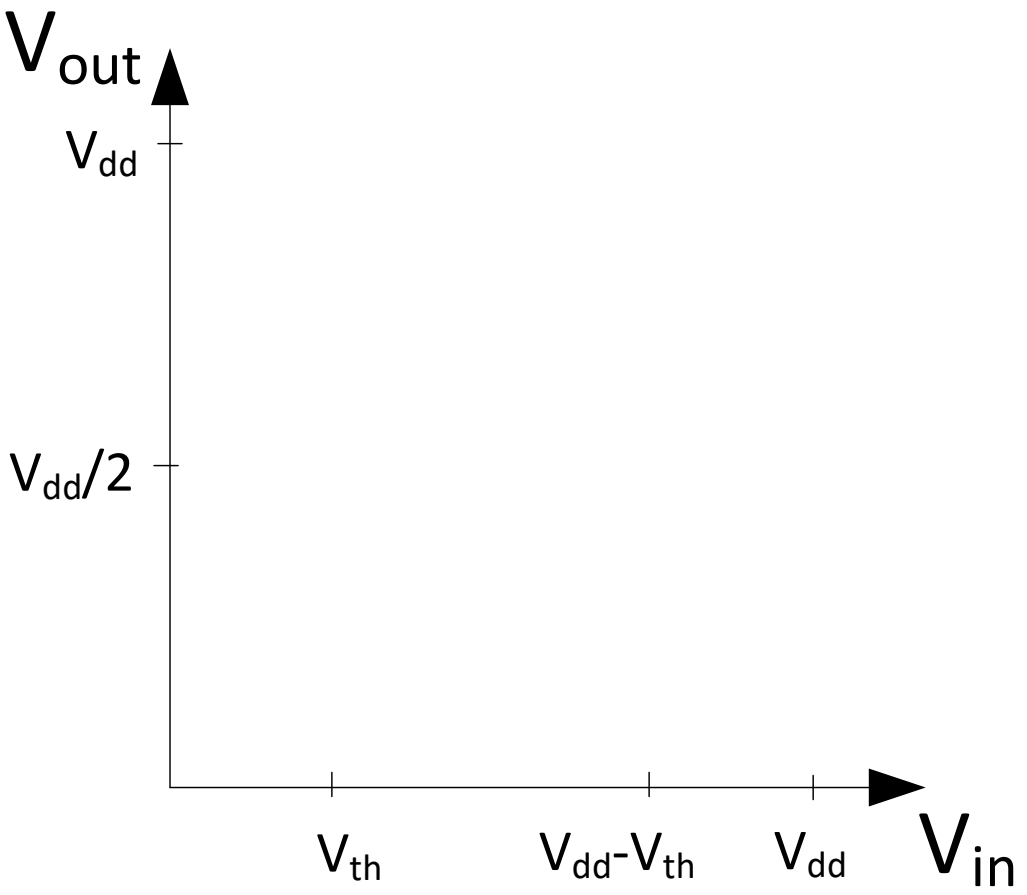
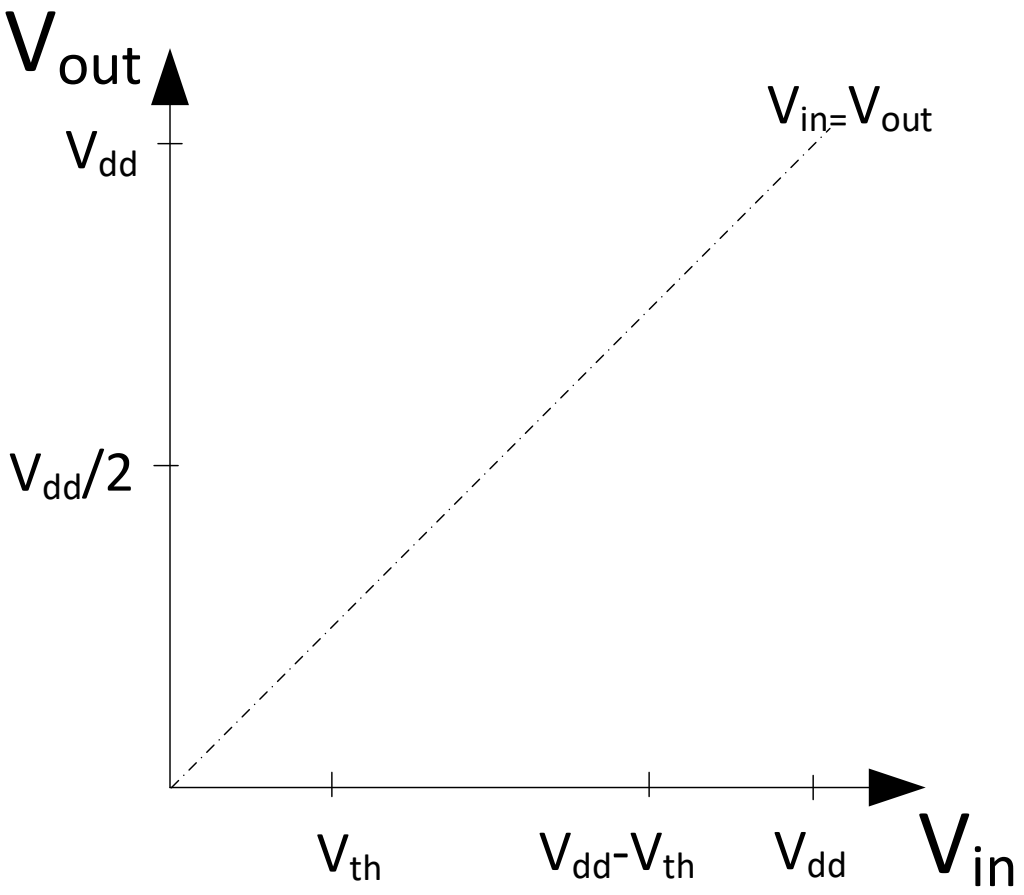
- Static analysis
  - Assumes load is capacitive (No steady-state current draw)
  - Voltages are dc (**Amount of capacitive load is irrelevant**)
- Inverter DC analysis
  - Devices operate over a variety of modes across voltage range
  - Governing equation: Pullup current == Pulldown current
  - Both, equation-based and graphical analysis is valuable
  - Useful in determining robustness to noise (Static Noise Margin/Holding Res)

Inverter DC Analysis



- $I_{dsat,n} = I_{dsat,p}$
- $V_{th,n} = V_{th,p} = 200mV$
- Mark out locus of operation

Inverter DC Analysis



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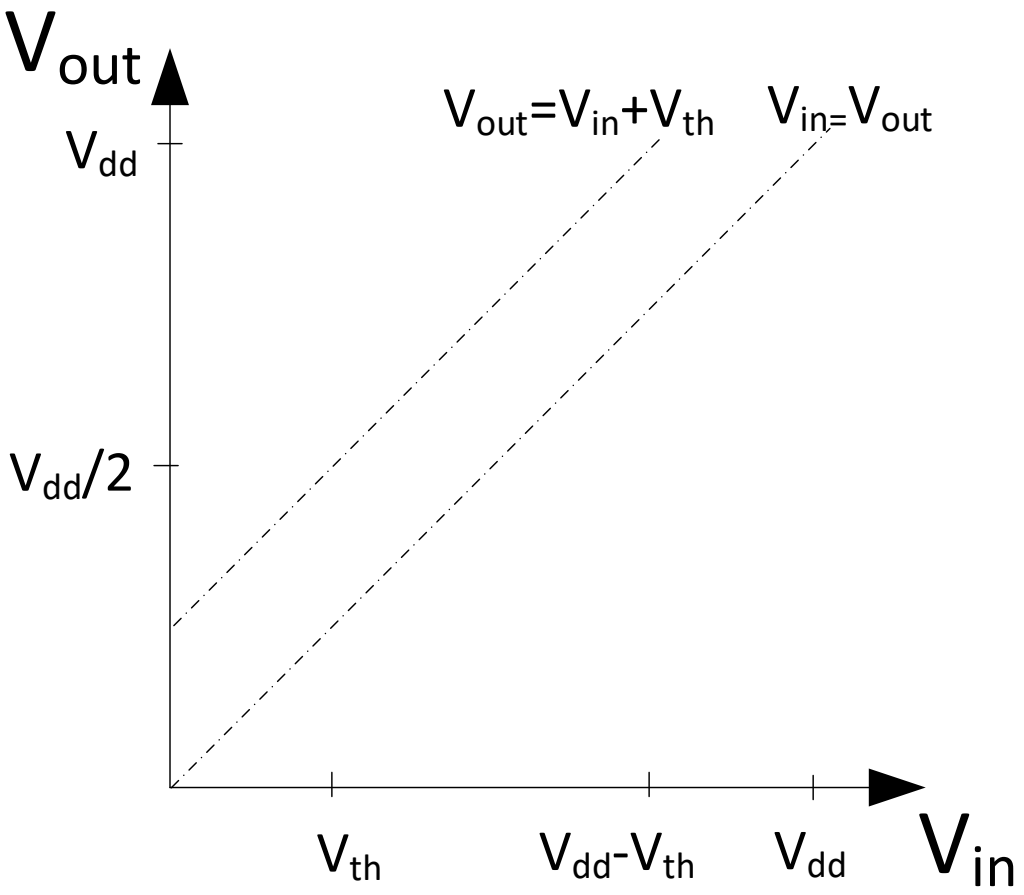

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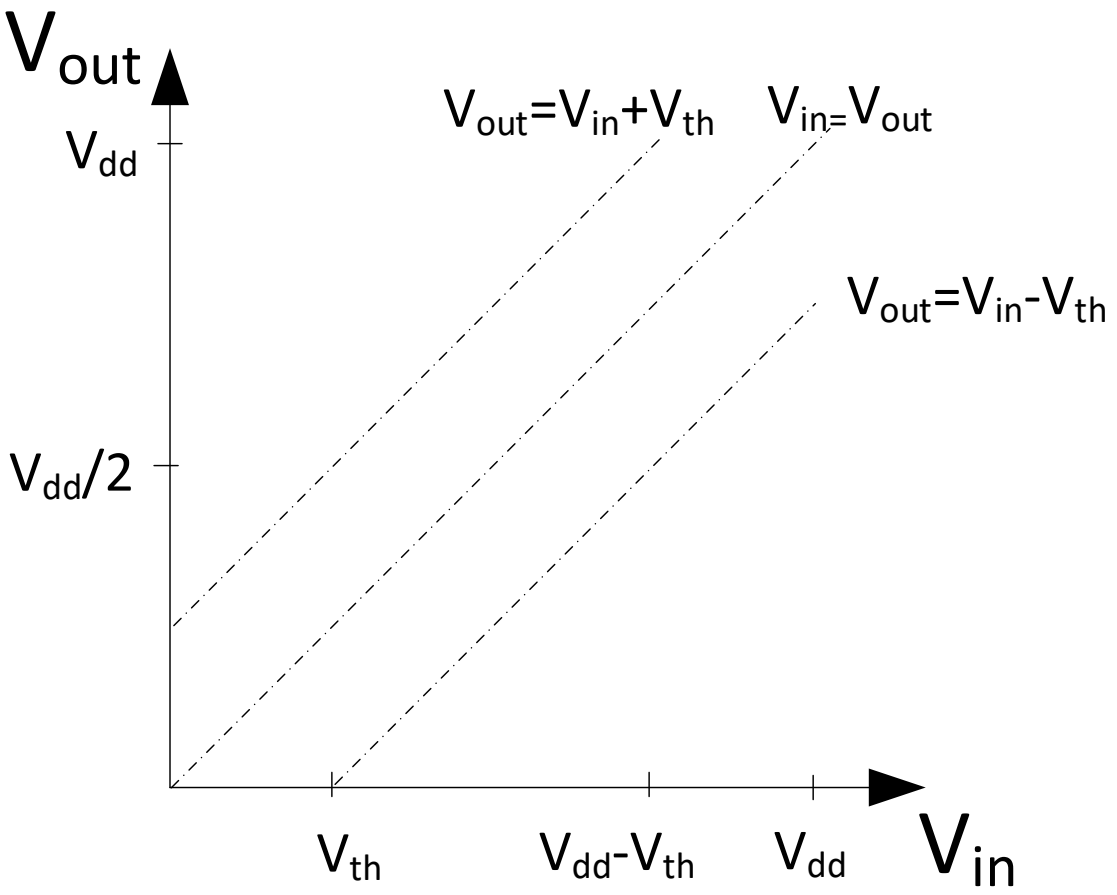

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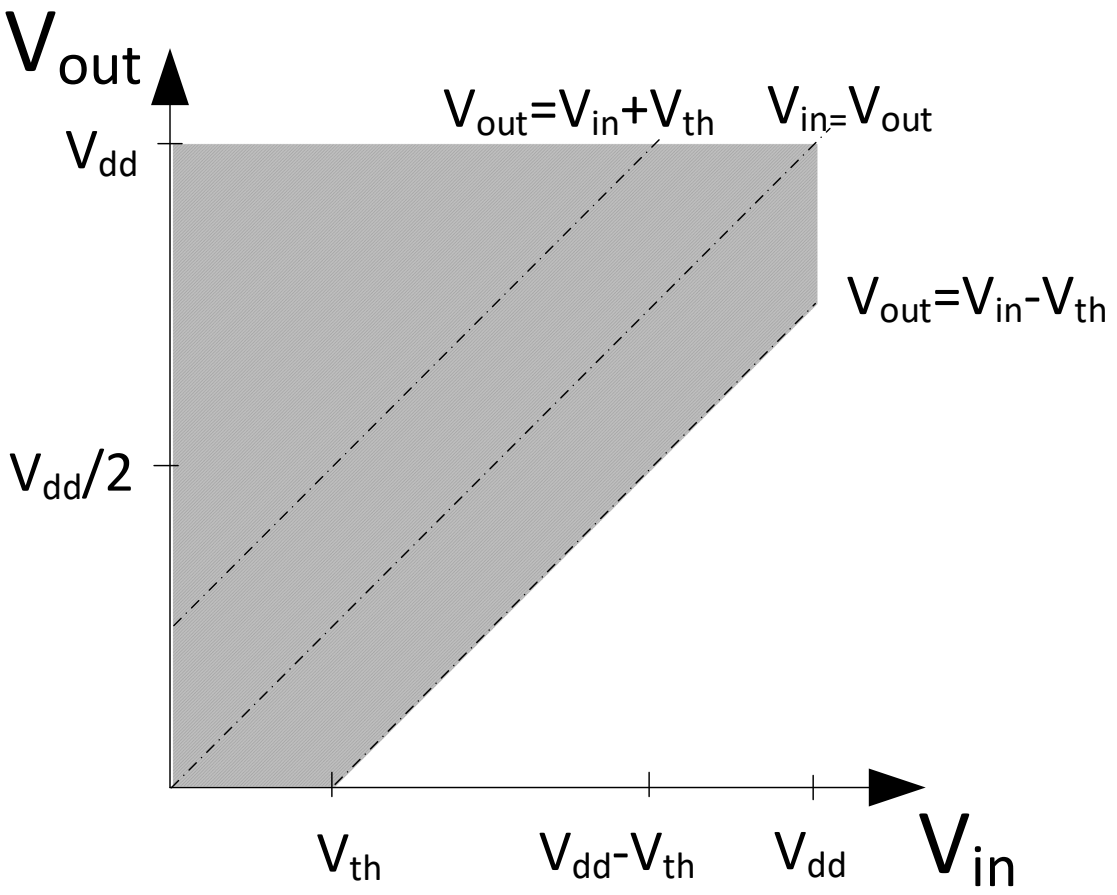

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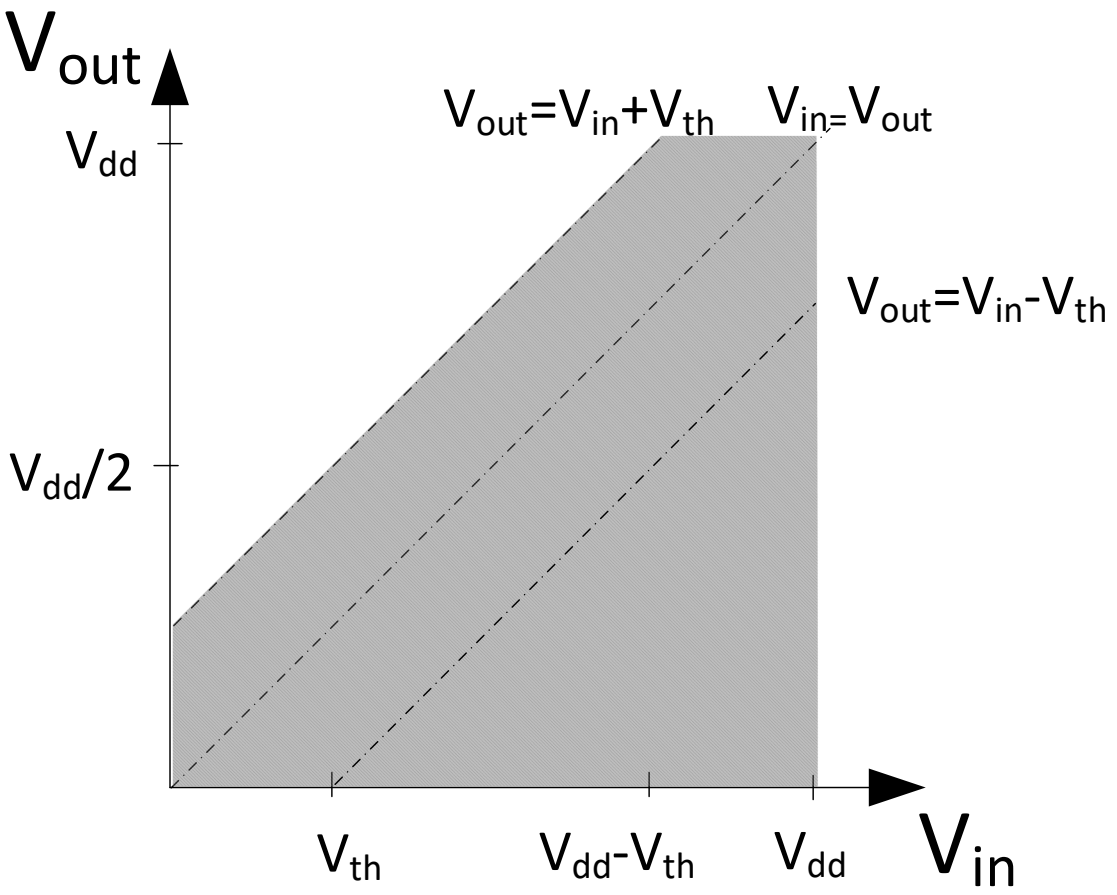

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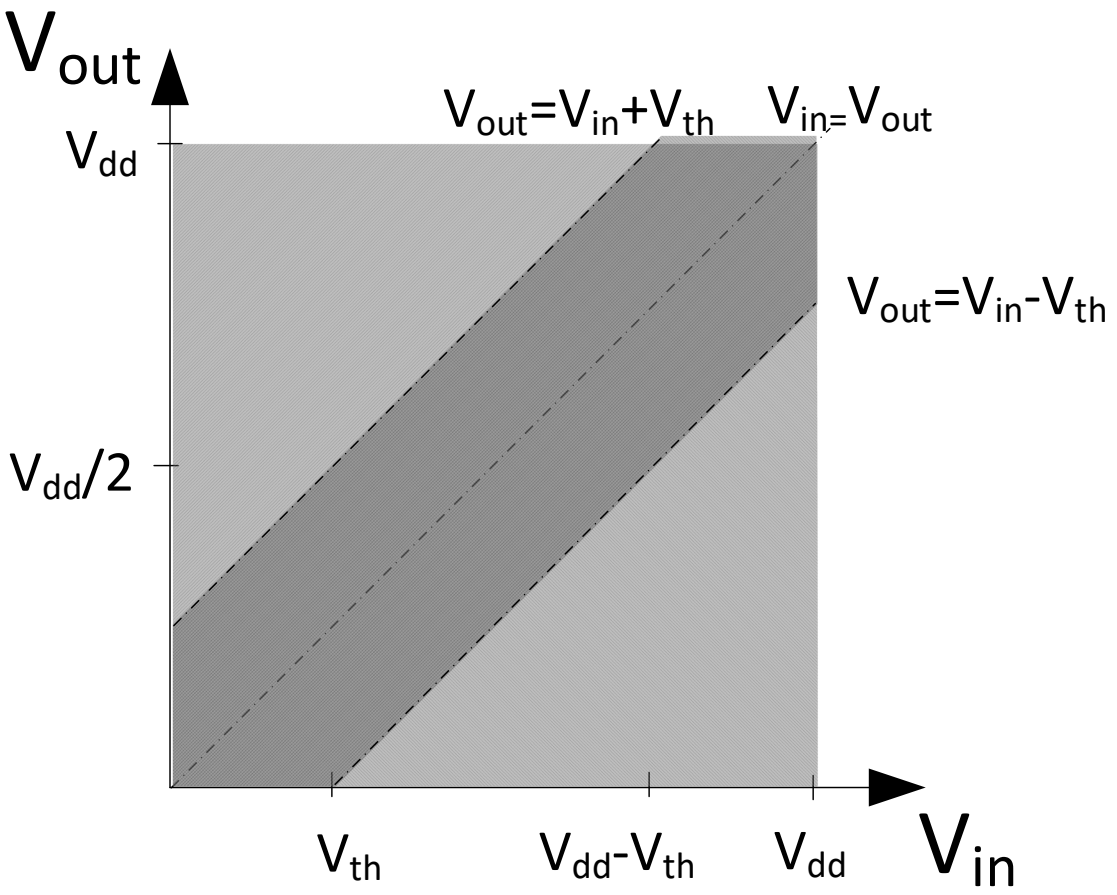

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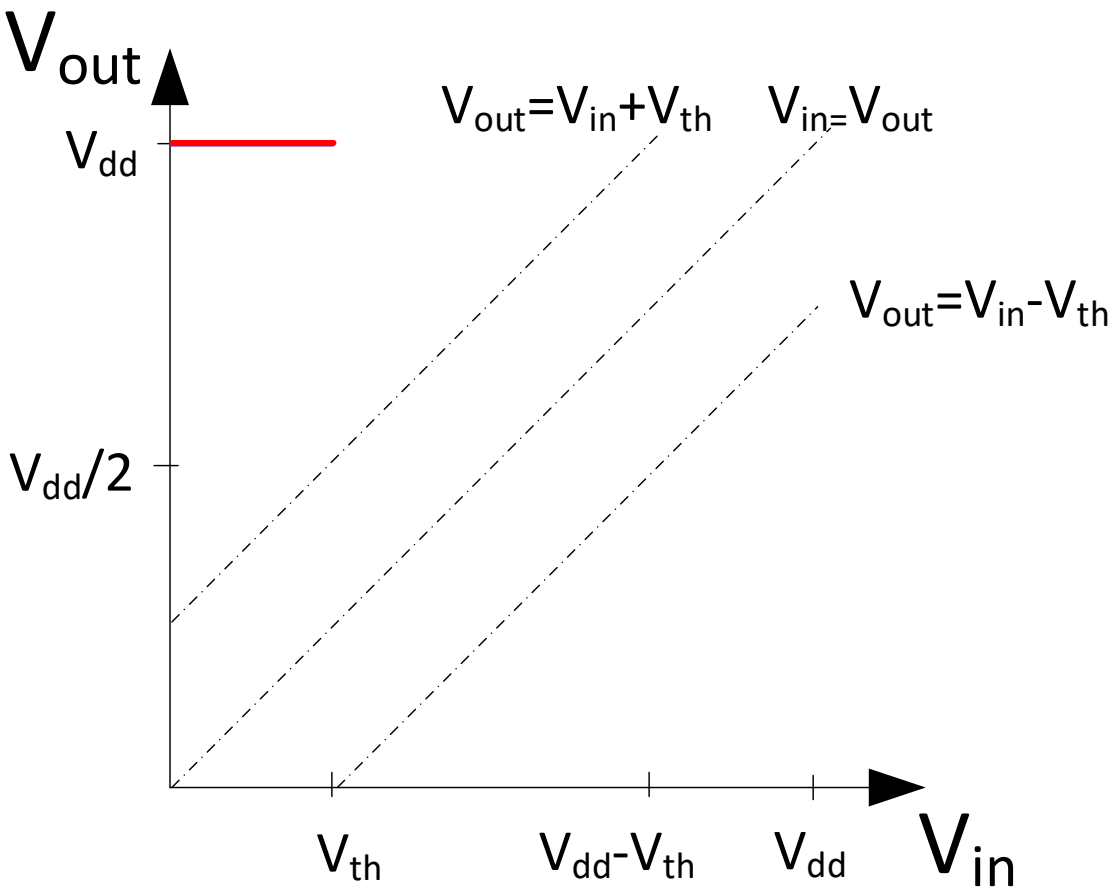
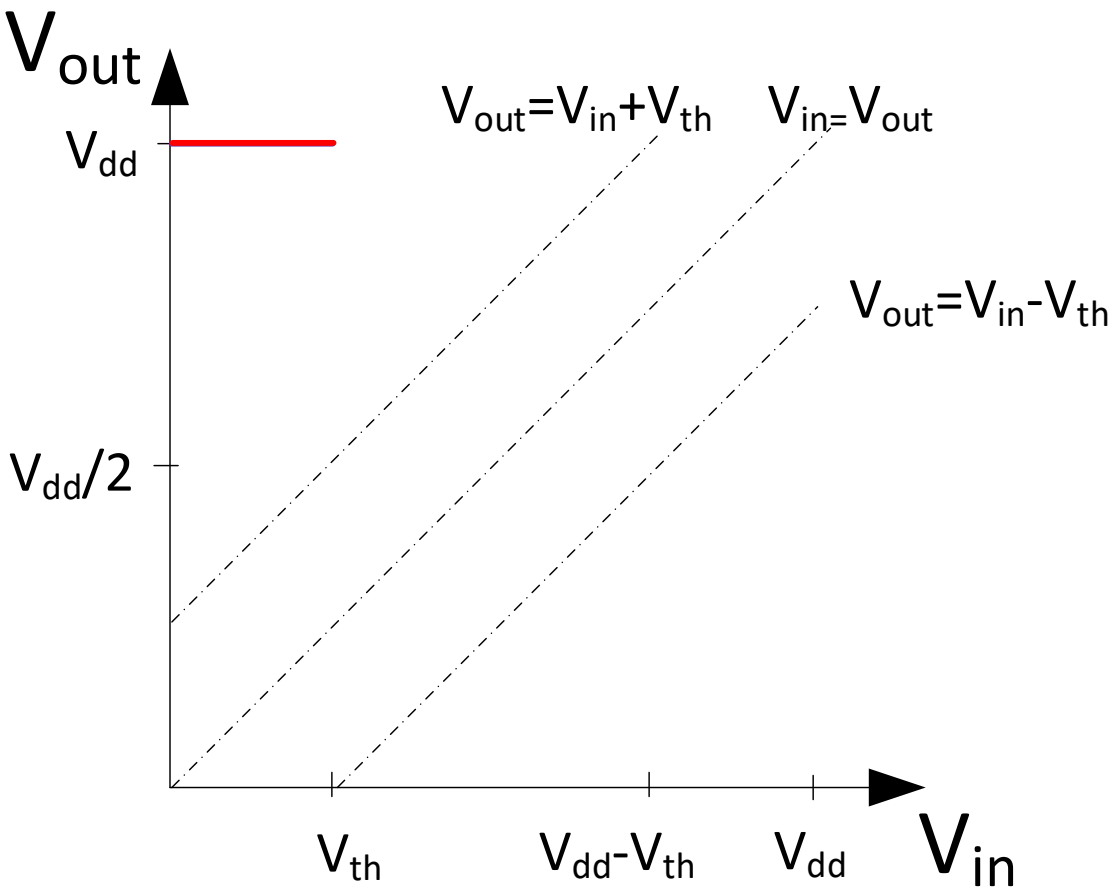


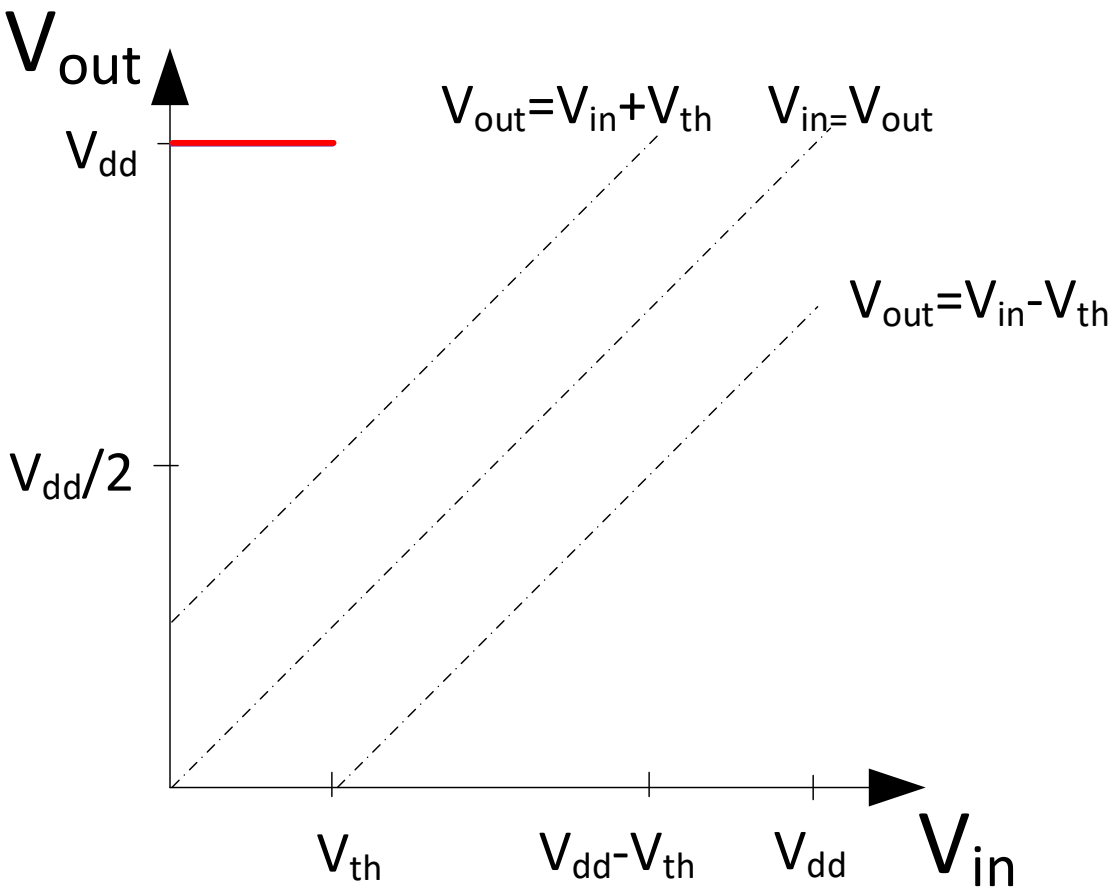
- $V_{in} = 0$

Inverter DC Analysis



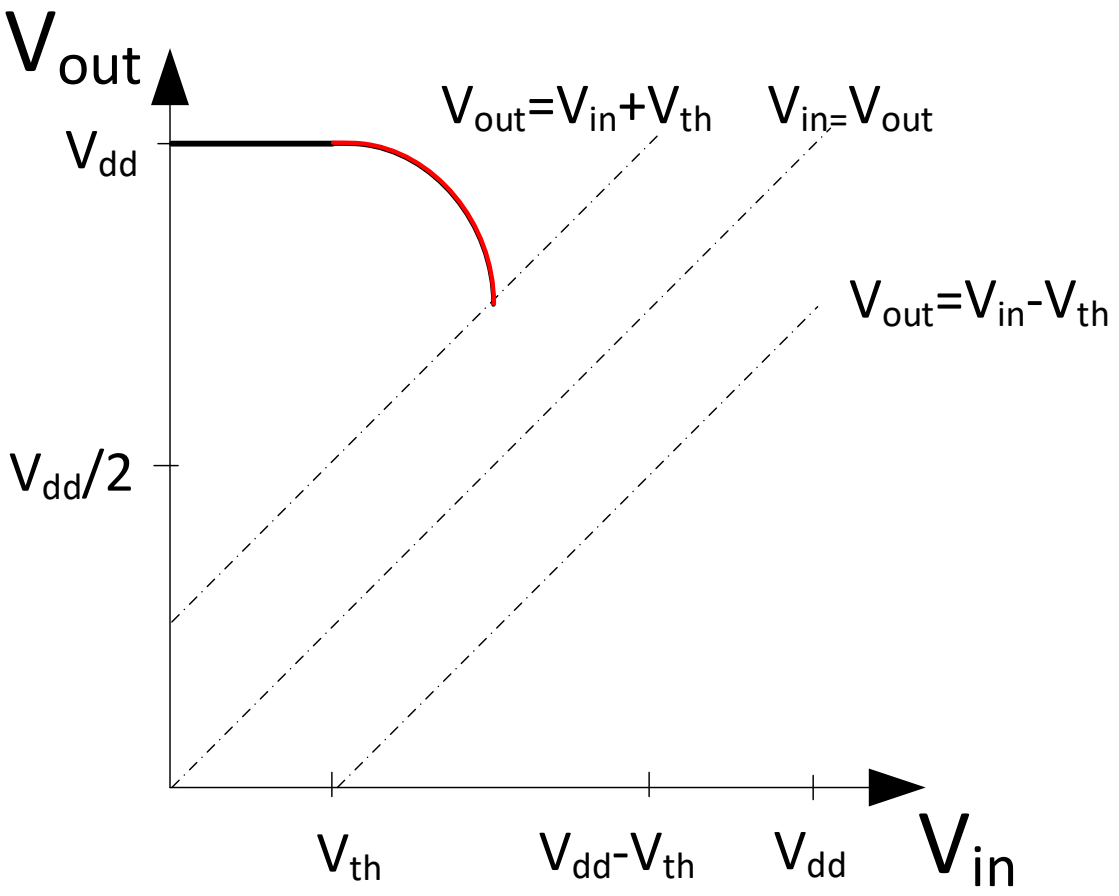
- V_{in} = 0 → Nmos in cutoff

Inverter DC Analysis



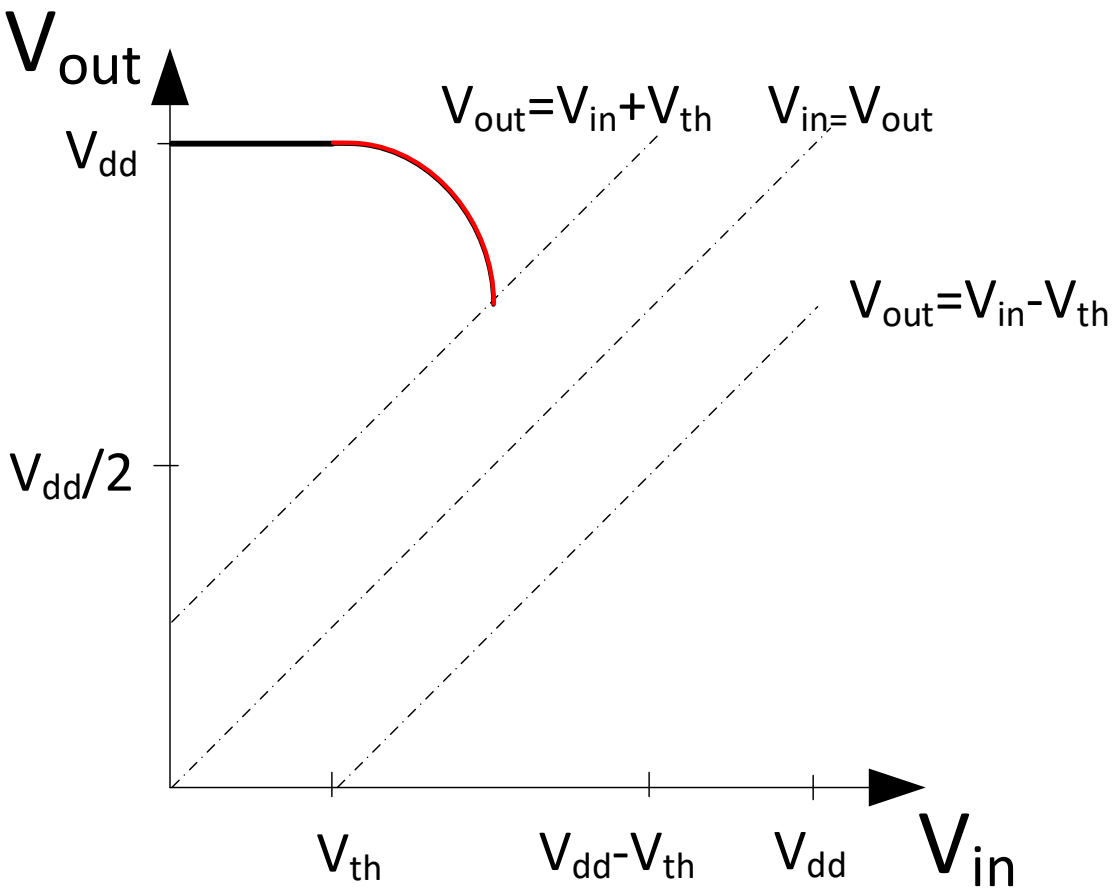
- V_{in} = 0 → Nmos in cutoff →Pmos in linear

Inverter DC Analysis



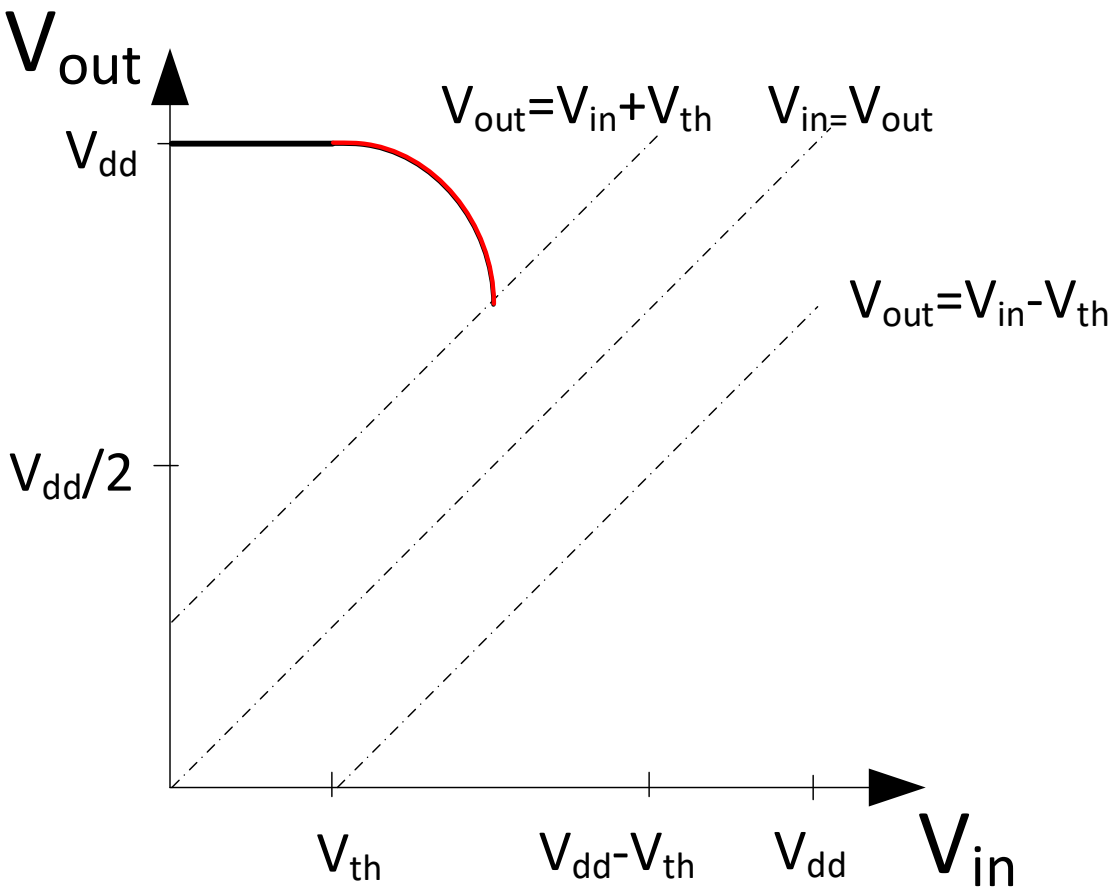
- $V_{th} < V_{in} < V_{out} - V_{th}$

Inverter DC Analysis



- $V_{th} < V_{in} < V_{out} - V_{th}$
  - Nmos turns on in saturation

Inverter DC Analysis



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  - Nmos turns on in saturation
  - Pmos in linear

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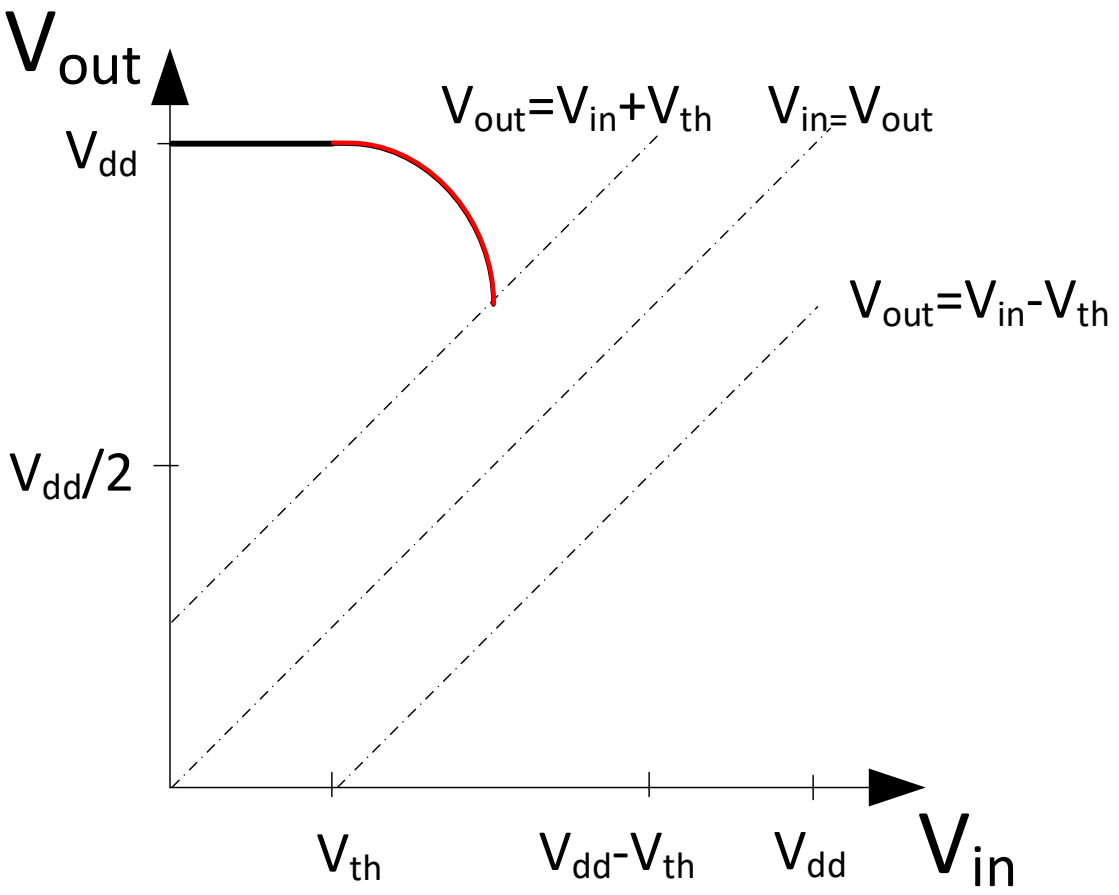
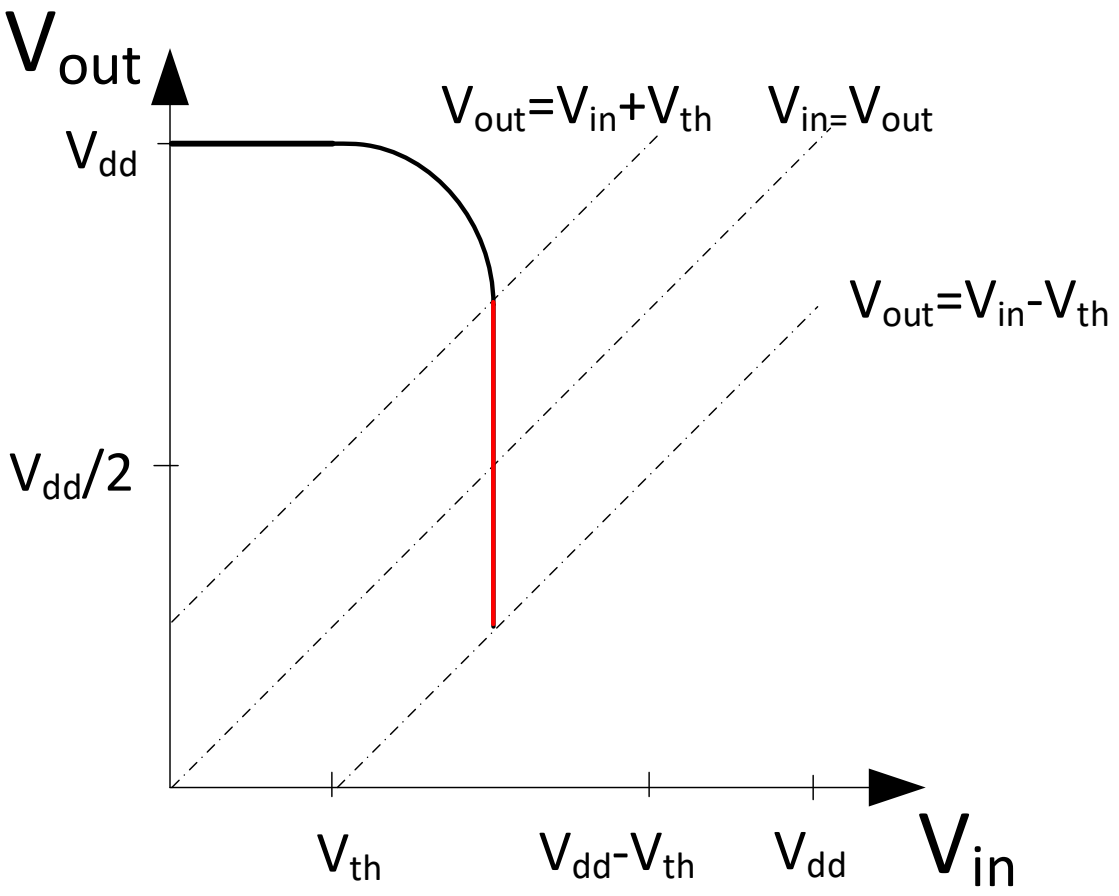


- $V_{th} < V_{in} < V_{out} - V_{th}$
  - Nmos turns on in saturation
  - Pmos in linear

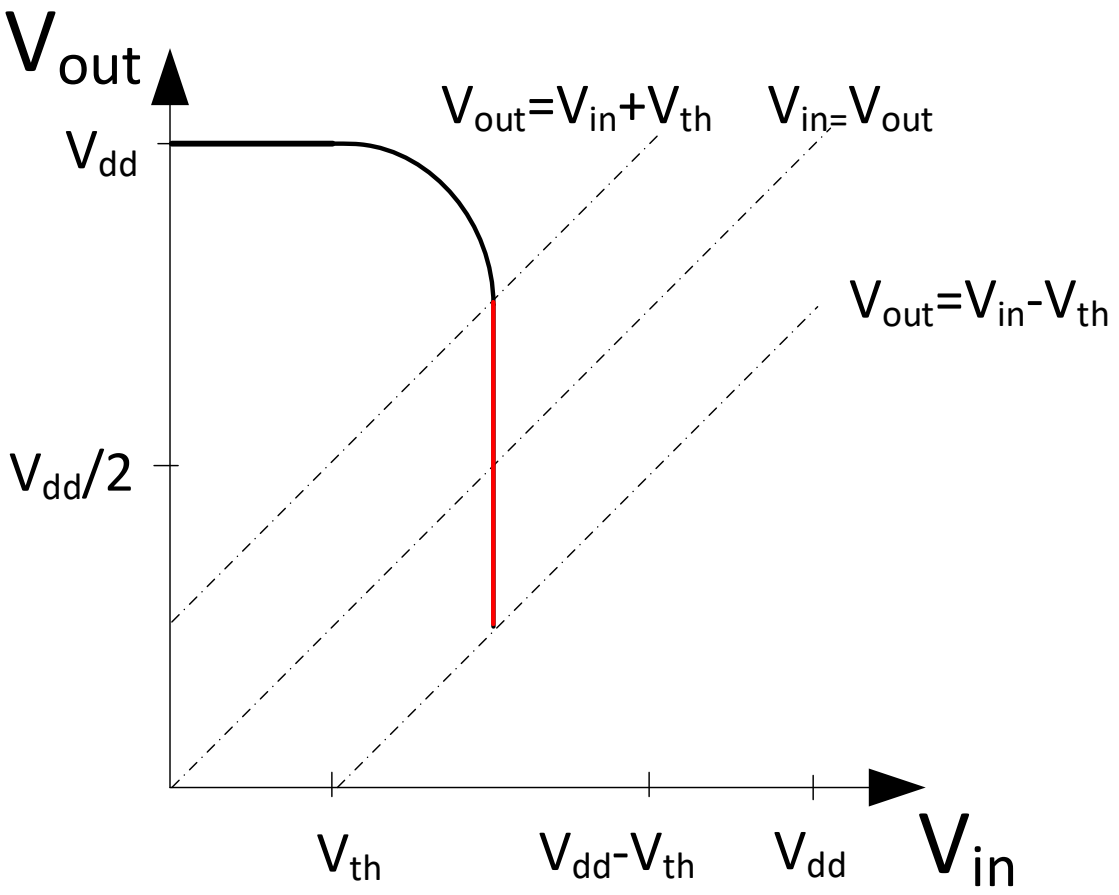
Analytically, approximate
The rate of descent of Vout.
(sub|super) (linear/quadratic/cubic)

Inverter DC Analysis



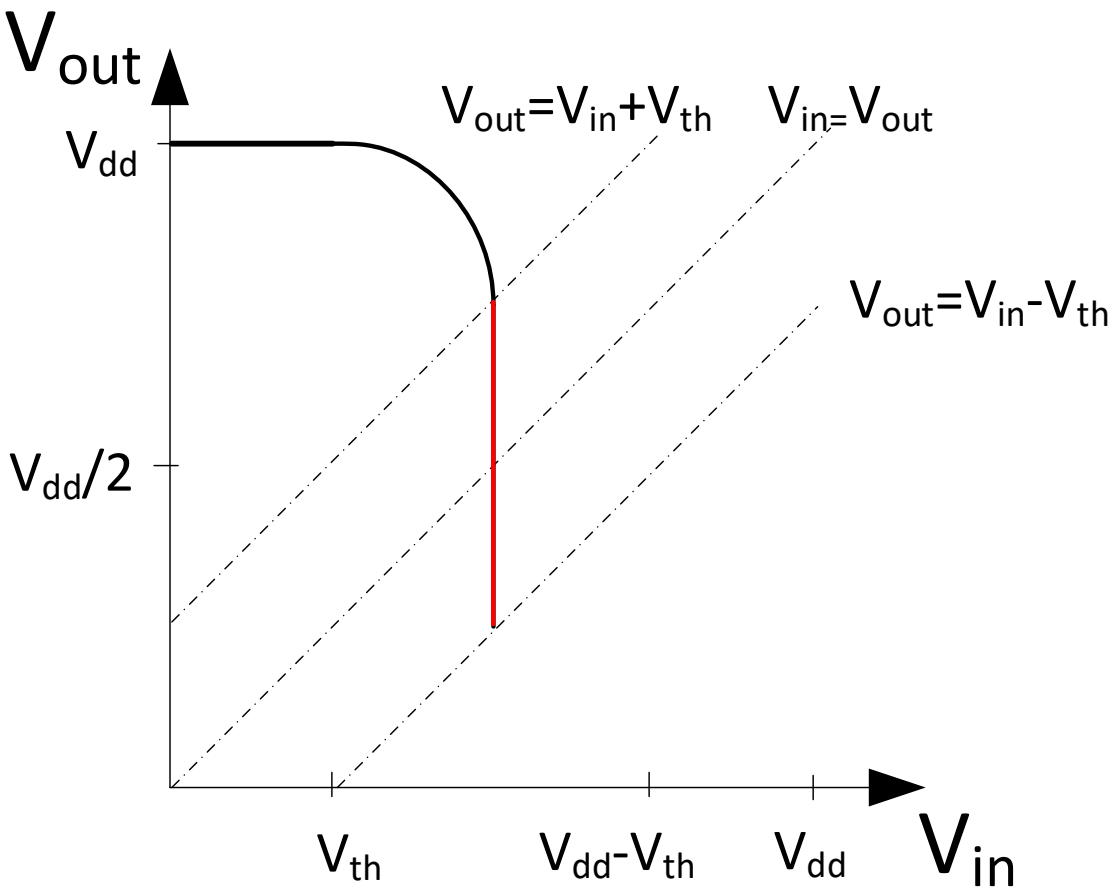
- $V_{out} - V_{th} < V_{in} < V_{out} + V_{th}$

Inverter DC Analysis



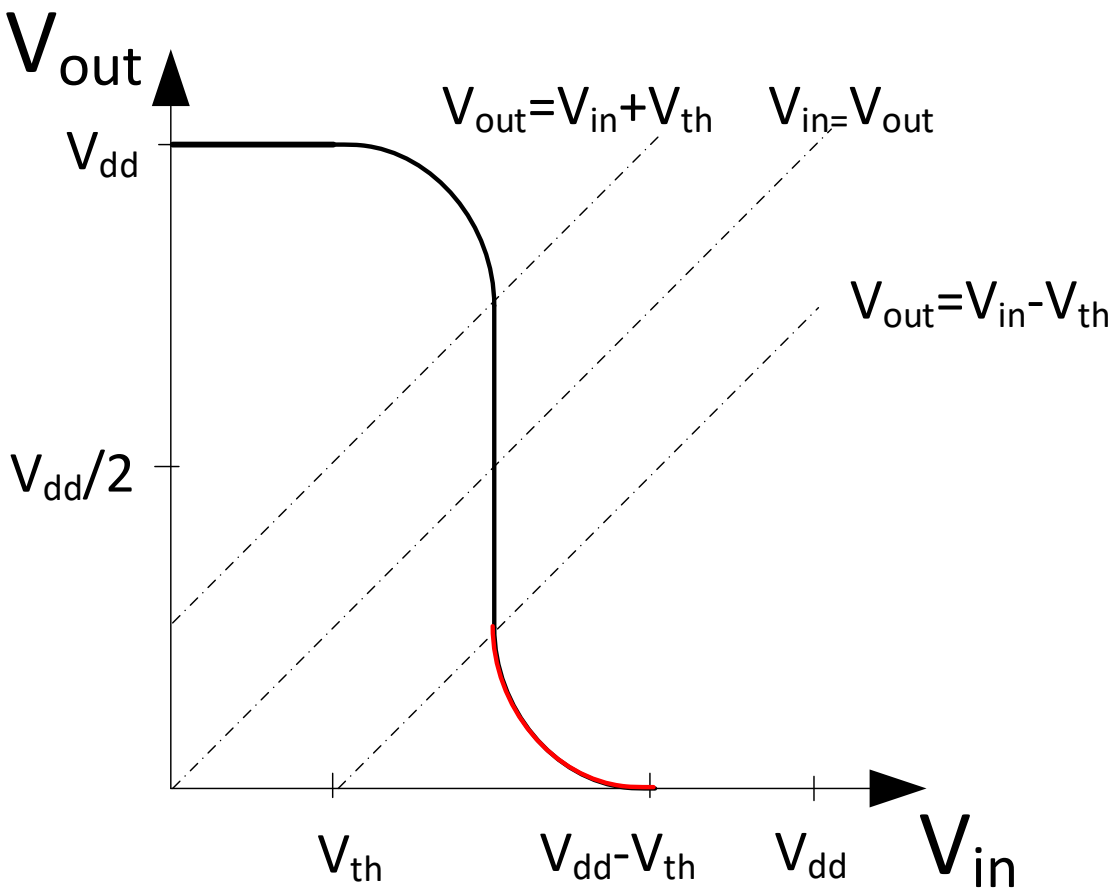
- $V_{out} - V_{th} < V_{in} < V_{out} + V_{th}$
  - Nmos remains in saturation

Inverter DC Analysis



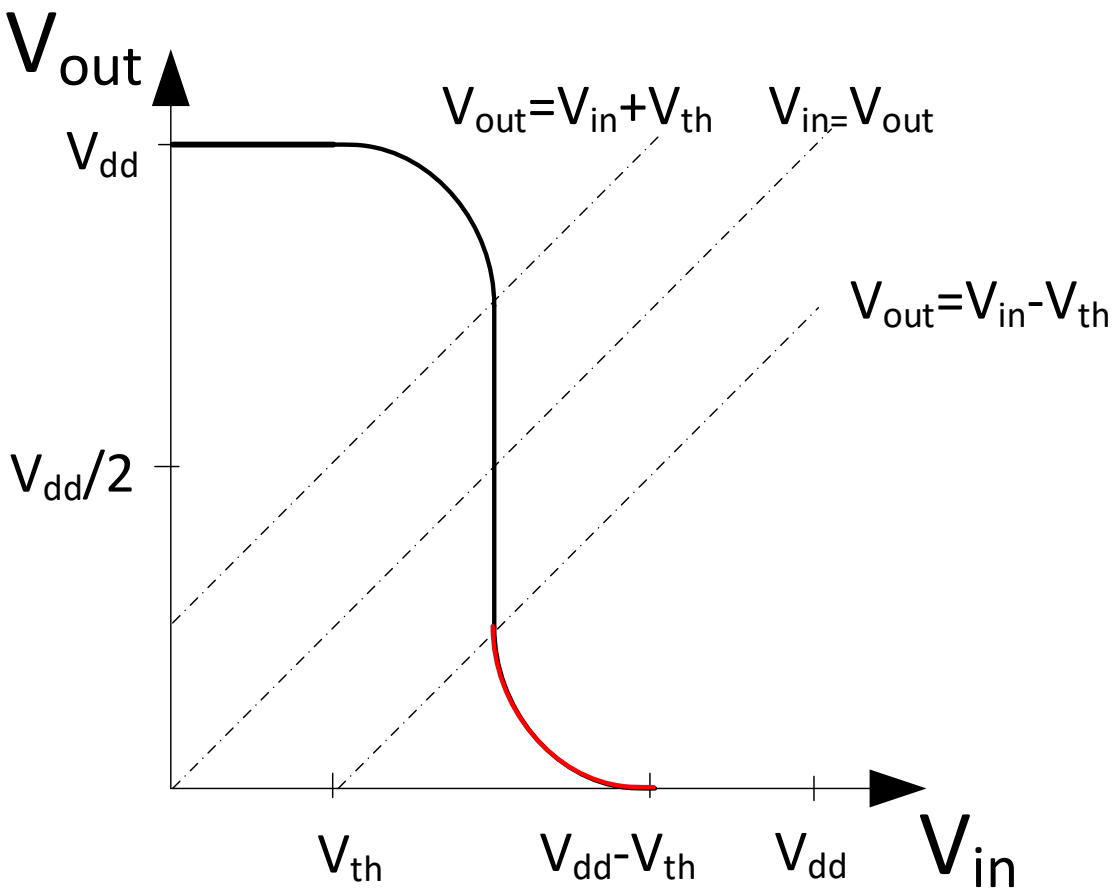
- $V_{out} - V_{th} < V_{in} < V_{out} + V_{th}$
  - Nmos remains in saturation
  - Pmos transitions to saturation

Inverter DC Analysis



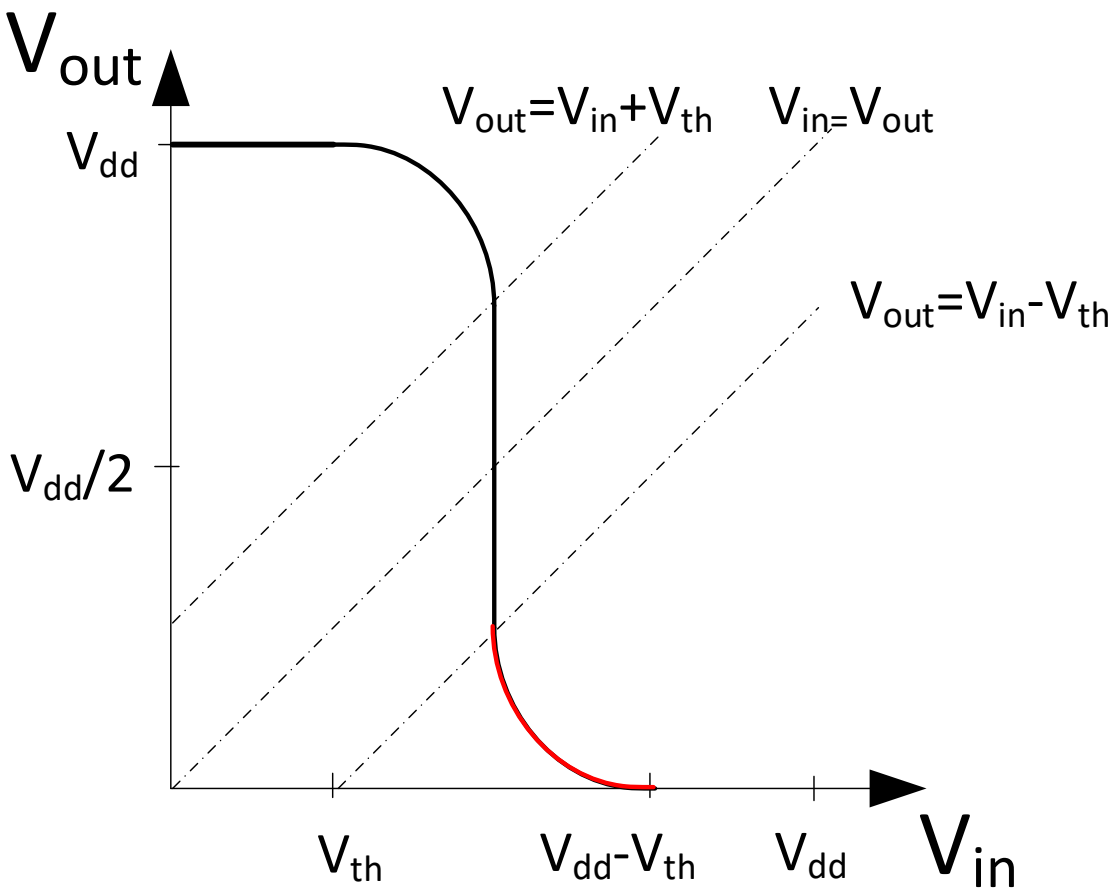
- $V_{out} + V_{th} < V_{in} < V_{dd} - V_{th}$

Inverter DC Analysis



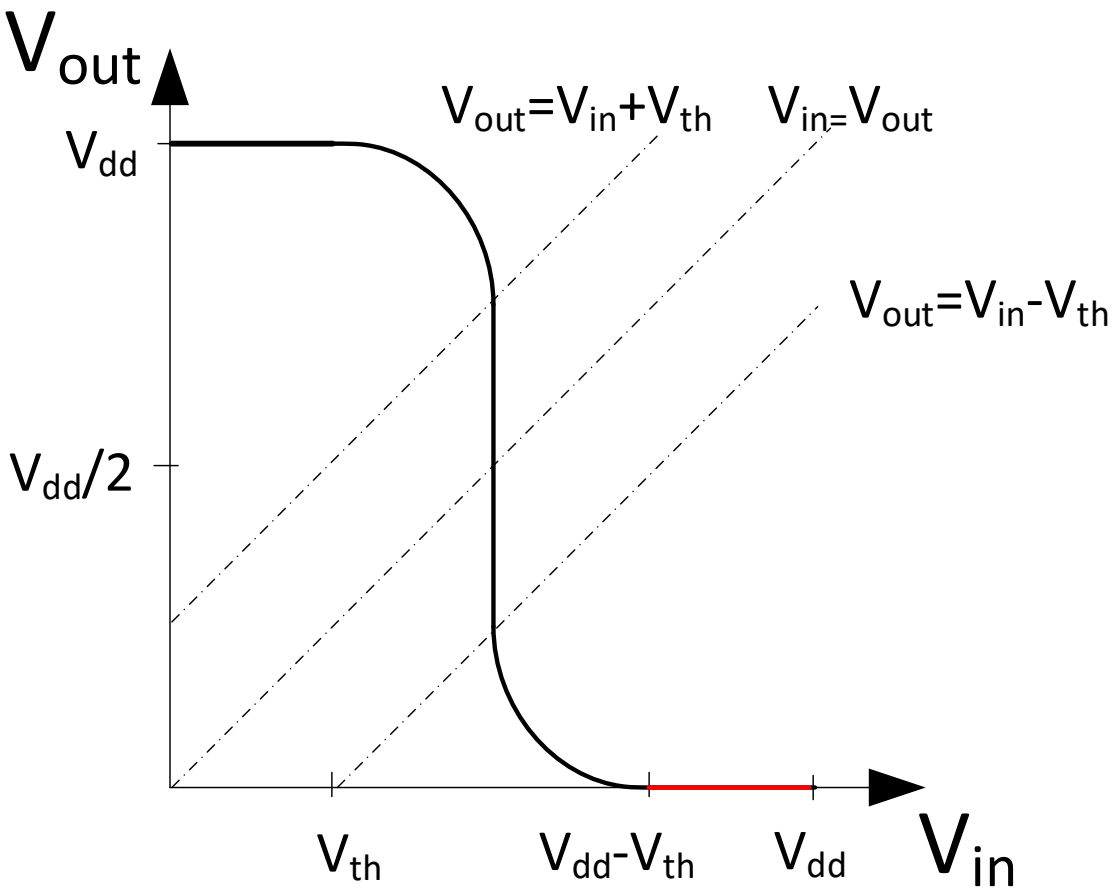
- $V_{out} + V_{th} < V_{in} < V_{dd} - V_{th}$
  - Nmos transitions to linear

Inverter DC Analysis



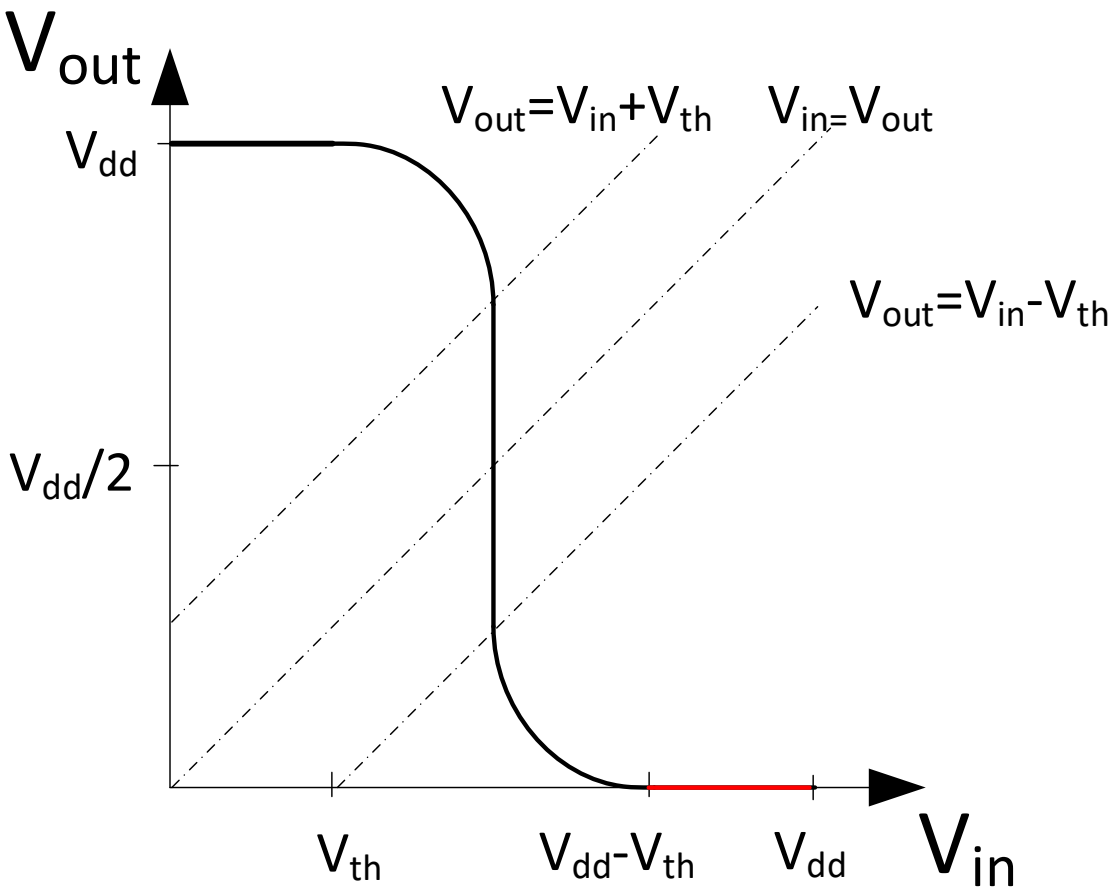
- $V_{out} + V_{th} < V_{in} < V_{dd} - V_{th}$
  - Nmos transitions to linear
  - Pmos remains in saturation

Inverter DC Analysis



- $V_{dd} - V_{th} < V_{in} < V_{dd}$

Inverter DC Analysis



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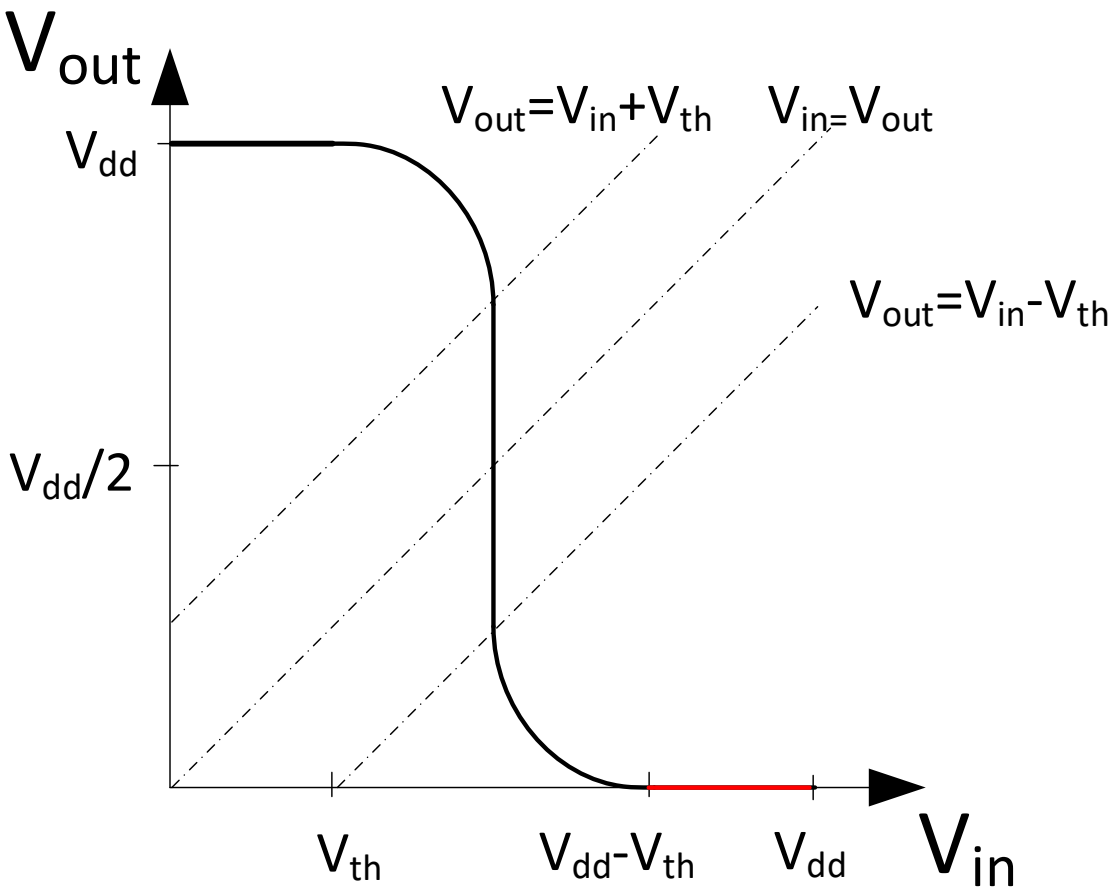
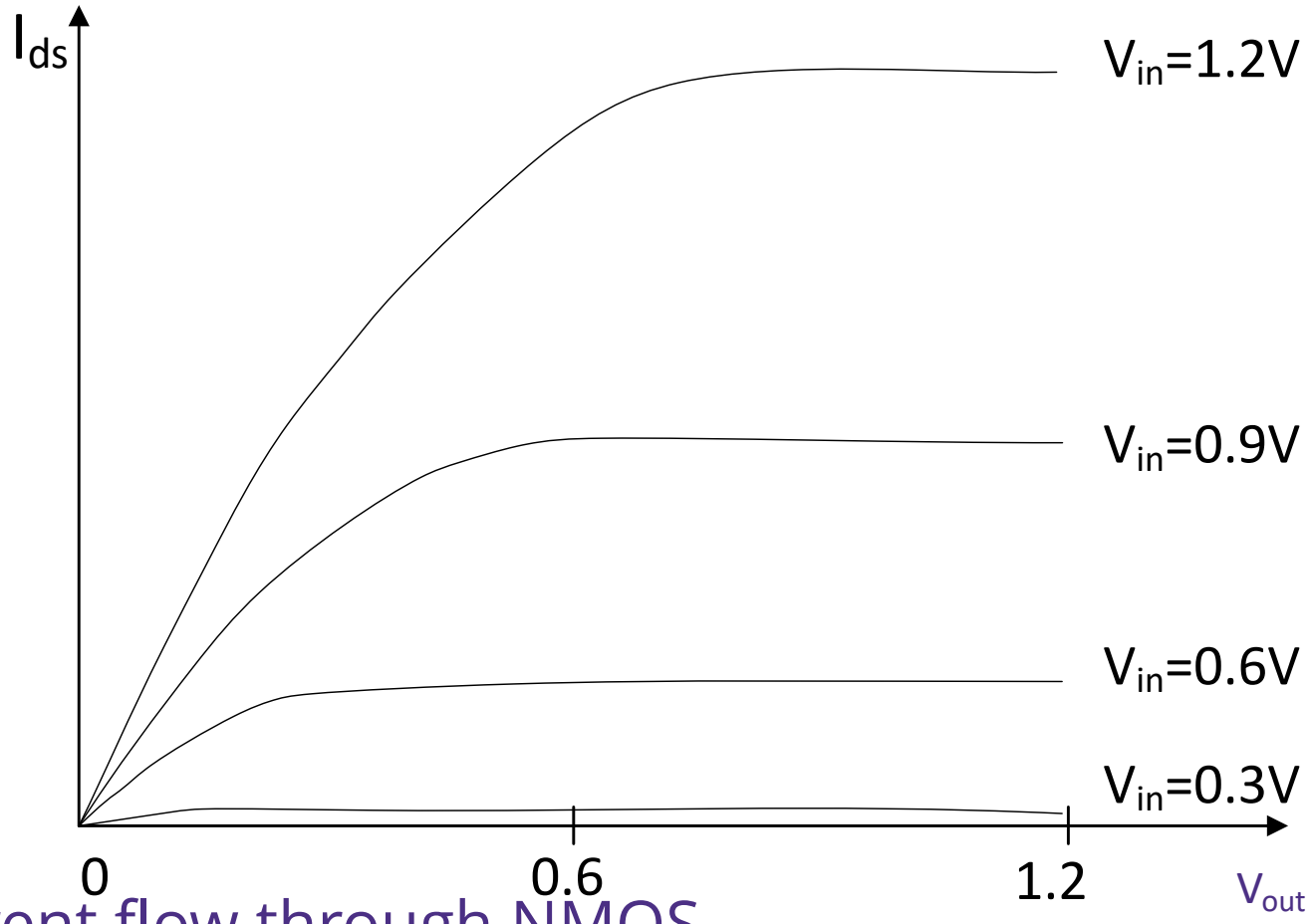
Inverter DC Analysis



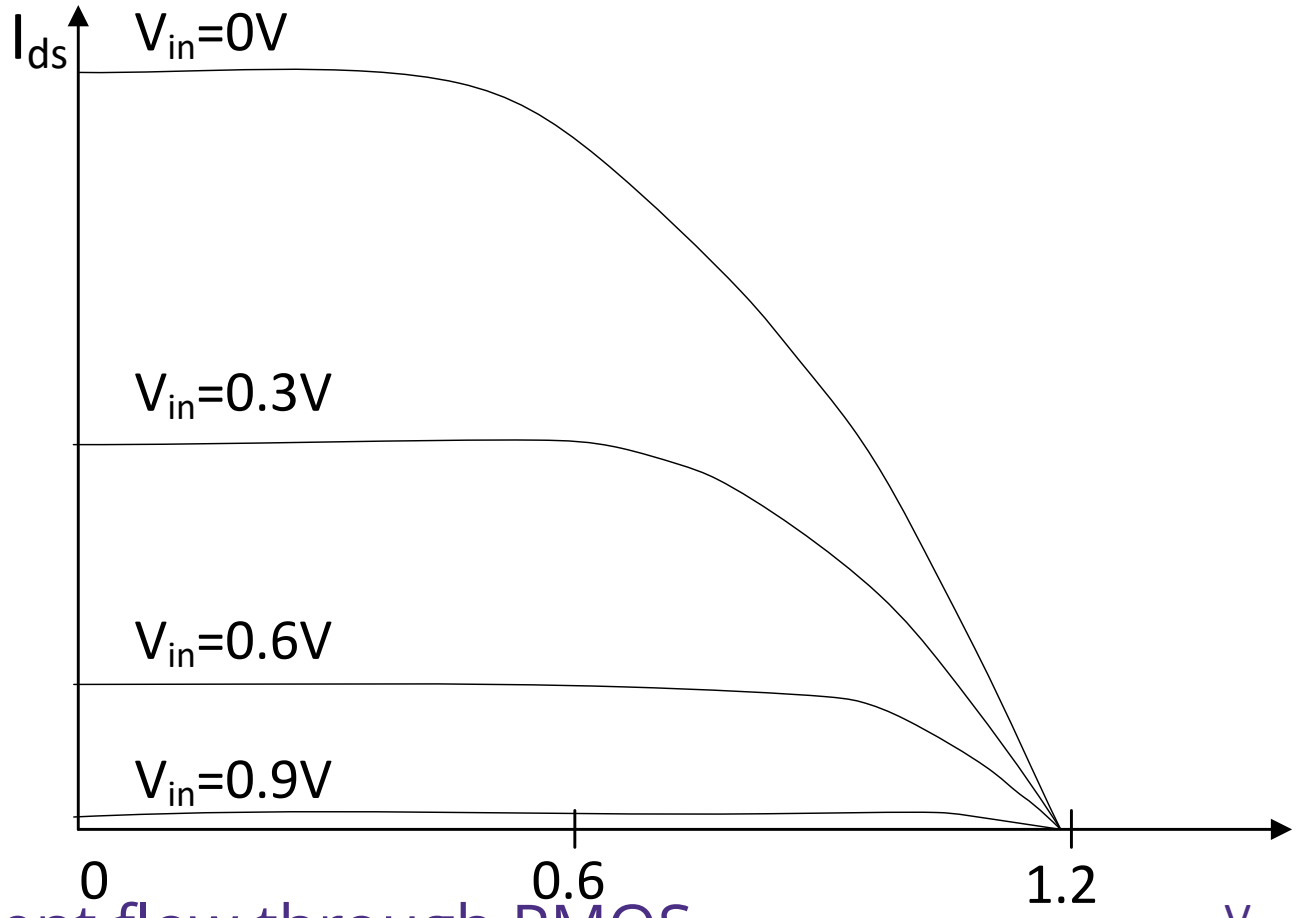
- $V_{dd} - V_{th} < V_{in} < V_{dd}$
  - Nmos remains in linear
  - Pmos transitions to cut-off

Graphical View: I_{ds} vs. V_{in}



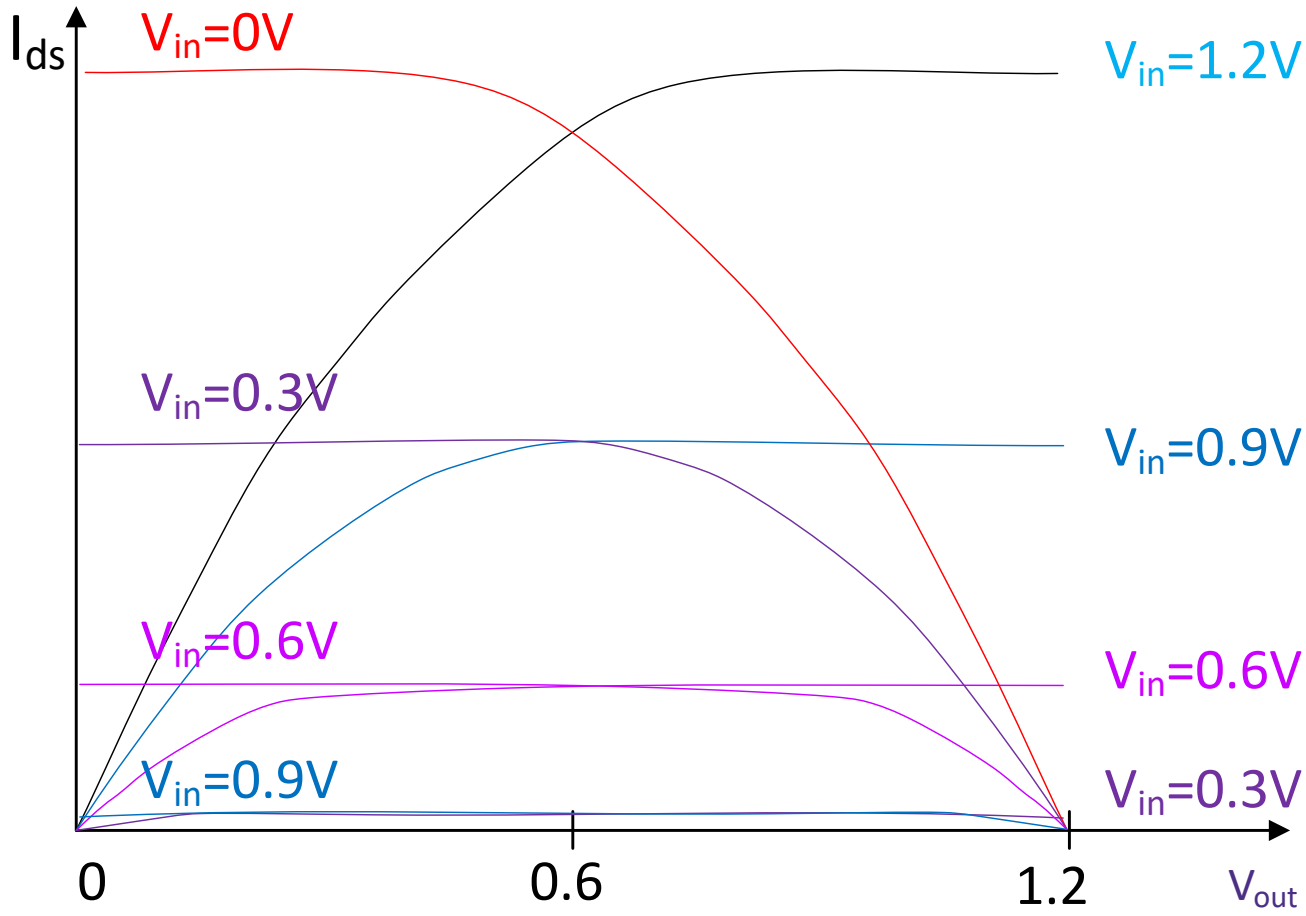
- Analyze the current flow through NMOS

Graphical View: I_{ds} vs. V_{out}



- Analyze the current flow through PMOS

Loadline Analysis



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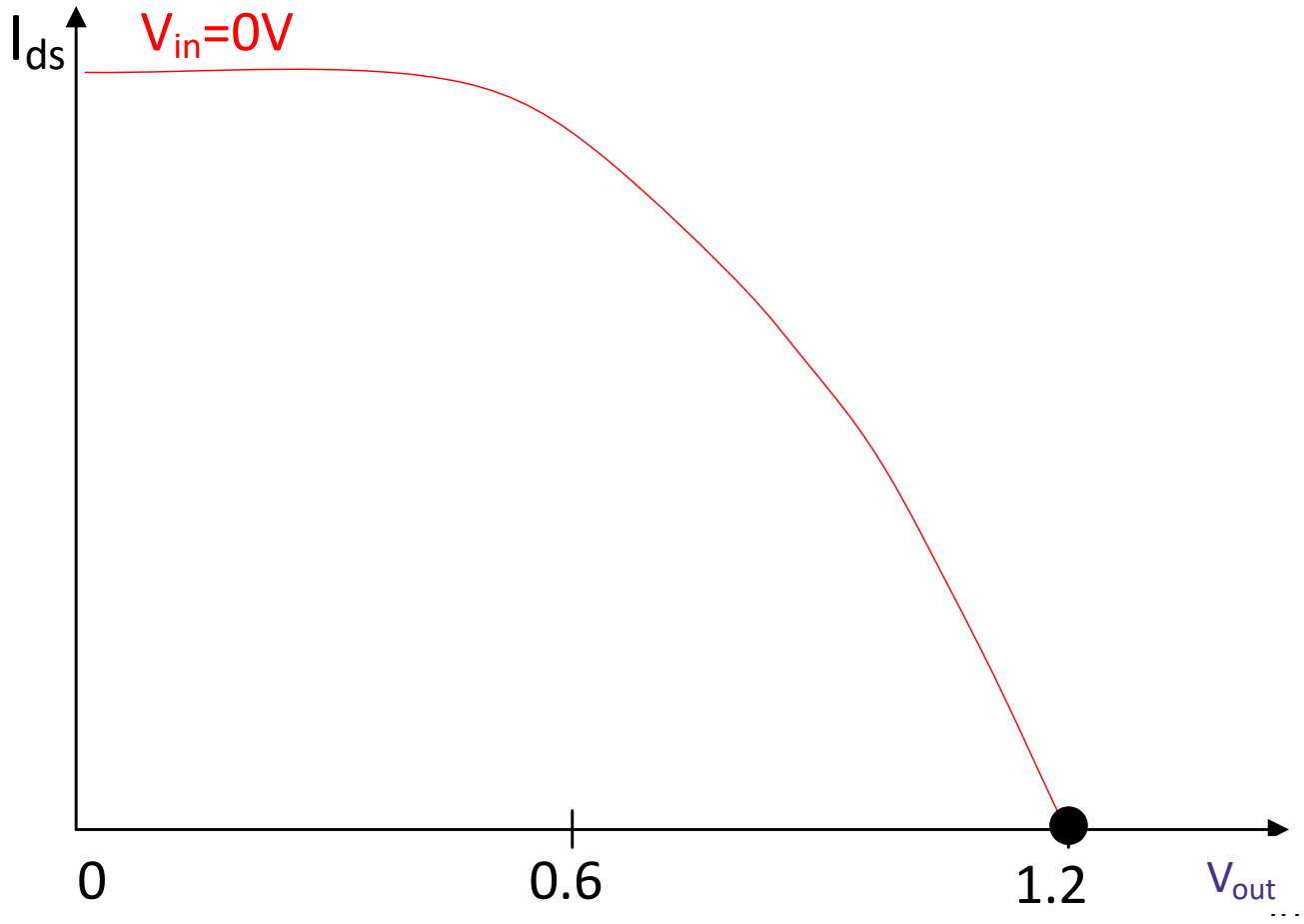

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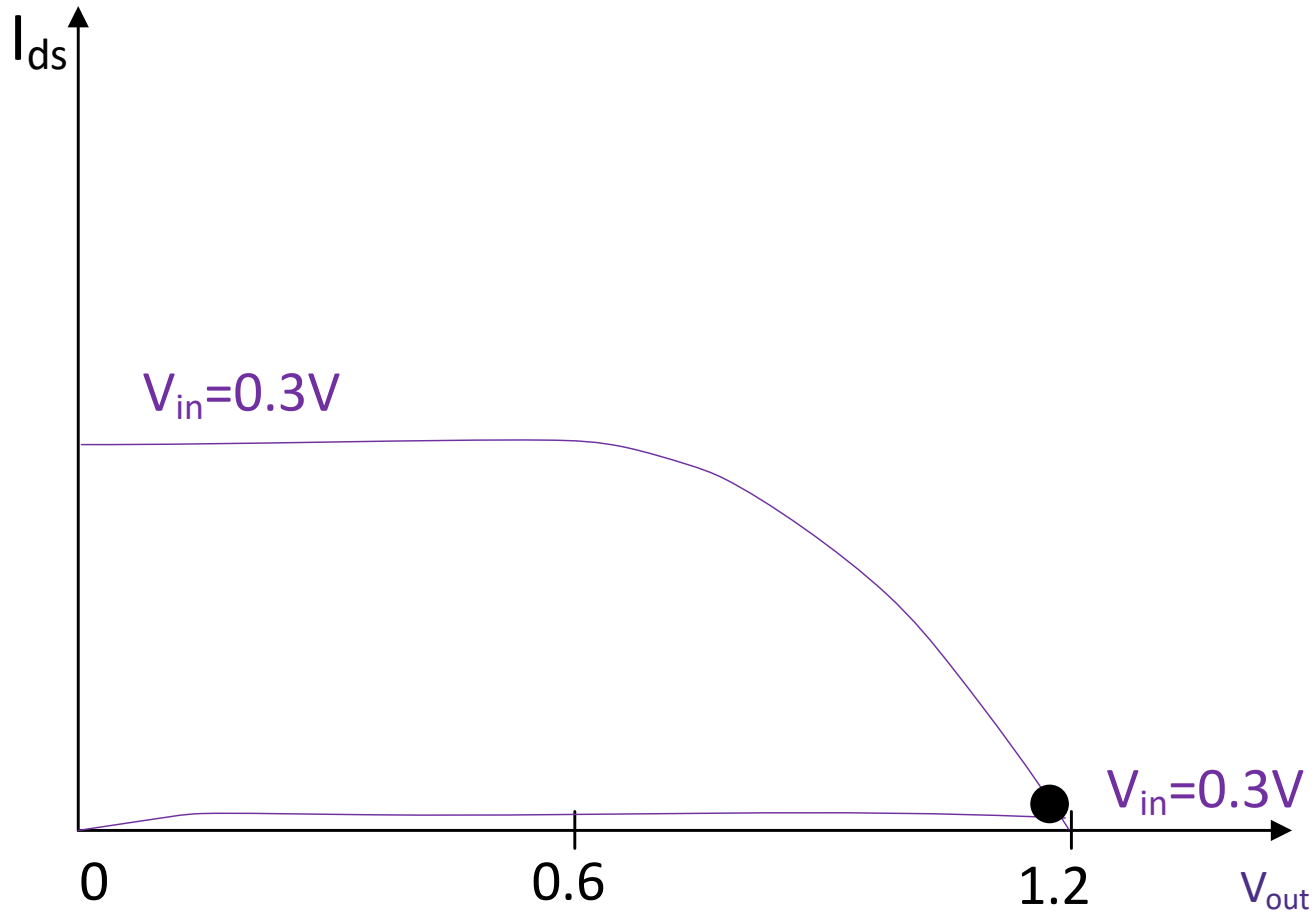

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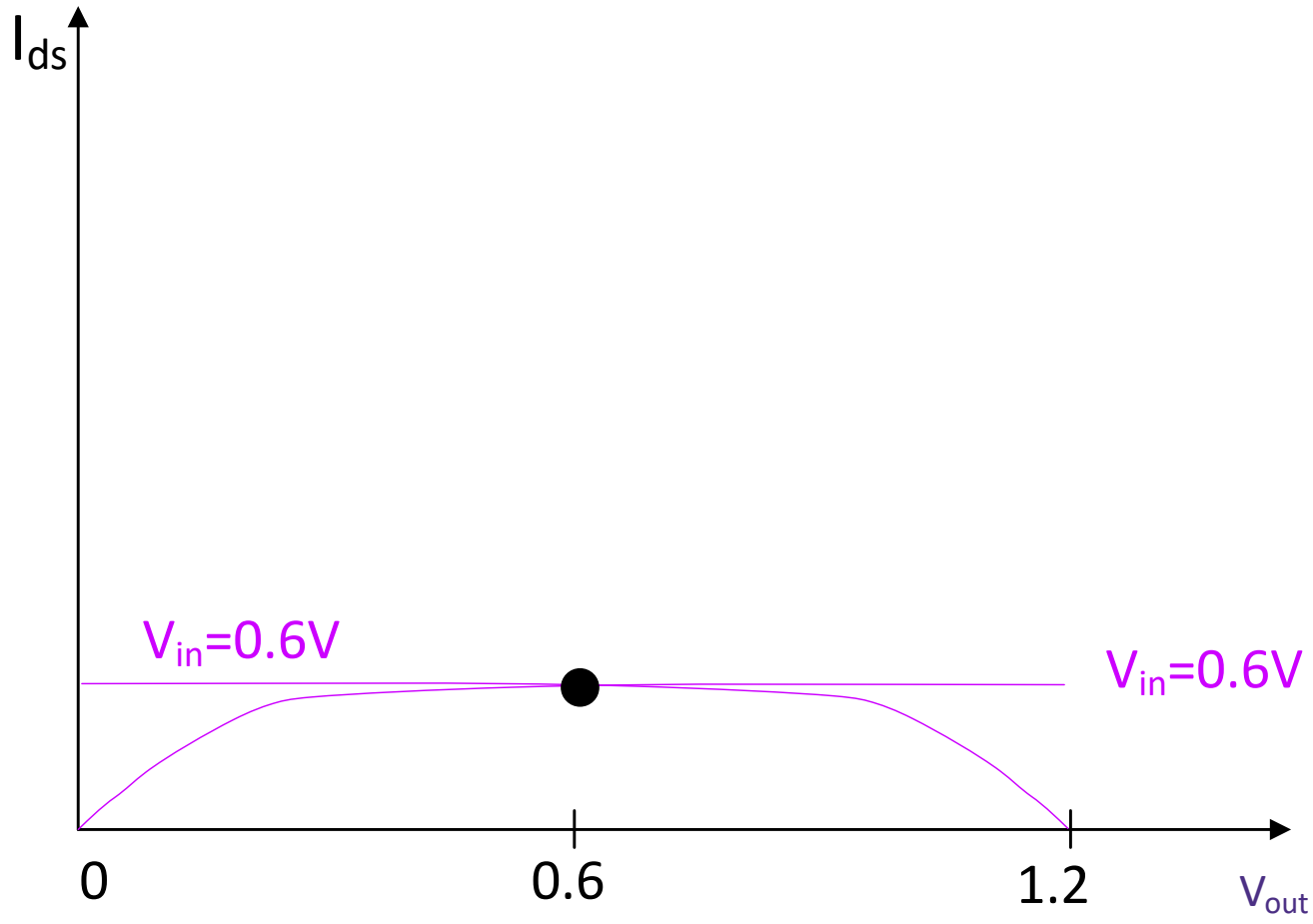
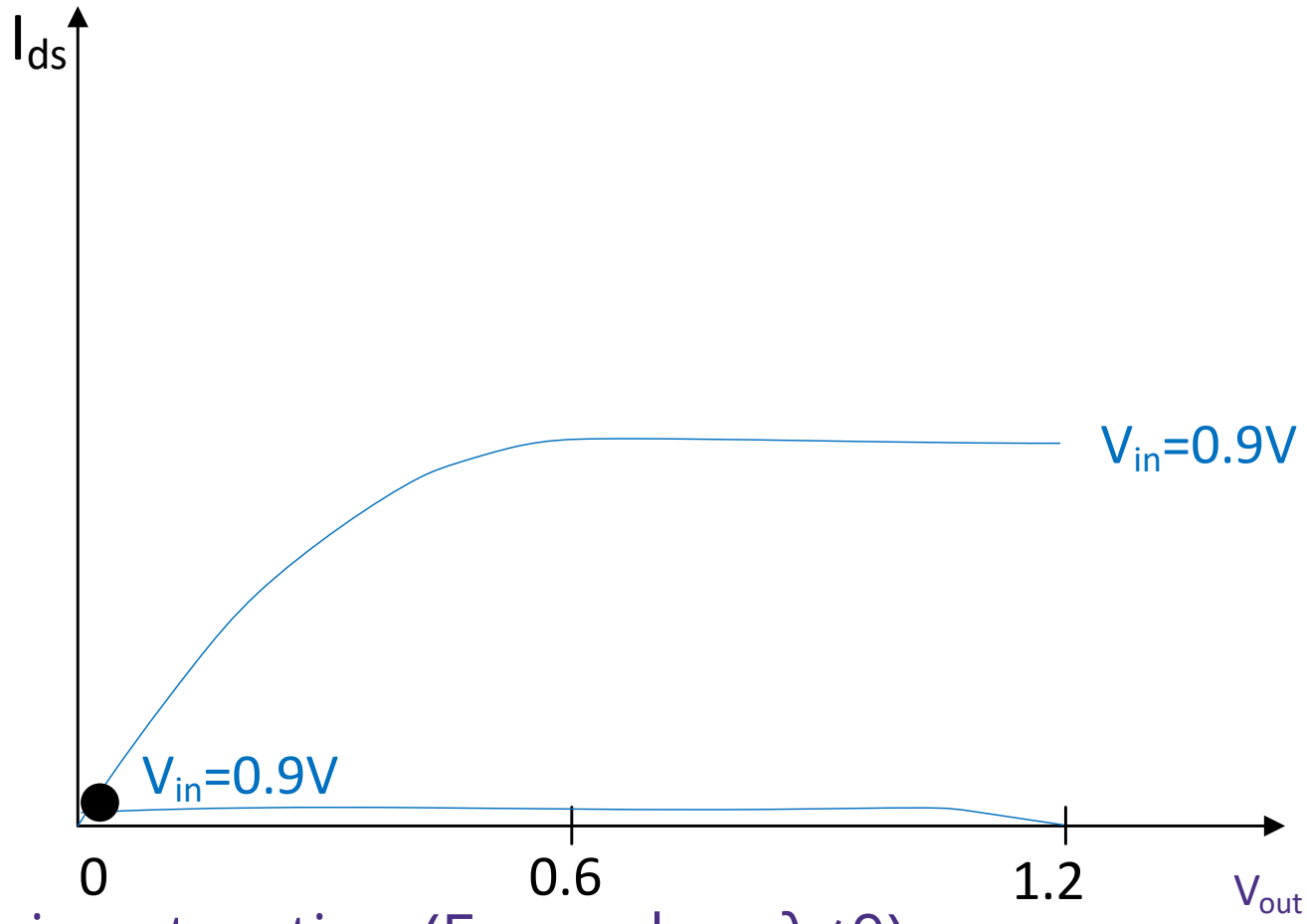


Current across the DC sweep



- Follow the device in saturation (Even when λ≠0)

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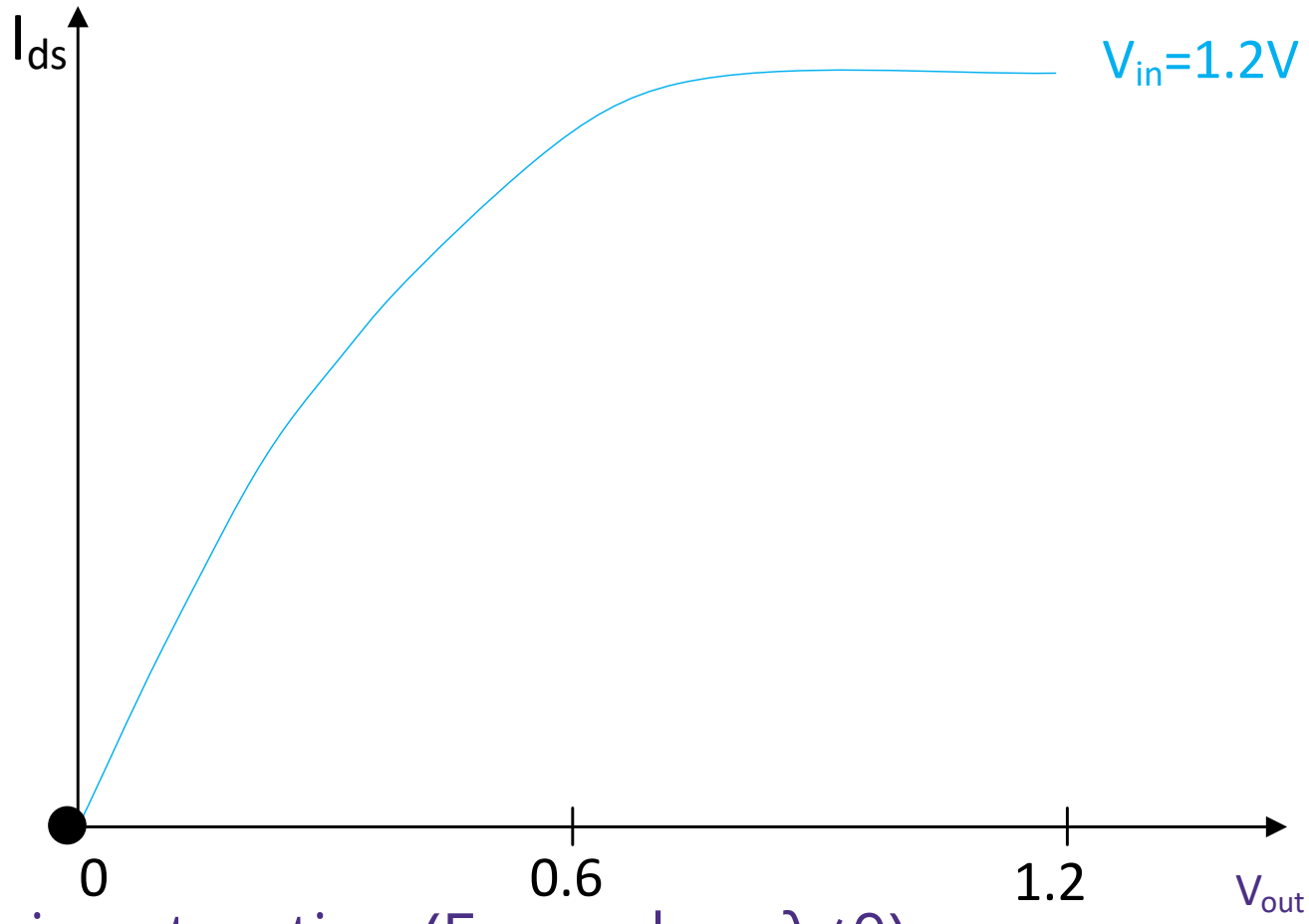

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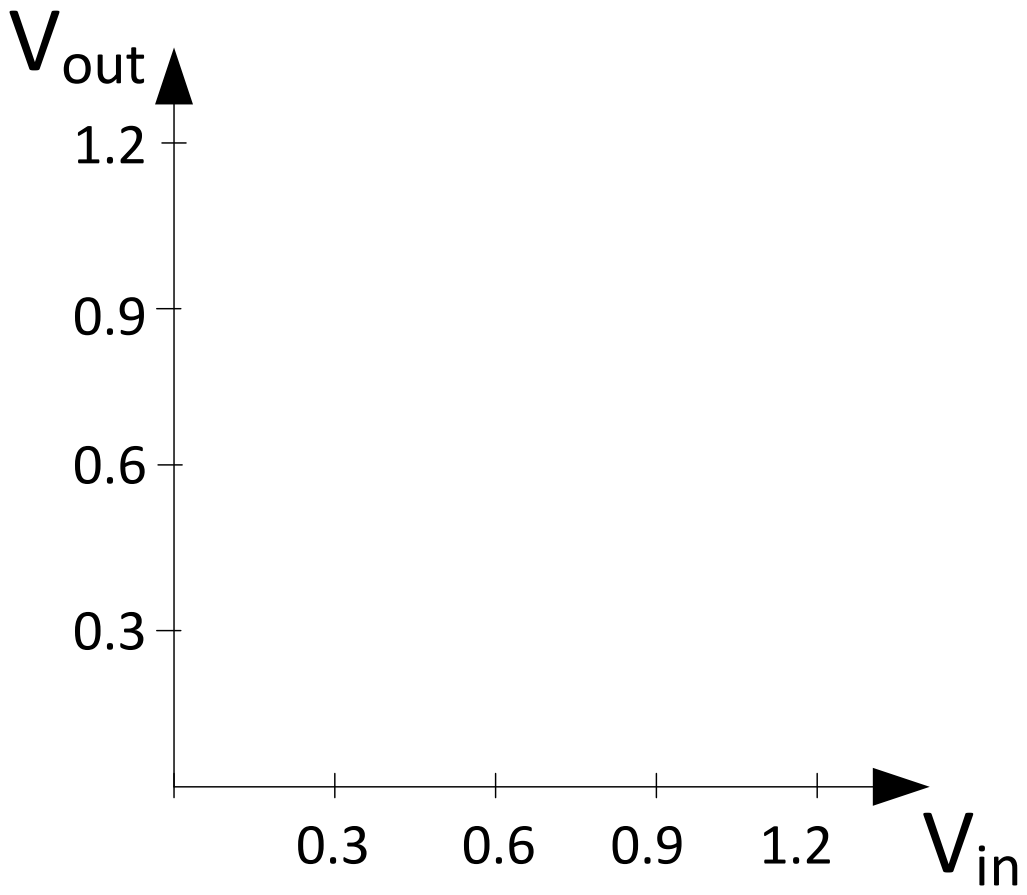

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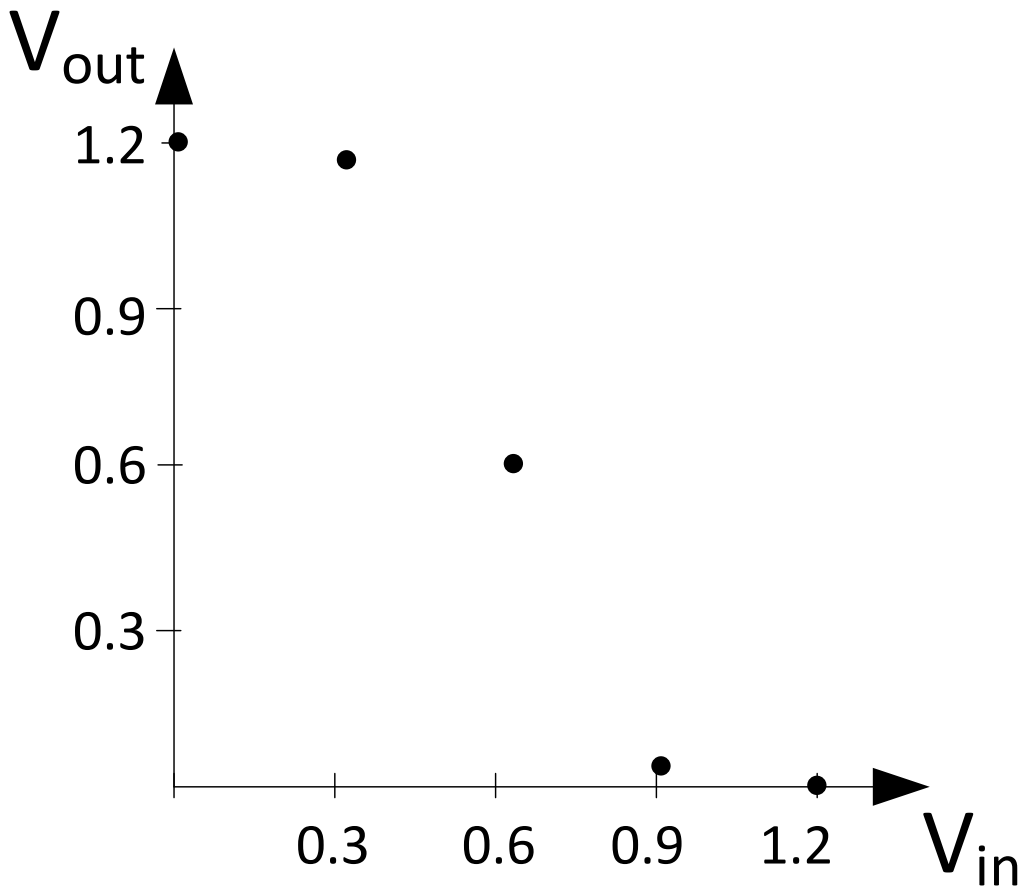

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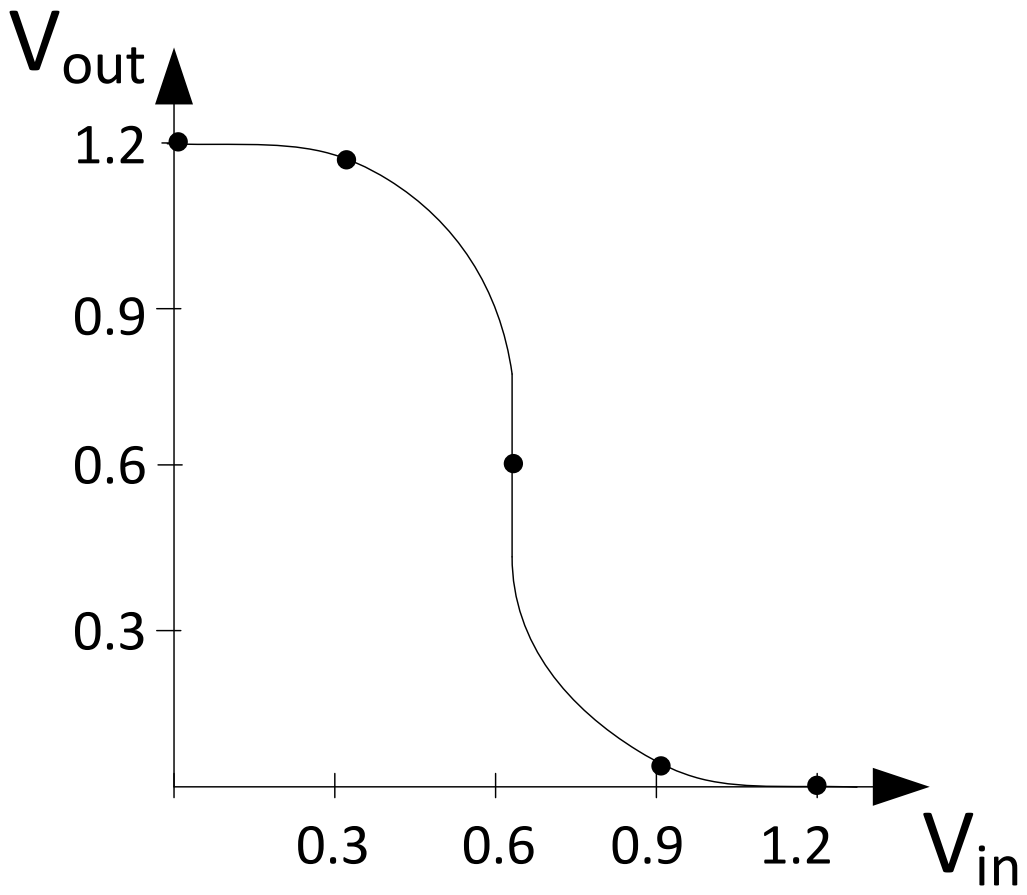
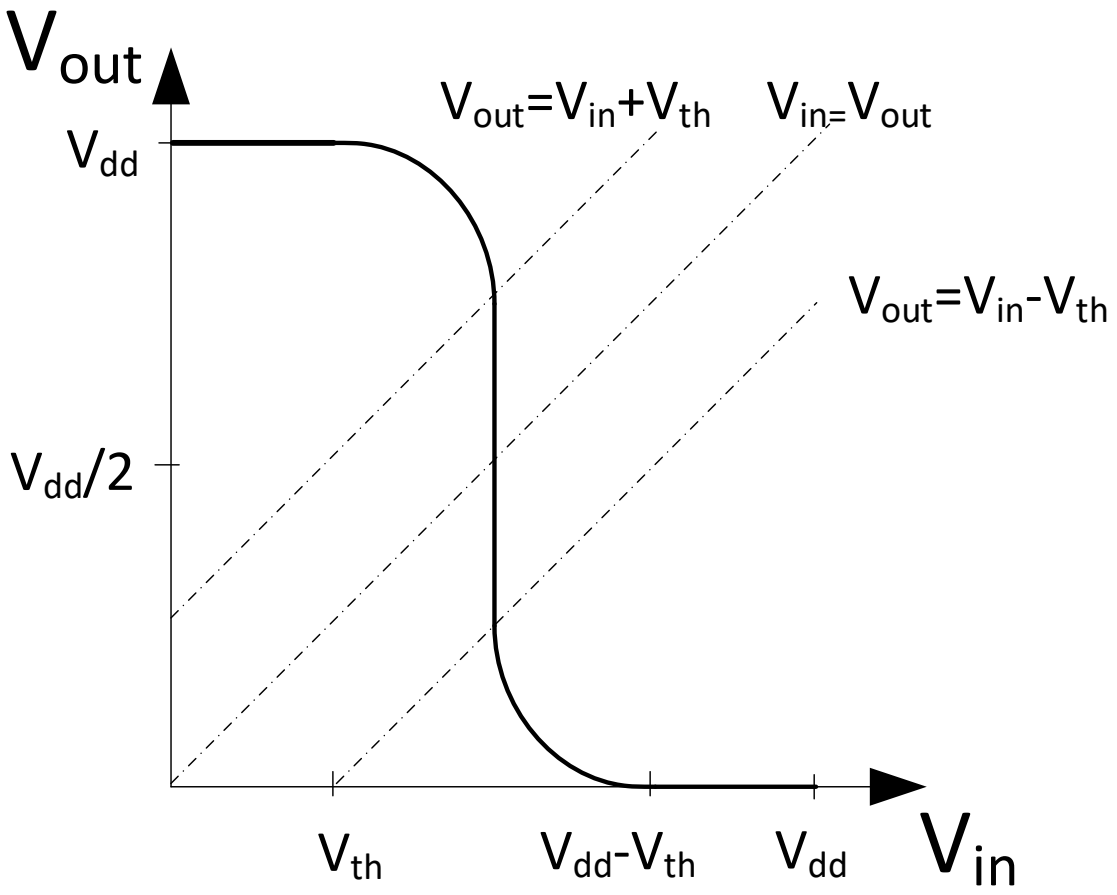
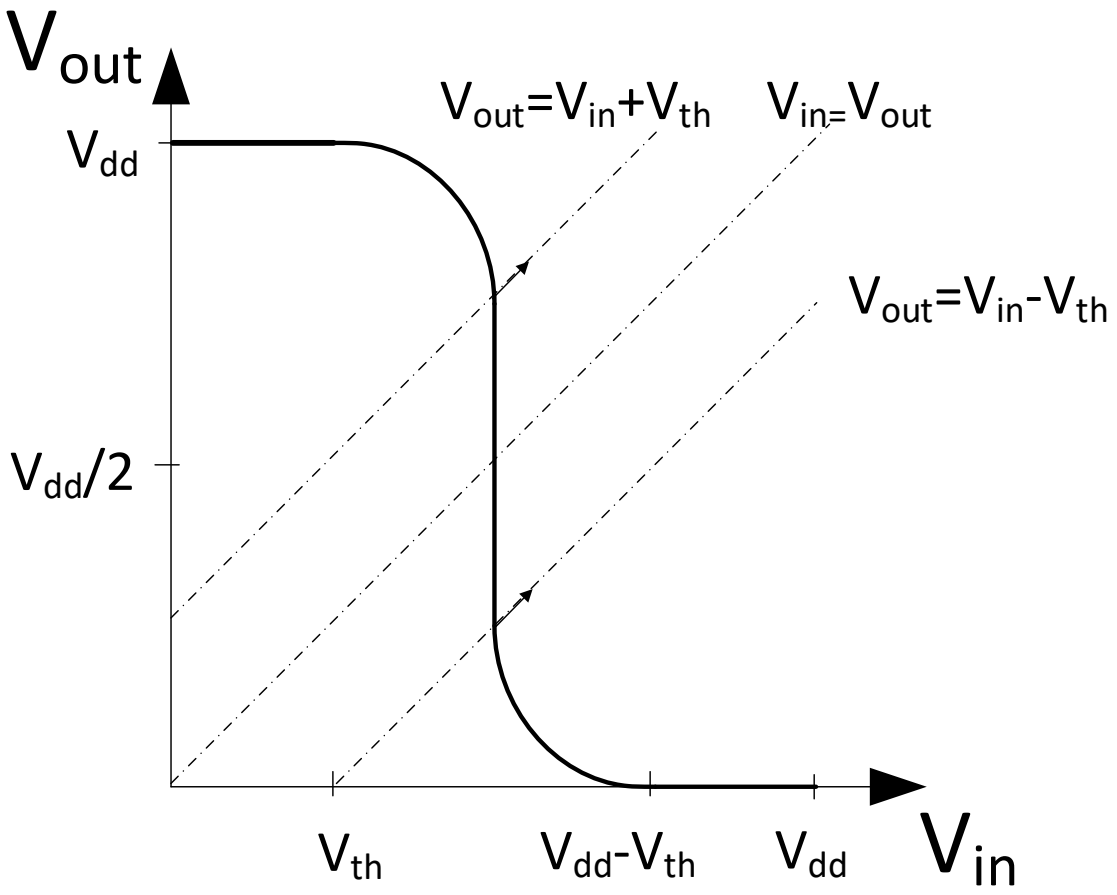


Breakout session



- If $I_{dsat,p}=2*I_{dsat,n}$, sketch the the DC transfer curve relative to the balanced case

Breakout session



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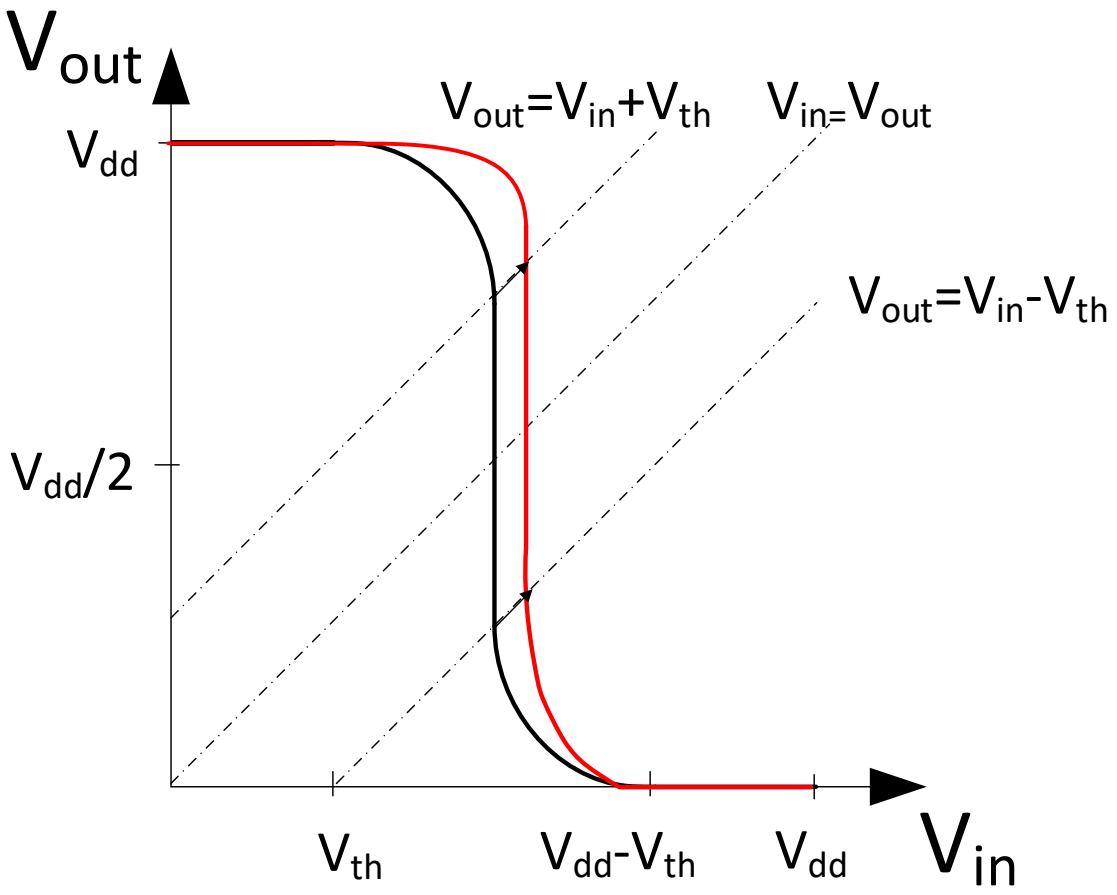
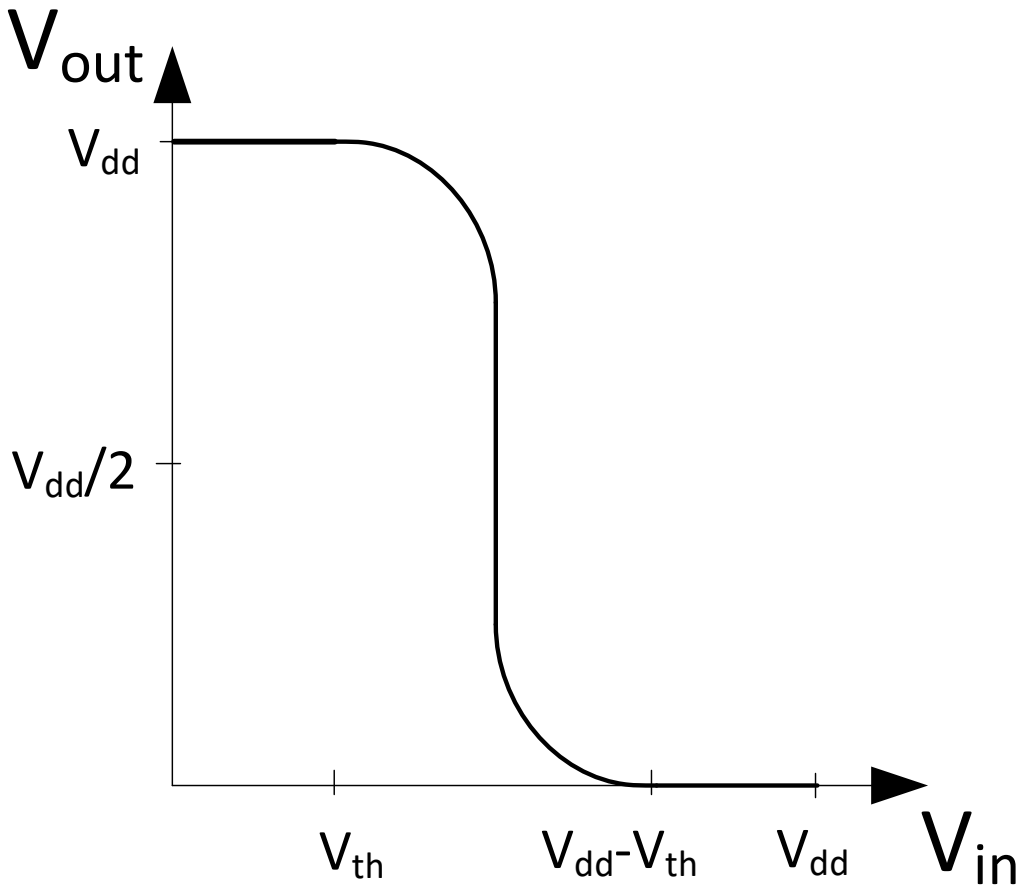
Breakout session



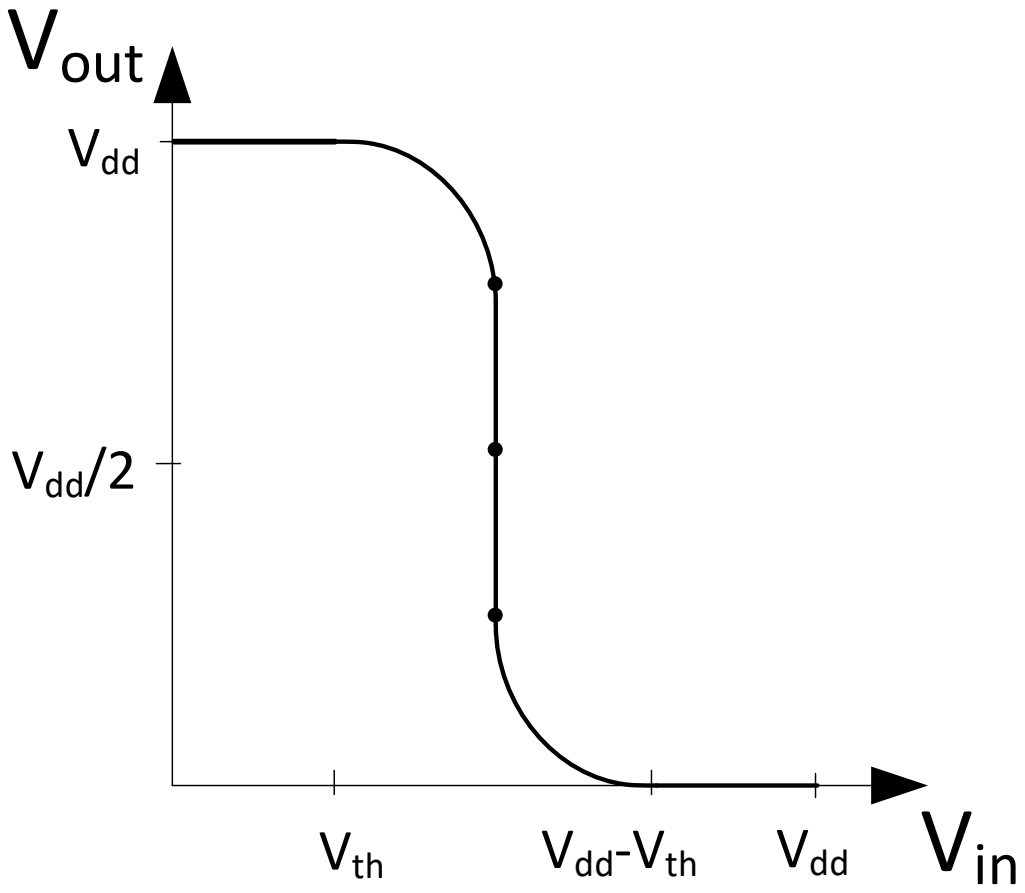
- If $I_{dsat,p}=2*I_{dsat,n}$, sketch the the DC transfer curve relative to the balanced case

Channel length modulation



- Channel length modulation ➔ Less abrupt DC transfer curve in "transition region" region where both devices are in saturation

Channel length modulation



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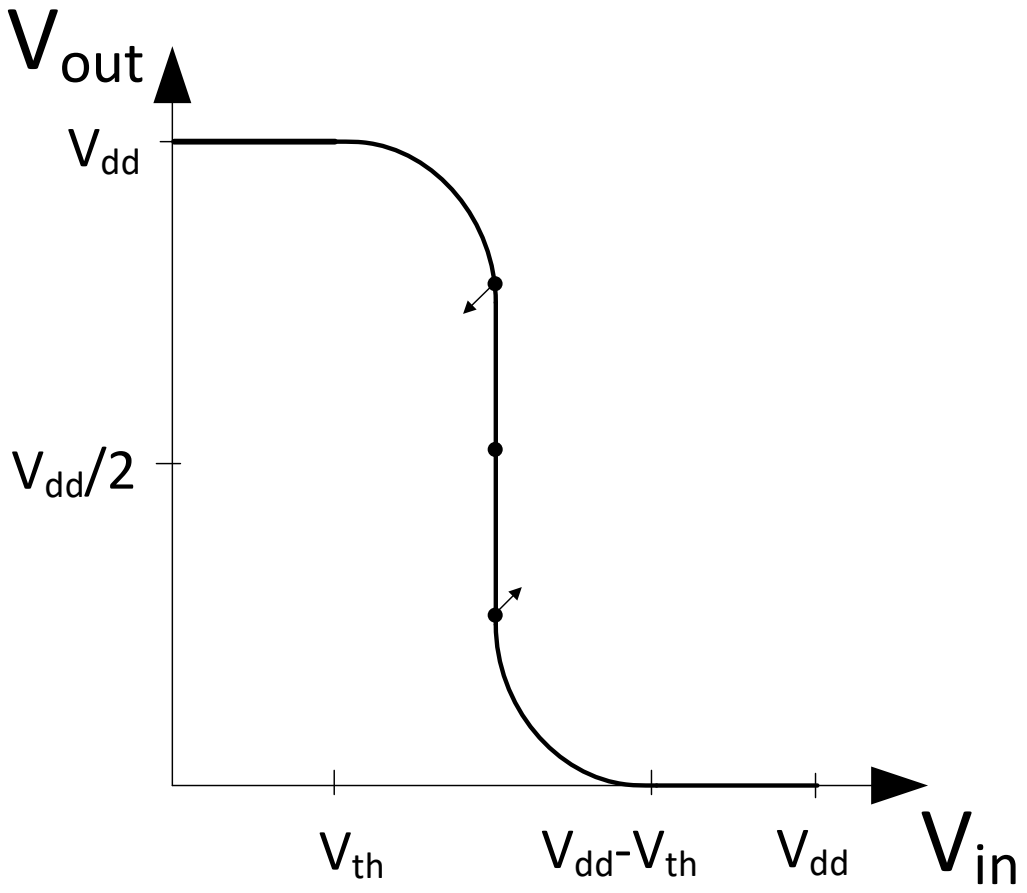

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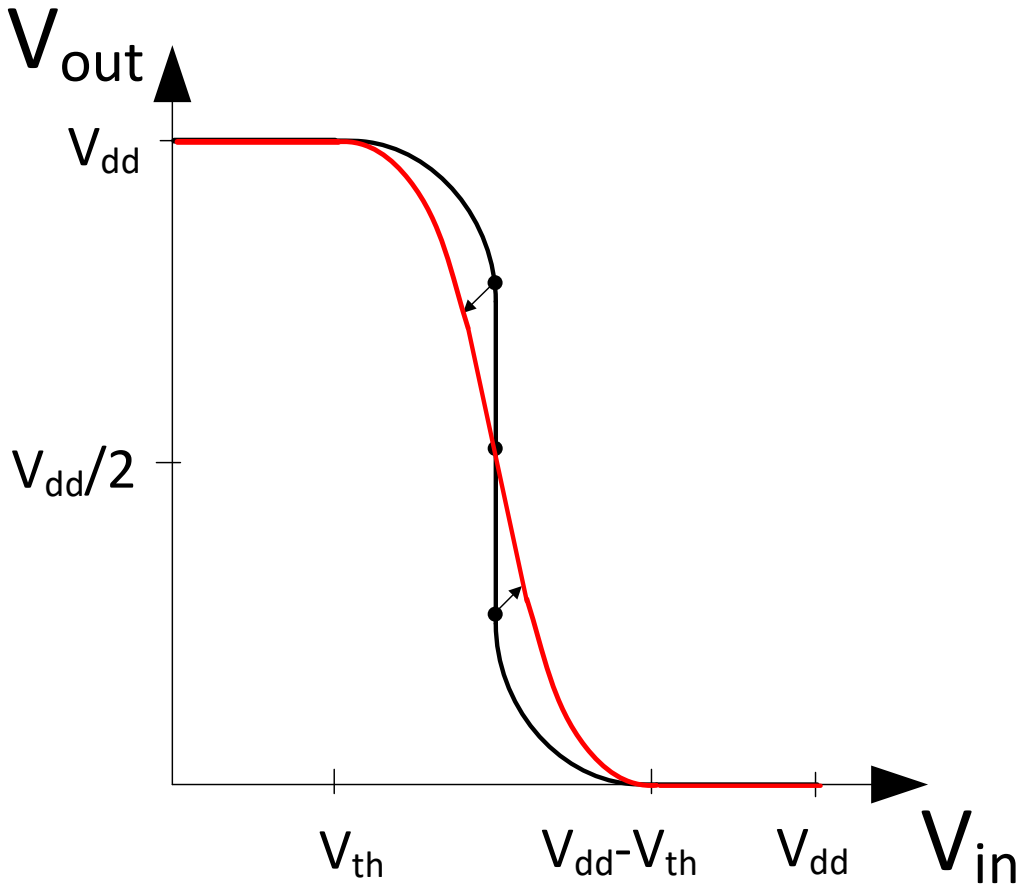
Channel length modulation



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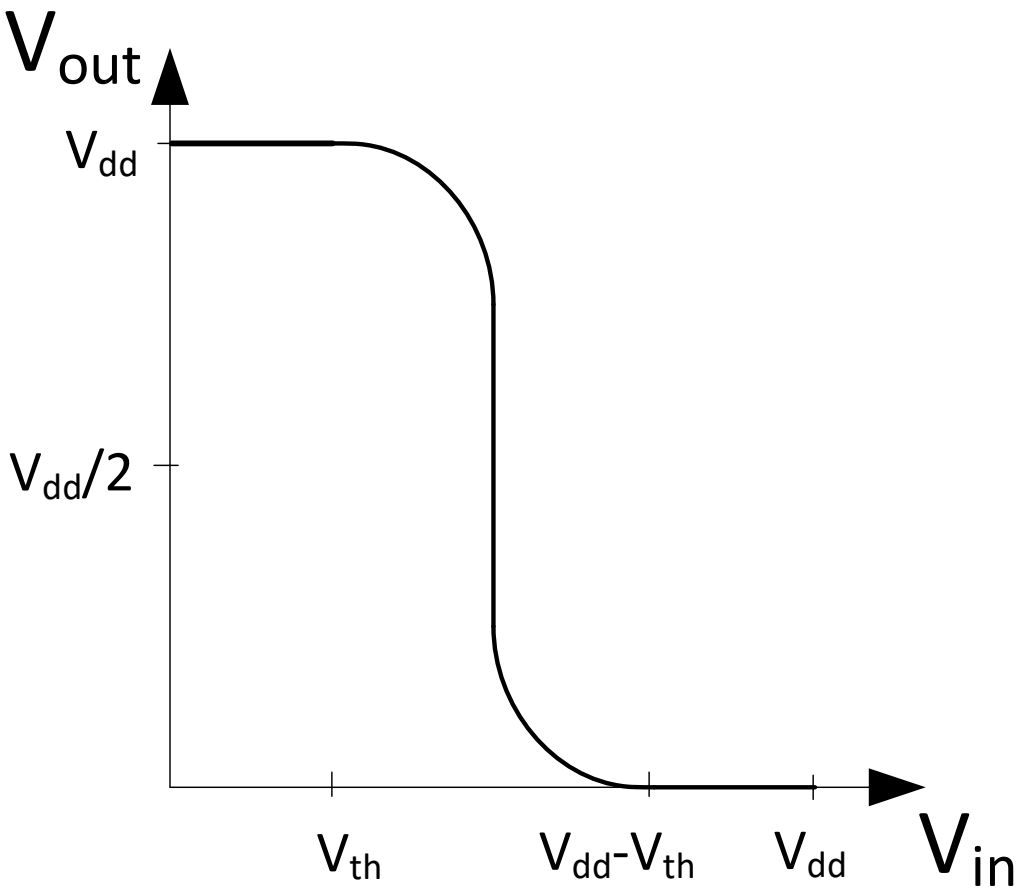
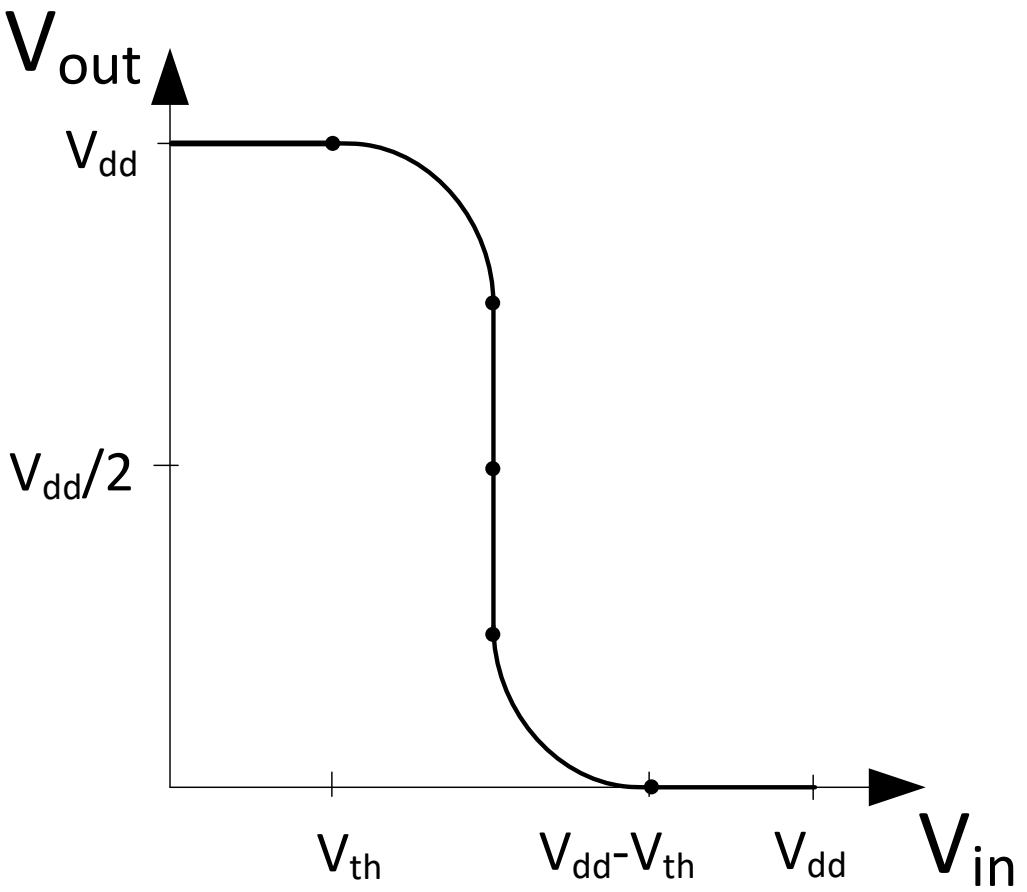
V_{th} Impact on DC Transfer Curve



- V_{th}, determines vertical window size of transition region

V_{th} Impact on DC Transfer Curve



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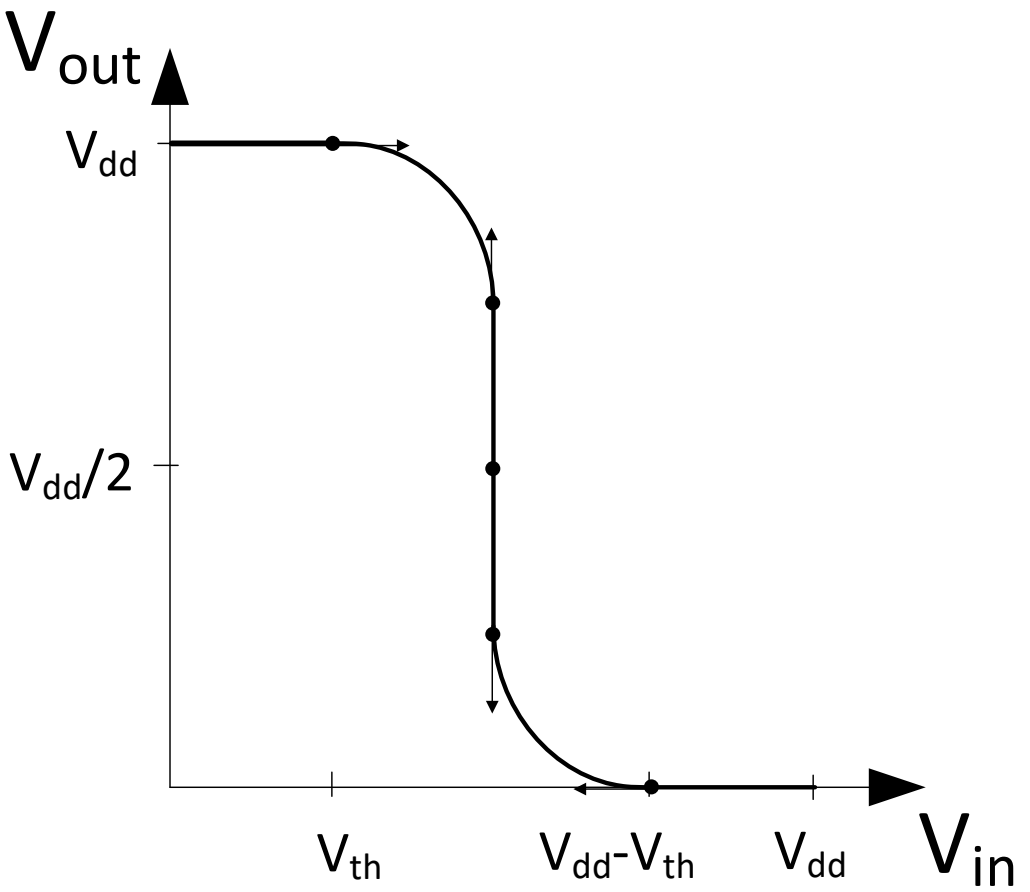

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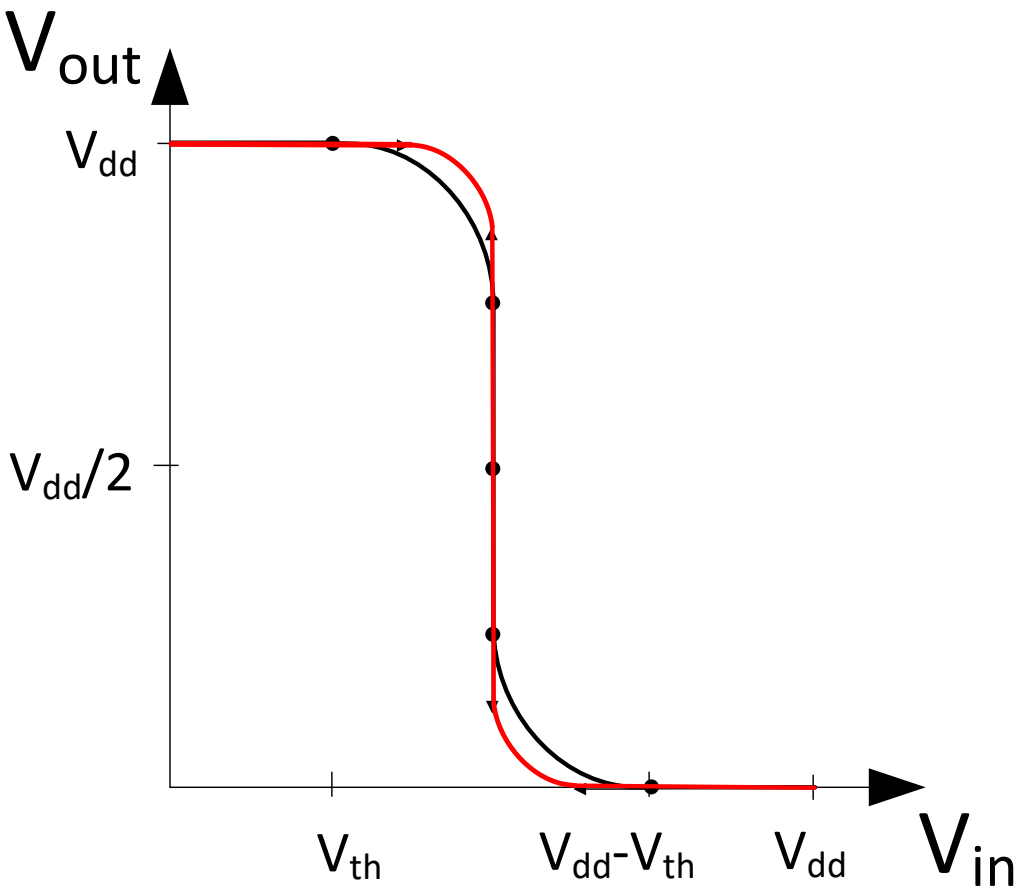
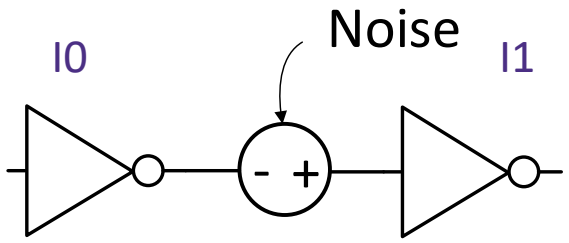


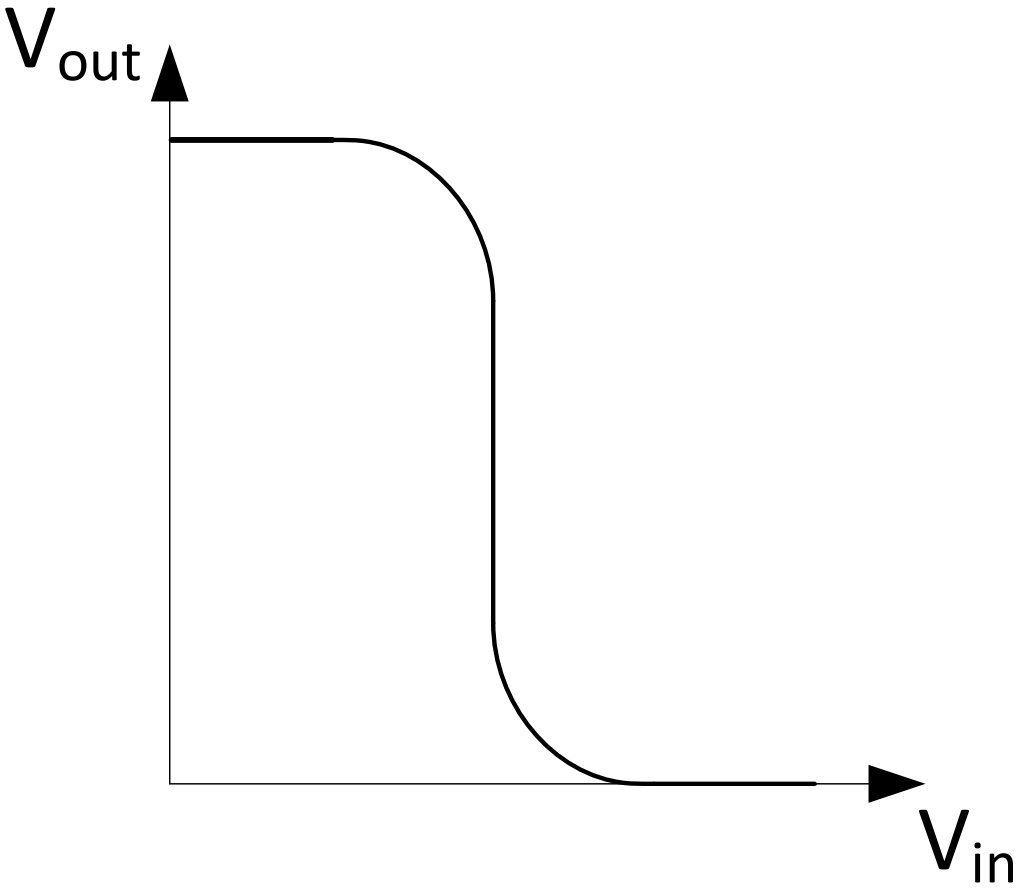
- V_{th}, determines vertical window size of transition region

V_{th} Impact on DC Transfer Curve

- What if $V_{th} = 0.6V_{dd}$?

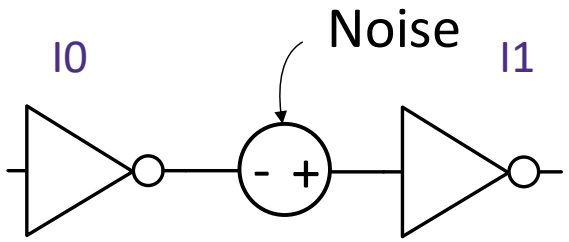
Importance of DC Transfer Function

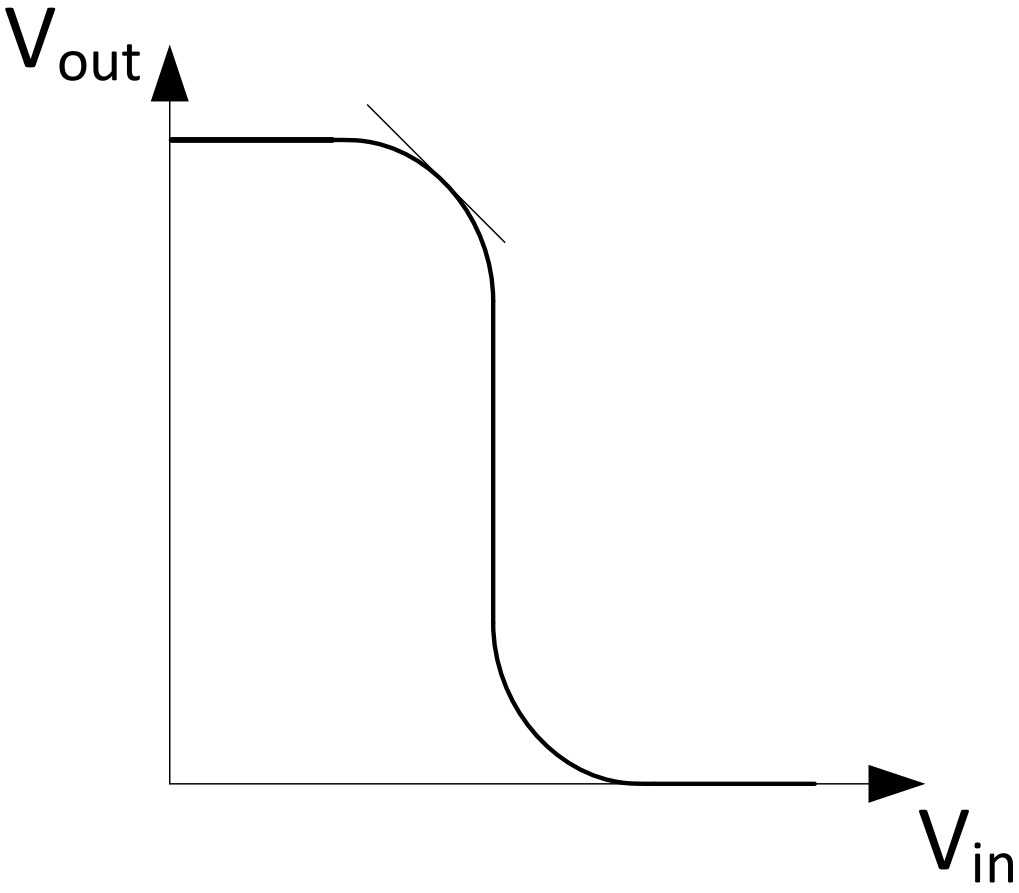




- Static Noise Margin (NM)

Importance of DC Transfer Function





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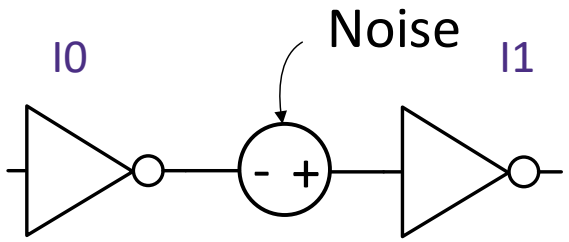
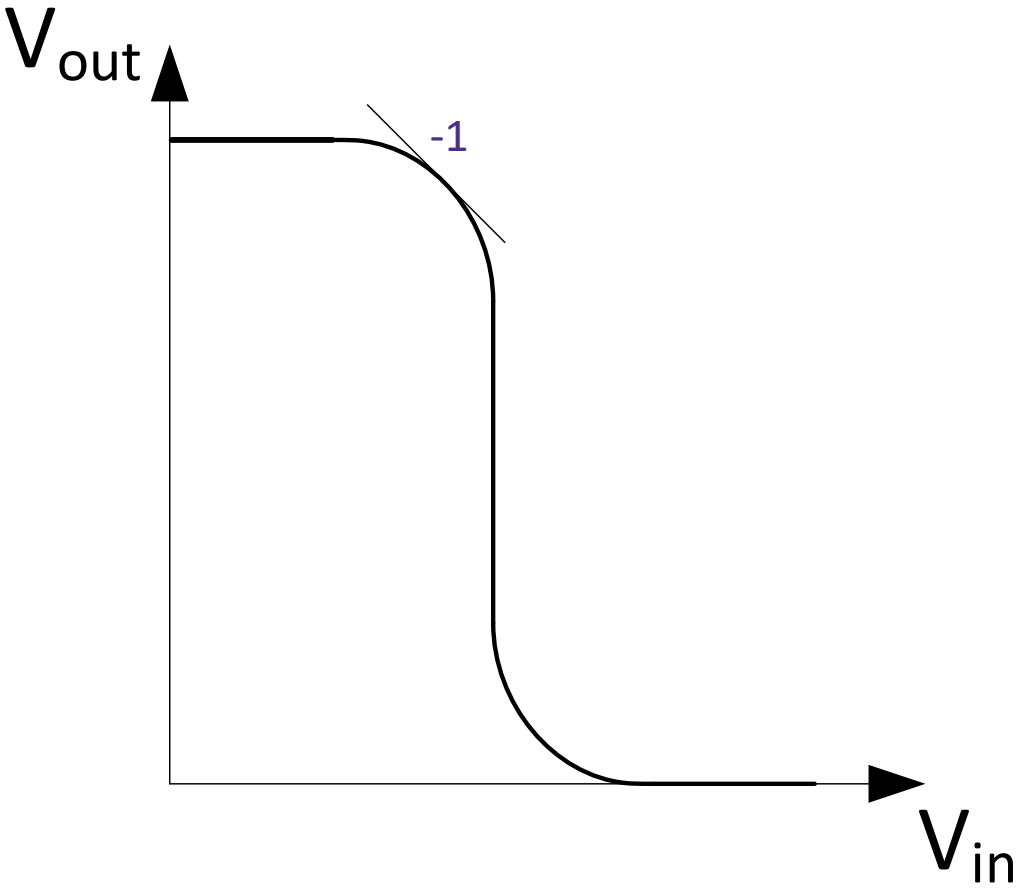
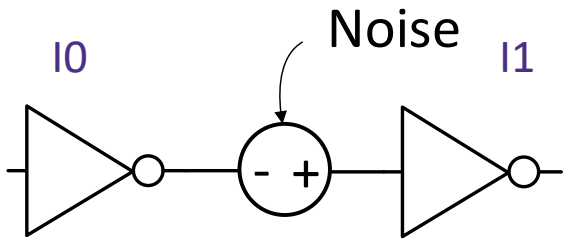
Importance of DC Transfer Function

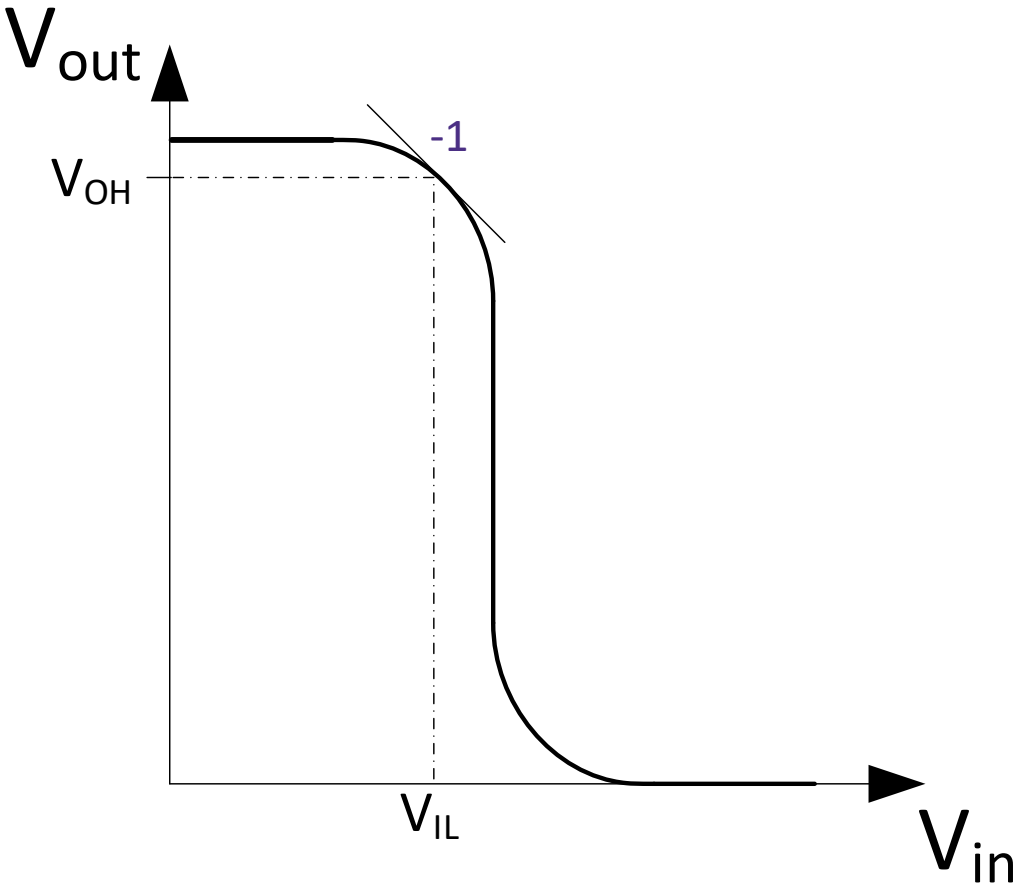




- Static Noise Margin (NM)

Importance of DC Transfer Function





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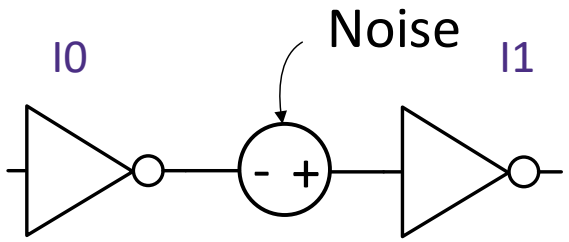
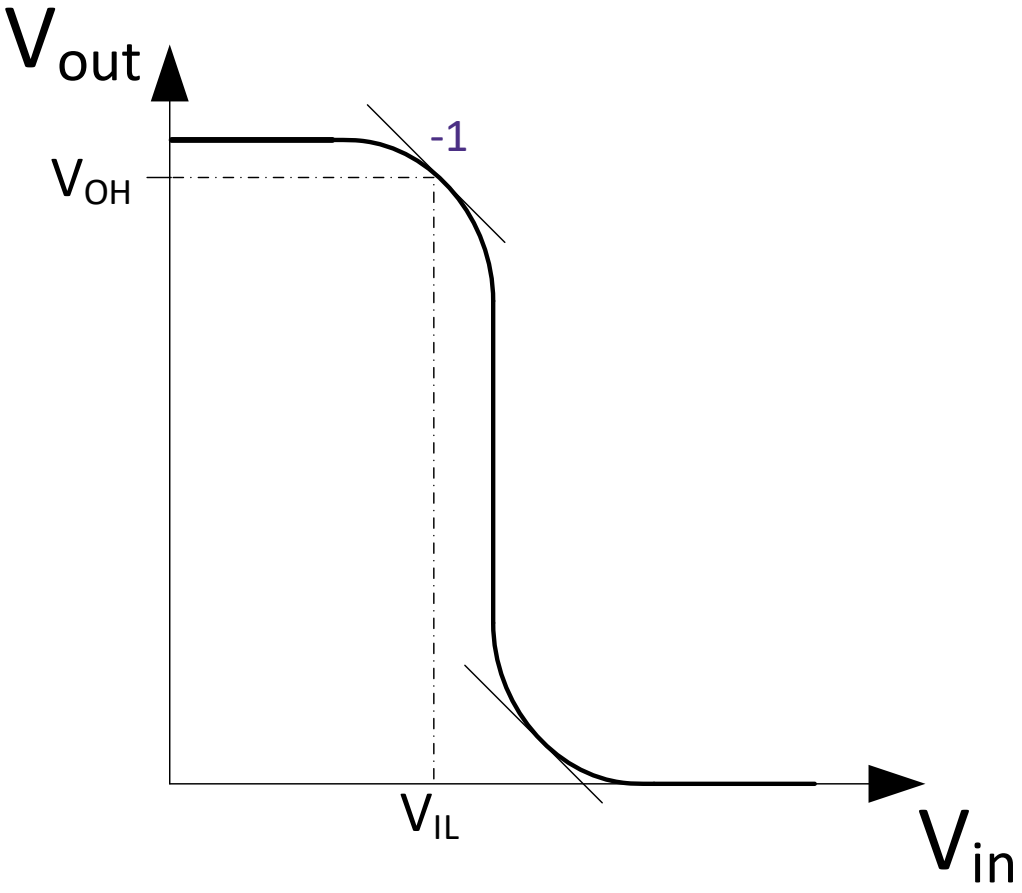
Importance of DC Transfer Function





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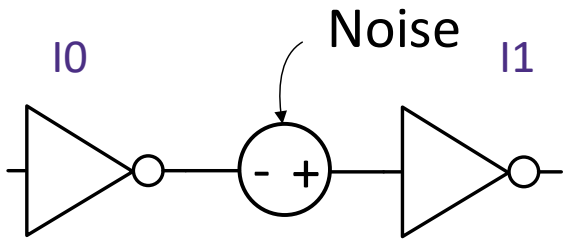
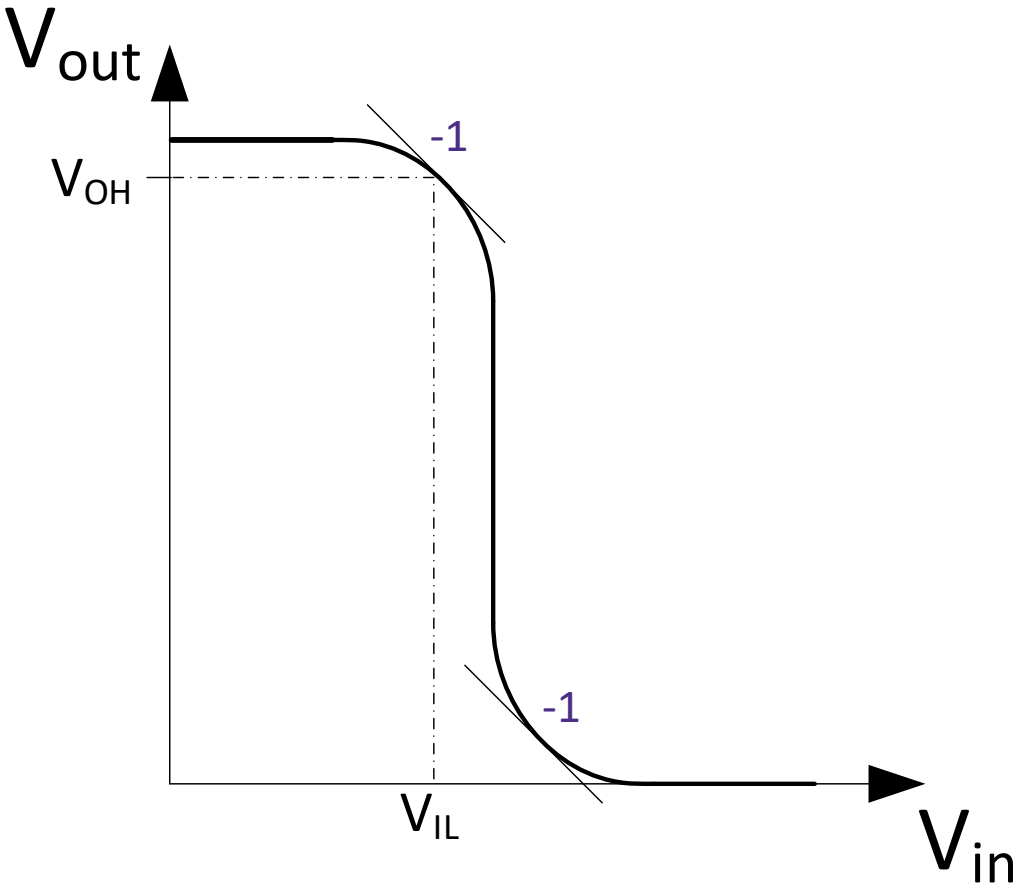
Importance of DC Transfer Function





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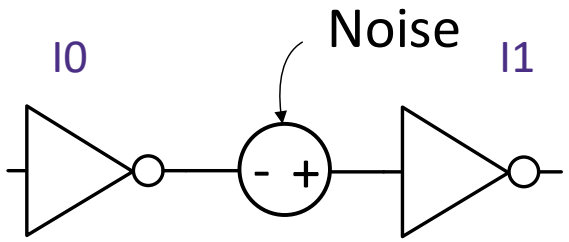
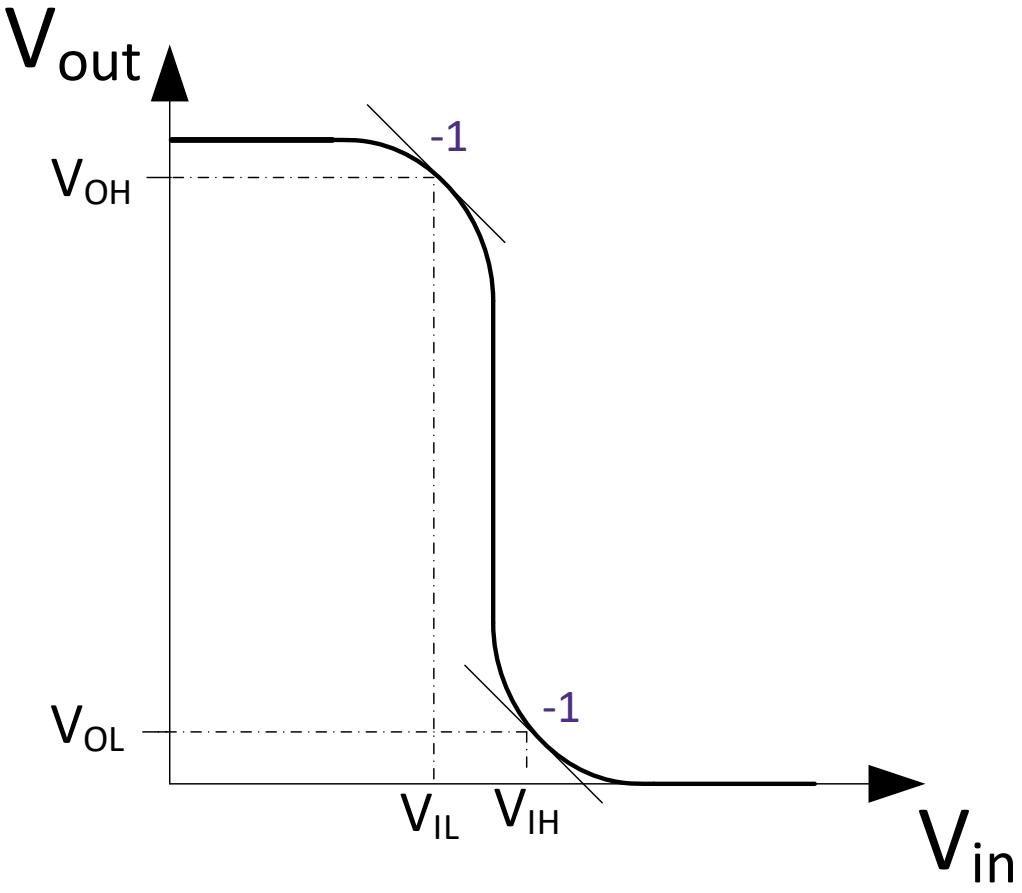
Importance of DC Transfer Function





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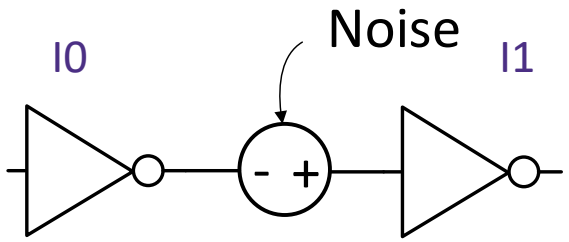
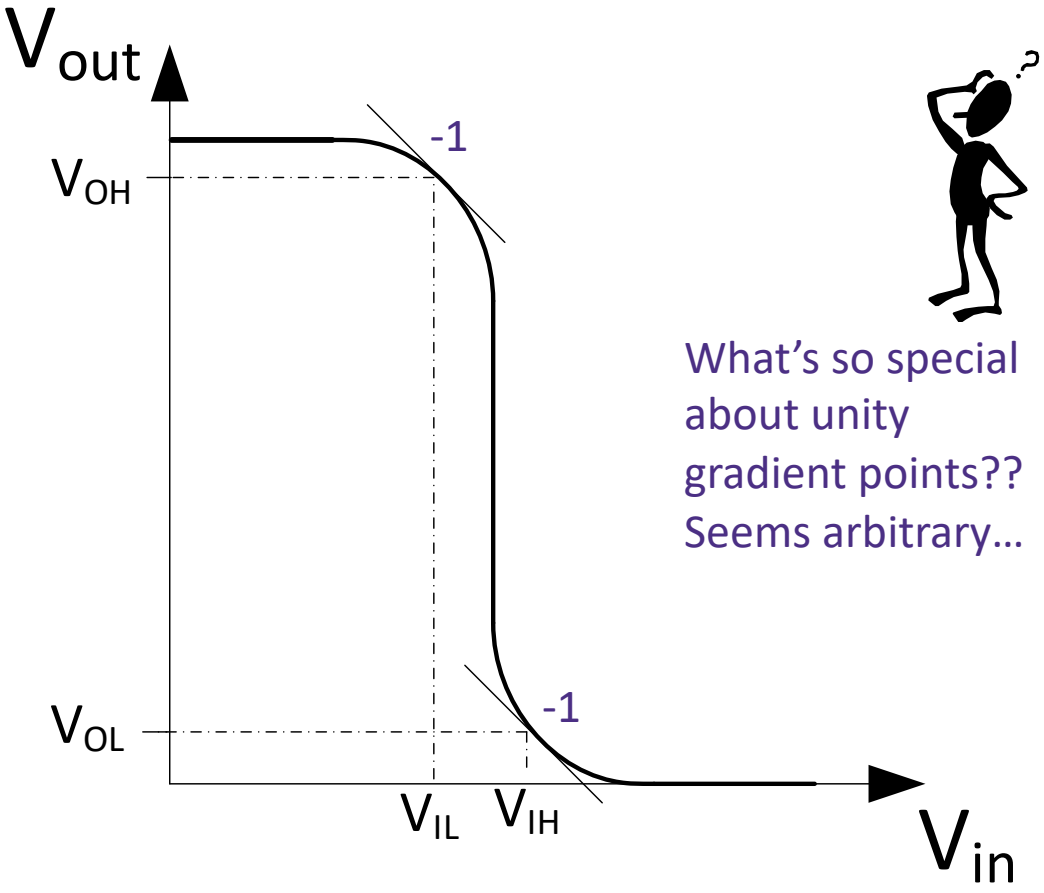
Importance of DC Transfer Function

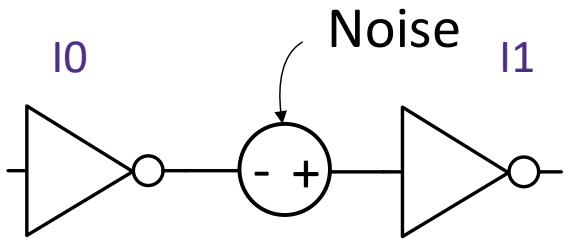


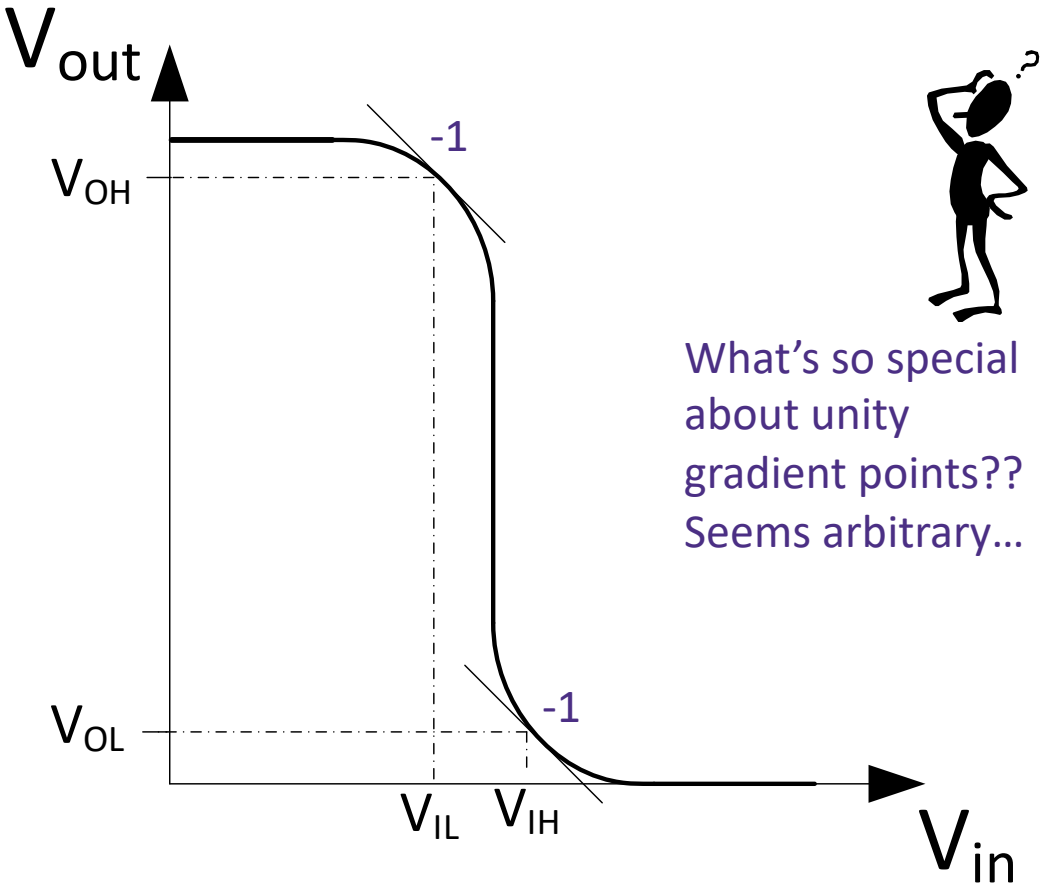


What's so special about unity gradient points?? Seems arbitrary…

- Static Noise Margin (NM)

Importance of DC Transfer Function

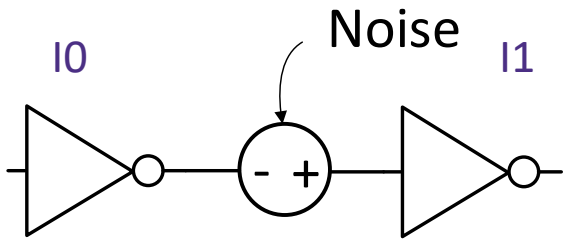


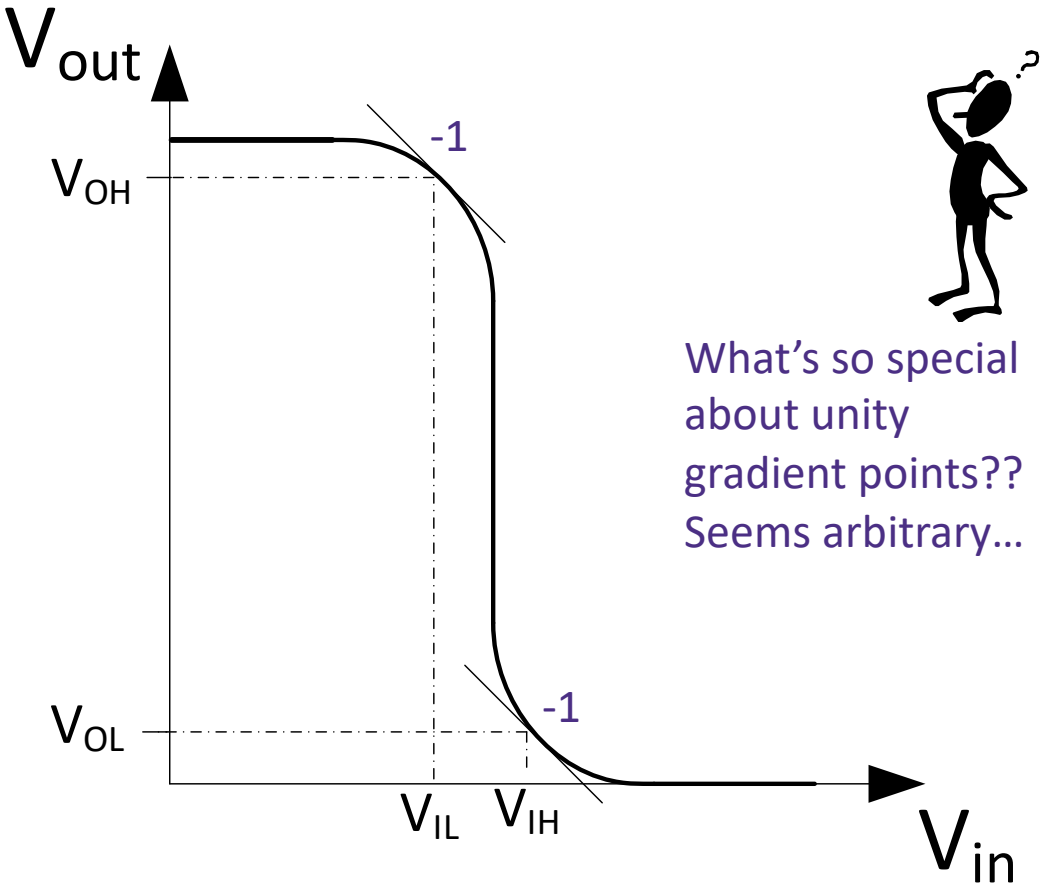


What's so special about unity gradient points?? Seems arbitrary…

- Static Noise Margin (NM)
- $NM_0 = V_{il} - V_{ol}$
- $NM_1 = V_{oh} - V_{ih}$

Importance of DC Transfer Function

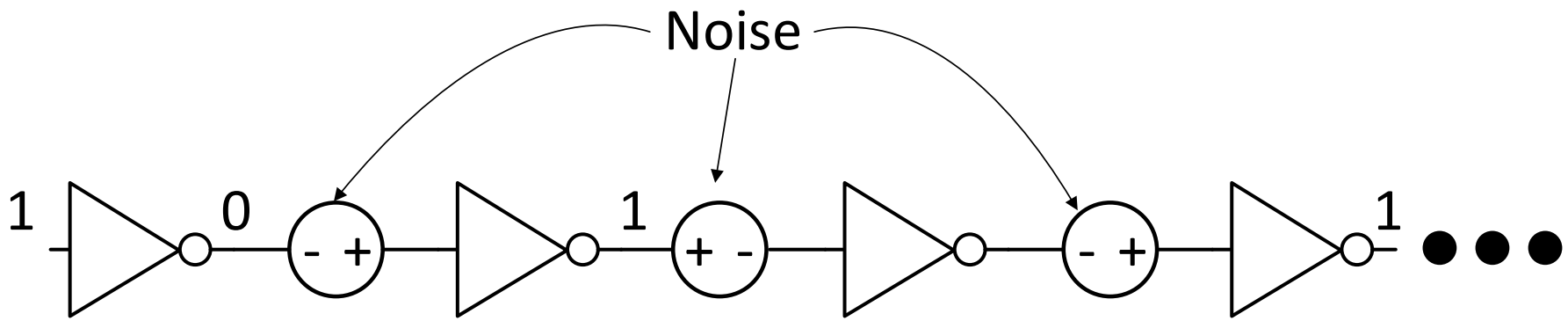




What's so special about unity gradient points?? Seems arbitrary…

- Static Noise Margin (NM)
- $NM_0 = V_{il} - V_{ol}$
- $NM_1 = V_{oh} - V_{ih}$
- What is the best possible NM for an inverter? What would it take?

Some More Thoughts on Noise Margins

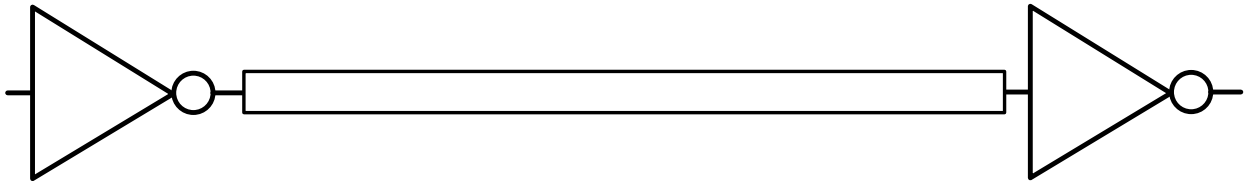


- Importance of unity-gain points (Cascade of inverters)
- What happens if noise voltage exceeds noise margin?
- Noise margin vs. V_{dd}

Holding Resistance

- Static inverter analysis also important for holding resistance analysis

Holding Resistance



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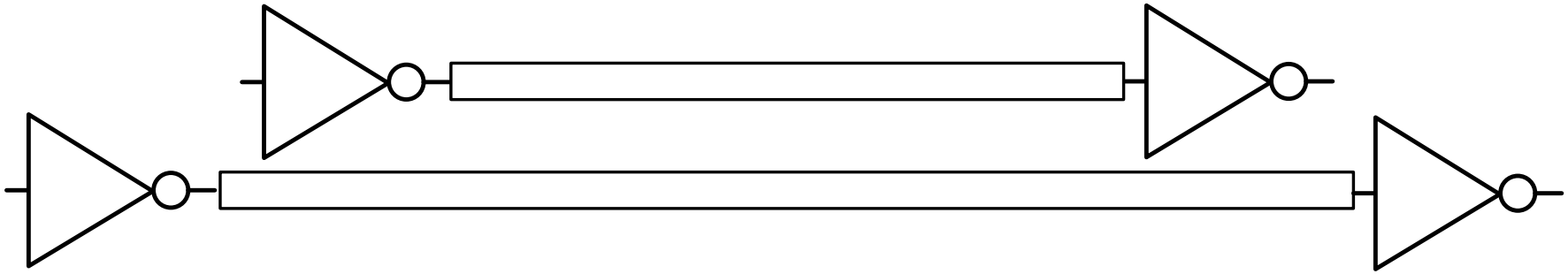
Holding Resistance



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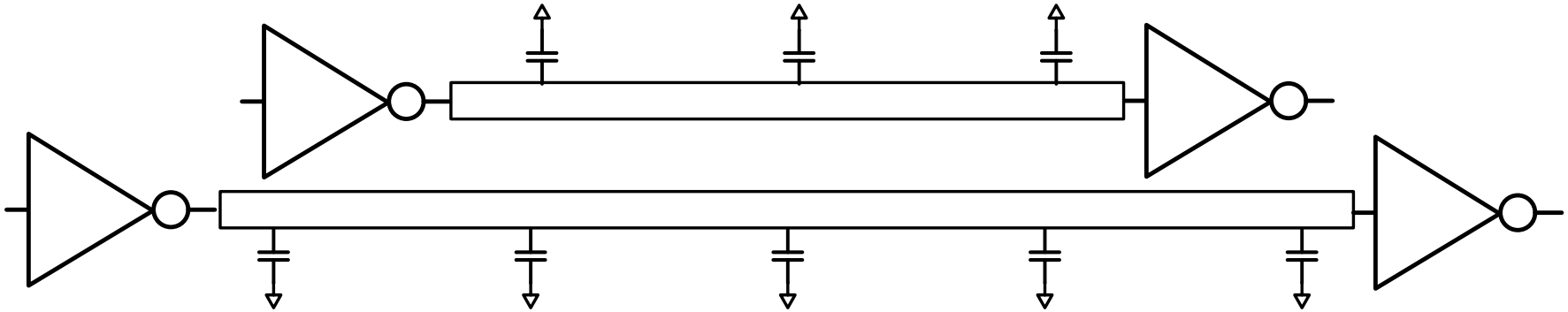

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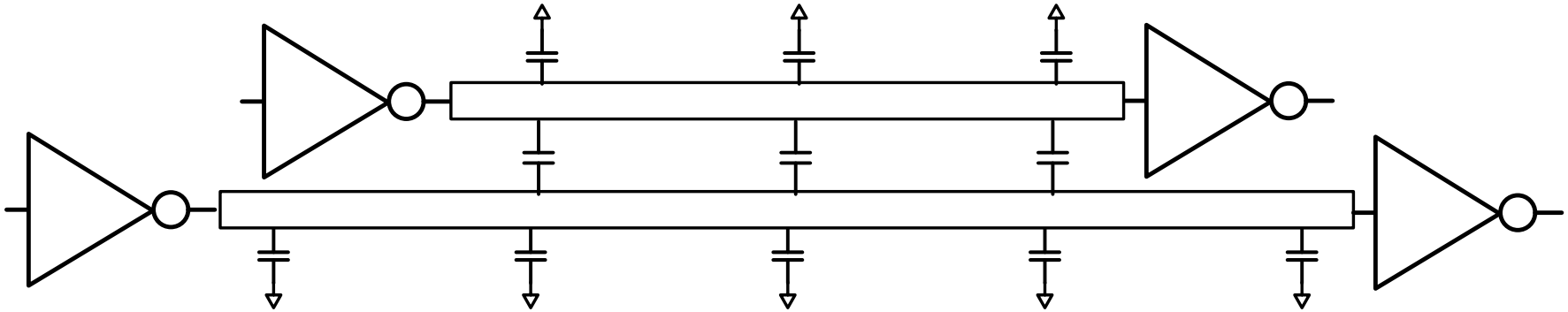

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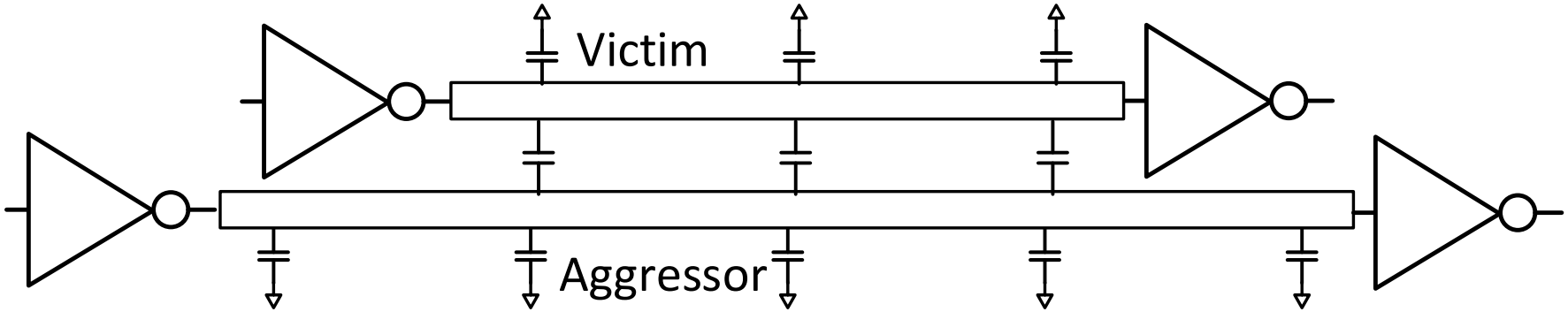

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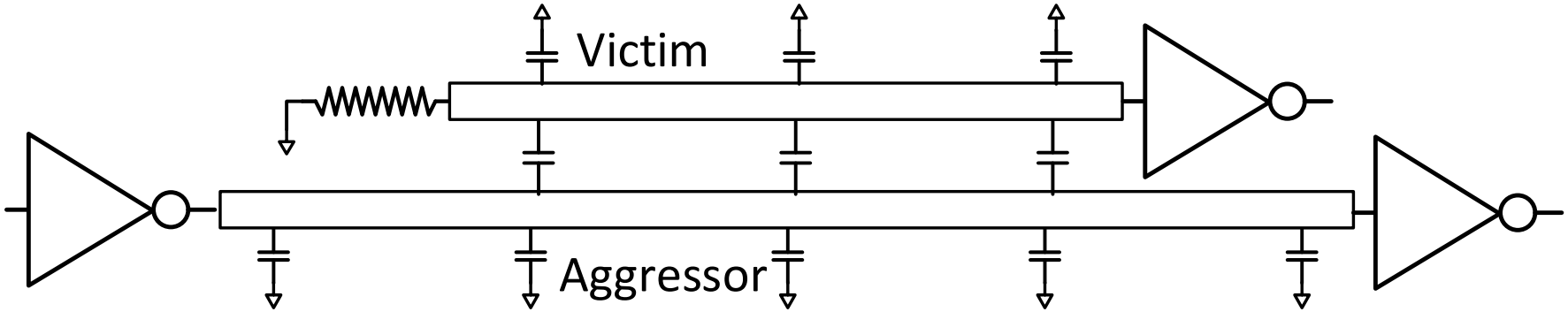

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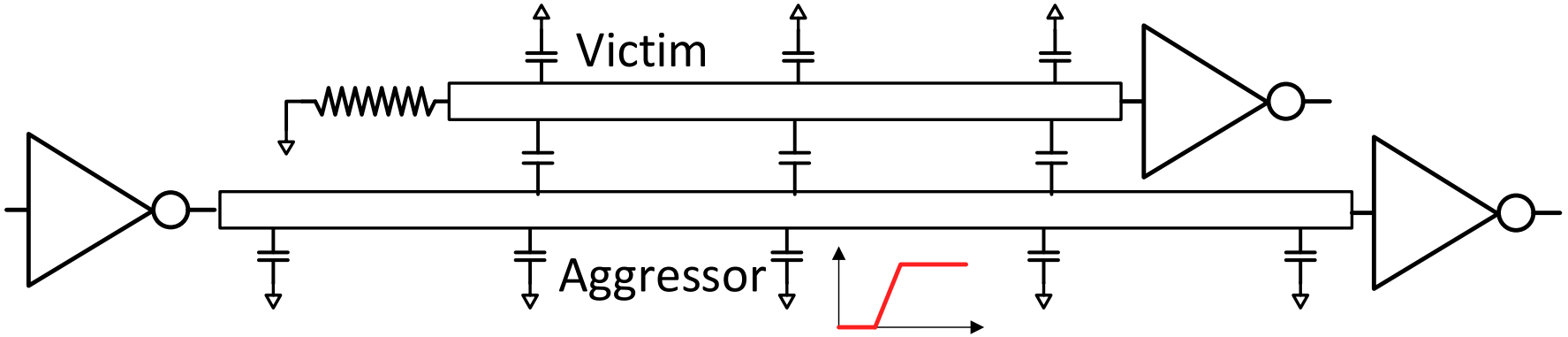
Holding Resistance



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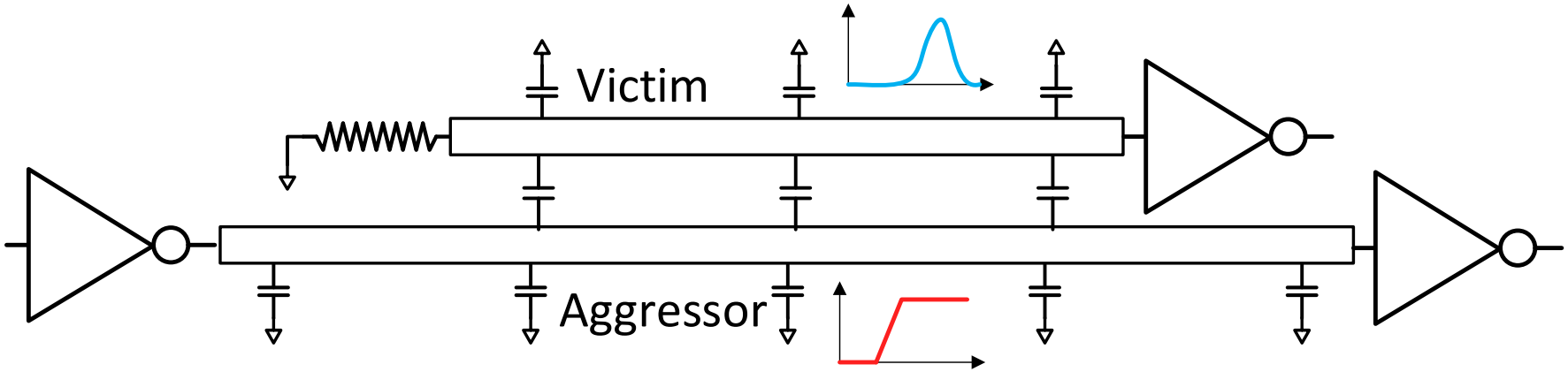
Holding Resistance



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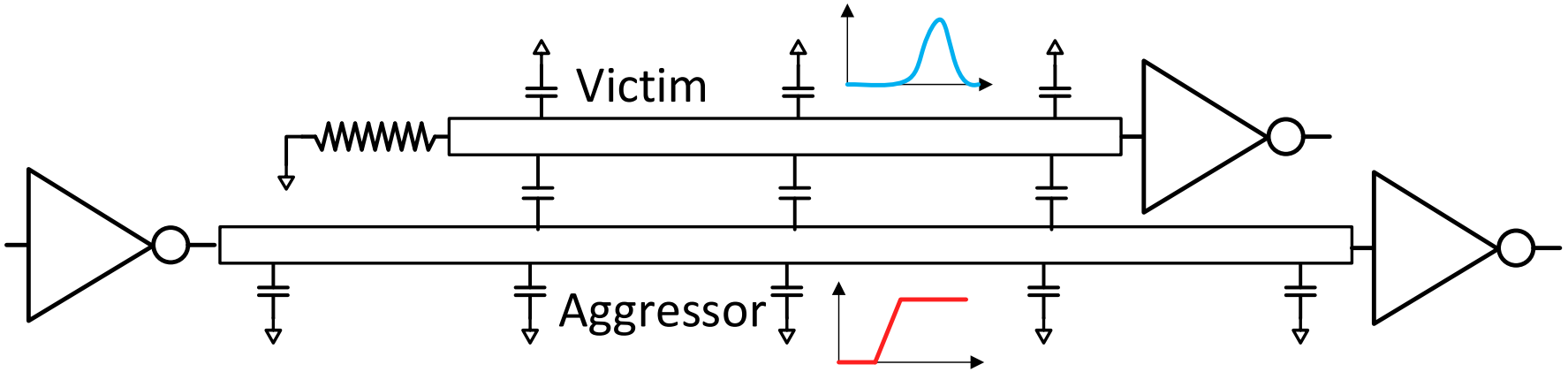
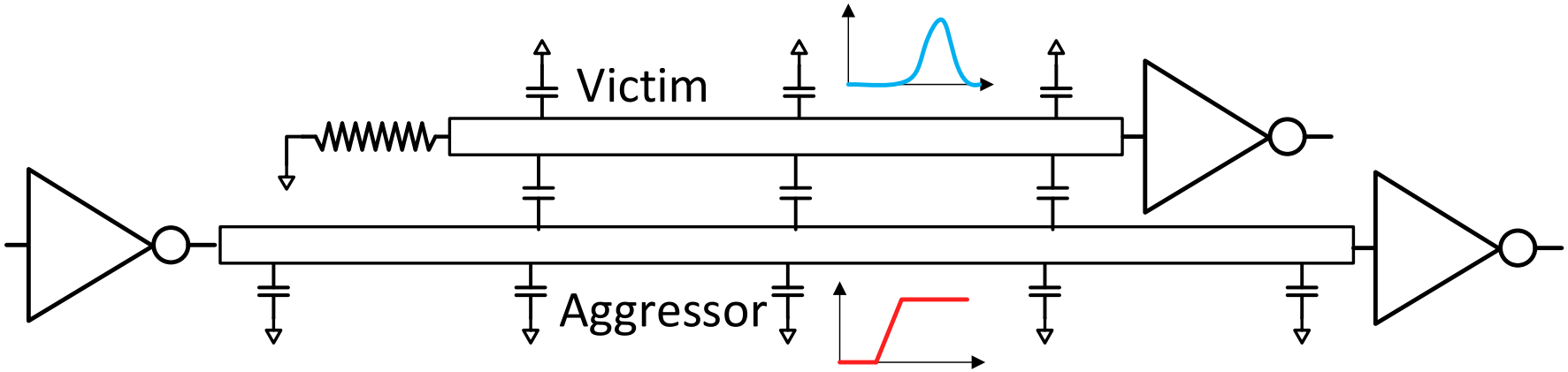
Holding Resistance



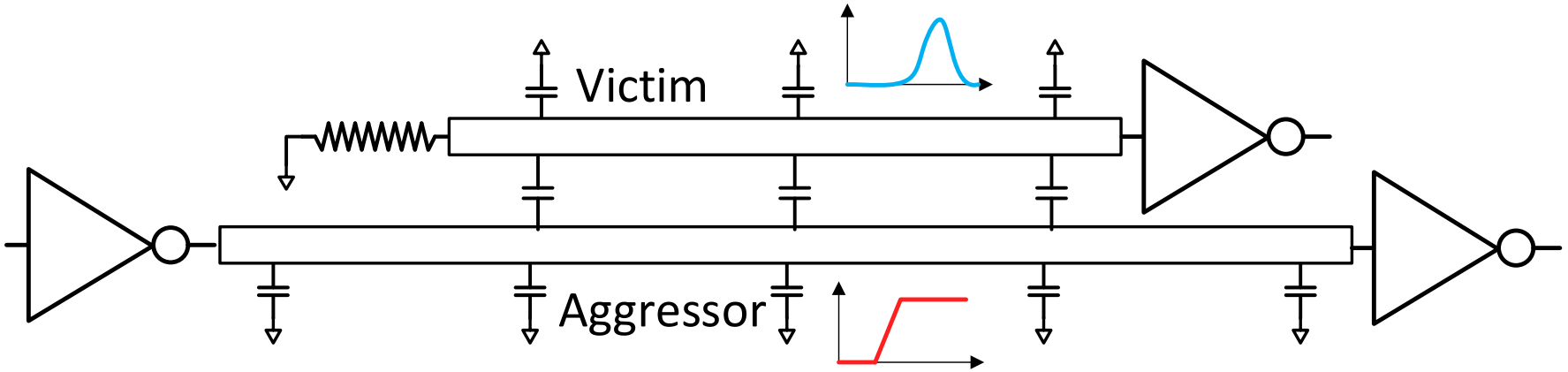
- Static inverter analysis also important for holding resistance analysis
  - Crosstalk analysis

Holding Resistance



- Static inverter analysis also important for holding resistance analysis
  - Crosstalk analysis
  - Holding resistance impacts peak noise glitch

Holding Resistance



Why does the glitch matter?
What are the key glitch parameters
What are the relevant glitch-determining parameters

- Static inverter analysis also important for holding resistance analysis
  - Crosstalk analysis
  - Holding resistance impacts peak noise glitch

Question

- What happens if a 1V inverter sees a 2V step (common ground)
- What happens if a 2V inverter sees a 1V step (0V->1V)

Reading assignment