Grade: /80

E E 476 – Introduction to VLSI Design
Mid-term examination
November 4th, 2022

I have not received nor obtained help from anyone in the completion of this examination. During the course of this mid-term examination, I have not engaged with any form of communication with my peers on any aspect of the contents of this exam. I understand that strict action will be taken resulting from my failure to comply with the mid-term examination policy. I also understand that it is my duty to not only adhere to the mid-term exam policy, but also report any other individual(s) who are violating this policy.

Name: _____

Signature: _____

The use of notes, calculators, or any electronic devices is not allowed during this midterm examination.

Duration: 50 minutes

Assume that all devices have 0 leakage current. Unless otherwise stated, the following default parameters apply:

V_{dd}	1.2 V	$C_{ox} = \frac{\epsilon_r \cdot \epsilon_0}{t_{ox}} = 0.01\ \mathrm{F/m^2}$
ϵ_r (Silicon-di-oxide)	3.8	
ϵ_0	$8.85 \cdot 10^{-12}$ F/m	
λ	0	
t_{ox}	$33.63\ A = 3.363$ nm	$\mu_n \cdot C_{ox} = 0.5$ mA $\mu_p \cdot C_{ox} = 0.25$ mA
μ_n	$500\ \mathrm{cm^2/V}$	
μ_p	$250\ \mathrm{cm^2/V}$	
$V_{th,n} = V_{th,p} = V_{th}$	0.2 V	$\mu_n \cdot C_{ox} \cdot \frac{W_n}{L} = 10$ mA $\mu_p \cdot C_{ox} \cdot \frac{W_p}{L} = 10$ mA
W_n	1 µm	
W_p	2 µm	
Beta ratio $= \frac{\mu_n}{\mu_p}$	2	
$L_n = L_p = L$	50 nm	

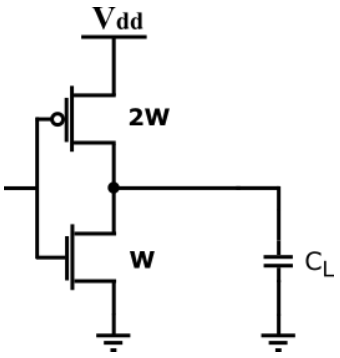
NMOS transistor:

Cut-off	$V_{GS} \leq V_{th}$	$I_D = 0$
Linear/Triode	$V_{GS} > V_{th}$ and $V_{DS} \leq V_{GS} - V_{th}$	$I_D = \mu_n \cdot C_{ox} \cdot \frac{W_n}{L}\left[(V_{GS} - V_{th}) \cdot V_{DS} - \frac{1}{2}V_{DS}^2\right]$
Saturation	$V_{GS} > V_{th}$ and $V_{DS} > V_{GS} - V_{th}$	$I_D = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W_n}{L}(V_{GS} - V_{th})^2(1 + \lambda \cdot V_{DS})$

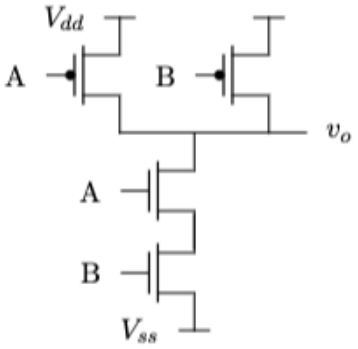
PMOS transistor:

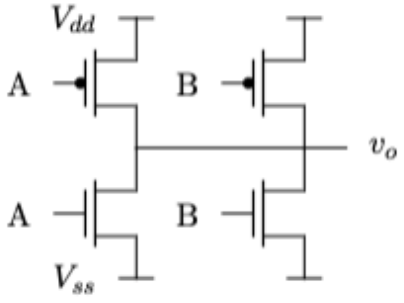
Cut-off	$V_{SG} \leq V_{th}$	$I_D = 0$
Linear/Triode	$V_{SG} > V_{th}$ and $V_{SD} \leq V_{SG} - V_{th}$	$I_D = \mu_p \cdot C_{ox} \cdot \frac{W_p}{L}\left[(V_{SG} - V_{th}) \cdot V_{SD} - \frac{1}{2}V_{SD}^2\right]$
Saturation	$V_{SG} > V_{th}$ and $V_{SD} > V_{SG} - V_{th}$	$I_D = \frac{1}{2} \cdot \mu_p \cdot C_{ox} \cdot \frac{W_p}{L}(V_{SG} - V_{th})^2(1 + \lambda \cdot V_{SD})$

1 .- **(5 points)** Consider the inverter in the figure to the right, where $C_L = 100$ fF. Is it true that we can make the propagation delay of this gate as small as we want by increasing W? Why or why not?

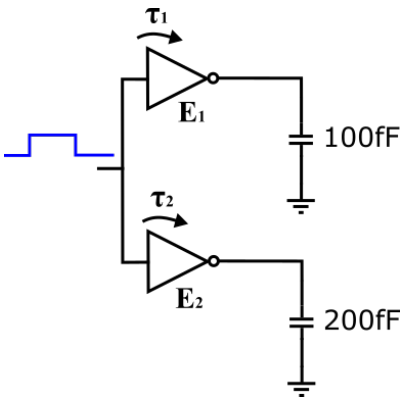


2 .- **(5 points)** Which of the following circuits is an acceptable implementation of CMOS logic? Why?





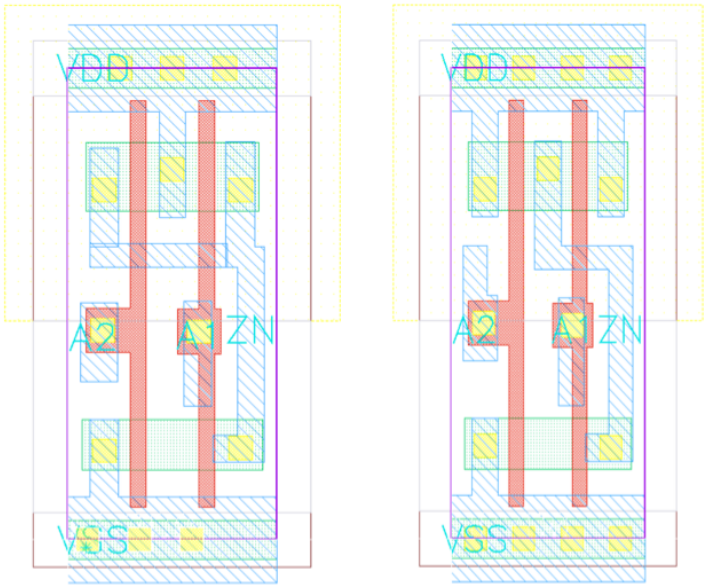
3.- **(5 points)** Consider the figure to the right, where the two inverters are identical. τ_1 and τ_2 are the propagation times for each inverter. Similarly, E_1 and E_2 are the energies consumed by each inverter when their input transitions twice, as shown with the blue waveform.



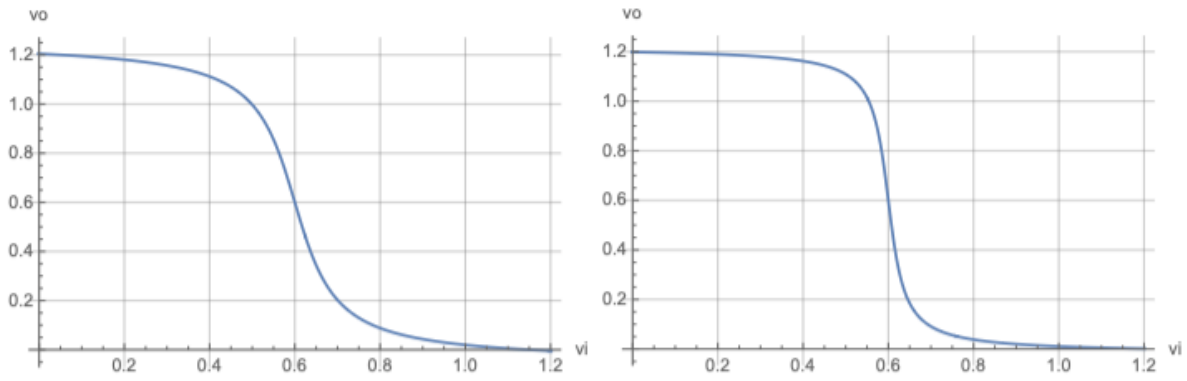
a) Are the two delays equal? If not, which is greater, τ_1 or τ_2?

b) If we assume that the inverters don't have any parasitic capacitance, what is the value of the ratio $\frac{E_2}{E_1}$?

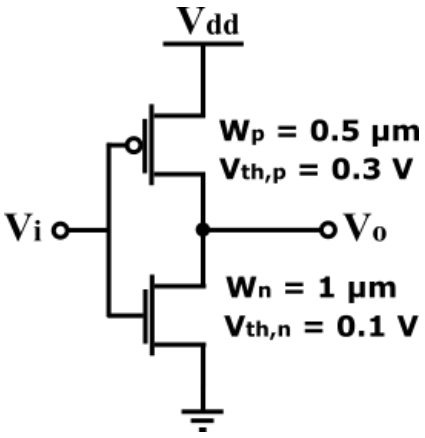
4,- **(5 points)** Which of the following two layouts of a NAND gate takes advantage of "drain sharing"?

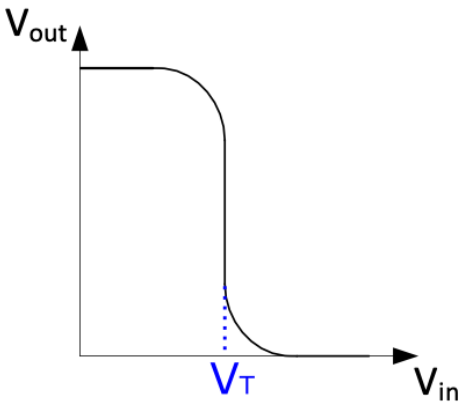


5 .- **(5 points)** Consider the following voltage-transfer curves for two separate inverters. Based on the curves, which inverter is more immune to noise in the input? Why?



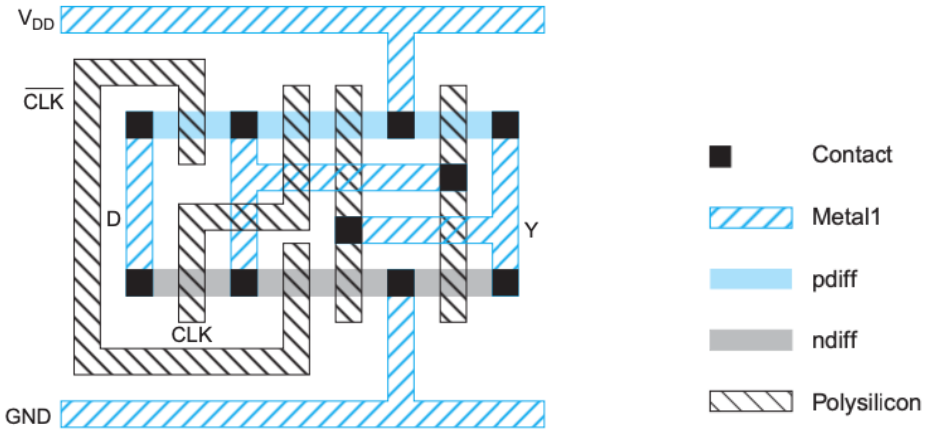
6 .- **(10 points)** The figure below shows an inverter, and a sketch of its DC voltage transfer characteristic. What is the value of V_T?



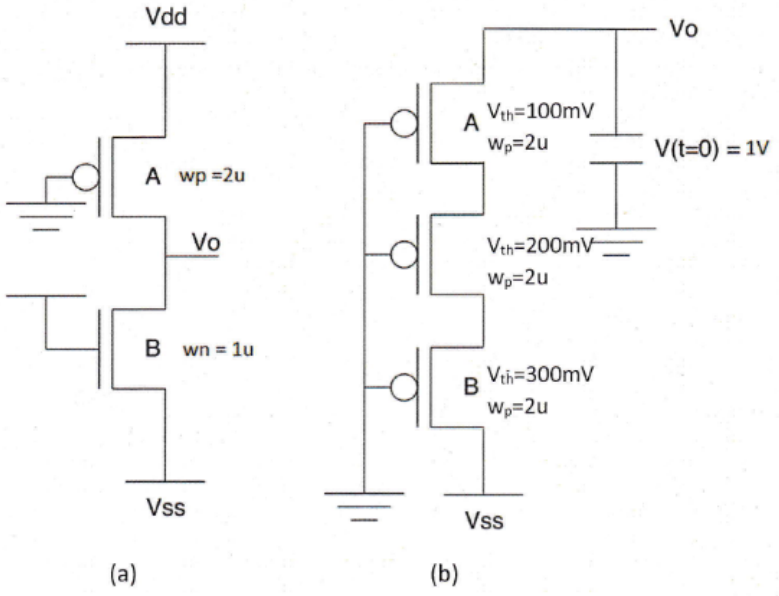


6 .- **(15 points)** Draw the transistor-level schematic that corresponds to the stick diagram in the figure below

(BONUS: 5 points) What is the function of this circuit?



7 .- **(10 points)** For the given circuits in the figure below, (a) and (b), find Vo and the state in which devices A and B are (linear/saturation/cutoff). Assume no leakage in the transistors. Fill up Table 1 to indicate your answers, and briefly explain how you deduced them.



	V_o	State of device A	State of device B
(a)			
(b)			