EE476 Sample Final Exam Questrions

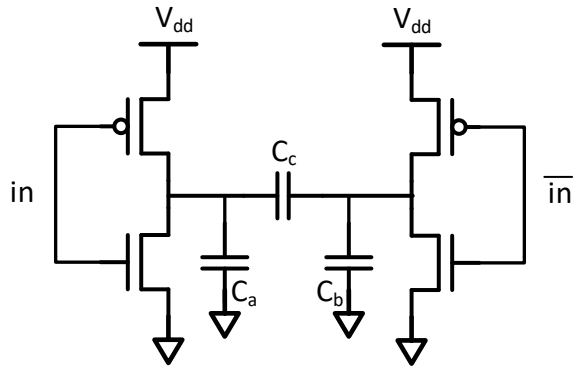
Duration: Up to 2 hours

Unless otherwise stated, the following default parameters apply:

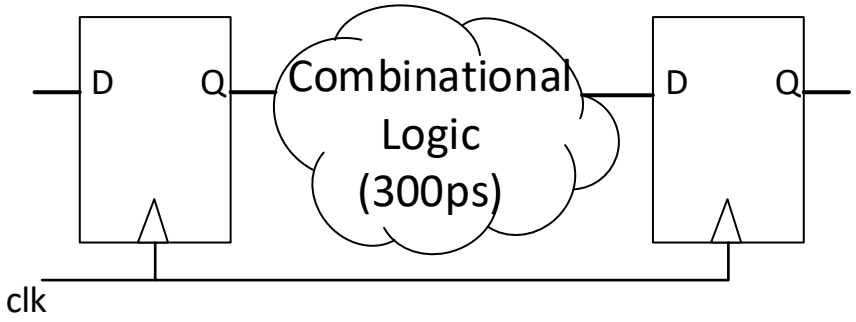
Vdd	1.2V
ε_r (Silicon-di-Oxide)	3.8
ε_0	8.85 E-12
λ	0
T_{ox}	100A
μ_n	500cm^2/V
μ_p	250cm^2/V
$V_{thn} = V_{thp}$	0.25V
W_n	1µm
W_p	2µm
$L_n=L_p$	60nm

1. (10 points) For the circuit shown below complete the table below for energy delivered by the supply and energy dissipated for each transition

Input Transition	Energy delivered by supply	Energy dissipated in circuit
Rising		
Falling		

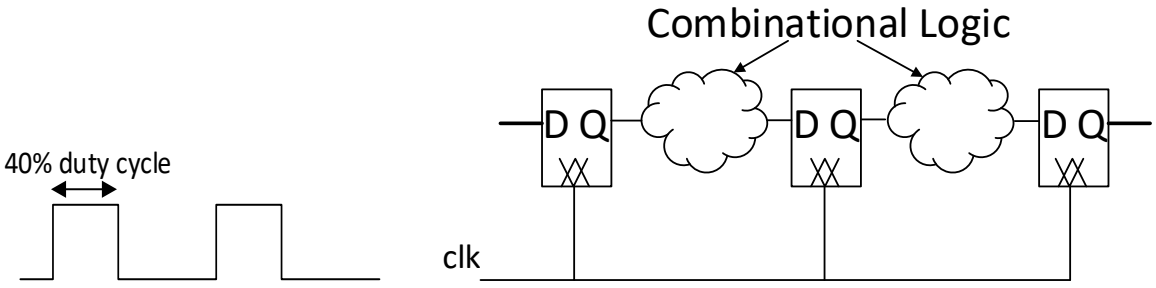


Timing Analysis and Voltage Scaling



Original unpipelined design

2. (20 points) Consider the Datapath shown in above. A designer decides to re-design it using a double-edge-triggered flip-flop (A flip flop that works on both, the rising and the falling edge of the clock). The pipelined design is shown below. The available clock has a 40% duty cycle. Timing properties of such a flip-flop are: T_{setup} = 50ps, T_{hold} = 50ps, T_{cq} = 50ps.



Pipelined design using double-edge triggered flops

a. (3 points) Determine the cycle-time of the original design
b. (8 points) Determine the maximum cycle time of such a pipelined design and its peak throughput.

Max Cycle Time :

Peak Throughput :

c. (9 points) Assuming a square-law current model, determine the energy savings obtained by such a pipelined design if it were voltage scaled to achieve the original . Ignore the power dissipation of the flip-flops.

Memory

3. (5 points)

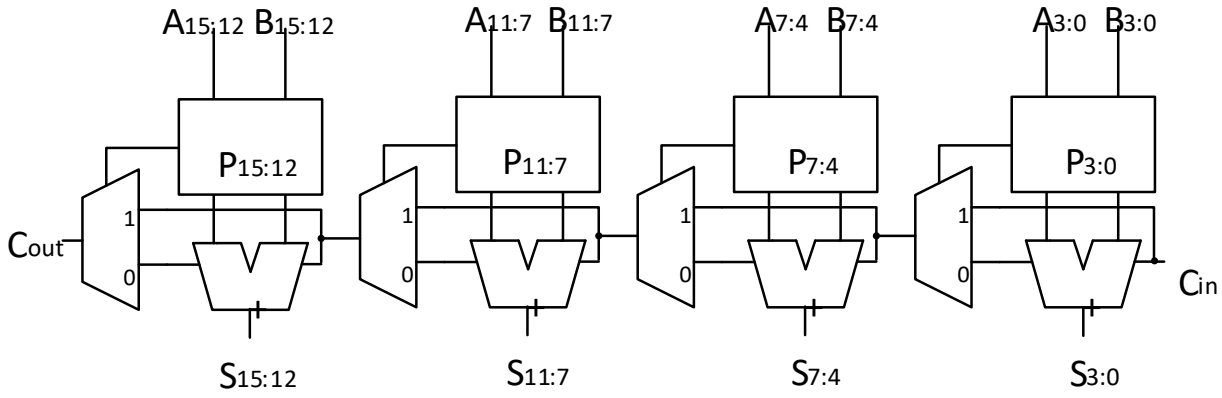
a. Why does a typical 6T SRAM cell pre-charge its bit-line to VDD instead of ground?

b. Consider an SRAM array with a 10-bit row-decoder, and a 5 bit column decoder. Each row of memory stores 4, 64-bit numbers. What is the capacity of the memory in Bytes

c. State the disadvantages of having many memory cells on a single bit-line

Adders

4a. (5 points) What is the **worst-possible delay** of a 16-bit carry skip adder that is made up of 4 equal skip-stages (4-bits each) Which gates would the path travel through (Sketch the path using a block diagram).

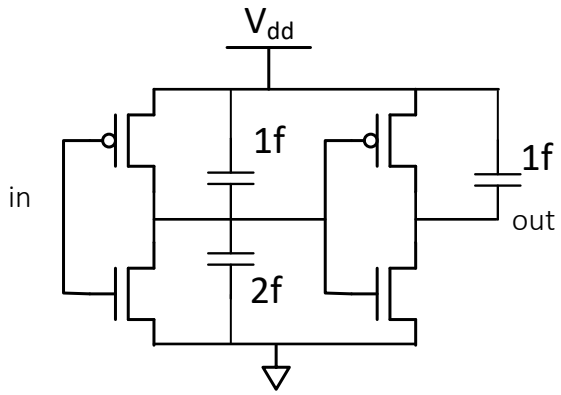


b. (5 points) Explain why it is not possible for the critical path to be equal to the carry-in rippling through every single 4-bit adder stage

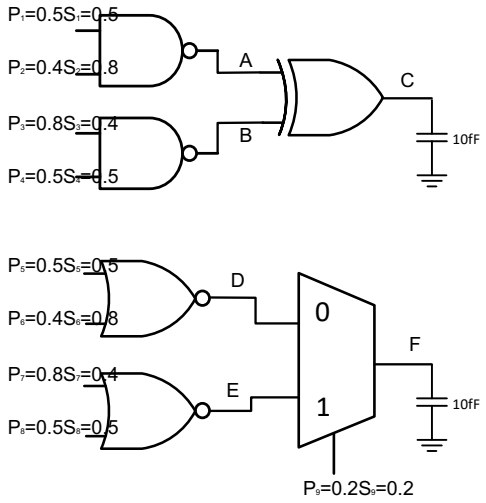
c. (5 points) Consider a carry skip adder built using 4 unequal sections of size 1,5,4,3,2,1. Write down the critical path of such an adder in terms of T_{AOI}, T_{mux}, T_{setup}. How does this delay compare to the traditional implementation if T_{AOI}, T_{MUX}, T_{setup} all take up 1 unit delay.

5. (12 points) For the circuit shown below complete the table below for energy delivered by the supply and energy dissipated for each transition

Input Transition	Energy delivered by supply	Energy dissipated in circuit
Rising		
Falling		



6. [2+2+3+4 = 11 points] Consider the circuit below with the provided switching activities and probabilities. Calculate the power dissipation expected in this netlist based on these parameters, and the load capacitance at nodes A, C, D and F . Report Energy for A, and C in terms of C_a and C_c.



7. [10 points] Consider the following inverter cascade. Solve for “x”, the input capacitance of the inverter to achieve the lowest energy-delay product. The input capacitance of the first stage is 1fF. Assume only contributor to energy is switching capacitance (ignore leakage and crowbar current)