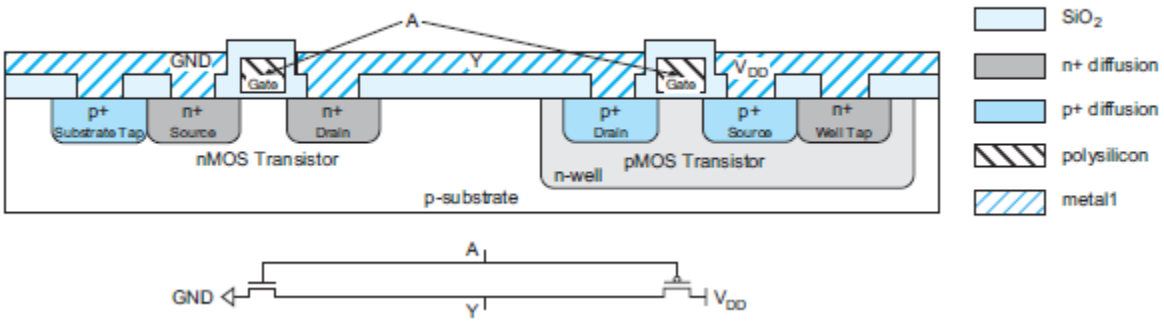
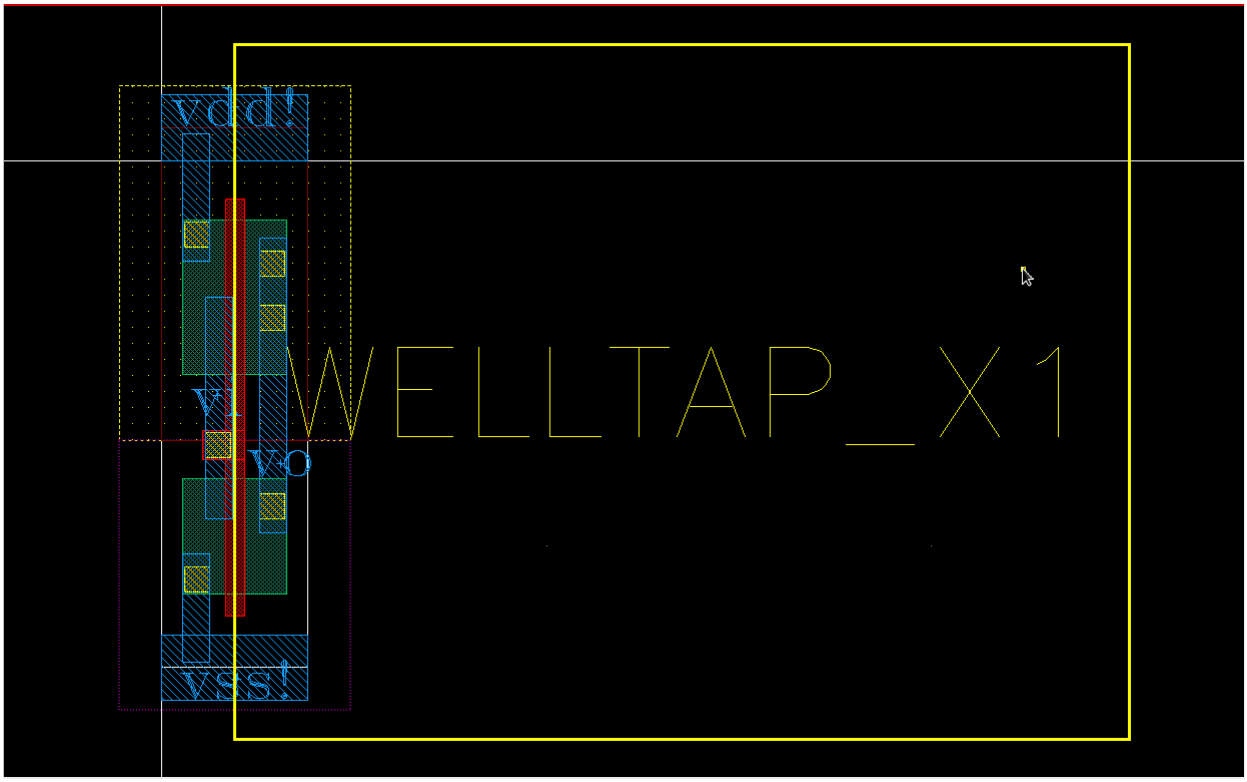
EE476: CAD 02

Kevin Egedy
October 27, 2022

Inverter Circuit



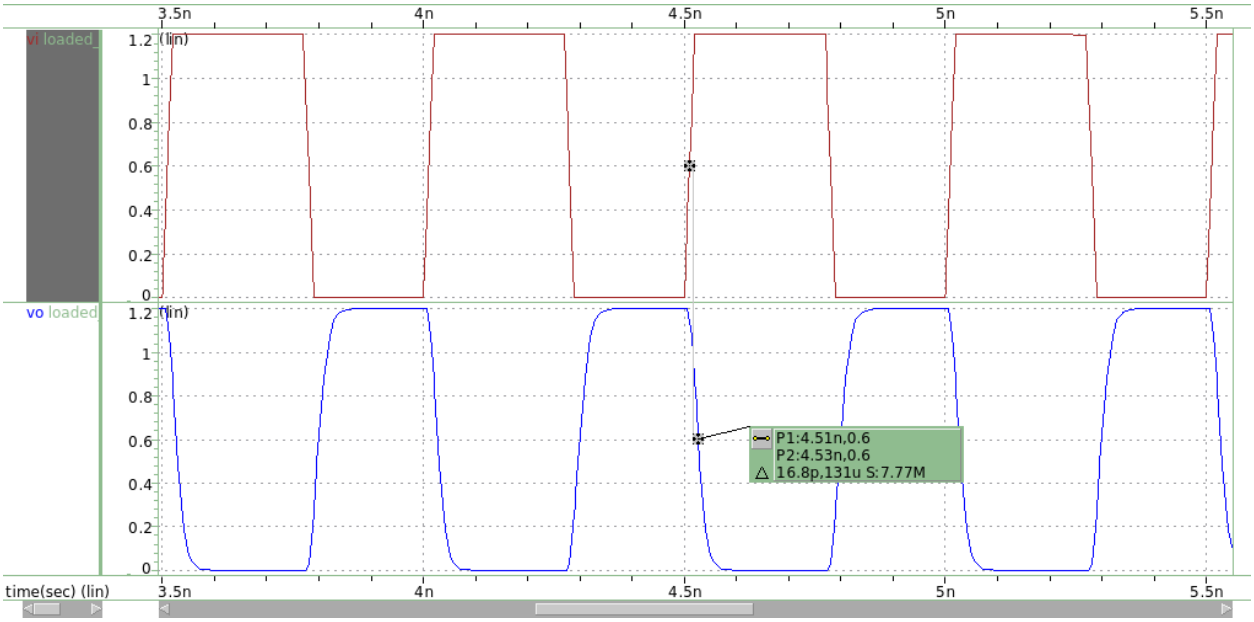


Inverter Layout

Schematic-Level Loaded Inverter

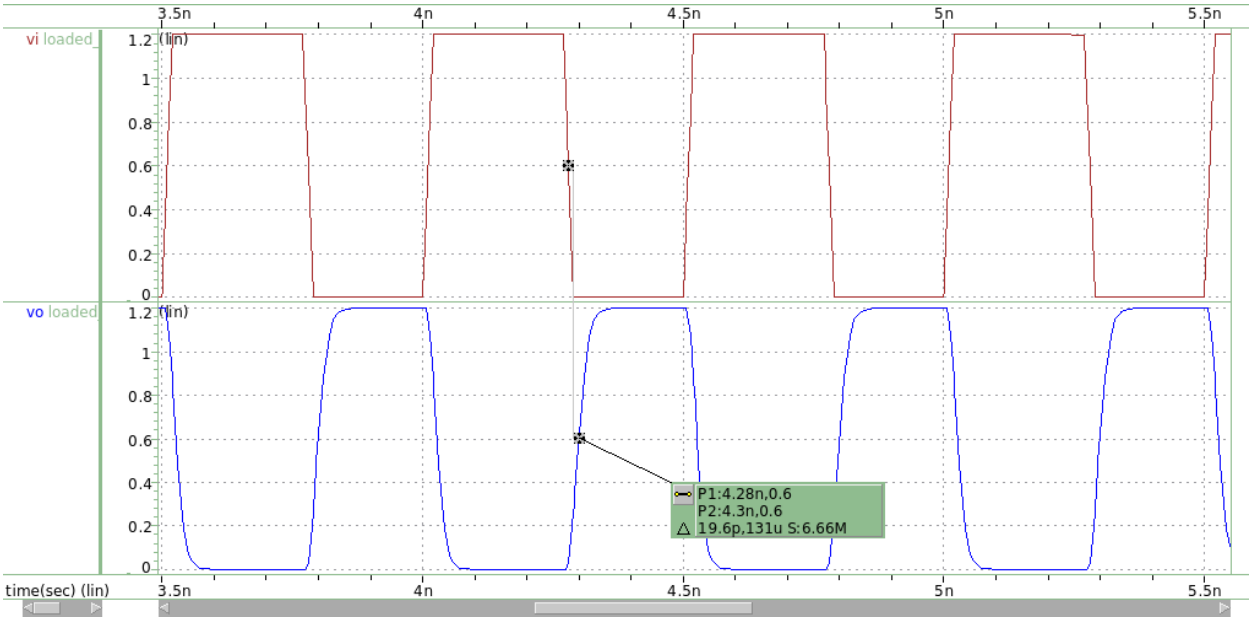
1.2V VDD

Rise Delay



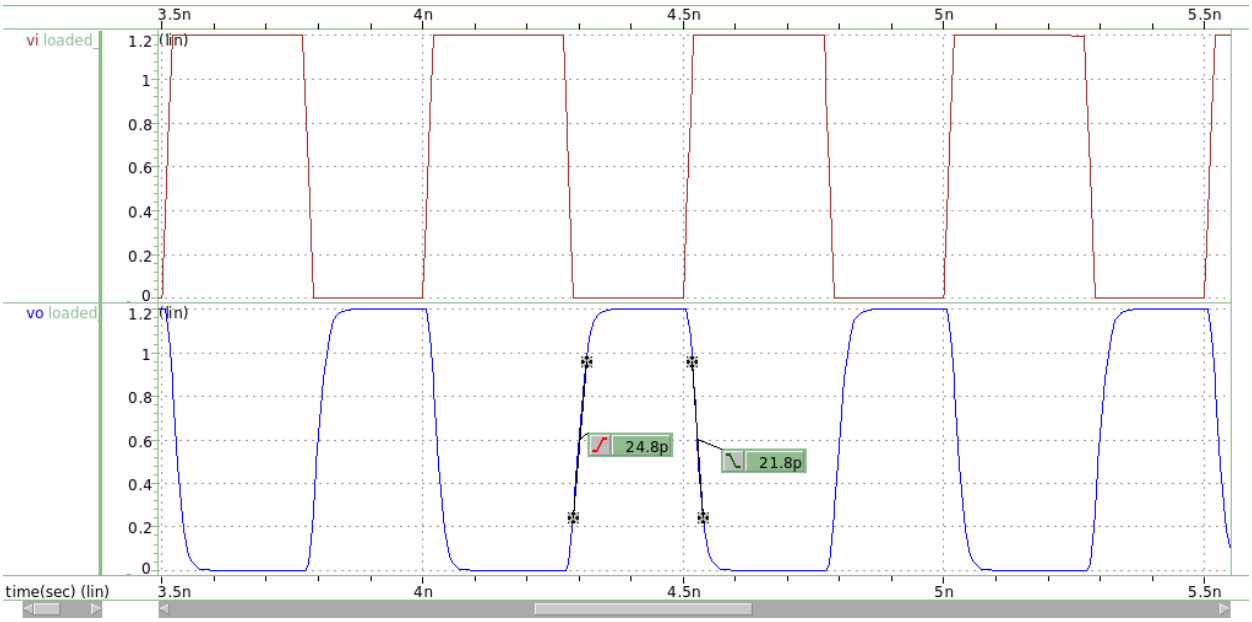
Output Rise Delay: 16.8ps

Fall Delay



Output Fall Delay: 19.6ps

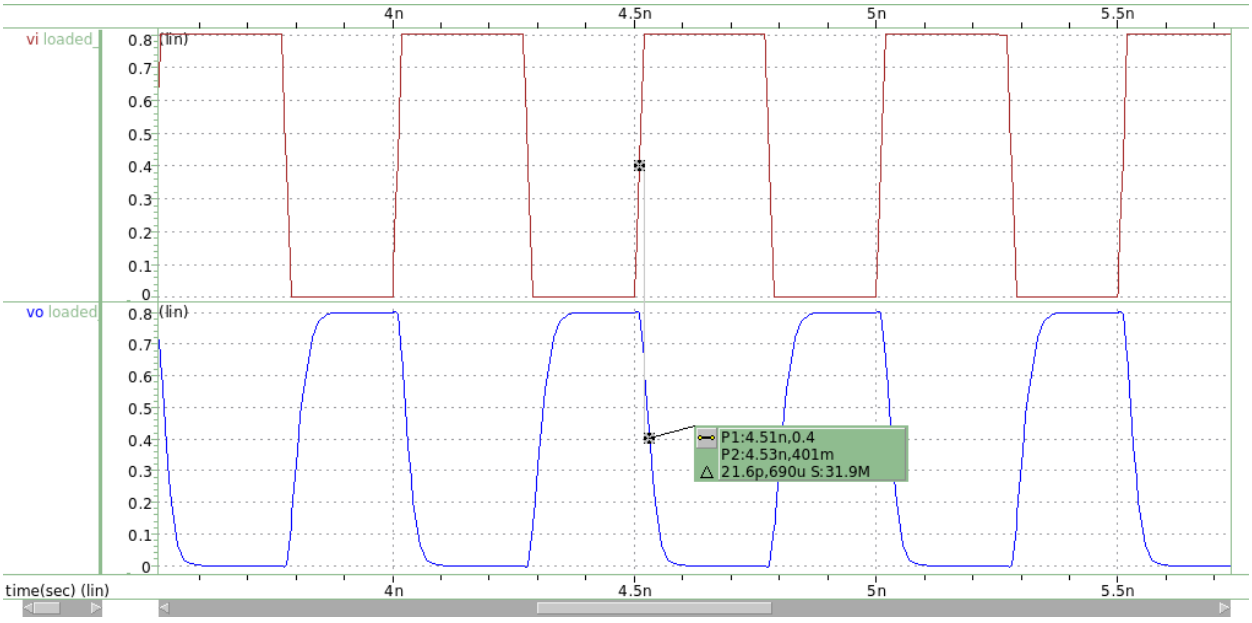
Rise Time / Fall Time



Output Rise Time: 24.8ps / Output Fall Time: 21.8ps

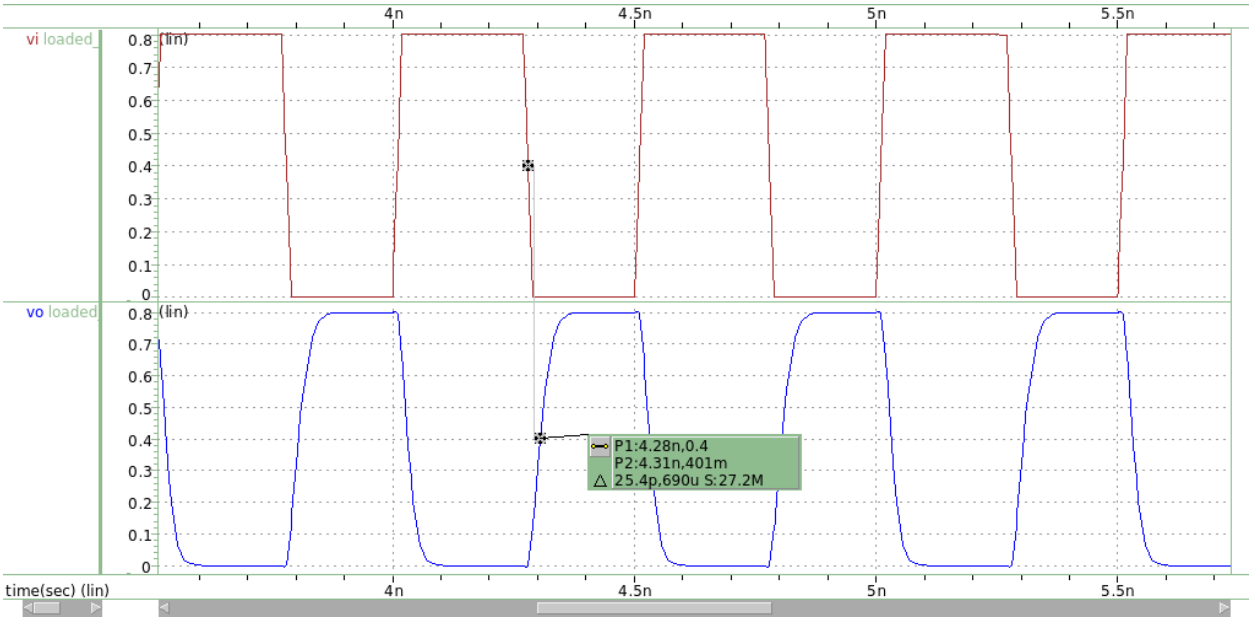
0.8V VDD

Rise Delay



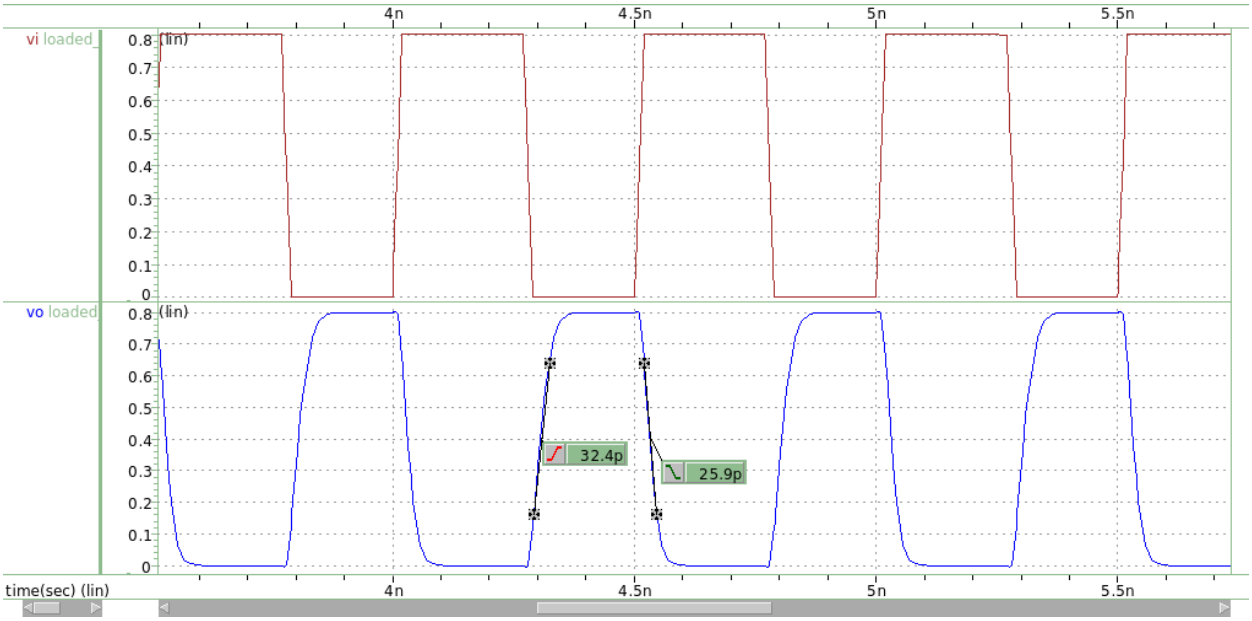
Output Rise Delay: 21.6ps

Fall Delay



Output Fall Delay: 25.4ps

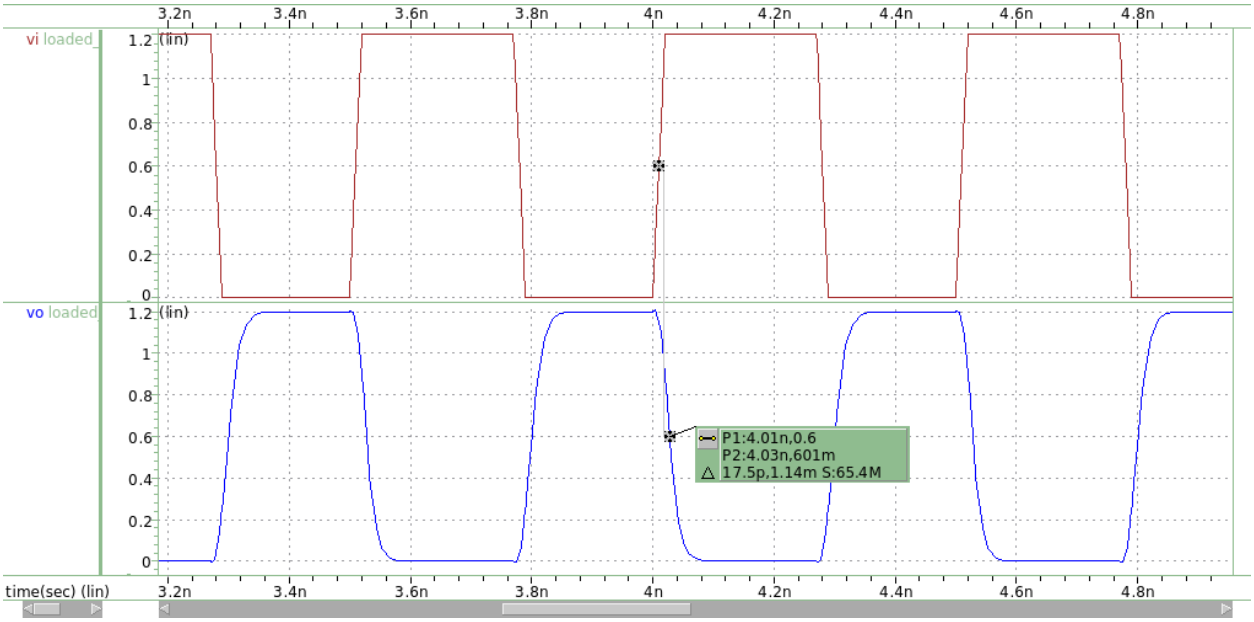
Rise Time / Fall Time



Output Rise Time: 32.4ps / Output Fall Time: 25.9ps

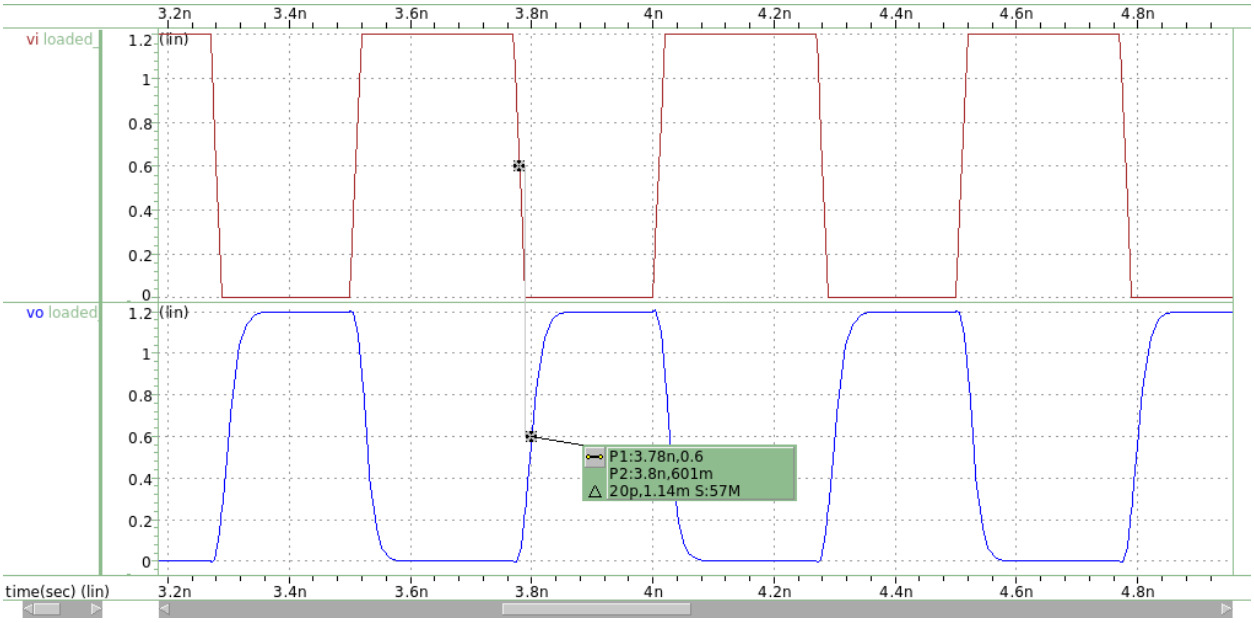
Post-layout Loaded Inverter (1.2V VDD)

Rise Delay



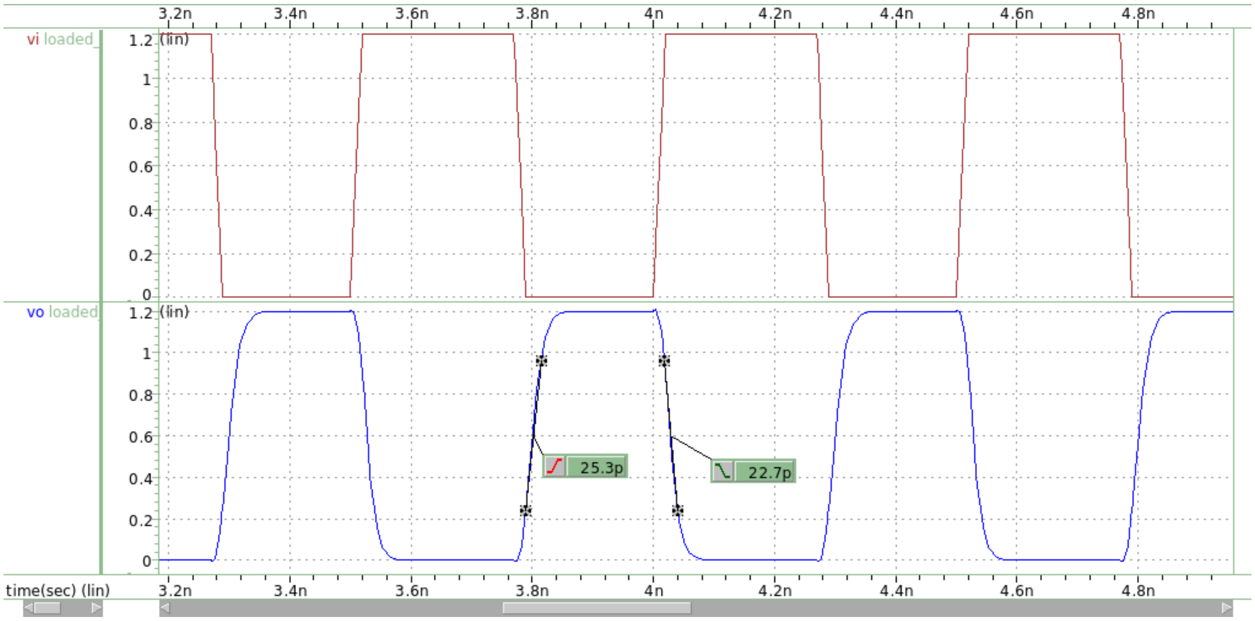
Output Rise Delay: 17.5ps

Fall Delay



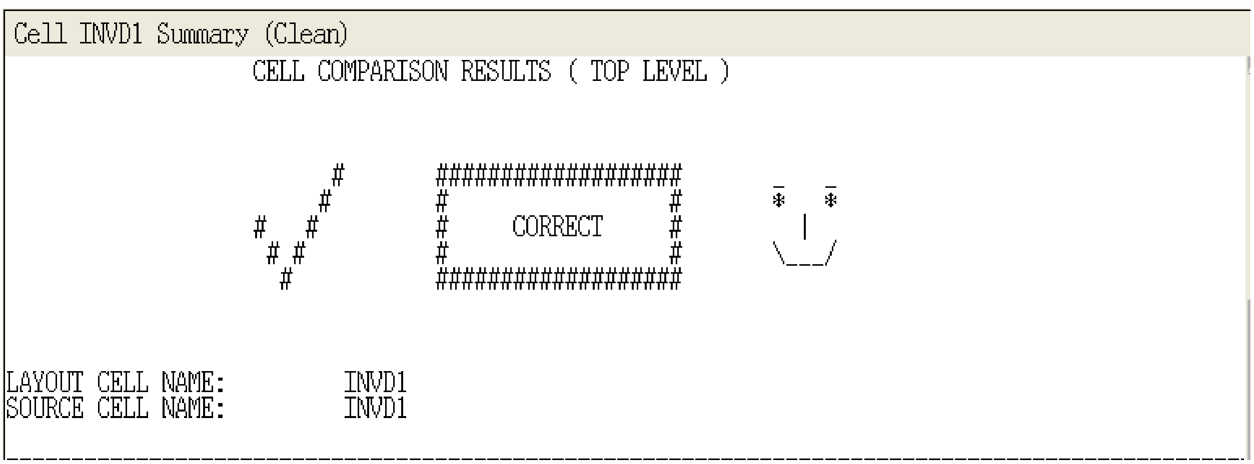
Output Fall Delay: 20.0ps

Rise Time / Fall Time



Output Rise Time: 25.3ps / Output Fall Time: 22.7ps

Layout LVS Report



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Cell INVD1 Summary (Clean)
                    CELL COMPARISON RESULTS ( TOP LEVEL )



                           #         ###################         _   _
                          #          #                 #         *   *
                    #    #           #     CORRECT     #           |
                     #  #            #                 #         \___/
                      #              ###################



LAYOUT CELL NAME:          INVD1
SOURCE CELL NAME:          INVD1

-------------------------------------------------------------------------------
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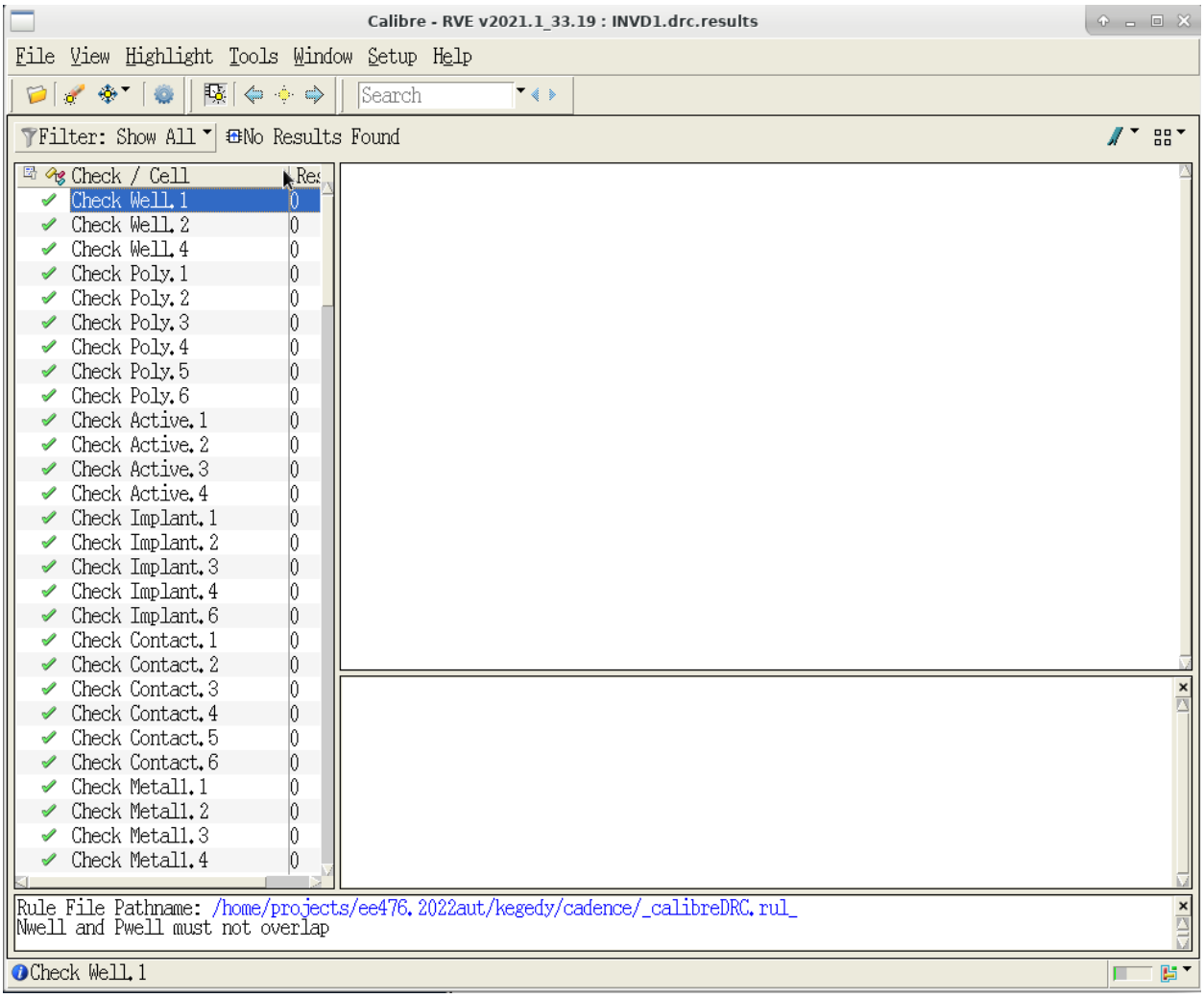
Inverter LVS Summary: INVD1.lvs.report

Layout DRC Summary



Inverter DRC Report: INVD1.drc.summary

Summary

Simulated a transient 500ps input pulse with 50% duty cycle and 20ps rise time / fall time.
All measurements for Vdd at 1.2V are faster than for Vdd at 0.8V. The layout measurements are slightly slower than the schematic equivalent using PMOS_VTL and NMOS_VTL.

	vdd08	vdd12	vddlayout
rise delay (s)	21.7E-12	16.8E-12	17.5E-12
fall delay (s)	25.4E-12	19.6E-12	19.7E-12
rise time (s)	32.4E-12	24.8E-12	25.3E-12
fall time (s)	25.9E-12	21.8E-12	22.7E-12

Double Fingered Inverter and Questions

1. The error in in Figures 27 such that Vo is only connected to one pair of the inverters. (Vi is connected to all gates in both figures.)

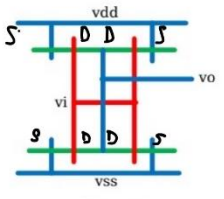


Figure 26

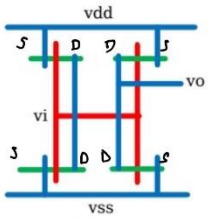
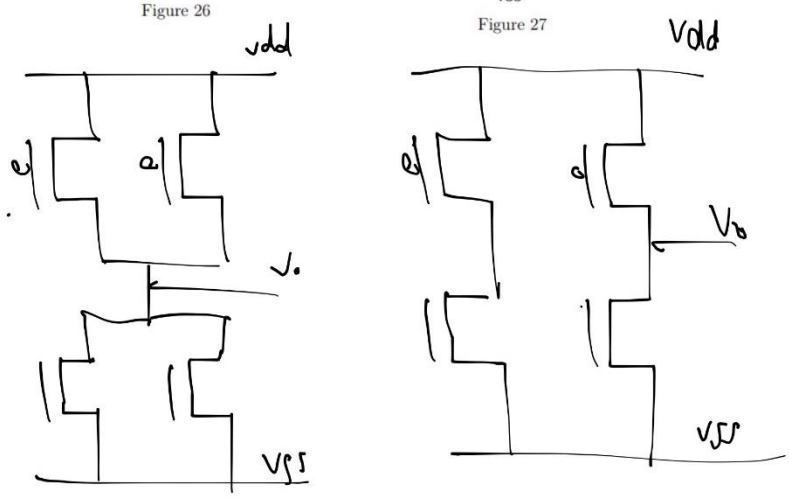


Figure 27



Vi is connected to all gates

2. Figure 26 is used in the standard inverter cell because it reduces the parasitic junction and wiring capacitance. Figure 26 uses less wire for Vo than Figure 27.