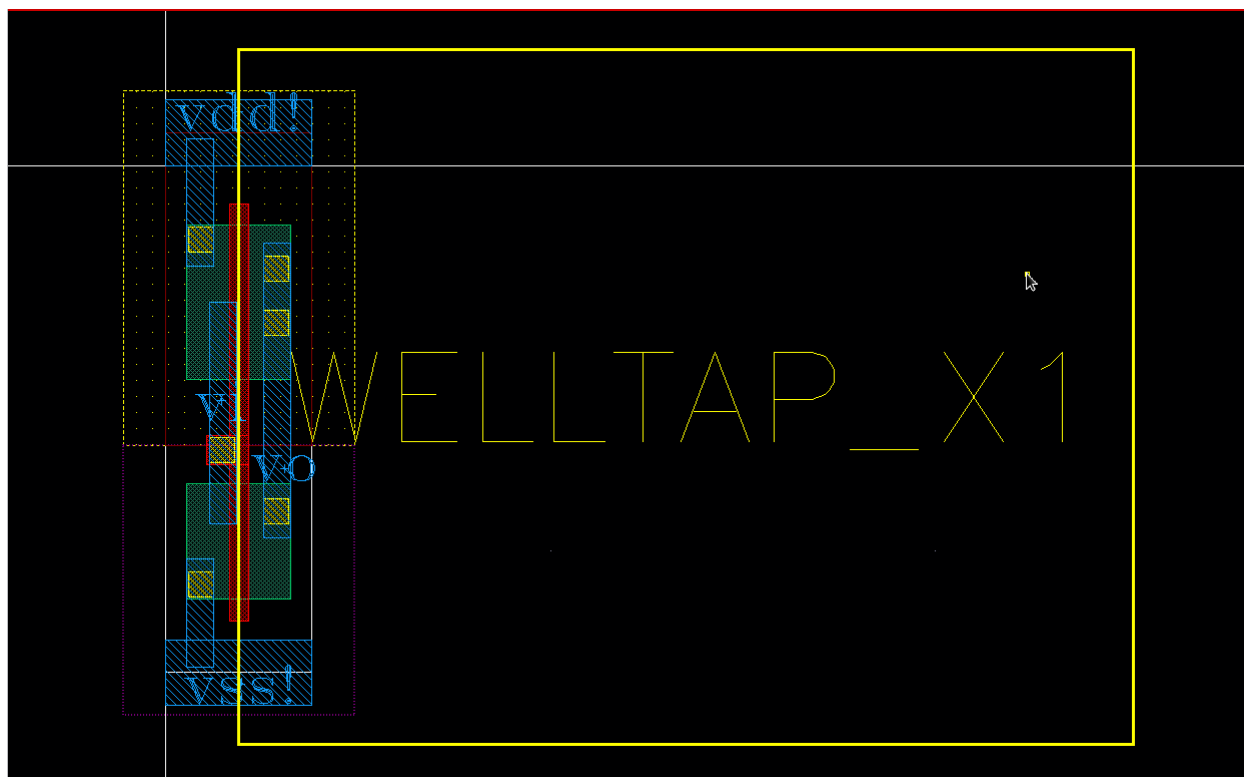
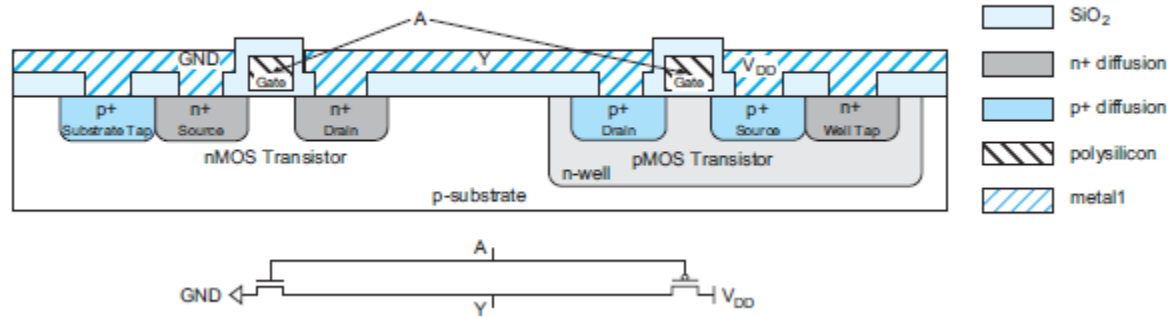


EE476: CAD 02

Kevin Egedy

October 27, 2022

Inverter Circuit

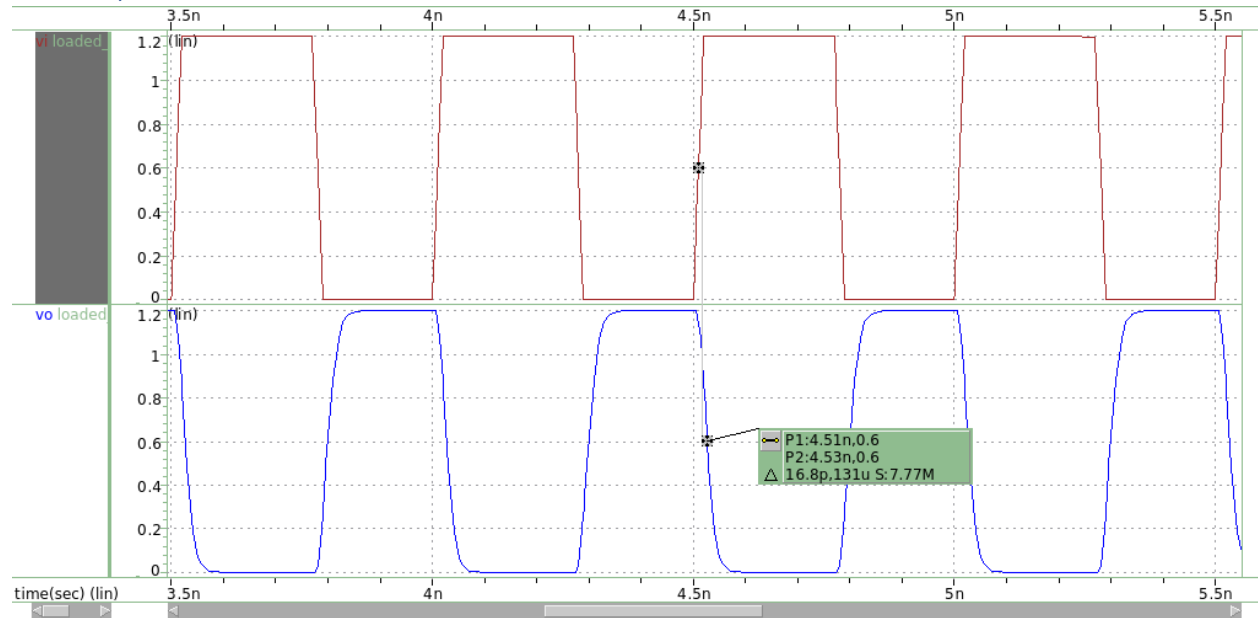


Inverter Layout

Schematic-Level Loaded Inverter

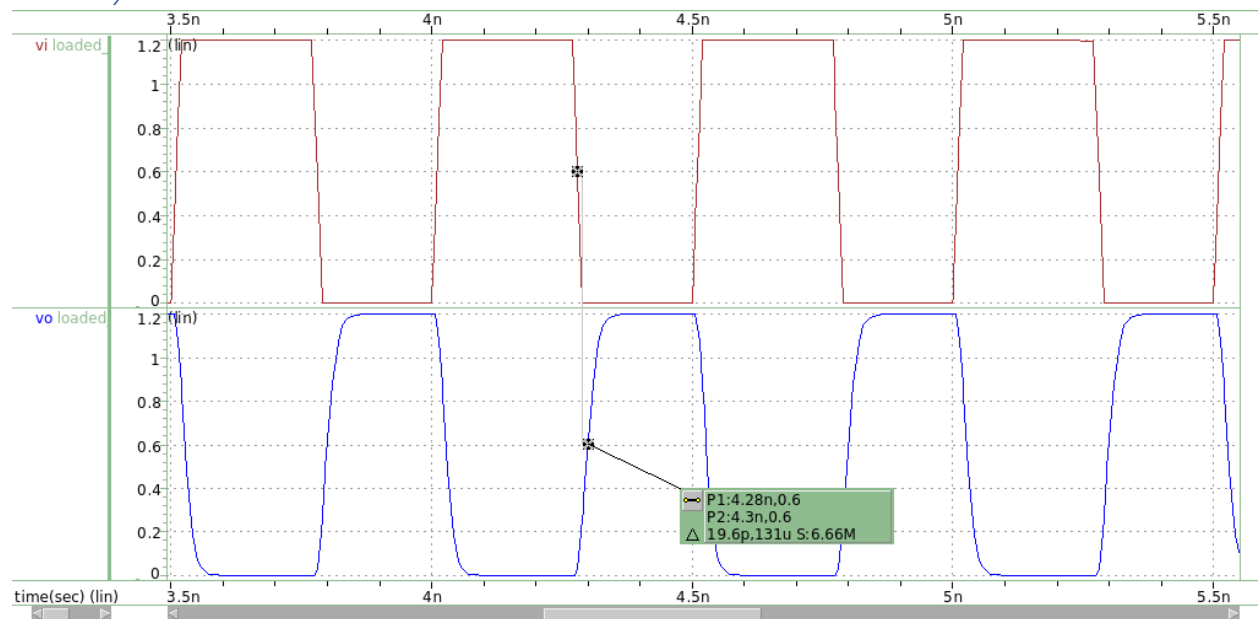
1.2V VDD

Rise Delay



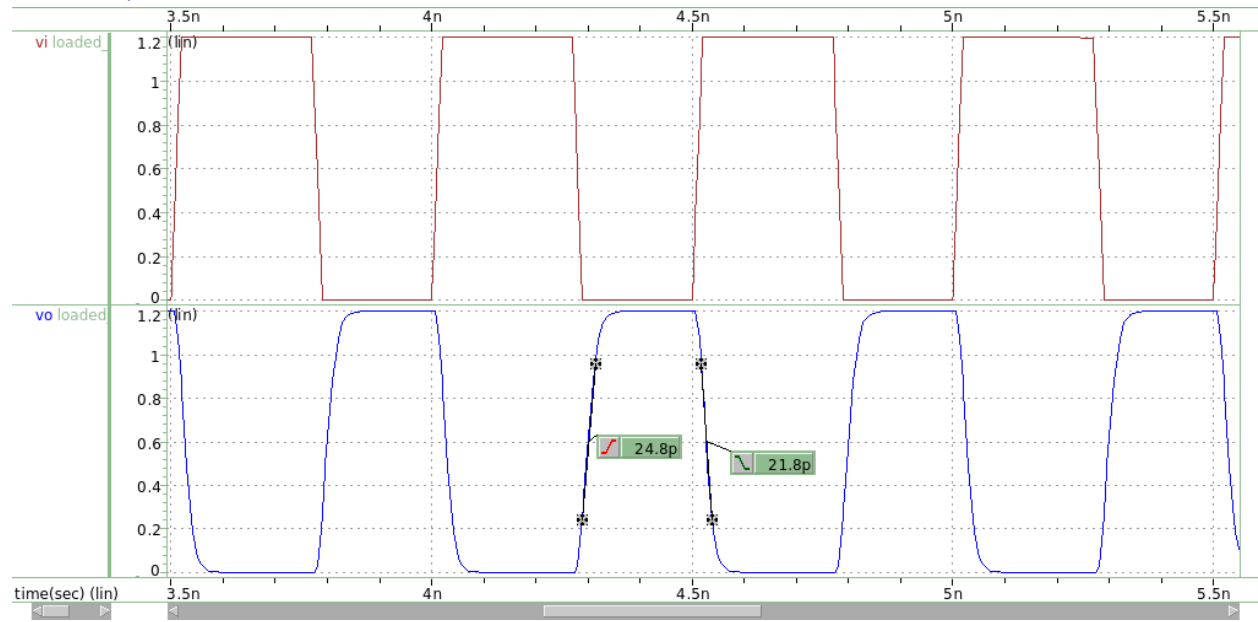
Output Rise Delay: 16.8ps

Fall Delay



Output Fall Delay: 19.6ps

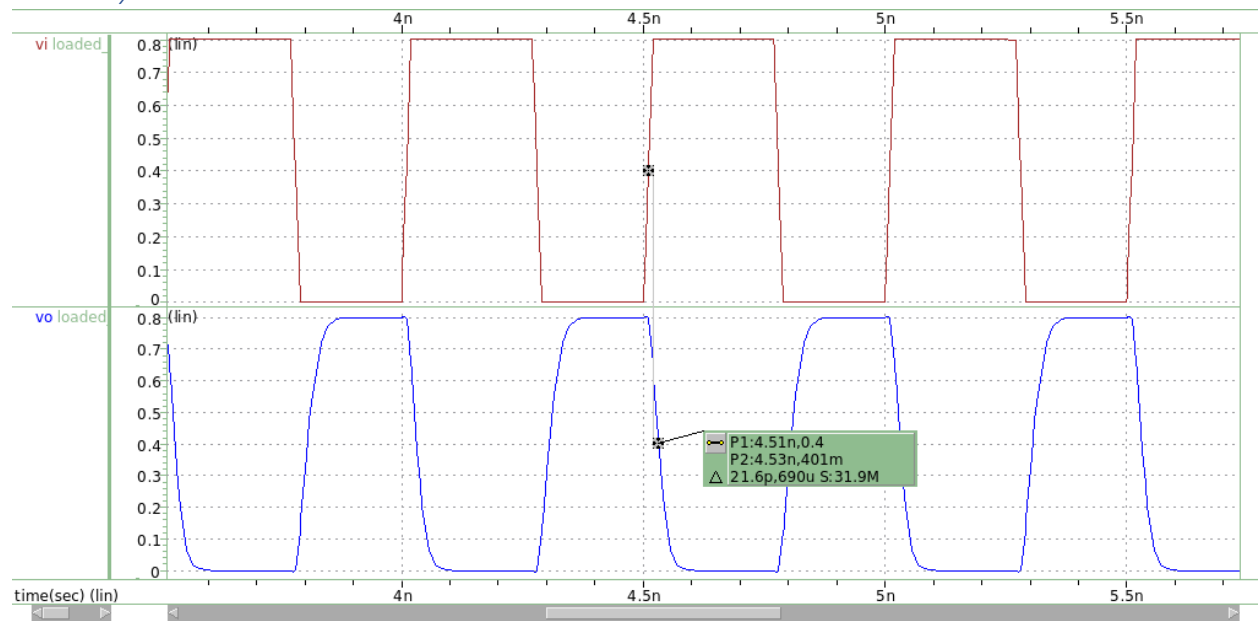
Rise Time / Fall Time



Output Rise Time: 24.8ps / Output Fall Time: 21.8ps

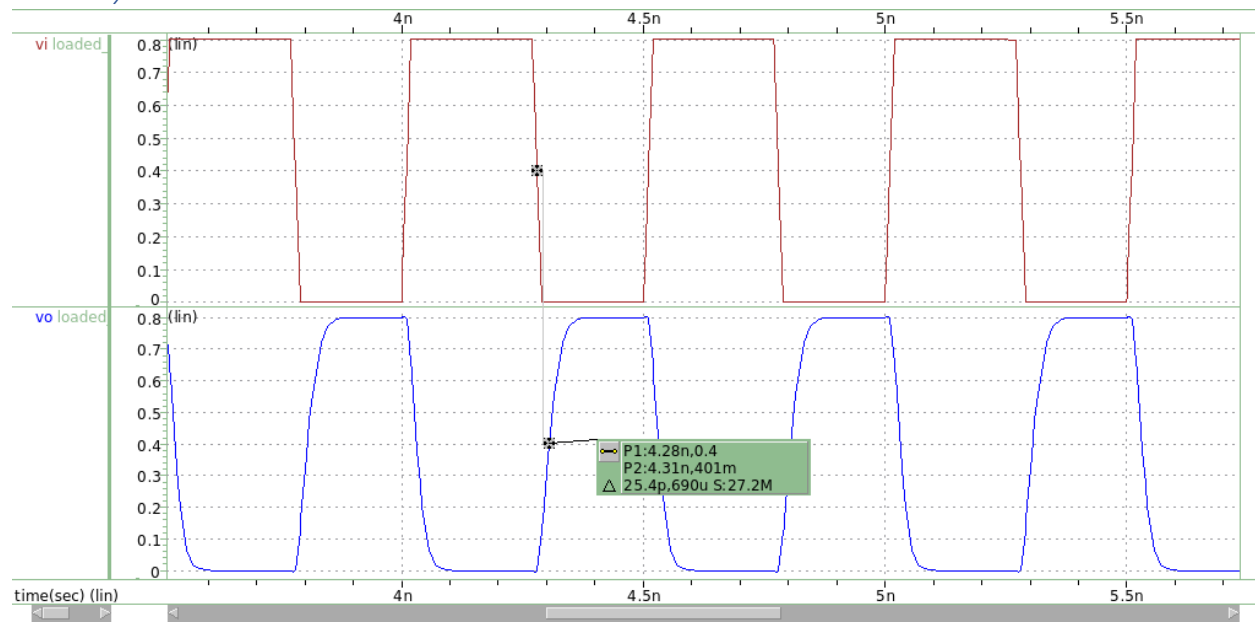
0.8V VDD

Rise Delay



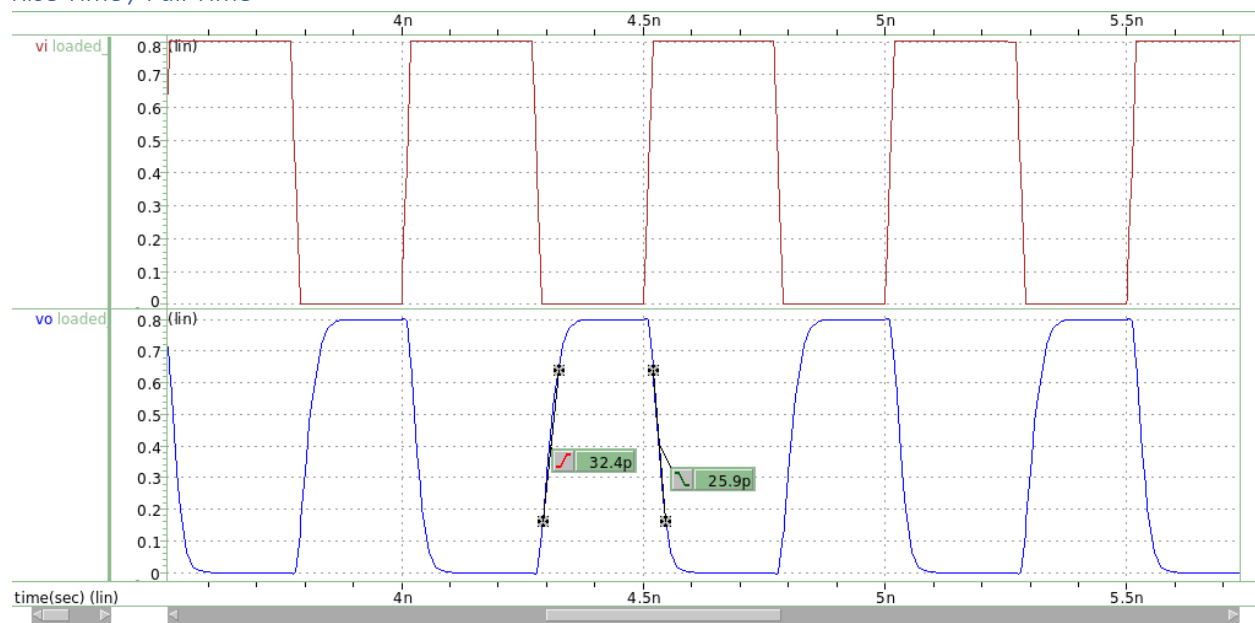
Output Rise Delay: 21.6ps

Fall Delay



Output Fall Delay: 25.4ps

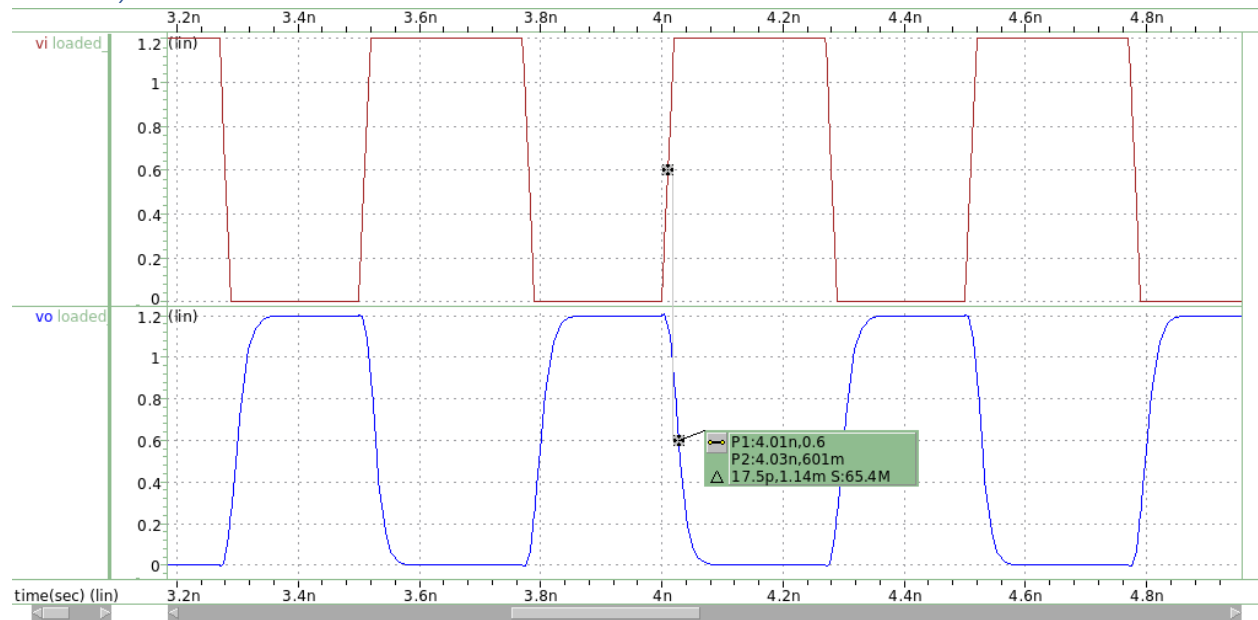
Rise Time / Fall Time



Output Rise Time: 32.4ps / Output Fall Time: 25.9ps

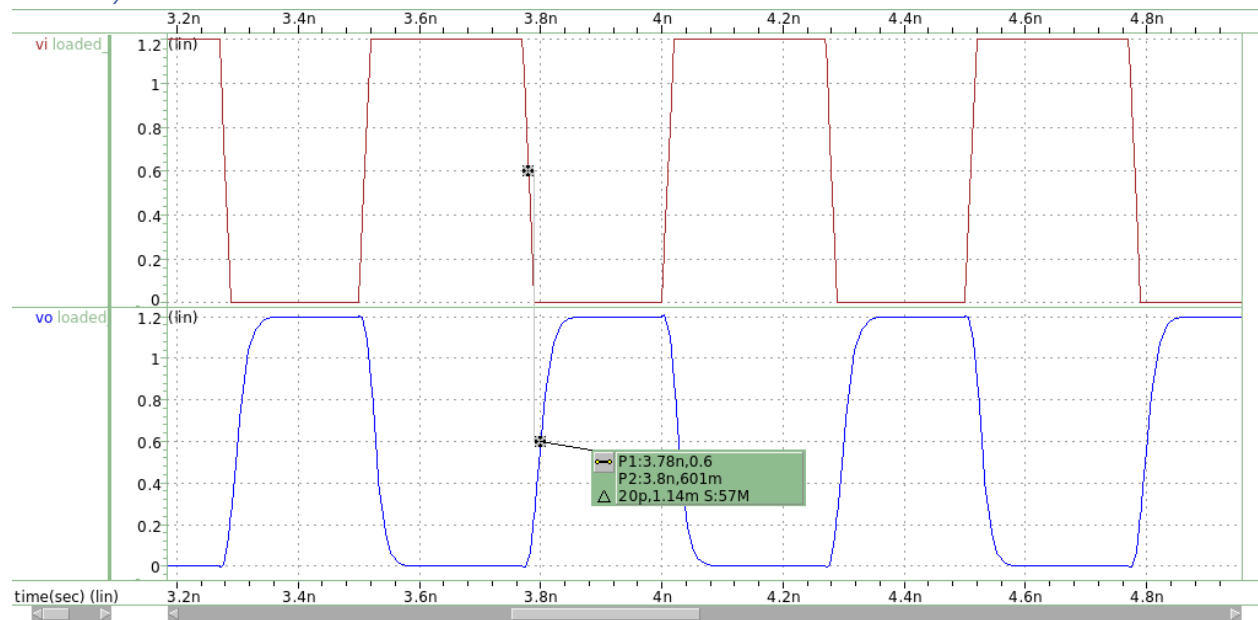
Post-layout Loaded Inverter (1.2V VDD)

Rise Delay



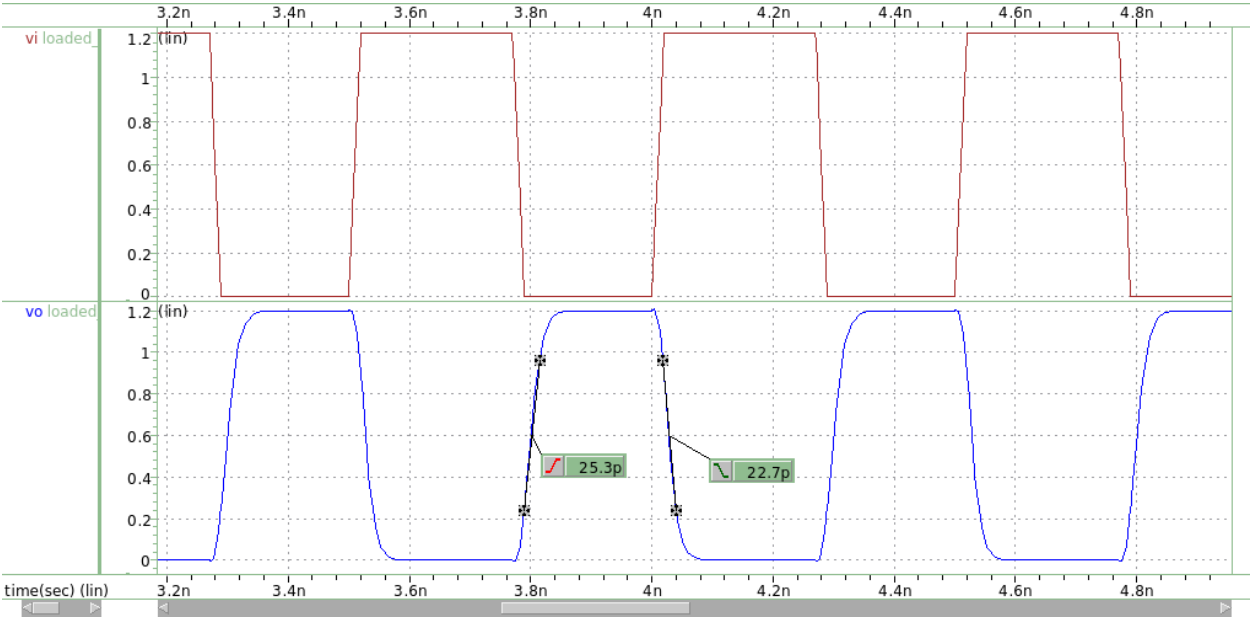
Output Rise Delay: 17.5ps

Fall Delay



Output Fall Delay: 20.0ps

Rise Time / Fall Time



Output Rise Time: 25.3ps / Output Fall Time: 22.7ps

Layout LVS Report

Cell INVD1 Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

#

CORRECT

#####

*
|
/ \

LAYOUT CELL NAME: INVD1

SOURCE CELL NAME: INVD1

Inverter LVS Summary: INVD1.lvs.report

Layout DRC Summary

The image shows a screenshot of the Calibre - RVE v2021.1_33.19 : INVD1.drc.results window. The window has a menu bar (File, View, Highlight, Tools, Window, Setup, Help) and a toolbar with icons for file operations and search. Below the toolbar is a filter section with a dropdown menu set to 'Show All' and a status indicator 'No Results Found'. The main area is a table with two columns: 'Check / Cell' and 'Results'. The table lists 28 checks, all of which have a green checkmark in the 'Check / Cell' column and a '0' in the 'Results' column. The checks are categorized by type: Well, Poly, Active, Implant, Contact, and Metall. The bottom of the window shows the rule file path and a specific rule: 'Rule File Pathname: /home/projects/ee476.2022aut/kegedy/cadence/_calibreDRC.rul_ (Nwell and Pwell must not overlap)'. The status bar at the very bottom shows 'Check Well.1'.

Check / Cell	Results
✓ Check Well.1	0
✓ Check Well.2	0
✓ Check Well.4	0
✓ Check Poly.1	0
✓ Check Poly.2	0
✓ Check Poly.3	0
✓ Check Poly.4	0
✓ Check Poly.5	0
✓ Check Poly.6	0
✓ Check Active.1	0
✓ Check Active.2	0
✓ Check Active.3	0
✓ Check Active.4	0
✓ Check Implant.1	0
✓ Check Implant.2	0
✓ Check Implant.3	0
✓ Check Implant.4	0
✓ Check Implant.6	0
✓ Check Contact.1	0
✓ Check Contact.2	0
✓ Check Contact.3	0
✓ Check Contact.4	0
✓ Check Contact.5	0
✓ Check Contact.6	0
✓ Check Metall.1	0
✓ Check Metall.2	0
✓ Check Metall.3	0
✓ Check Metall.4	0

Rule File Pathname: /home/projects/ee476.2022aut/kegedy/cadence/_calibreDRC.rul_
(Nwell and Pwell must not overlap)

Check Well.1

Inverter DRC Report: INVD1.drc.summary

Summary

Simulated a transient 500ps input pulse with 50% duty cycle and 20ps rise time / fall time.

All measurements for Vdd at 1.2V are faster than for Vdd at 0.8V. The layout measurements are slightly slower than the schematic equivalent using PMOS_VTL and NMOS_VTL.

	vdd08	vdd12	vddlayout
rise delay (s)	21.7E-12	16.8E-12	17.5E-12
fall delay (s)	25.4E-12	19.6E-12	19.7E-12
rise time (s)	32.4E-12	24.8E-12	25.3E-12
fall time (s)	25.9E-12	21.8E-12	22.7E-12

Double Fingered Inverter and Questions

1. The error in in Figures 27 such that Vo is only connected to one pair of the inverters. (Vi is connected to all gates in both figures.)

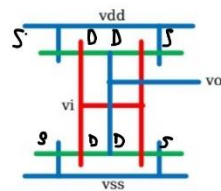


Figure 26

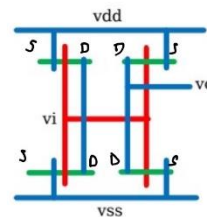
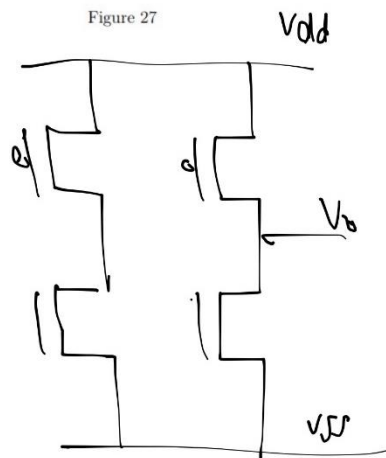
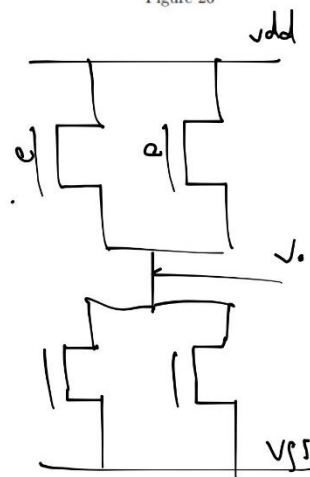


Figure 27



Vi is connected to all gates

2. Figure 26 is used in the standard inverter cell because it reduces the parasitic junction and wiring capacitance. Figure 26 uses less wire for Vo than Figure 27.