EE 458/ 533 – Power Electronics Controls, Winter 2022

Midterm – Cover Page

Due: Sunday February 6th 2022, 11:59 pm Pacific Time

Name: _____

Instructions.

- Show all your work and clearly indicate your final answer for each problem.
- Open-book, use any resource you want.
- Submit your solution and all the PLECS/ Simulink models and Matlab/ Python scripts you might have used. Comment the script as well as simulation models to help us evaluate what you have tried to do.
- While overlapping waveforms and recording bode plots, ensure the axis, legends and other relevant details are clear. Provide zoomed in waveforms in addition to the normal waveform to show the crossover frequencies and tracking / disturbance rejection etc.
- Please do not discuss this exam with anyone else until submission.
- There is a choice between Prob 3 (e) and (f). Do only one. You *might* get extra credit if you solve both.

Problem 1: Conceptual Questions [10 Points Total]
For each of the statements below, state if they are true or false.
If true, provide justification, if false provide a counter-example or a logical explanation. No marks will be rewarded for only true or false identification without proper reasoning.

1. For the same PWM clock frequency as I keep increasing the number of bits available for PWM (assume $N_r = 2^{\text{no of PWM bits}}$), both switching frequency and quantization of duty ratio increases.

2. For a synchronous boost converter in Fig. 1, for unidirectional power transfer (power flows from v_g to R), the MOSFET used for storing energy in L suffers both switching and conduction loss, whereas the MOSFET used for transfering energy from L to C suffers only conduction loss.

3. For an input signal $x(t)$,

$$x(t) = a_1 \sin(2\pi\, 900t) + a_2 \sin(2\pi\, 1001t) + a_3 \sin(2\pi\, 2004t),$$

   sampled at a frequency of 2000 Hz, the reconstructed signal will have frequencies of the following three components: $1, 4, 900$ Hz.

4. For a minimum phase system (system with no right half zero, right half pole or delay) a *sufficient* condition of stability is that the system's gain cross over frequency has a value smaller than the system's phase cross over frequency.

5. For a buck converter, the input voltage-to-duty ratio transfer function can be described by the following system of differential equation,

$$LC\frac{d^2 v_g(t)}{dt^2} + \frac{L}{R}\frac{dv_g(t)}{dt} + v_g(t) = Dd(t), \tag{1}$$

   where $d(t)$ is the duty ratio input and $v_g(t)$ is the input voltage.

   We can claim that if the duty ratio input, $d(t)$ is a function with magnitude of 1 at t = 0 and zero elsewhere (in literature we call this the delta dirac function), the same system can be described as, $\frac{dv_g(t)}{dt}|_{t=0} = D$.

Problem 2: Mathematical Methods for Dynamic Modeling [40 Points Total]
Consider the boost converter in Fig. 1. The input voltage is $v_g(t)$, and output voltage is $v(t)$. Configuration ① has a duty ratio of $d(t)$, and ② has a duty ratio of $d'(t) = 1 - d(t)$. Each MOSFET has an on-state resistance of R_{on} (all other elements are lossless). The states are the capacitor voltage $v(t)$, and current $i(t)$ through the inductor.

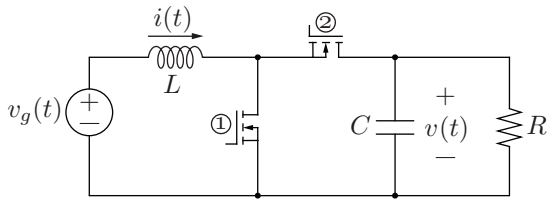

Figure 1: Boost converter for Problems 2 and 3.

(a) **[10 Points]** Derive the differential equations for the averaged inductor current, $\langle i(t)\rangle$, and averaged capacitor voltage, $\langle v(t)\rangle$. Put your result into the form

$$\dot{x}(t) = f(x(t), u(t)),$$

where

$$x(t) = \begin{bmatrix} \langle i(t)\rangle \\ \langle v(t)\rangle \end{bmatrix}, \quad u(t) = \begin{bmatrix} d'(t) \\ \langle v_g(t)\rangle \end{bmatrix}, \quad f(x(t), u(t)) = \begin{bmatrix} f_1(x(t), u(t)) \\ f_2(x(t), u(t)) \end{bmatrix}.$$

(b) **[15 Points]** Derive a linearized small-signal model of the form

$$\dot{\widehat{x}}(t) \approx \mathcal{A}\widehat{x}(t) + \mathcal{B}\widehat{u}(t),$$
$$\widehat{y}(t) = \mathcal{C}\widehat{x}(t) + \mathcal{E}\widehat{u}(t),$$

where $\mathcal{A}, \mathcal{B} \in \mathbb{R}^{2\times 2}$ are real-valued square 2×2 matrices, and

$$x(t) = \widehat{x}(t) + X, \quad u(t) = \widehat{u}(t) + U, \quad X = \begin{bmatrix} I \\ V \end{bmatrix}, \quad U = \begin{bmatrix} D' \\ V_g \end{bmatrix}.$$

$\widehat{y}(t)$ is chosen to correspond to the capacitor state such that

$$\widehat{y}(t) = \langle \widehat{v}(t) \rangle.$$

Express all entries in $\mathcal{A}$ and $\mathcal{B}$ in terms of $I, V, D', V_g, R, L, C, R_{\text{on}}$ and give $\mathcal{C}$ and $\mathcal{E}$.

(c) **[15 Points]** Given the matrices $\mathcal{A}, \mathcal{B}, \mathcal{C}$, and $\mathcal{E}$, derive the capacitor voltage in the frequency domain using the following formula:

$$\widehat{y}(s) = \langle v(s) \rangle = \underbrace{\left(\mathcal{C}(s\mathcal{I} - \mathcal{A})^{-1}\mathcal{B} + \mathcal{E}\right)}_{G(s)} \widehat{u}(s),$$

where $\mathcal{I}$ is the 2×2 identity matrix, $\widehat{u}(s) \in \mathbb{C}^{2\times 1}$ is a complex column vector, and $G(s) \in \mathbb{C}^{1\times 2}$ is a complex 1×2 row vector given by

$$G(s) = \begin{bmatrix} G_{vd}(s) & G_{vg}(s) \end{bmatrix}.$$

Problem 3: Controller Design Problem [30 Points Total]- a,b,c,d are compulsory, choose one from e,f.

The theoretical model of a closed loop system is shown in Fig. 2 where $C(s)$ is the controller and $P(s)$ is the plant transfer function.

Also note, $r(s)$ is the reference, $y(s)$ is the output, $e(s)$ is the error and $u(s)$ is the control effort.

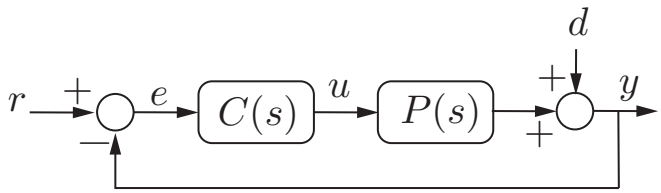

Figure 2: Closed loop control system

(a) **[10 Points]** Derive the following transfer functions:

1. $\frac{y(s)}{r(s)}$ (consider $d(s) = 0$ for this),**[4 Points]**
2. $\frac{y(s)}{d(s)}$ (consider $r(s) = 0$ for this),**[4 Points]**

in terms of $C(s)$ and $P(s)$.

Let $\frac{y(s)}{r(s)} := T(s)$ and $\frac{y(s)}{d(s)} := S(s)$, then which of the following is/are true? **[2 Points]**

1. $T(s) = -S(s)$,
2. $T(s) = 1 - S(s)$,
3. $\frac{dT(s)}{ds} + \frac{dS(s)}{ds} = 0$.

(b) **[5 Points]** Assume the transfer function $P(s)$ in Fig. 2 has the following form,

$$P(s) = \frac{0.35p}{(\frac{4s}{3p} + 1)\,(\frac{s}{5p} + 1)\,(\frac{5s}{p^2} + 1)}, \tag{2}$$

where p is the sum of day, month and year of your birth-date divided by ten: (dd+mm+yyyy)/10. (For example, for 10th December 1993, p = (10+12+1993)/10 = 201.5)

You should not reveal your date of birth, please proceed by mentioning the value of p and solving the subsequent questions.

Sketch the bode plot of the plant, $P(s)$ and find the gain and phase margin.

Show the following in your plot clearly: gain cross over frequency, phase cross over frequency, gain margin, phase margin.

(c) **[5 Points]**Assume there is no disturbance in the system ($d = 0$). Design a controller $C(s)$ such that the closed loop system tracks a steady dc reference perfectly and the compensated loop gain, $\ell(s) = C(s)P(s)$, has a phase margin of *at least* 30°.

Report $C(s)$ and elucidate the steps of your controller design. Report the new gain and phase margins of the compensated system, $\ell(s)$. Overlay the bode plot of plant $P(s)$ and the loop gain $\ell(s) = C(s)P(s)$ on a single plot.

(d) **[5 Points]** Plot the response of your closed loop system (with the controller derived in previous part) to a step function (r is a step function changing from 0 to 1 at 0.1 seconds) and show the tracking performance. Record reference (r), output (y), error (e) and control effort (u) on the same plot till the output, y converges to 1.

Zoom in considerably to convince that you have achieved zero steady-state error.

[Hint: You can use Transfer Function Blocks in Plecs to simulate the system.]

(e) **[5 Points]** Again, assume $d = 0$. You are now asked to design a controller that has the following time domain specifications:

- Maximum permissible overshoot is 30% (so for a unit step reference, maximum output permissible is 1.3).
- Rise time to be less than 5 ms (the time taken for output to rise from 0.1 to 0.9 is at worst 5 ms).

[2 Points] From the time domain data, what target bandwidth and phase margin are you going to design your controllers for?

[3 points] Write down the steps of controller design and explicitly write the final form of controller $C(s)$. Plot the response of your closed loop system to a step function (r is a step function changing from 0 to 1 at 0.1 seconds) and show the tracking performance. Record reference (r), output (y), error (e) and control effort (u) on the same plot till the output, y converges to 1.

(f) **[5 Points]** Disturbance Rejection

- **[3 Points]** In your original control system of Fig.2, now introduce a disturbance, $d = 0.5\ \sin(2\pi\, 10\, t)$ that is present at all times.

  Plot the response of your closed loop system to a step change in reference (r is a step function changing from 0 to 1 at 0.1 seconds), include disturbance as mentioned. Show the tracking performance by zooming appropriately. Record reference (r), output (y) and disturbance(d) on the same plot till the output, y converges around 1.

- **[2 Points]** Redesign your controller so that in addition to the design constraints of part (c), you now ensure that the oscillation in output voltage is reduced to less than 20% of the input disturbance magnitude.

  Report $C(s)$ and the new gain and phase margins of the compensated system, $\ell(s)$.

  Plot the response of your closed loop system to a step change in reference (r is a step function changing from 0 to 1 at 0.1 seconds), use disturbance as mentioned. Show the tracking performance and disturbance rejection by zooming appropriately. Record reference (r), output (y) and disturbance(d) on the same plot till the output, y converges around 1.

Problem 4: Digital Systems [20 Points Total]

(a) **[10 Points]** On the top, draw an asymmetric trailing-edge carrier with period T_s and whose counter varies between $0 \leq x_\mathrm{pwm} \leq N_r$. Sketch a compare value, x_c, that updates each time the counter equals zero. On the bottom, draw the PWM output. Clearly mark the modulation delay, t_mod, and express it in terms of D and T_s.

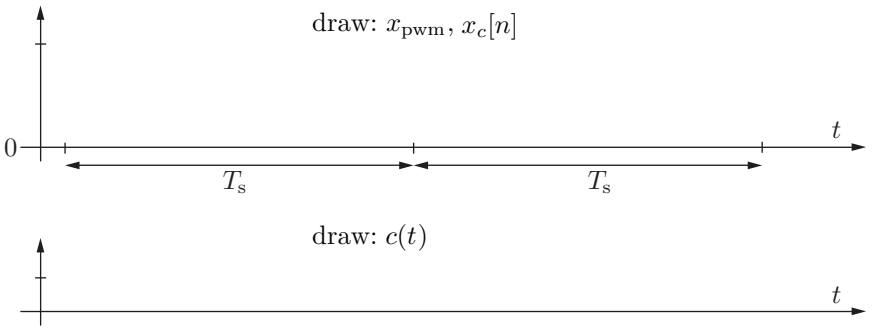

Figure 3: Template for PWM waveforms.

(b) **[5 Points]** Given the carrier in (a) and clock period $T_\mathrm{clk} = (100\,\mathrm{MHz})^{-1}$, compute N_r such that the $f_s = 50\,\mathrm{kHz}$.

(c) **[5 Points]** Consider an 8-bit ADC with full-scale range $V_\mathrm{FS} = 1\,\mathrm{V}$. If the digital integer produced by the ADC is $x_\mathrm{A/D} = 107$, then what is the physical voltage, $v_\mathrm{A/D}$, on the ADC pin? Hint: You can neglect the rounding behavior of the ADC for this calculation.