DacaRegs.DACCTL.bit.DACREFSEL pg(1635,1639)
Def: DAC Control Register
EE533:

- DACREFSEL: set to ADC reference
- LOADMODE: update DAC value on SYSCLK
- MODE: set Gain=2

DacaRegs.DACOUTEN.bit.DACOUTEN pg(1642)
Def: DAC Output Enable Register
EE533: Enable output

DacaRegs.DACVALS.all pg(1641)
Def: DAC Value Register - Shadow
EE533: Clear to start

```
void initDAC(void); //line82

initDAC(); //line144

void initDAC(void) //line360
{
  EALLOW;
  DacaRegs.DACCTL.bit.DACREFSEL = 0b1;
  DacaRegs.DACCTL.bit.LOADMODE = 0b0;
  DacaRegs.DACCTL.bit.MODE = 0b1;
  DacaRegs.DACOUTEN.bit.DACOUTEN = 0b1;
  DacaRegs.DACVALS.all = 0b0;
  EDIS;
}
```

15.2.1 Initialization Sequence

1. Enable the buffered DAC clock.
2. Set DACREF with DACREFSEL.
3. Power up the buffered DAC with DACOUTEN.
4. Wait for the power-up time to elapse before outputting a voltage. To determine the power-up time of the buffered DAC, see the device-specific data manual.
5. For predictable behavior of the buffered DAC, consecutive writes to DACVALS should be spaced apart according to the settling time of the buffered DAC. To determine the settling time of the buffered DAC, see the device-specific data manual.

15.2.2 DAC Offset Adjustment

Zero offset error is defined as the difference between the voltage at midcode (2048) and 1.25v (for 2.5v reference voltage). DAC offset error is calibrated at 2.5v reference voltage and loaded into the DAC offset trim register as part of the Device_cal() function. If the DAC is used at any reference voltage other than 2.5v, the offset trim must be adjusted to ensure the offset error performance stays within the device-specific data manual limits. The DAC offset register is a 16-bit register that contains the 8-bit signed offset trim in the lower half of the register. Use the function call DAC_tuneOffsetTrim() found in C2000Ware to adjust the offset.

Table 15-1. DAC Supported Gain Mode Combinations

DACREFSEL	ANAREFxSEL	ANAREFx2P5	Reference Source	Reference Voltage (V)	Mode	Maximum DAC Output (V)	Support Status
0	X	X	External	VDAC	0	2.5	Supported
0	X	X	External	VDAC	1	2.5	Not Supported
1	0	0	Internal	1.65	0	1.65	Not Supported
1	0	0	Internal	1.65	1	3.3	Supported
1	0	1	Internal	2.5	0	2.5	Supported
1	0	1	Internal	2.5	1	3.3	Not Supported
1	1	X	External	VREFHI	0	2.5	Supported
1	1	X	External	VREFHI	1	2.5	Not Supported

Table 15-9. DACOUTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	DACOUTEN	R/W	0h	DAC output enable 0 DAC output is disabled 1 DAC output is enabled Reset type: SYSRSn

Table 15-8. DACVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DACVALS	R/W	0h	Shadow output code to be loaded into DACVALA Reset type: SYSRSn

Table 15-6. DACCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-4	SYNCSEL	R/W	0h	DAC EPWMSYNCPER select. Determines which EPWMSYNCPER signal will update the DACVALA register. Where n represents the maximum number of EPWMSYNCPER signals available on the device: 0 EPWM1SYNCPER 1 EPWM2SYNCPER 2 EPWM3SYNCPER ... n-1 EPWMnSYNCPER Reset type: SYSRSn
3	RESERVED	R	0h	Reserved
2	LOADMODE	R/W	0h	DACVALA load mode. Determines when the DACVALA register is updated with the value from DACVALS. 0 Load on next SYSCLK 1 Load on next EPWMSYNCPER specified by SYNCSEL Reset type: SYSRSn
1	MODE	R/W	0h	DAC gain mode select. Selects the gain mode for the buffered output. The MODE value is only used when DACREFSEL=1 and internal ADC reference mode is selected. 0 Gain is 1 1 Gain is 2 Reset type: SYSRSn
0	DACREFSEL	R/W	0h	DAC reference select. Selects which voltage references are used by the DAC. 0 VDAC/VSSA are the reference voltages 1 ADC VREFHI/VSSA are the reference voltages Reset type: SYSRSn