

# EE 458/533 – Power Electronics Controls, Winter 2022

## Homework 1

**Due Date:** Thursday January 20 2022

**Instructions.** You must scan your completed homework assignment into a pdf file, and upload your file to the Canvas Assignment page before 4:30 pm on the due date. All pages must be gathered into a single file of moderate size, with the pages in the correct order. Use basic black and white scanning. Please note that the grader will not be obligated to grade your assignment if the file is unreadable or very large.

**Description** In Problems 1–2 on the last page, the input voltage is  $v_g(t)$ , and output voltage is  $v(t)$ . Configuration ① has a duty ratio of  $d(t)$ , and ② has a duty ratio of  $d'(t) = 1 - d(t)$ . Each MOSFET has an on-state resistance of  $R_{on}$  (all other elements are lossless). In both circuits, the states are the capacitor voltage  $v(t)$ , and current  $i(t)$  through the inductor (or magnetizing inductance). In other words, the notation is consistent for both circuits. For each problem, do the following:

- (a) Express the averaged dynamics in the form

$$\dot{x}(t) = f(x(t), u(t)),$$

where

$$x(t) = \begin{bmatrix} \langle i(t) \rangle \\ \langle v(t) \rangle \end{bmatrix},$$

$$u(t) = \begin{bmatrix} d(t) \\ \langle v_g(t) \rangle \end{bmatrix},$$

$$f(x(t), u(t)) = \begin{bmatrix} f_1(x(t), u(t)) \\ f_2(x(t), u(t)) \end{bmatrix}.$$

- (b) Derive the steady-state averaged values of the state variables ( $I$  and  $V$ ) in each circuit given a set of corresponding steady-state inputs ( $D$  and  $V_g$ ).
- (c) Derive a linearized model of the form

$$\dot{x}(t) \approx A(x(t) - X) + B(u(t) - U),$$

where  $A, B \in \mathbb{R}^{2 \times 2}$  are real-valued square  $2 \times 2$  matrices, and

$$X = \begin{bmatrix} I \\ V \end{bmatrix},$$

$$U = \begin{bmatrix} D \\ V_g \end{bmatrix}.$$

(d) Using PLECS, create three simulations where:

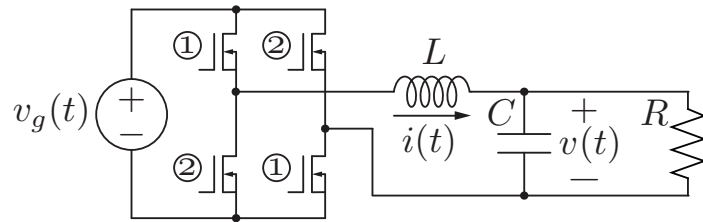
- “simulation #1” is a switched model of the converter
- “simulation #2” is the averaged model from part (a)
- “simulation #3” is the linearized model from part (d)

In all models, initialize the states at  $t = 0$  according to the steady-state equations in part (c) (i.e.,  $x(0) = X$ ) and given the numerical values for  $u(0)$  implied below. Write a script that executes models #1, #2, and #3 sequentially, and records the state variables (load voltage, and inductor/magnetizing current) in each model. Plot the same corresponding state from each simulation overlaid on the same plot for comparison (so we can compare the switched, averaged, and linearized). Make one plot for each state and use different colors, line thicknesses, and a legend to distinguish between all three models. Your plot must be clearly labeled. Each simulation should finish when  $t = t_{\text{stop}} = 60 \text{ ms}$ . Use the parameters below:

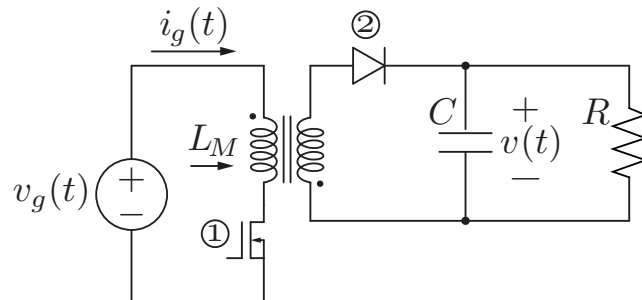
- $f_s = T_s^{-1} = 25 \text{ kHz}$
- A  $1 : n$  primary-to-secondary turns ratio is used in Problem 2 where  $n = 2$
- $L = L_M = 300 \mu\text{H}$ ,  $C = 10 \mu\text{F}$ ,  $R = 10 \Omega$ ,  $R_{on} = 15 \text{ m}\Omega$

and the following time-domain inputs:

- $v_g(t) = \begin{cases} 100 \text{ V}, & \text{for } 0 \leq t < 20 \text{ ms} \\ 75 \text{ V}, & \text{for } 20 \text{ ms} \leq t \leq t_{\text{stop}}. \end{cases}$  ————— For Both Problems
- $d(t) = \begin{cases} \frac{1}{2}(1 + 0.7 \sin(2\pi 50t)), & \text{for } 0 \leq t < 40 \text{ ms} \\ \frac{1}{2}(1 + 0.9 \sin(2\pi 50t)), & \text{for } 40 \text{ ms} \leq t \leq t_{\text{stop}}. \end{cases}$  ——— For Problem #1
- $d(t) = \begin{cases} 0.5, & \text{for } 0 \leq t < 40 \text{ ms} \\ 0.75, & \text{for } 40 \text{ ms} \leq t \leq t_{\text{stop}}. \end{cases}$  ————— For Problem #2

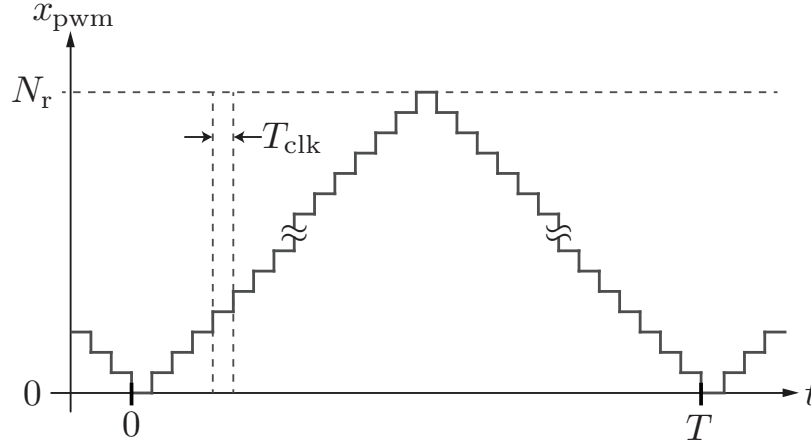


Circuit for Problem 1: The single-phase voltage source inverter.



Circuit for Problem 2: The flyback converter.

**Problem 3:** Consider the digital PWM waveform below. The clock frequency is  $f_{\text{clk}} = T_{\text{clk}}^{-1}$  and the switching frequency is  $f_{\text{sw}} = T^{-1}$ . The PWM up/down counter takes on  $N_r + 1$  discrete integer values to produce a symmetric triangular carrier.



Problem 3: Digital PWM waveform.

- If  $f_{\text{clk}} = 100 \text{ MHz}$ , what is the maximum feasible switching frequency if we need at least 2% of duty ratio resolution?
- Assuming your counter has 16 bits, what is the lowest feasible switching frequency.
- For your solution in part (b), what is the duty ratio resolution?
- If this same PWM scheme of (a) is applied to the flyback converter shown in Problem 2, what would be the output voltage resolution?