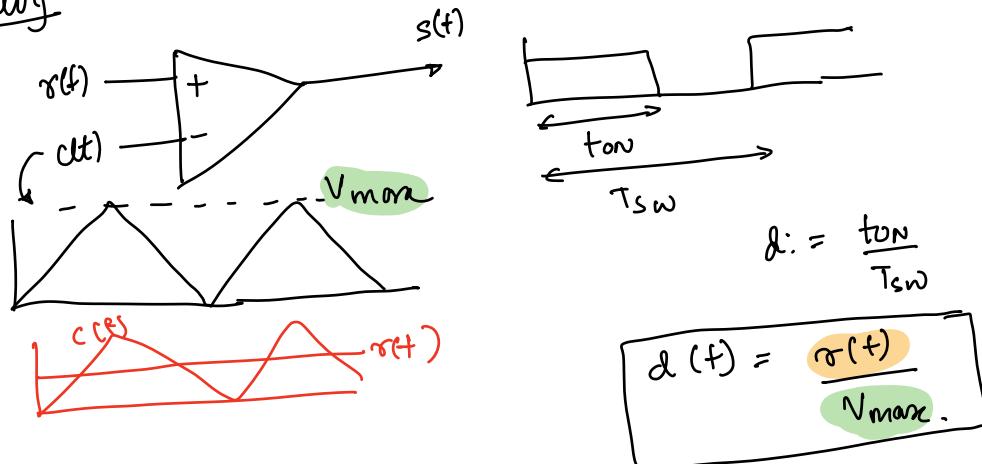


Lecture 2

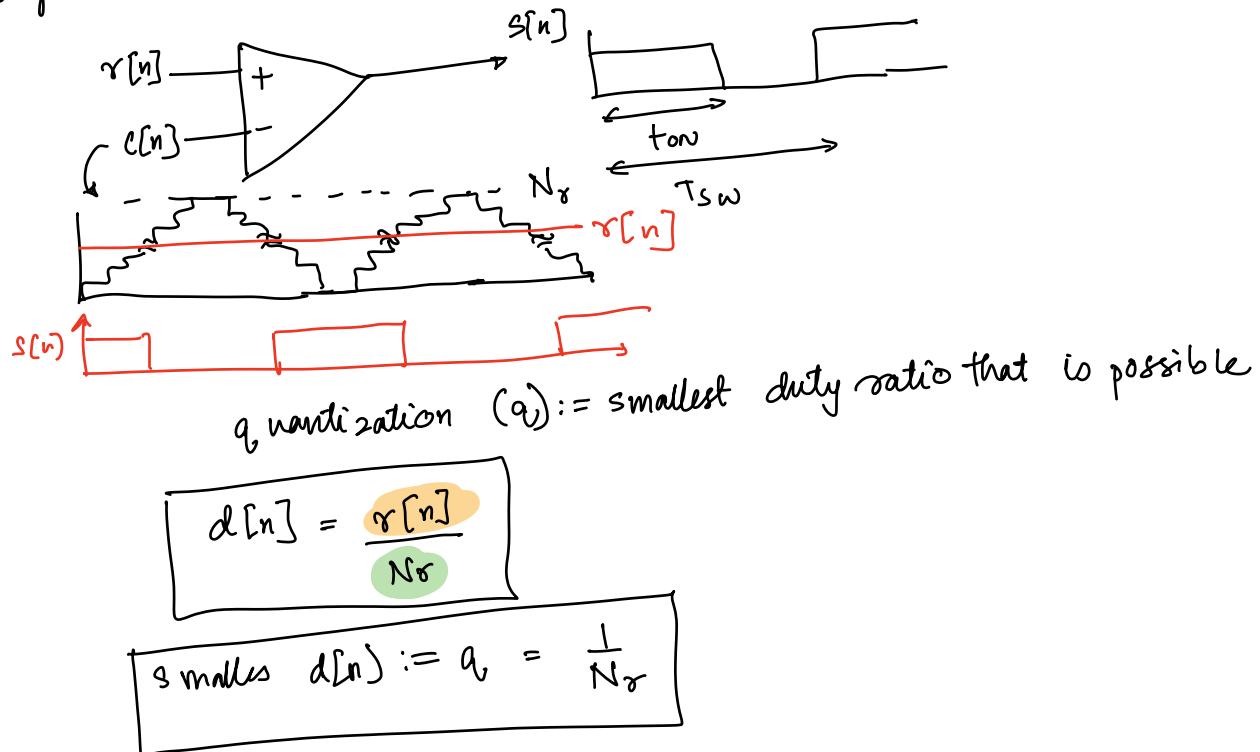
6th Jan 2022

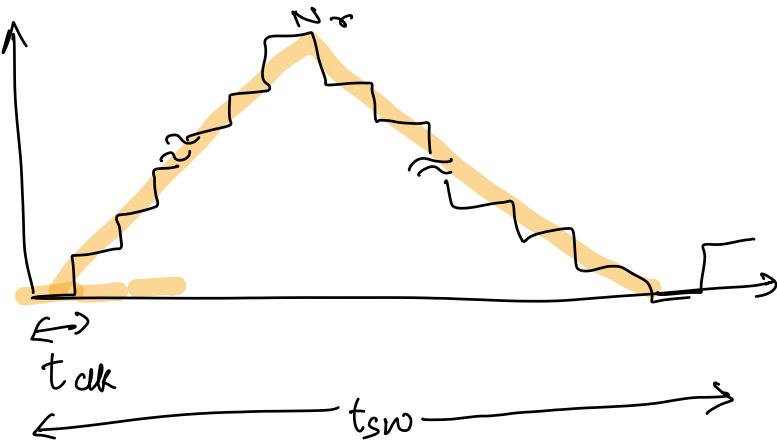
- o Revise PWM
- o Start ADC.

analog



digital





$$t_{\text{clk}} \times 2N_r = T_{\text{sw}}$$

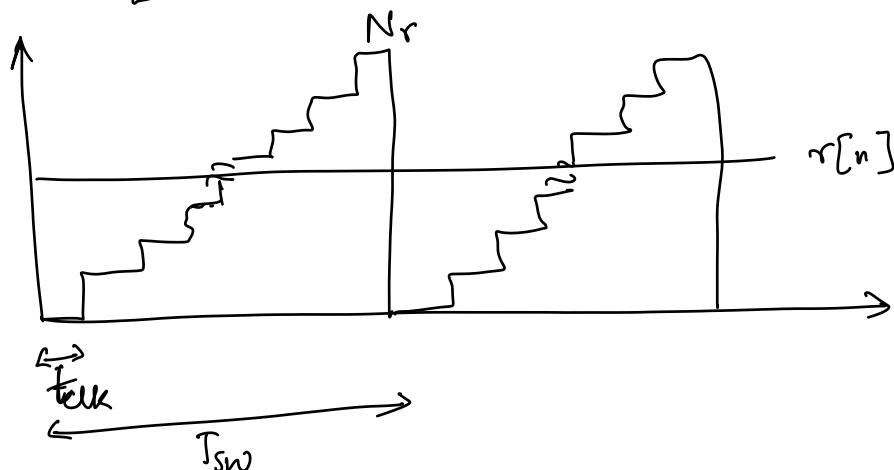
$$\therefore N_r = \frac{T_{\text{sw}}}{2t_{\text{clk}}} = \frac{f_{\text{clk}}}{2f_{\text{sw}}} \quad (2)$$

$$q_r = \frac{1}{N_r} \quad (1)$$

Combining ① & ②

$$q_r = \frac{1}{N_r} = \frac{2f_{\text{sw}}}{f_{\text{clk}}}$$

Symmetric carrier.



$$\alpha = \frac{r[n]}{N_r}$$

$$q_r = \frac{1}{N_r} \quad (1)$$

$$t_{\text{clk}} \cdot N_r = T_{\text{sw}}$$

$$\therefore \frac{1}{N_r} = \frac{t_{\text{clk}}}{T_{\text{sw}}} \quad (2)$$

Combining ① & ②

$$q_r = \frac{1}{N_r} = \frac{t_{alk}}{T_{SW}} = \frac{f_{SW}}{f_{alk}}$$

Asymmetric carrier

* How is no of PWR bits related to N_r?

$$N_r \leq 2^{N_{PWR}} - 1$$

- Q A buck converter is operated with a digital controller, $f_{clk} = 1 \text{ MHz}$. If you want a resolution of 1% in duty ratio [$q = 1\% = \frac{1}{100} = 0.01$]
- ✓ (i) Find what is the no of bits you need (for asymmetric PWM)
 - ✓ (ii) Max / Min fsw of buck converter.
 - (iii) If $V_{in} = 24 \text{ V}$, what is output voltage resolution?

$$q = \frac{1}{N_r} \quad \text{(1)}$$

$$t_{clk} \cdot N_r = T_{sw} \quad \text{Nr}$$

$$\therefore \frac{1}{N_r} = \frac{t_{clk}}{T_{sw}} \quad \text{(2)}$$

Combining (1) & (2)

$$q_r = \frac{1}{N_r} = \frac{t_{clk}}{T_{sw}} = \frac{f_{sw}}{f_{clk}}$$

Asymmetric carrier

* How is no of PWM bits related to N_r ?

$$N_r \leq 2^{N_{pwm}} - 1 \quad \text{(3)}$$

$$\frac{1}{N_r} = \frac{t_{clk}}{T_{sw}} = \frac{f_{sw}}{f_{clk}}$$

$$f_{sw} = \frac{f_{clk}}{N_r} > \frac{1 \text{ MHz}}{100} = \frac{10^6}{10^2} = 10^4 = 10 \text{ kHz}$$

$$\text{Max } f_{sw} = \underline{\underline{10 \text{ kHz}}}$$

Answer \rightarrow Q1, Q3

$$f_{clk} = 1 \text{ MHz}$$

$$q_r = 0.01$$

$$0.01 = \frac{1}{N_r}$$

$$\therefore N_r = 100$$

$$100 \leq 2^{N_{pwm}} - 1$$

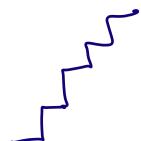
$$101 \leq 2^{N_{pwm}}$$

$$\log_2 101 \leq \log_2 2^{N_{pwm}}$$

$$\log_2 101 \leq N_{pwm}$$

$$6.67$$

$$N_{pwm} = 7$$



$$0 \text{ to } 2^7$$

Max sw freq: $f_{sw} = \frac{f_{clk}}{2^{N_{prm}}} = \frac{1\text{MHz}}{2^7} = \underline{\underline{\underline{125\text{kHz}}}}$

(ii)

Buck

$$V_o = D V_{in}$$

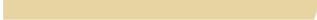
$$\text{min poss } V_o = \text{min poss } D \cdot V_{in}$$

$$\Delta V_o = \Delta D \cdot V_{in}$$

$$\begin{aligned}\Delta V_o &= q_v \cdot V_{in} \\ &= (0.01)(24) \\ &= \underline{\underline{0.24V}}\end{aligned}$$

ADC tutorial for EE-458/533 (2022)

F28069M MCU



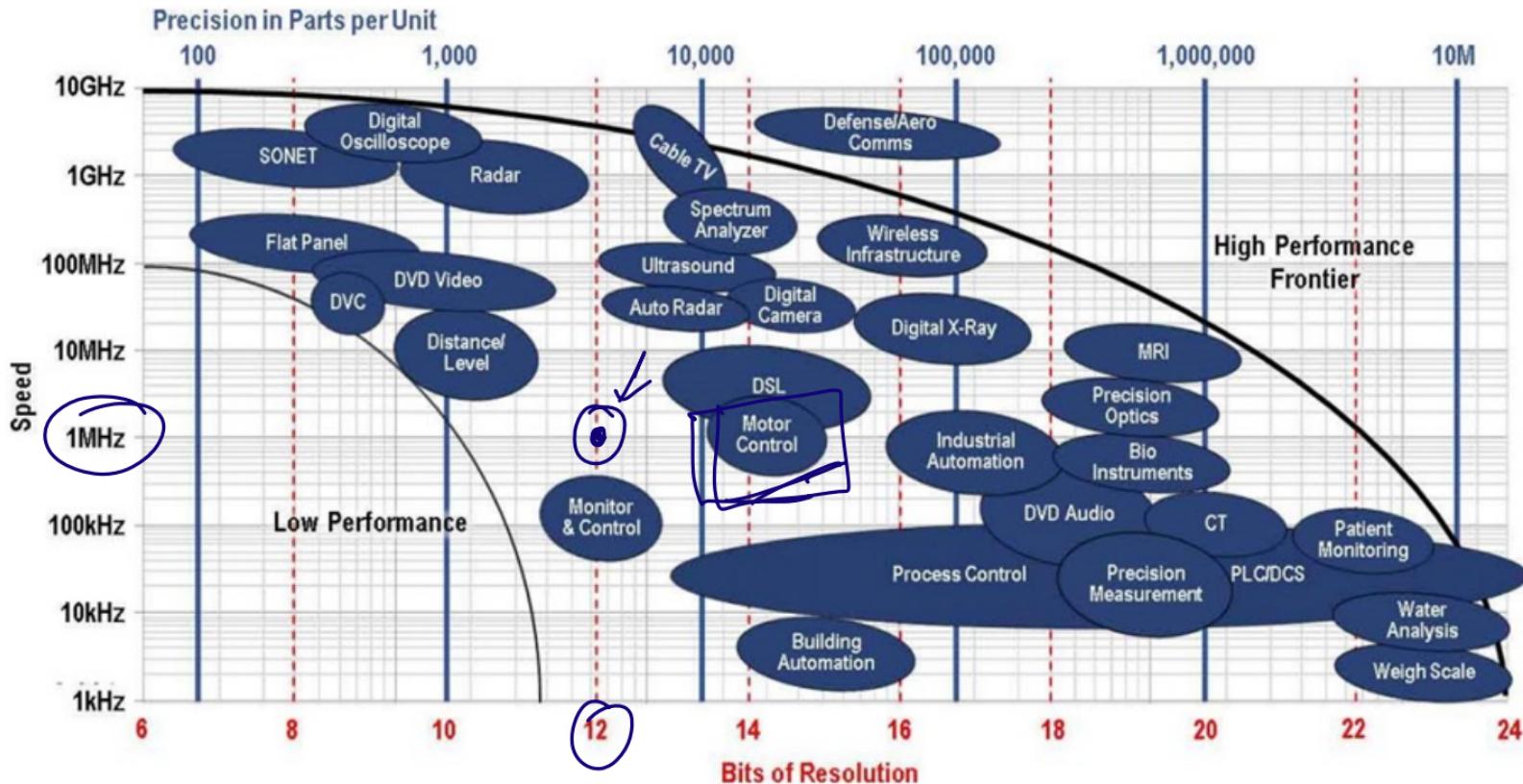
Rahul Mallik, UW ECE

Sources :

DCA LECTURE FALL08 (gatech.edu)

$\Delta\Sigma$ ADC High-Precision Data Converters by Arindam Mandal, UW ECE

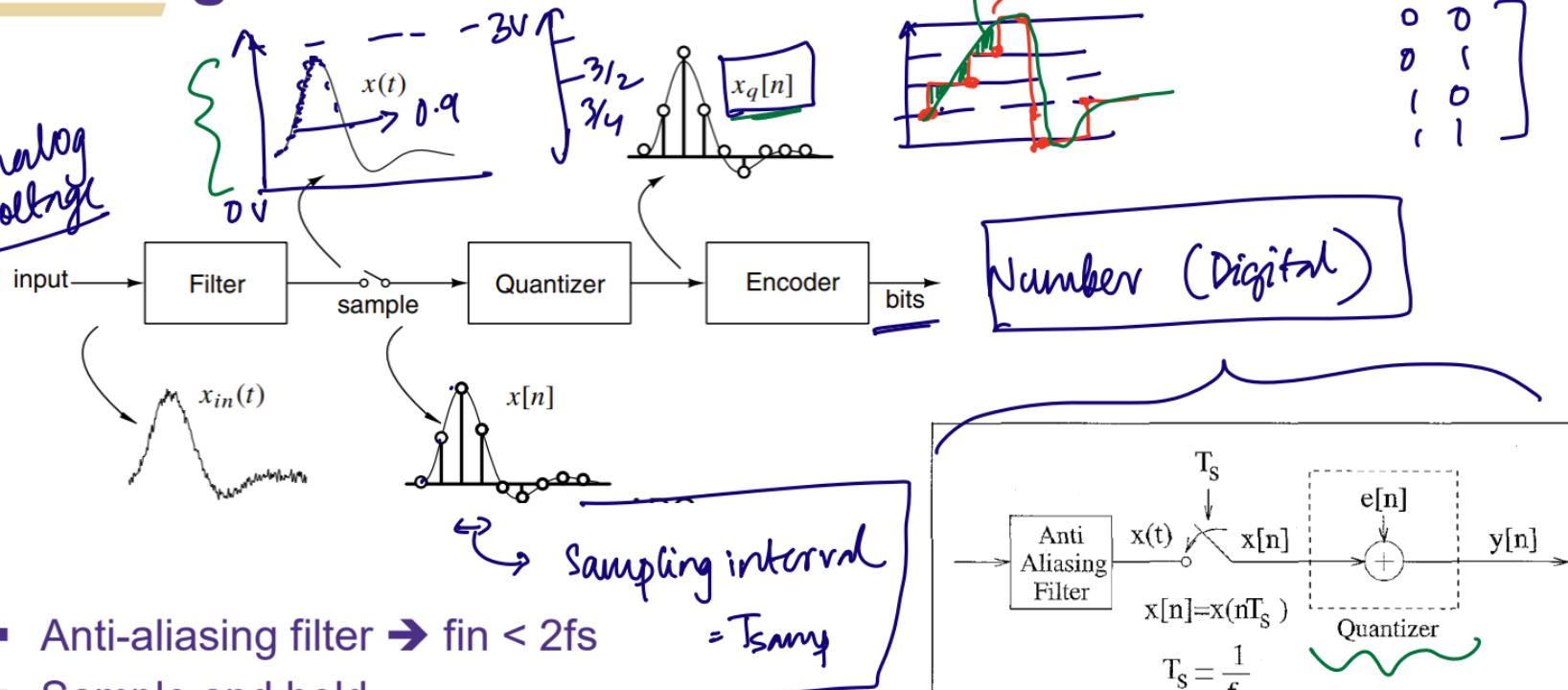
ADC Applications



Source: ADI

ADC Signal Chain

analog voltage



- Anti-aliasing filter $\rightarrow f_{in} < 2f_s$
- Sample and hold
- Quantizer

Source: [1]

Sample and hold

Resolution:

The smallest change in analog signal that will result in a change in the digital output.

$$\Delta V = \frac{V_r}{2^N} = \text{analogous to } q \text{ in PWN}$$

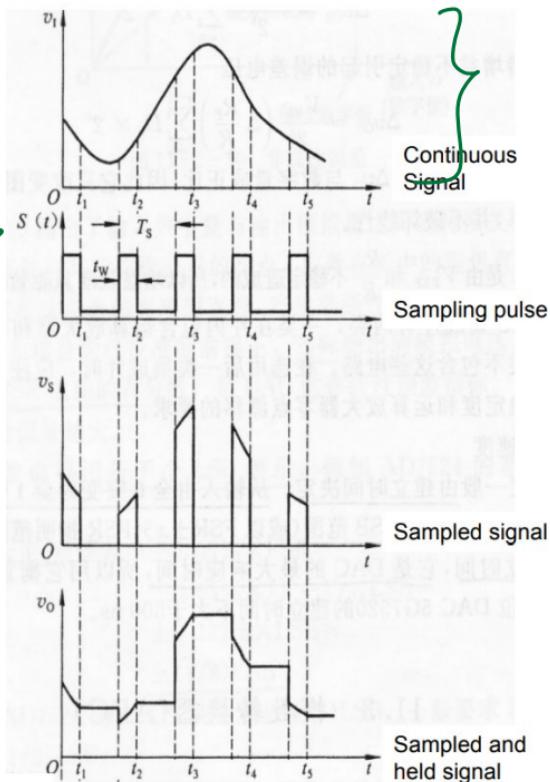
V = Reference voltage range

N = Number of bits in digital output.

2^N = Number of states.

ΔV = Resolution

The resolution represents the quantization error inherent in the conversion of the signal to digital form

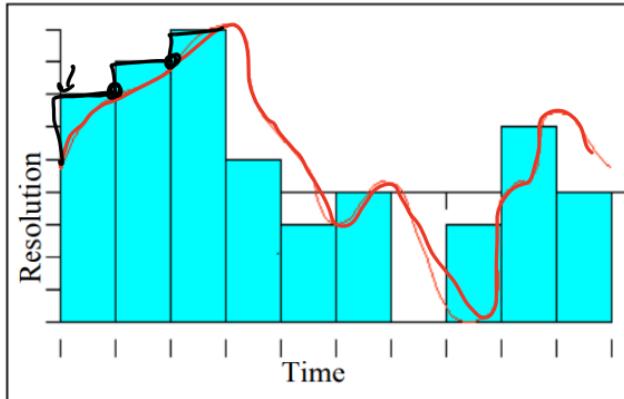


Accuracy improvement

Increase accuracy by

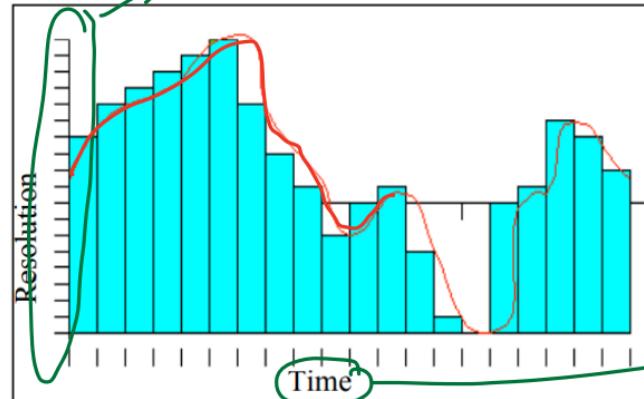
- increasing sampling frequency
- Increasing resolution

■ Low Accuracy

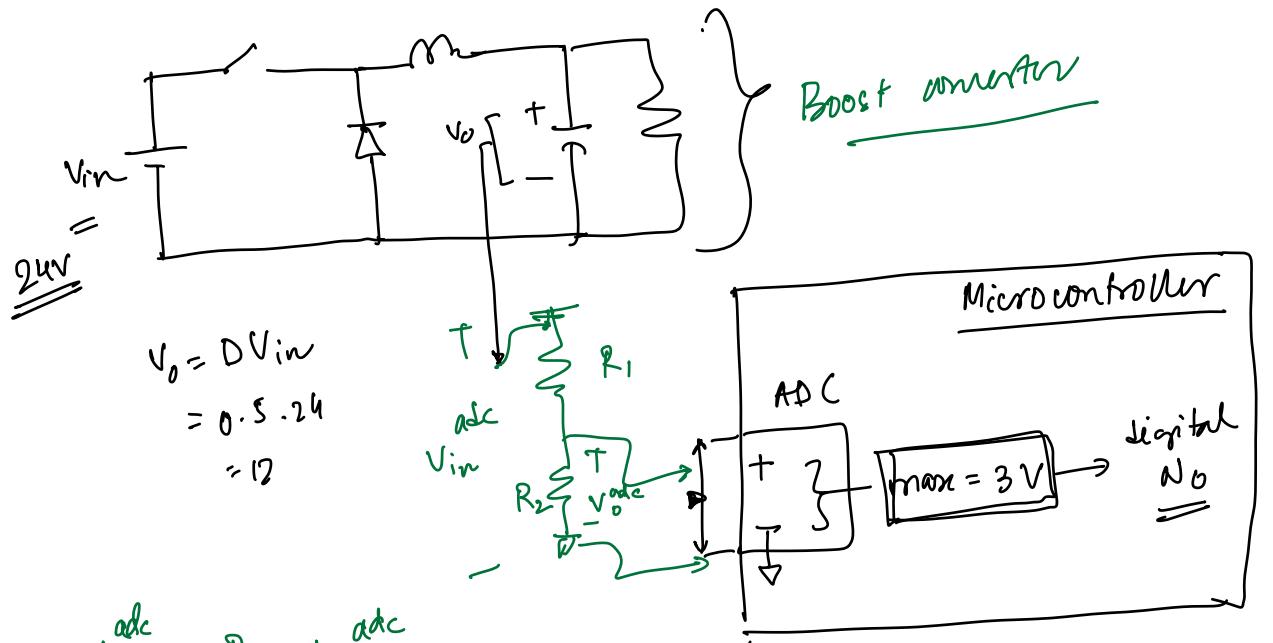


■ Improved

increase no of bits



ADC operation for buck converter.



$$\begin{aligned} V_o &= D V_{in} \\ &= 0.5 \cdot 24 \\ &\approx 12 \end{aligned}$$

$$V_o^{adc} = \frac{R_2}{R_1 + R_2} \cdot V_{in}^{adc}$$

constraint ① for highest V_{in}^{adc} , you want $V_o^{adc} < 3V$.

$$(3 - \Delta) = \frac{R_2}{R_1 + R_2} \cdot 24$$

Δ = safety limit

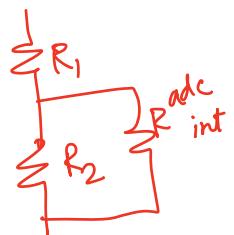
$R_1 = 1\text{ohm} \rightarrow$ bad design choice

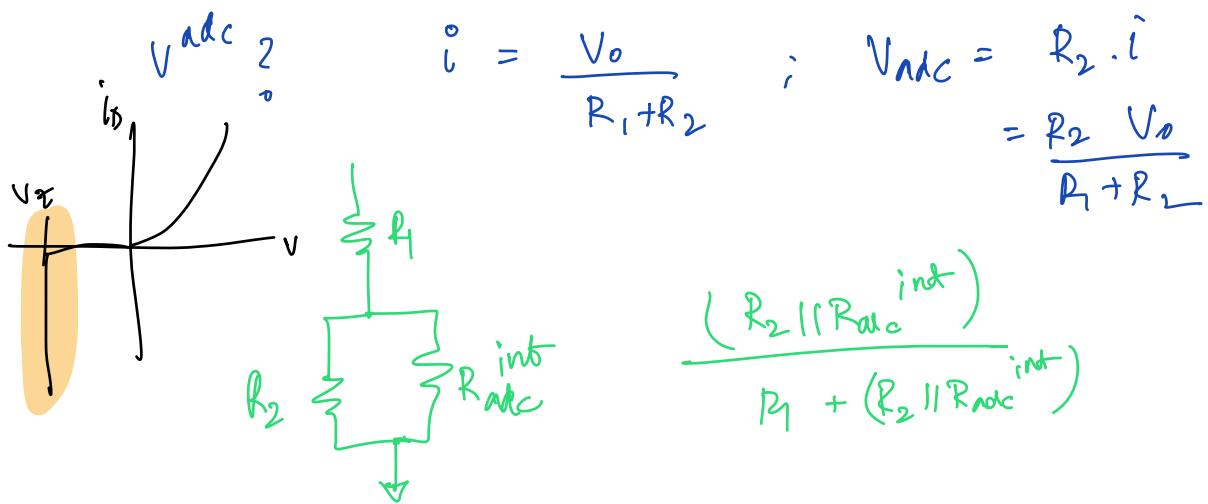
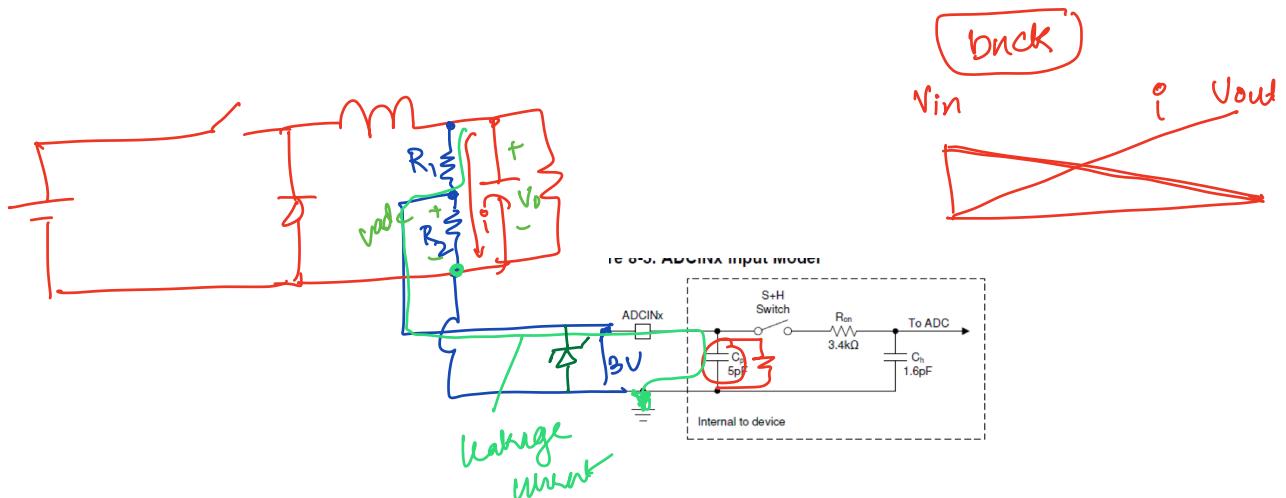
$$\frac{V^2}{I}$$

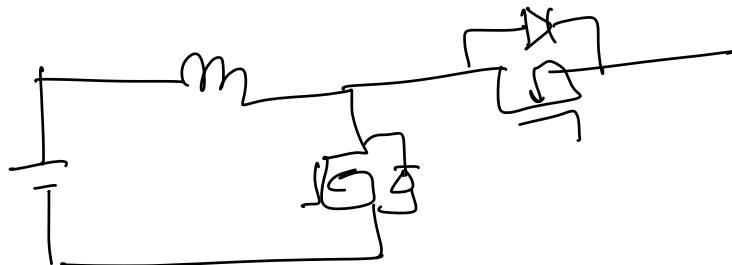
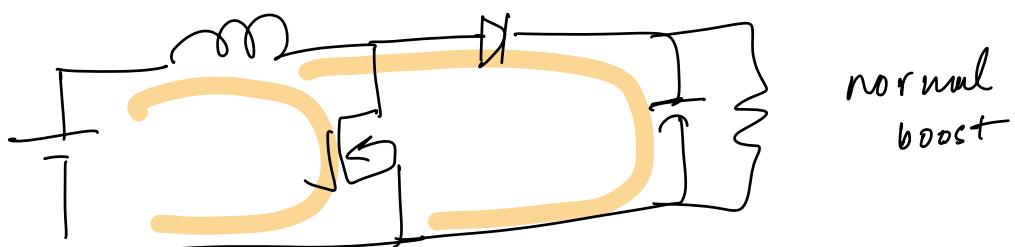
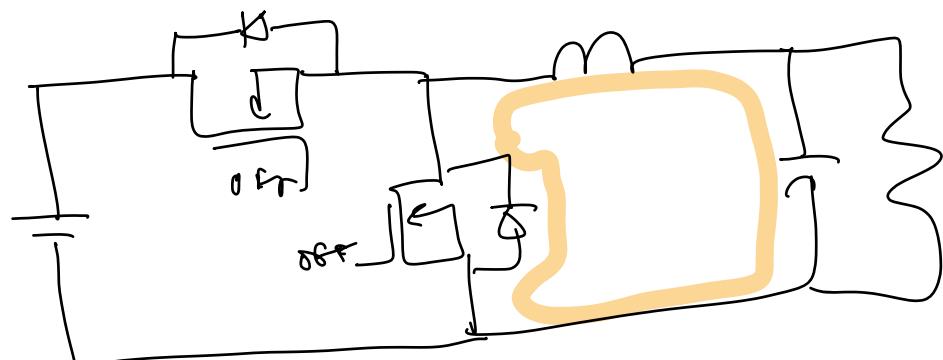
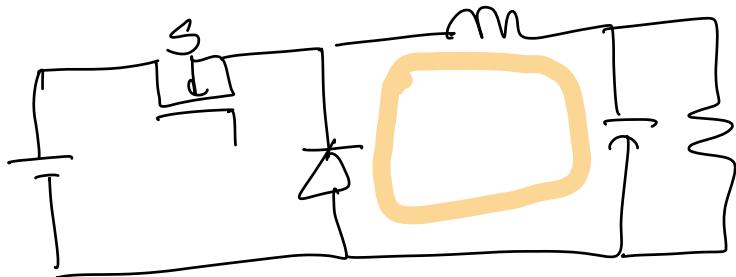
why: it draws huge power

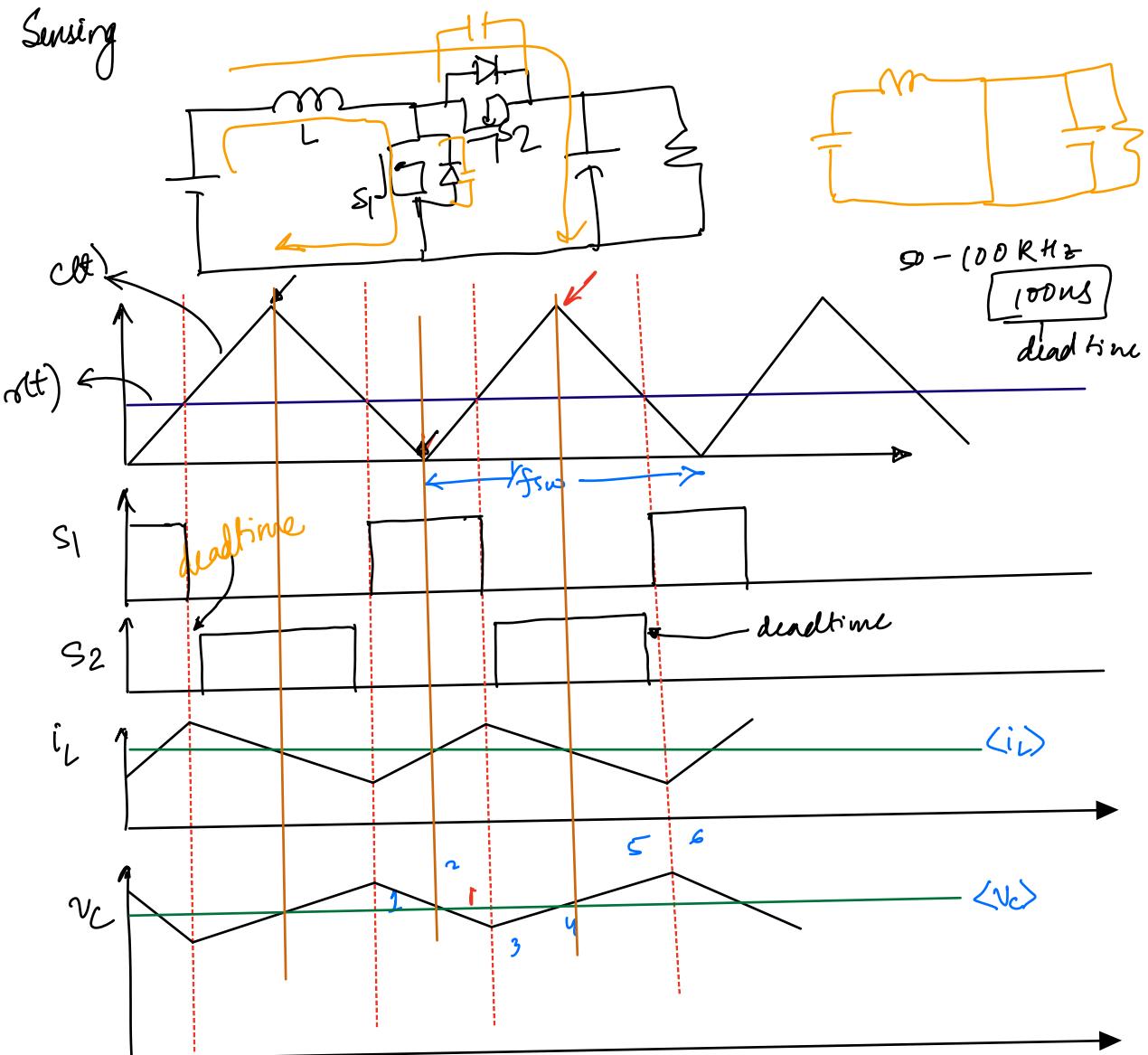
$R_1 = 10\text{mohm} \rightarrow$ bad design choice

why: it becomes comparable with ADC internal resistance









→ ② & ⑦ gives you the correct average for both inductor current & capacitor voltage

→ these are the quietest points

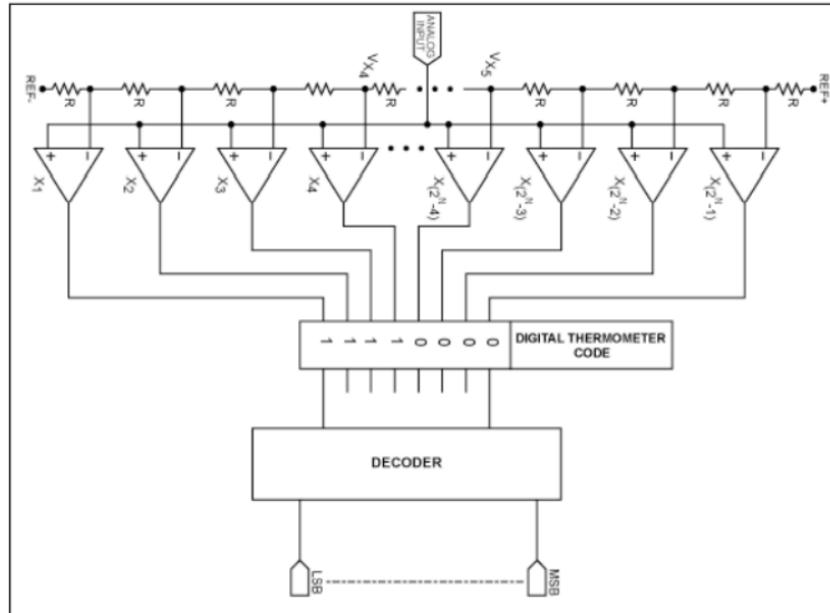
peak-valley sampling.

Flash A/D converter

(good to know,
will not be in exams)

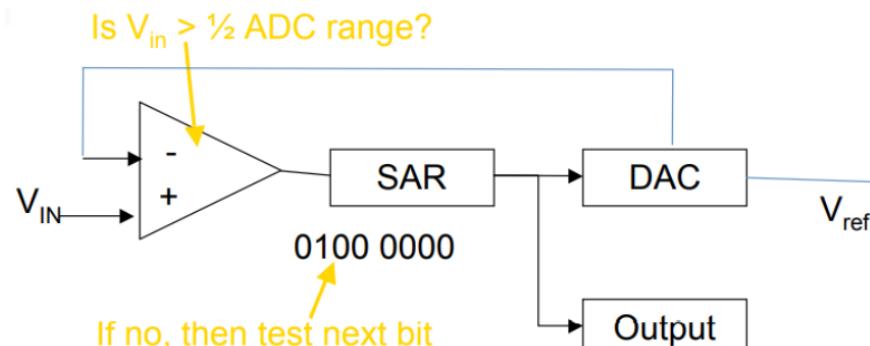
- Fundamental Components (For N bit Flash A/D)

- 2^{N-1} Comparators
- 2^N Resistors
- Control Logic



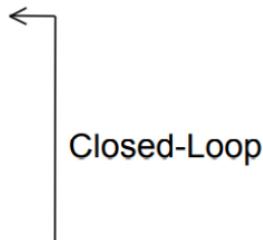
Successive Approximation ADC

(good to know,
will not be in exams)



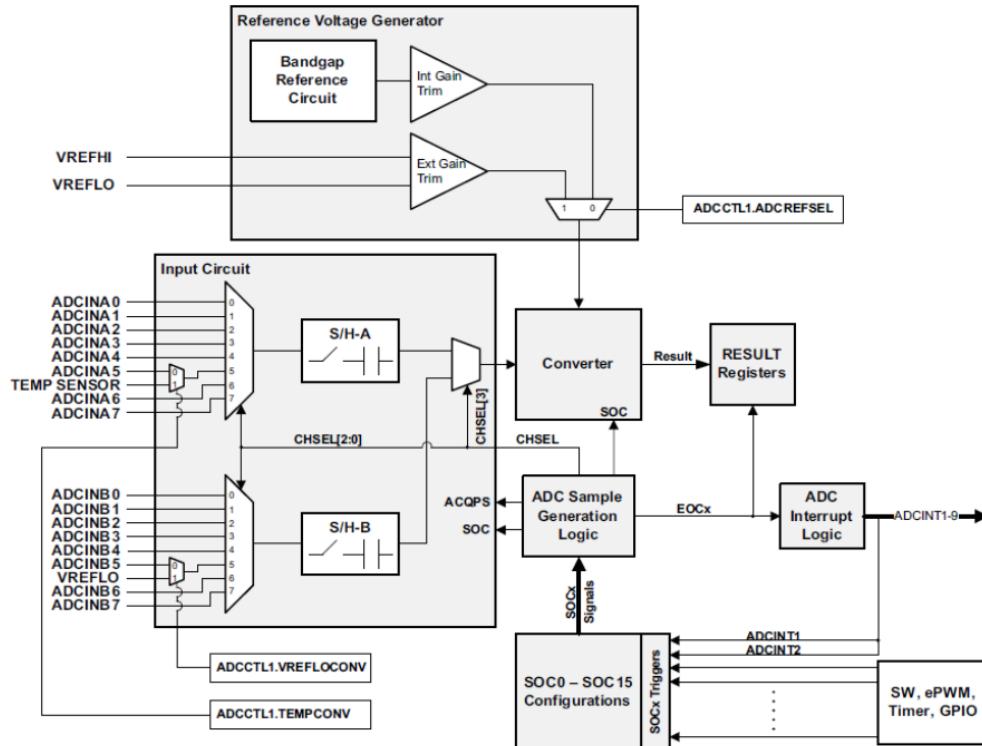
Process

1. MSB initialized as 1
2. Convert digital value to analog using DAC
3. Compares guess to analog input
4. Is $V_{in} > V_{DAC}$
 - Set bit 1
 - If no, bit is 0 and test next bit



F28069M ADC : 16 channels in two groups

Figure 8-1. ADC Block Diagram



Sampling and holding - capacitors

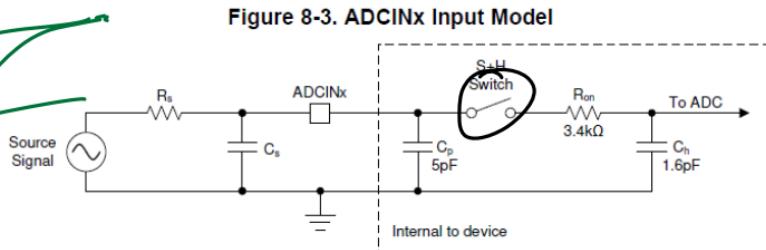
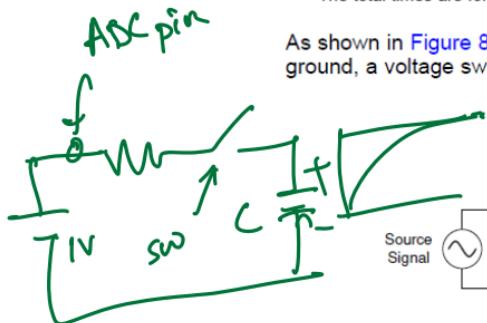
- Ensure enough ACQPS : acquisition window to have stable digital values

Table 8-1. Sample Timings with Different Values of ACQPS

SYSCLKOUT	ADC Clock	ACQPS	Sample Window	Conversion Time (13 cycles)	Total Time to Process Analog Voltage ⁽¹⁾
90Mhz	45MHz	6	155.56ns	288.89ns	444.44ns
90Mhz	45MHz	25	577.78ns	288.89ns	866.67ns

⁽¹⁾ The total times are for a single conversion and do not include pipelining effects that increase the average speed over time.

As shown in Figure 8-3 , the ADCIN pins can be modeled as an RC circuit. With VREFLO connected to ground, a voltage swing from 0 to 3.3v on ADCIN yields a typical RC time constant of 2ns.



Microcontroller

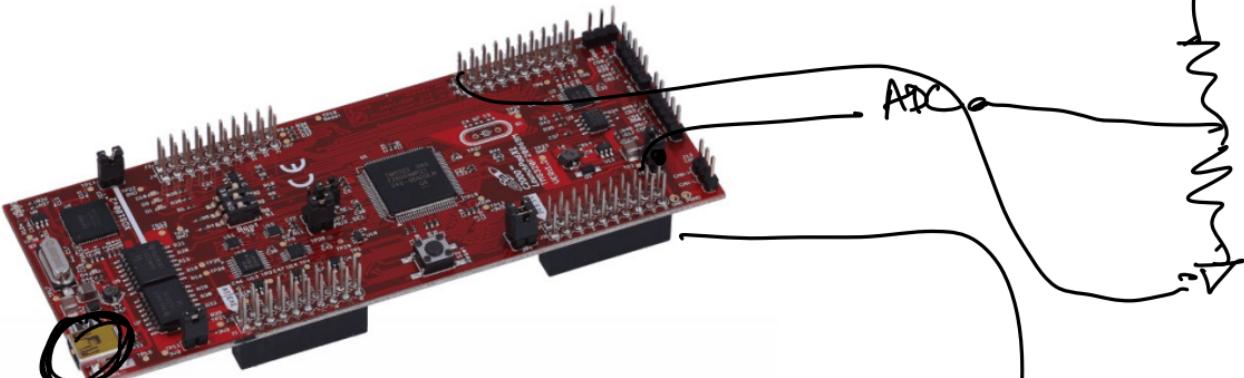
samples by the
switch & holds
the voltage by
the capacitor

Registers

Three registers that you need to set:

- ACQPS: influences how long it takes to “sample and hold”
- CHSEL : which channel are you converting from
- SOC Who initiates the ADC conversion process

MCU



Resources
ti.com/launchpad

{
Code examples
Open Source Design Files
Documentation
Example projects
Videos
Tutorials
Other TI products
}

Below are the pins exposed @ the BoosterPack connector.

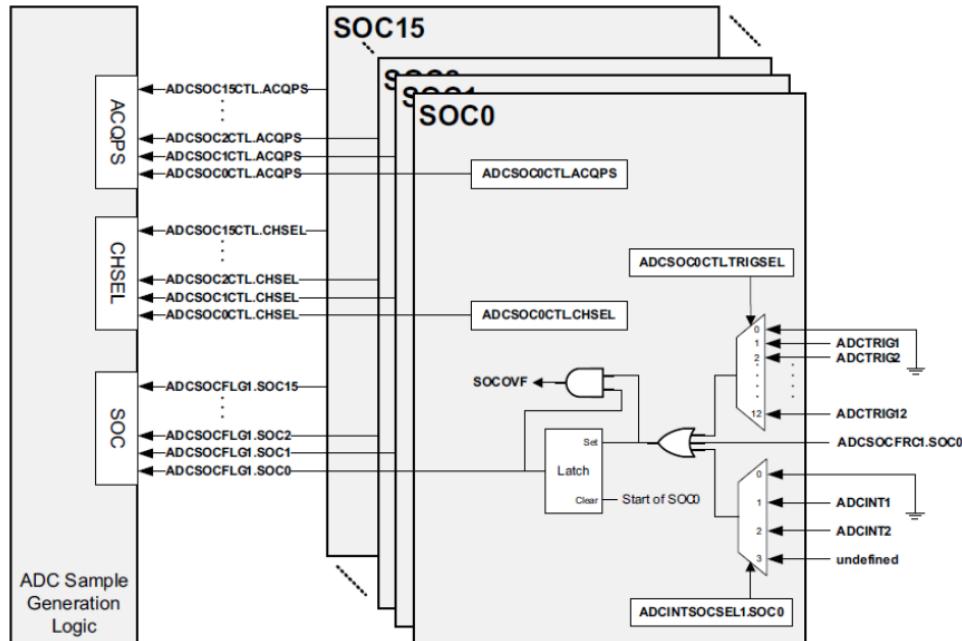
Also shown are functions that map with the BoosterPack standard.

- Note that to comply with the I2C channels of the BoosterPack standard, a software-emulated I2C must be used.
- Some LaunchPads do not 100% comply with the standard, please check your LaunchPad to ensure compliance.
- Denotes I/O pins that are interrupt-capable.

LAUNCHXL-F28069M Pin map		BoosterPack standard		LAUNCHXL-F28069M Pin map		BoosterPack standard		LAUNCHXL-F28069M Pin map		BoosterPack standard		LAUNCHXL-F28069M Pin map		BoosterPack standard	
+3.3V	+3.3V	+5V	+5V	SCIA RXD	(P28)	Analog In	GND	SCIA TXD	(P29)	UART RX (→MCU)	Analog In	ADCIN46	ADCIN47	ADCIN48	ADCIN49
SCIA RXD	(P28)	Analog In	GND	SCIA TXD	(P29)	UART TX (←MCU)	Analog In	SCIA TXD	(P29)	UART TX (←MCU)	Analog In	ADCIN46	ADCIN47	ADCIN48	ADCIN49
(I) P12	GPIO	(I)	GPIO	(I) P12	GPIO	(I)	GPIO	(I) P12	GPIO	(I)	GPIO	ADCIN46	ADCIN47	ADCIN48	ADCIN49
SPIA CLK	(P18)	SPI CLK	Analog In	SPIA CLK	(P18)	SPI CLK	Analog In	SPIA CLK	(P18)	SPI CLK	Analog In	ADCIN46	ADCIN47	ADCIN48	ADCIN49
(I) P22	GPIO	(I)	GPIO	(I) P22	GPIO	(I)	GPIO	(I) P22	GPIO	(I)	GPIO	ADCIN46	ADCIN47	ADCIN48	ADCIN49
I2CA SCL	(P33)	I2C SCL	SDA	I2CA SCL	(P33)	I2C SCL	SDA	I2CA SCL	(P33)	I2C SCL	SDA	ADCIN46	ADCIN47	ADCIN48	ADCIN49
I2CA SDA	(P32)	Reserved	Reserved	I2CA SDA	(P32)	Reserved	Reserved	I2CA SDA	(P32)	Reserved	Reserved	ADCIN46	ADCIN47	ADCIN48	ADCIN49
+3.3V	+3.3V	+5V	+5V	SCIB RXD	(P15)	UART RX (→MCU)	Analog In	SCIB RXD	(P15)	UART RX (→MCU)	Analog In	ADCIN46	ADCIN47	ADCIN48	ADCIN49
SCIB RXD	(P15)	UART RX (→MCU)	Analog In	SCIB TXD	(P58)	UART TX (←MCU)	Analog In	SCIB TXD	(P58)	UART TX (←MCU)	Analog In	ADCIN46	ADCIN47	ADCIN48	ADCIN49
(I) P20	GPIO	(I)	GPIO	(I) P20	GPIO	(I)	GPIO	(I) P20	GPIO	(I)	GPIO	ADCIN46	ADCIN47	ADCIN48	ADCIN49
SPIB CLK	(P14)	SPI CLK	Analog In	SPIB CLK	(P14)	SPI CLK	Analog In	SPIB CLK	(P14)	SPI CLK	Analog In	ADCIN46	ADCIN47	ADCIN48	ADCIN49
(I) P21	GPIO	(I)	GPIO	(I) P21	GPIO	(I)	GPIO	(I) P21	GPIO	(I)	GPIO	ADCIN46	ADCIN47	ADCIN48	ADCIN49
I2C	(P54)	SCL	SDA	I2C	(P54)	SCL	SDA	I2C	(P54)	SCL	SDA	ADCIN46	ADCIN47	ADCIN48	ADCIN49
DAC1				DAC1				DAC1							
DAC2				DAC2				DAC2							
P6	(I)	EPWM4A	PWM	P6	(I)	EPWM4A	PWM	P6	(I)	EPWM4A	PWM	GND		GND	
P7	(I)	EPWM4B	PWM	P7	(I)	EPWM4B	PWM	P7	(I)	EPWM4B	PWM	GND		GND	
P8	(I)	EPWM5A	PWM	P8	(I)	EPWM5A	PWM	P8	(I)	EPWM5A	PWM	GND		GND	
P9	(I)	EPWM5B	PWM	P9	(I)	EPWM5B	PWM	P9	(I)	EPWM5B	PWM	GND		GND	
P10	(I)	EPWM6A	Timer	P10	(I)	EPWM6A	Timer	P10	(I)	EPWM6A	Timer	GND		GND	
P11	(I)	EPWM6B	Timer	P11	(I)	EPWM6B	Timer	P11	(I)	EPWM6B	Timer	GND		GND	
P12	(I)			P12	(I)			P12	(I)			RST		RST	
P13	(I)			P13	(I)			P13	(I)			GPIO		GPIO	
P14	(I)			P14	(I)			P14	(I)			GPIO		GPIO	
P15	(I)			P15	(I)			P15	(I)			GPIO		GPIO	
P16	(I)			P16	(I)			P16	(I)			GPIO		GPIO	
P17	(I)			P17	(I)			P17	(I)			GPIO		GPIO	
P18	(I)			P18	(I)			P18	(I)			GPIO		GPIO	
P19	(I)			P19	(I)			P19	(I)			ECAP1		ECAP1	
P20	(I)			P20	(I)			P20	(I)			P44		P44	
P21	(I)			P21	(I)			P21	(I)						
P22	(I)			P22	(I)			P22	(I)						
P23	(I)			P23	(I)			P23	(I)						
P24	(I)			P24	(I)			P24	(I)						
P25	(I)			P25	(I)			P25	(I)						
P26	(I)			P26	(I)			P26	(I)						
P27	(I)			P27	(I)			P27	(I)						
P28	(I)			P28	(I)			P28	(I)						
P29	(I)			P29	(I)			P29	(I)						
P30	(I)			P30	(I)			P30	(I)						
P31	(I)			P31	(I)			P31	(I)						
P32	(I)			P32	(I)			P32	(I)						
P33	(I)			P33	(I)			P33	(I)						
P34	(I)			P34	(I)			P34	(I)						
P35	(I)			P35	(I)			P35	(I)						
P36	(I)			P36	(I)			P36	(I)						
P37	(I)			P37	(I)			P37	(I)						
P38	(I)			P38	(I)			P38	(I)						
P39	(I)			P39	(I)			P39	(I)						
P40	(I)			P40	(I)			P40	(I)						
P41	(I)			P41	(I)			P41	(I)						
P42	(I)			P42	(I)			P42	(I)						
P43	(I)			P43	(I)			P43	(I)						
P44	(I)			P44	(I)			P44	(I)						
P45	(I)			P45	(I)			P45	(I)						
P46	(I)			P46	(I)			P46	(I)						
P47	(I)			P47	(I)			P47	(I)						
P48	(I)			P48	(I)			P48	(I)						
P49	(I)			P49	(I)			P49	(I)						
P50	(I)			P50	(I)			P50	(I)						
P51	(I)			P51	(I)			P51	(I)						
P52	(I)			P52	(I)			P52	(I)						
P53	(I)			P53	(I)			P53	(I)						
P54	(I)			P54	(I)			P54	(I)						

Block diagram of F28069M

Figure 8-2. SOC Block Diagram



- How to know what analog input voltage corresponds to what digital value inside the microcontroller ??

8.12.1 Internal Reference Voltage

The ADC can operate in two different reference modes, selected by the ADCCTL1.ADCREFSEL bit. By default the internal bandgap is chosen to generate the reference voltage for the ADC. This will convert the voltage presented according to a fixed scale 0 to 3.3v range. The equation governing conversions in this mode is:

$$\text{Digital Value} = 0$$

when Input $\leq 0v$

$$\text{Digital Value} = 4096 [(Input - VREFLO)/3.3v]$$

when $0v < Input < 3.3v$

$$\text{Digital Value} = 4095,$$

when Input $\geq 3.3v$

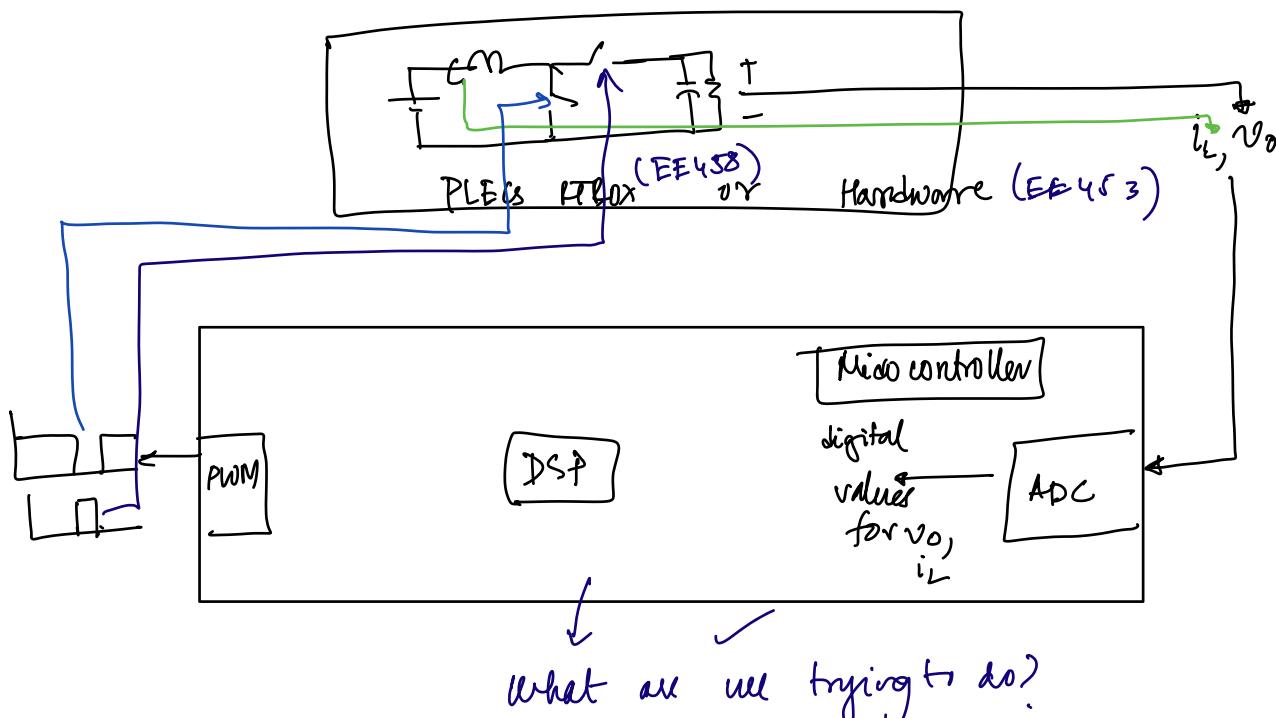
*All fractional values are truncated

**VREFLO must be tied to ground in this mode. This is done internally on some devices.

Further Reading

- Pavan, S., Schreier, R. and Temes, G.C., 2017. *Understanding delta-sigma data converters*. John Wiley & Sons
- Shanti Pavan video lectures: <https://nptel.ac.in/courses/117/106/117106034/>
- Delta Sigma Toolbox:
 - <https://www.mathworks.com/matlabcentral/fileexchange/19-delta-sigma-toolbox>
 - <http://www.python-deltasigma.io/>

Chapter 7 Erickson & Maksimovic-



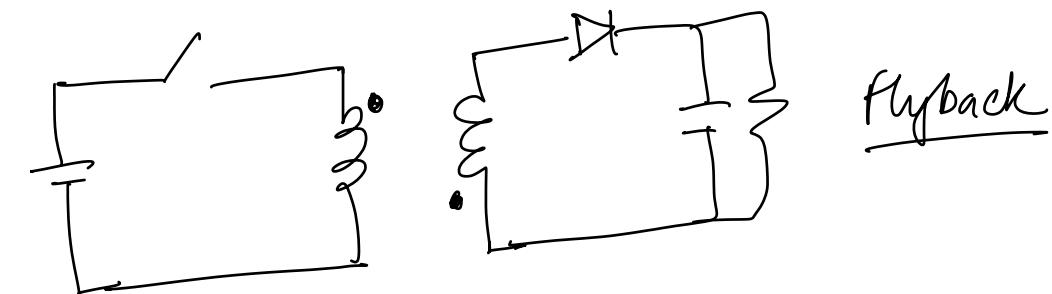
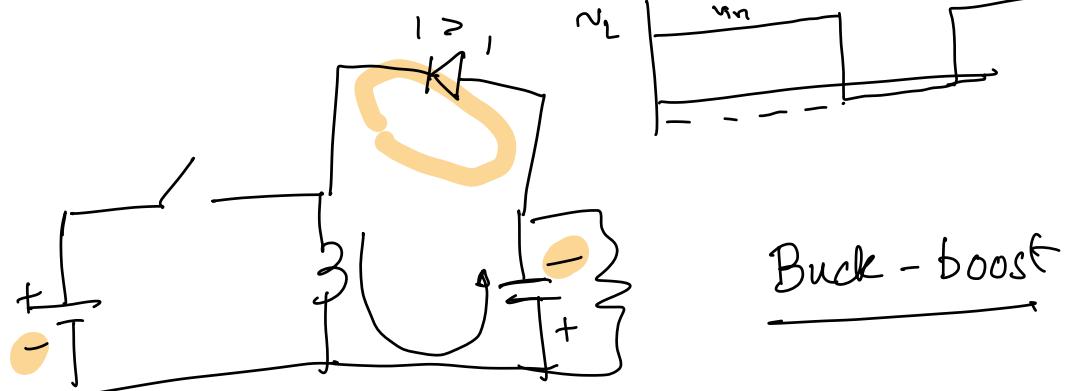
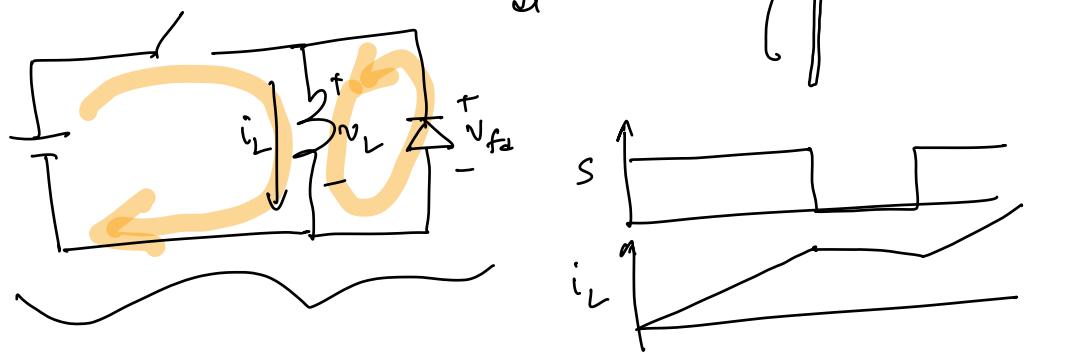
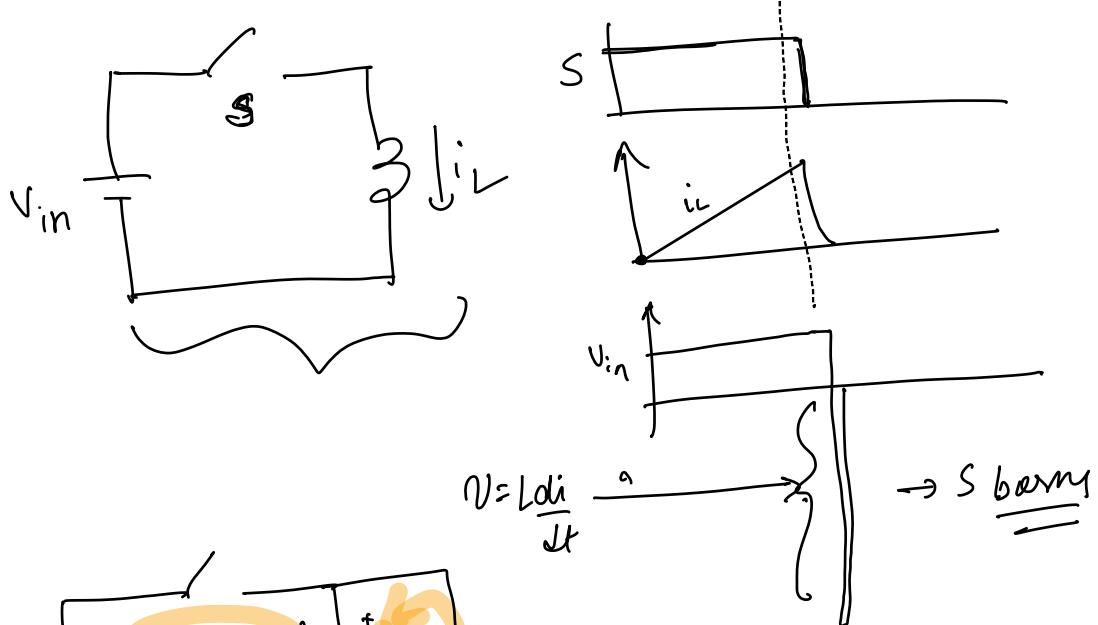
- trying to control inductor current
or
capacitor voltage
or
both -

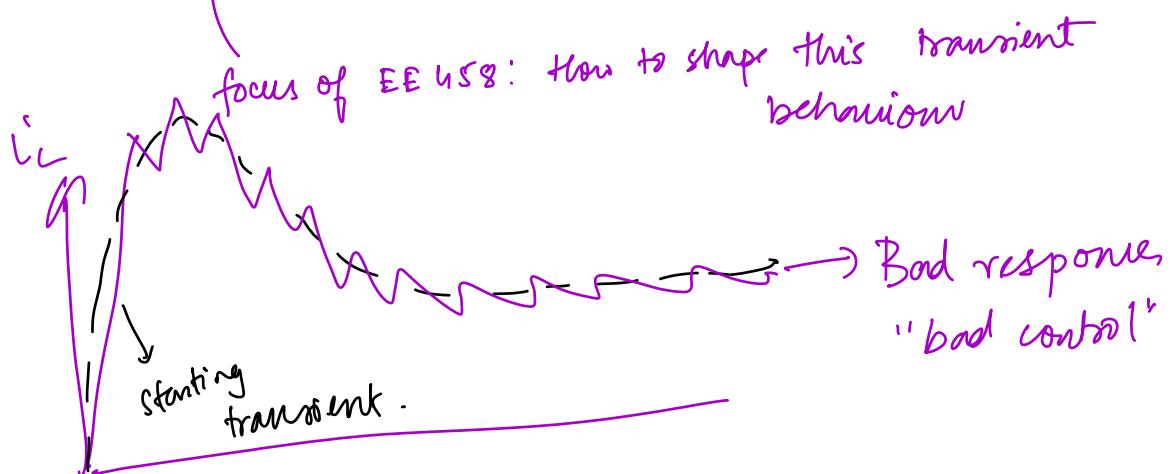
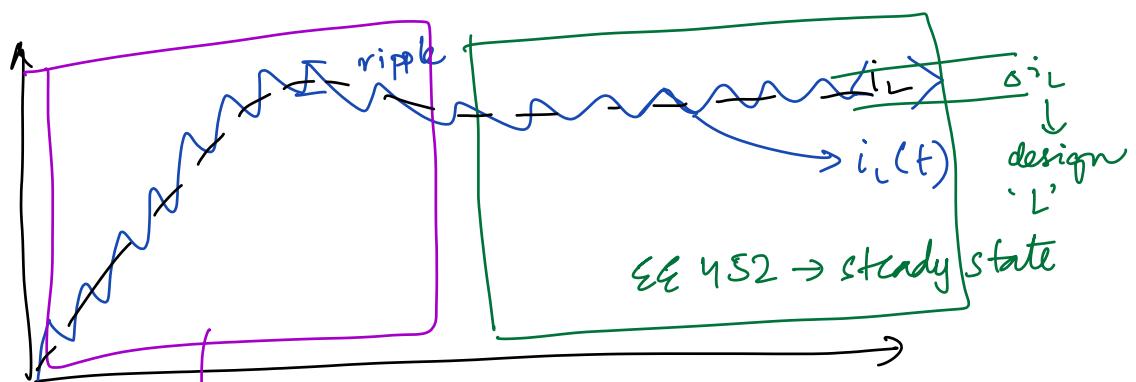
Ques is How?

Ans : By changing the duty ratio

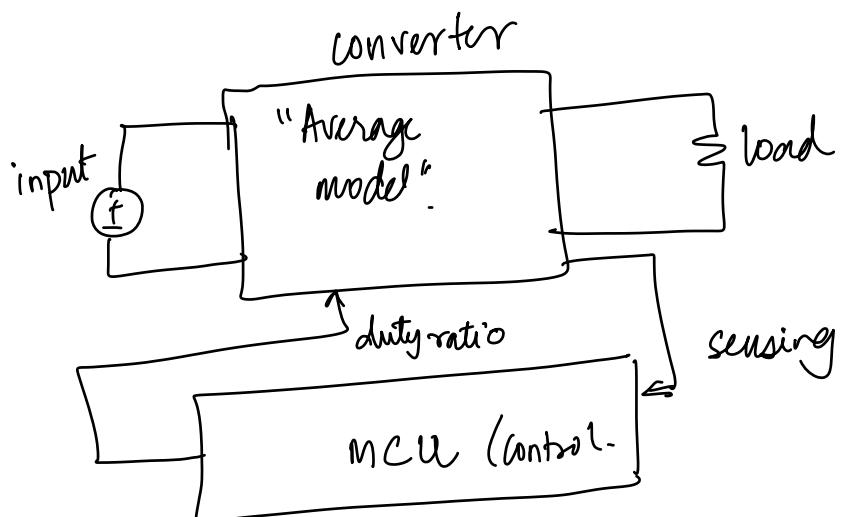
The next set of discussion is :-

how to use duty ratio to ensure I meet
the control requirements of capacitor voltage &
inductor current .

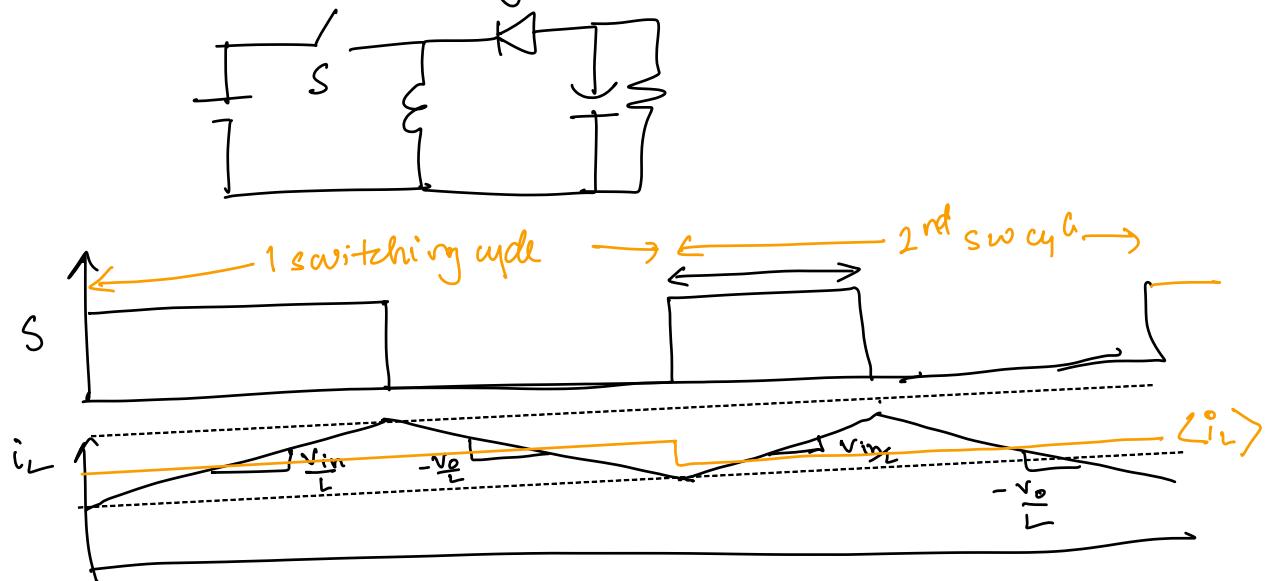




- ① We want to control the average inductor current
- ② Switch level behavior are ignored in modeling for control



What do we mean by average?



When S is ON

$$v_L = L \frac{di_L}{dt} = V_{in}$$



When S is OFF

$$v_L = L \frac{di_L}{dt} = -V_o$$



We are interested in only the average value over
one switching cycle.

$$\langle i_L(t) \rangle_{T_S} = \frac{1}{T_S} \int_0^{T_S} i_L(z) dz$$

First switching cycle

average = sum over something
 someth-

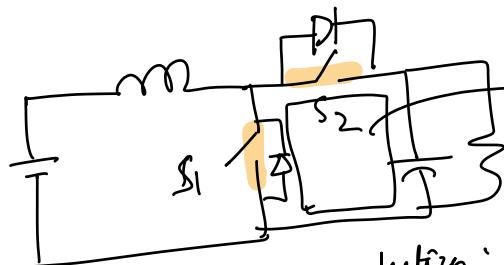
For any general time

$$\langle i_L(t) \rangle_{T_S} = \frac{1}{T_S} \int_t^{t+T_S} i_L(\tau) d\tau.$$

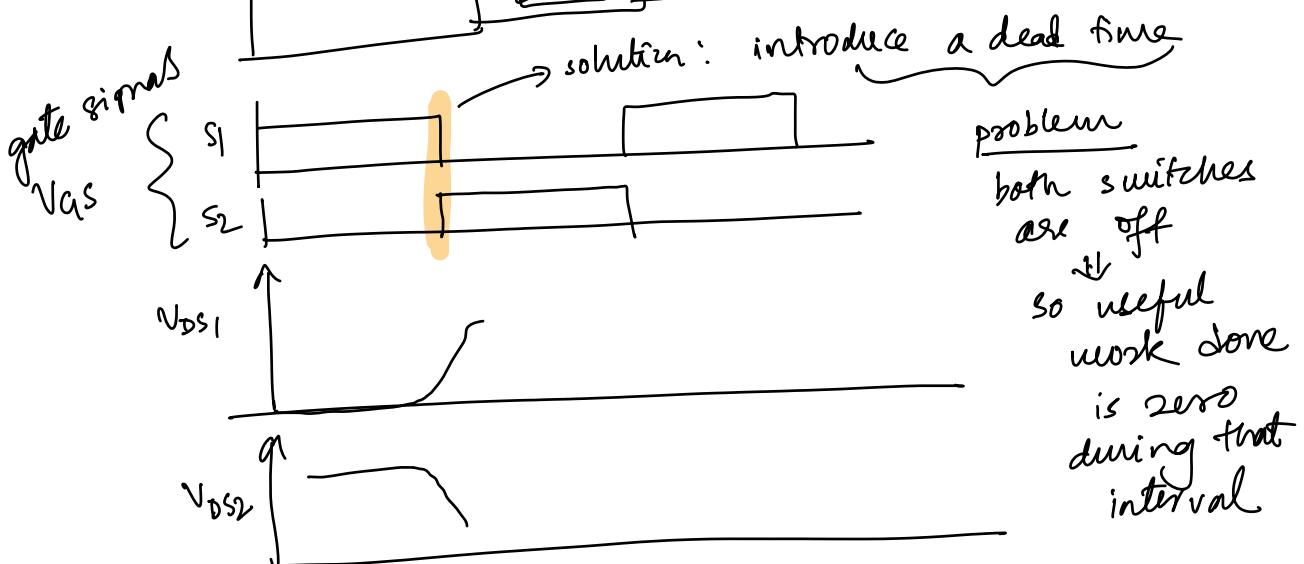
x^2 have to be different

$$\int_x f(x) dx$$

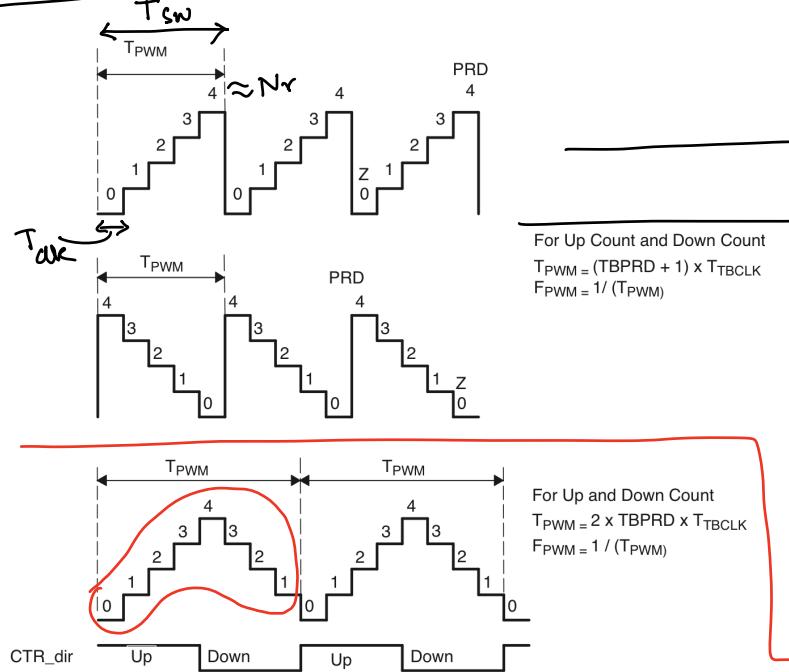
$$\frac{1}{T_S} \int_t^{t+T_S} i_L(\tau) d\tau = 0$$



capacitor gets shorted.



Corrections to Lecture 2



Asymmetric

So,

$$T_{SW} = (N_r + 1) \cdot T_{clk}$$

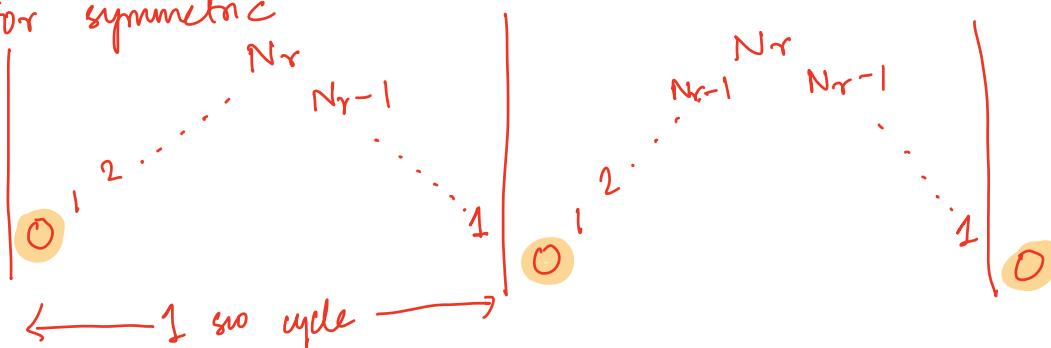
$$\Rightarrow N_r + 1 = \frac{T_{SW}}{T_{clk}}$$

Smallest duty ratio

$$= q_v = \frac{1}{N_r + 1} = \frac{T_{clk}}{T_{SW}}$$

$$= \frac{f_{clk}}{f_{sw}}$$

For symmetric



$$\text{So, } T_{sw} = 2 \cdot N_r \cdot T_{clk} \quad \therefore \quad N_r = \frac{T_{sw}}{2 T_{clk}}$$

$$\text{quantization} = \text{smallest duty ratio} = \frac{1}{N_r + 1} = q_v$$

$$\therefore q_v = \frac{1}{N_r + 1} = \frac{1}{\frac{T_{sw}}{2 T_{clk}} + 1} = \frac{1}{\frac{f_{clk}}{2 f_{sw}} + 1} = \frac{2 f_{sw}}{f_{clk} + 2 f_{sw}}$$

Under the assumption, $f_{clk} \gg f_{sw}$,

$$q_v = \frac{2 f_{sw}}{f_{clk}}$$

Correction #2

Q The problem about the buck converter.

(ii) I said we will be limited by max. switching freq.

I was wrong. We will be limited by minimum switching freq.

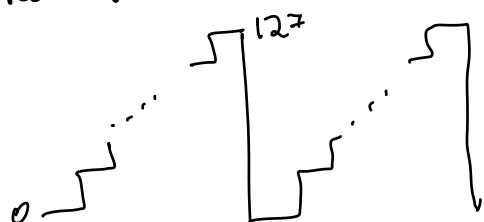
Reason:

① f_{sw} is fixed = 1 MHz.

② $N_{pwm} = 7 \therefore 2^{N_{pwm}} = 2^7 = 128$

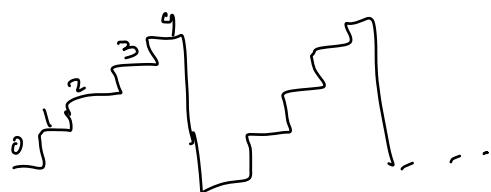
③ So, N_r can vary from 1 to 127.

④ Let us choose $N_r = 127$.



$$\therefore f_{sw1} = \frac{f_{sw}}{128}$$

⑤ Let us choose $N_r = 4$



$$\therefore f_{sw2} = \frac{f_{sw}}{5}$$

\therefore Clearly $f_{sw1} < f_{sw2}$ & f_{sw1} is the minimum switching freq.

Why do we still use two? Because it gives the best resolution.

⑥ Resolution (q) when $N_r = 127$:-

$$q_1 = \frac{1}{128} = 0.0078125 \quad (\text{satisfies the problem requirement})$$

⑦ Resolution (q) when $N_r = 4$:-

$$q_2 = \frac{1}{5} = 0.2 \quad (\text{does not satisfy problem requirement})$$

$$(iii) V_o = d \cdot V_{in}$$

$$\begin{aligned} \Delta(V_o) &= \Delta(d) V_{in} \\ &= (\Delta d) (V_{in}) \end{aligned}$$

$$\Delta d = q \quad \text{If we used } N_r = 127.$$

$$\therefore \Delta V_o = q_1 (V_{in})$$

$$= (0.0078125) \cdot (24) = 0.1875 V.$$