Lab 2 Lecture Notes

Monday, January 31, 2022 5:12 PM

Agenda:

- · Inner Current / outer voltage control (Background)

- · week 1: controller design · week z: implementation and HTL · week 3: works time and wrop-up.

1) Backgrowe.

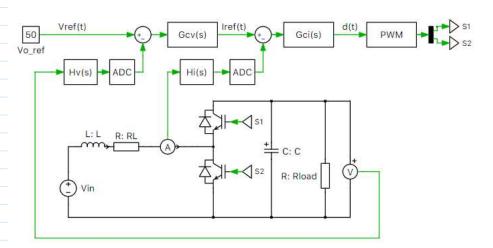


Figure 1: Conceptual diagram of ICOV control for a synchronous boost

I notice inputs fortputs

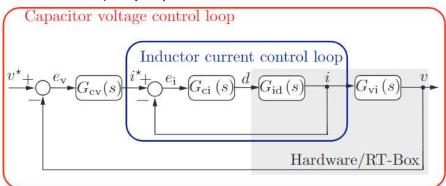
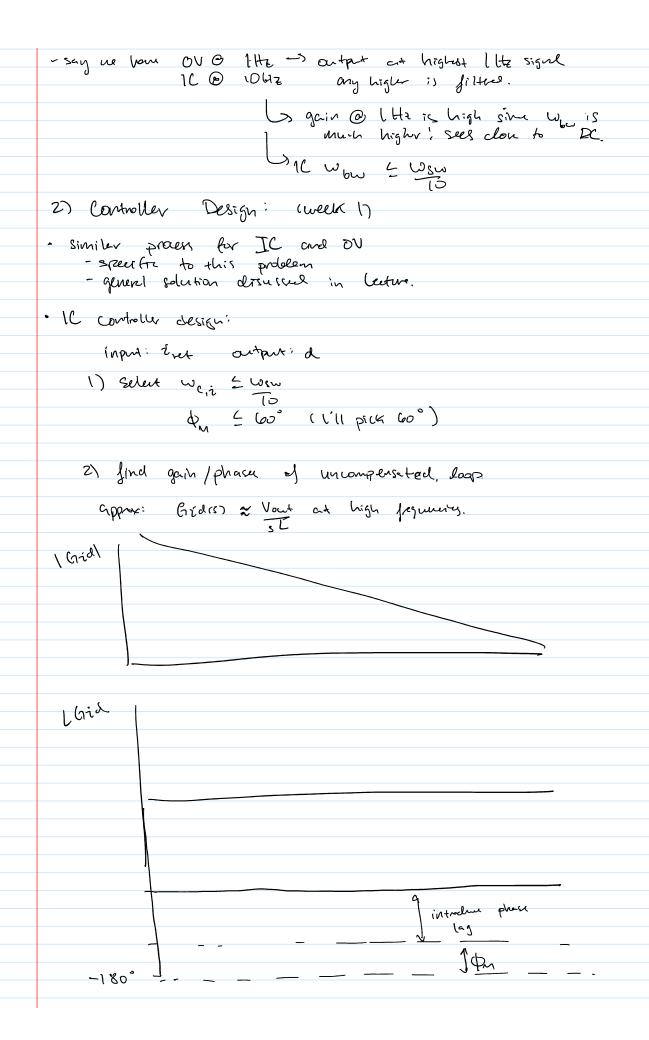


Figure 2: Transfer function diagram of ICOV control

Wow for IC loop 10x HIGHER flan Wow for OV loop Why?

- say ne bon OV & lite -> output at highest lite signe 10 @ 10612 any higher is filters.



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Mex value + safety
  i. 3.34 3.34 Vant: 334 3.34 Tool
   " USing ~ 25% SE
- you can close they baced on your design last
  questo
- implemed PI in code;
      tur = ivel . t
      Yim: lep ien som also un an avray
      Yeins = Tomy (O.S) (ter. Iter. prev) ki + y-int- prev
               Cotrape Zoidel integration
     - some idea for V
- saturation
     - Saturak y int [-0.95] 0.95]
     · cature y, on wer land duty
    · Saturck y, or maximin cumit
 code strutue: (Suggested)
  Chlobals I const delines
· State variables for at least ( precious cycle
· returence voviables
 = saturation values
 · controller gains
 · scalings
 ADC intempt:
// colter control
   ULV = Vrex - Vio
   Yim, v = (Ts x 0.5) (ver + Ver prev) ki, + y<sub>vine</sub> prev)

if y ivt, v to local a
   Yvior = ven·lepin
   if y irt, v too high/low;
         se twell.
   updete y prev, your prev, ver prev, etc.
   Yv: Yint + Yin
```

upelete y prev, your prev, ver prev, etc. Yv = Yinz + Yizv it y too high low llyv is used ret! 11 current control. iru = Yv replat PI calculations but for IC loop senturate yz if needed 11 yz = duty. updak PWM duty registr (CMPA)