Lab 2 Lecture Notes Clean

Monday, January 31, 2022 5:12 PM

Agenda:

- · Inner Current / outer voltage control (Background)

- · week 1: controller design · week z: implementation and HIL · week 3: work time and wrop-up.

1) Backgrows.

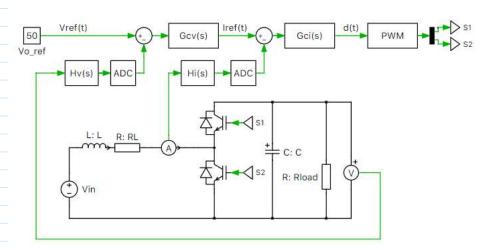


Figure 1: Conceptual diagram of ICOV control for a synchronous boost

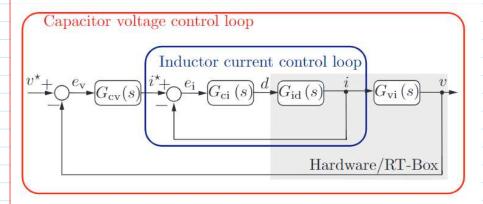
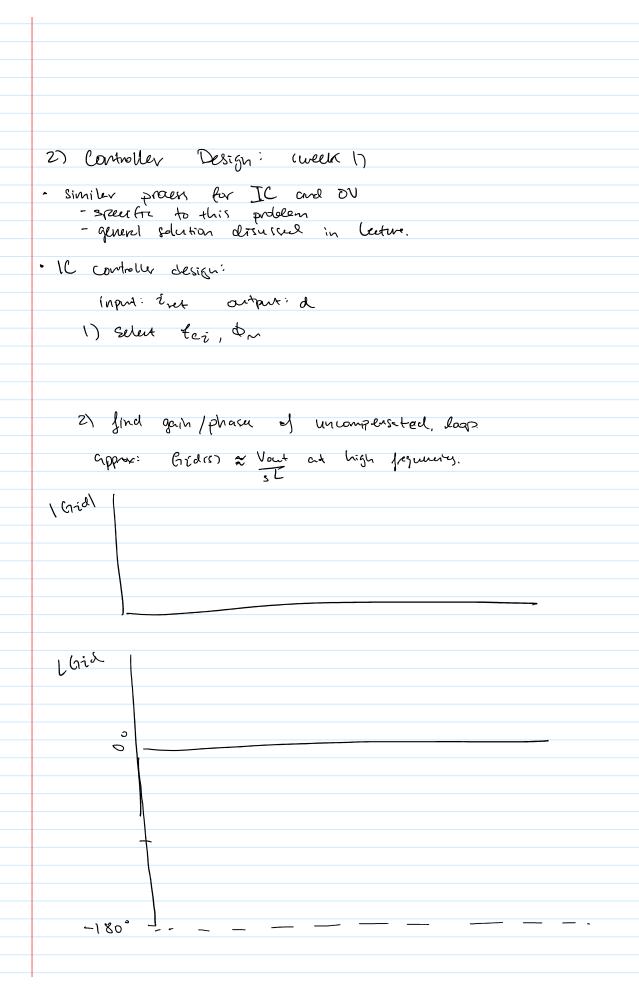


Figure 2: Transfer function diagram of ICOV control

Wow for IC 200p 10x HIGHER than Wow for OV loop Why?



3) Use PI controller: Crs) = (kp + ki)

$$L_i(s)$$
 = Crs) Prs) = Crs) Giaco

 $= \binom{kp + ki}{s} \binom{Vant}{sL}$

Use this to

 $= \binom{kp + ki}{sL}$

Use this to

 $= \binom{kp + ki}{sL}$
 $= \binom{kp + ki}{sL}$

Note: Kptki Gra (1 + Wps): Gc Use (1) and (2) to get Gera were · Simulate count control. · Storter file for control in Canvas - this is a transtr function model - also need to implement u/ switched would · OV controller design input: Vret output: ircl select wer & wer lickething Guill =1 > Jeg + kig ? [DR RL] (3) L (Mithis Guz = - 180° + Pm L'kpt ti i L'Evi Es approx O at low frequez. -arcton (wile) = - (80° +ch = auton (wilp) -180 = -180 + Um Tarcten (ki usus) = Pm (cm) · uch (3) (4) to get hy/hi for voltage controller. 3) Implementation (well 2) - Set up RT Box (see auxiliany video) - Scaling - scale in NECS, sent to MLM -reed in ADC ph - Scale to actual numerical value Scale: 3.3V - new ADC wolter Mex value + satety

```
- you can close they based on your design last
 quester
- implemed PI in code;
     - save idea for V
- saturation
     · Saturck Yint [-0.95, 0.95]
     · satural y; on wex (min duty
    · Saturch y ou max min cumi
 code strutue: (Suggested)
 Globals / Const defines
· State variables for at lost (previous cycle · returner variables
 " saturation values
" controller gains
 · scalings
 ADC intempt:
// coltese control
   Ver = Vrey - Vio
                                                   PI colculation
   Yvor = ver· kpin
   Yim, v = (Tsyo. 5) (ver + Verpon) kin + you prev.
   if yirt, V too high/low;
          sature.
   updete y prev, your prev, ver prev, etc.
    M: Yint + Yin
```

it y too high low lyv is wont ret!

it y too high low llyv is used ret! // current control. iru = Yv replace FI calculations but for IC loop contract yi it needed 11 yi = duty. upuck PWM duty registr (CMPA)