EE 458 – Power Electronics Controls, Winter 2021

Homework 3

Due Date: Thursday February 3rd, 2022, 4:30pm PT

Problem 1: For the given boost converter circuit in Fig. 1, assume the following,

1. The input voltage V_{in} is perfectly stiff.
2. The duty ratio $d(t)$ represents the time for which S_1 is turned ON. For the complement, $1-d(t)$, S_2 is turned ON.
3. Output capacitor is ideal, lossless.
4. Assume $R_{\text{L}} = 0$

Let us assume the ratio of small signal output voltage to duty ratio transfer function is defined as follows,

$$G_{\text{vd}}(s) = G_o \frac{1 - \frac{s}{\omega_z}}{1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2}.$$

Specify the values of G_o, ω_z, Q, and ω_o analytically in terms of the circuit parameters R, L, C and the nominal duty ratio, D, the nominal output voltage, V.

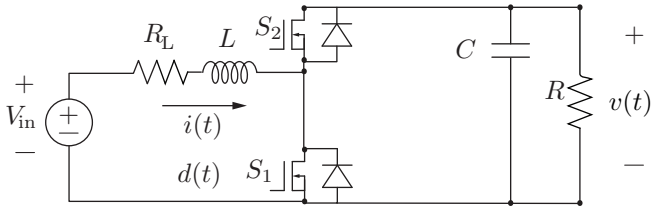

Figure 1: Boost converter circuit for Problem 1.

[*Refer to Fundamentals of Power Electronics E&M, pp 300, Table 8.2 to check your solution.*]

Problem 2: We operate the boost converter of Problem 1 at the following nominal conditions : $V_{\text{in}} = 24\text{V}$, output voltage = 48V, output power = 250 W, $f_{sw} = 100$ kHz, $L = 1.25\text{mH}$, $C = 250\mu\text{F}$.
Does the stability of the system $G_{\text{vd}}(s)$ with no compensation (controller, $C(s) = 1$) *increases, decreases, or remains unaffected* when

- You redesign inductance, L to reduce the current ripple of $i(t)$ shown in Figure 1.
- You change the output power to 100 W.

- You change the switching frequency to 10 kHz.
- You change the output voltage to be at 30 V.

You might use bode plots of $G_{\text{vd}}(s)$ with these operating conditions to explain, or give an intuitive explanation.

Problem 3: Consider the transfer functions

$$G_1(s) = G_o \frac{1}{1 + \frac{s}{\omega_1}}, \quad G_2(s) = \frac{1}{1 + \frac{s}{\omega_2}}.$$

where $G_o = 100$, $f_1 = \omega_1/(2\pi) = 1\,\text{kHz}$, and $f_2 = \omega_2/(2\pi) = 10\,\text{kHz}$. For the questions below, your frequency axes should be in Hz, amplitude in dB, and phase in degrees.

(a) Sketch the Bode plots for G_1 and G_2 using the linear asymptote approximations for both amplitude and phase.

(b) Using your result from (a) sketch the Bode plot for the product $G_1(s)G_2(s)$. You can use a computer to check your result.

Problem 4: In this problem we will study the complete digital control loop. In the questions on the next page, assume

- $f_{\text{clk}} = T_{\text{clk}}^{-1} = 100\,\text{MHz}$, and the switching period is $T_{\text{s}} = (100\,\text{kHz})^{-1}$.
- Asymmetric leading edge modulation is used, N_{r} is the maximum counter value, and the counter increments every clock cycle.
- The ADC has $n_{\text{A/D}} = 12$ bits and the ADC pin can sample an analog voltage between $0\,\text{V}$ and $V_{\text{FS}} = 3\,\text{V}$.
- The time interval between the ADC start of conversion (SOC) and end of conversion (EOC) takes 50 clock cycles. Denote this time as $T_{\text{A/D}}$. The SOC is triggered each time the DPWM counter resets to N_{r}.
- The arithmetic to carry out the controller code consumes 500 clock cycles. Denote this time as T_{comp}.
- After the processor finishes the controller arithmetic, the a new value of $x_c[n]$ is available where $x_c[n]$ will eventually be loaded into the DPWM compare register. Before the value of $x_c[n]$ is loaded into the DPWM compare register, it is held temporarily in a shadow register. The time this value is held in the shadow register is called T_{hold}.
- The value of $x_c[n]$ is read into the DPWM compare register when the counter resets to N_{r}. The cumulative time between the ADC SOC and when $x_c[n]$ is written into the DPWM compare register is denoted as T_{ctrl} where $T_{\text{ctrl}} = T_{\text{A/D}} + T_{\text{comp}} + T_{\text{hold}}$.
- The time interval between when $x_c[n]$ is read into the DPWM module and the next transition in the PWM pin $c(t)$ is called T_{mod}.

Answer the questions below:

(a) If the voltage on the ADC pin, $v_{\mathrm{A/D}}$, is 0.75 V, what digital integer value, $x_{\mathrm{A/D}}$, will the ADC produce?

(b) What is the voltage resolution, $q_{\mathrm{A/D}}$, of the ADC analog input?

(c) Compute T_{hold} and the ratio $T_{\mathrm{hold}}/T_{\mathrm{ctrl}}$. What does the value of $T_{\mathrm{hold}}/T_{\mathrm{ctrl}}$ tell us about the computational burden on the processor? What happens to the ratio $T_{\mathrm{hold}}/T_{\mathrm{ctrl}}$ as the controller requires more computations?

(d) Compute T_{ctrl}, T_{mod}, and T_{d}. Express your results in terms of T_{clk} and D.

(e) Sketch the binary PWM output $c(t)$ and sampled ADC value $x_{\mathrm{A/D}}$ waveforms onto Figure 2. Overlay $x_{\mathrm{A/D}}$ on the same plot as $v_{\mathrm{A/D}}$.

(f) Add the following items onto Figure 2: Label the maximum feasible integer value of $x_{\mathrm{A/D}}$ vertical axis, specify the DPWM counter maximum N_{r}, label the duty D, and the delays T_{ctrl} and T_{mod}. Also draw the delays $T_{\mathrm{A/D}}, T_{\mathrm{comp}}$, and T_{hold} within T_{ctrl} and try to draw them to scale.

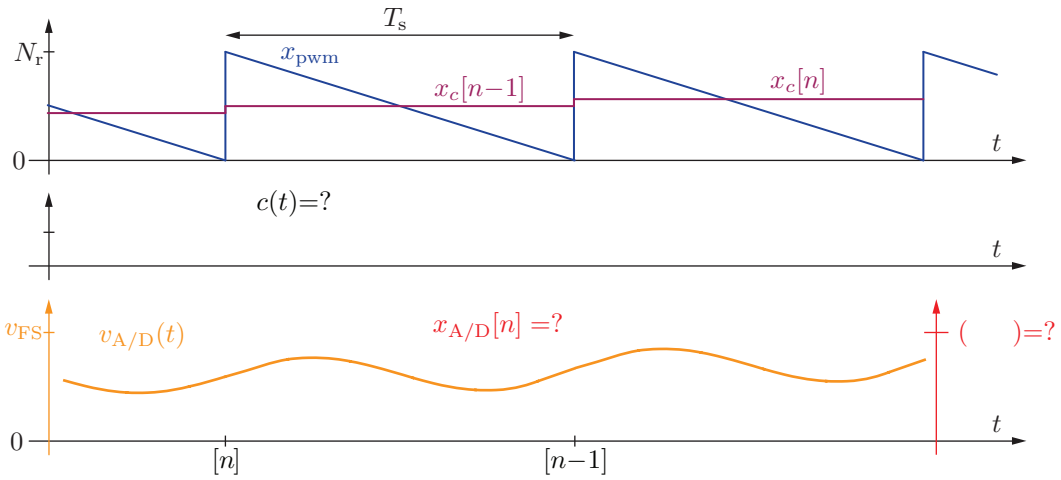

Figure 2: Digital system waveforms for Problem 3.