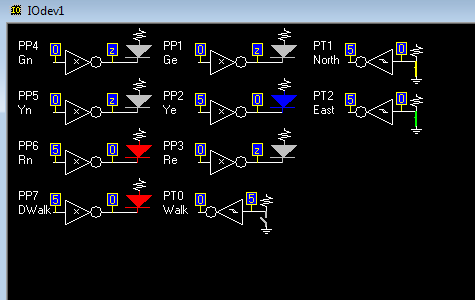
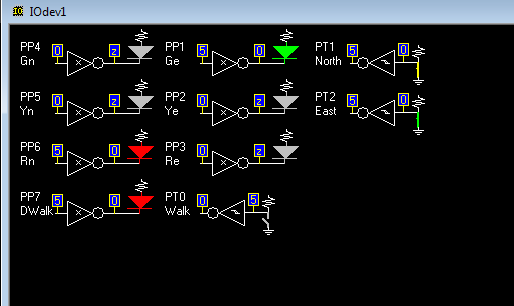
Kevin Gilbert and Graham Gilvar

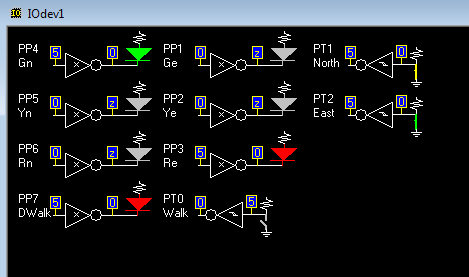
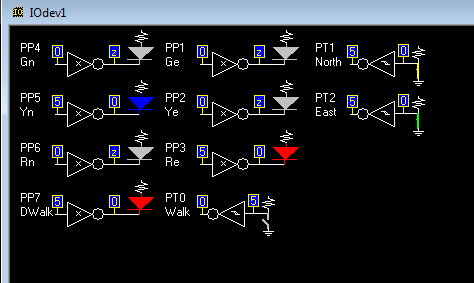
06 March 2012

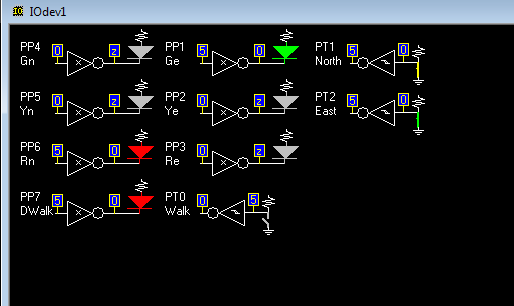
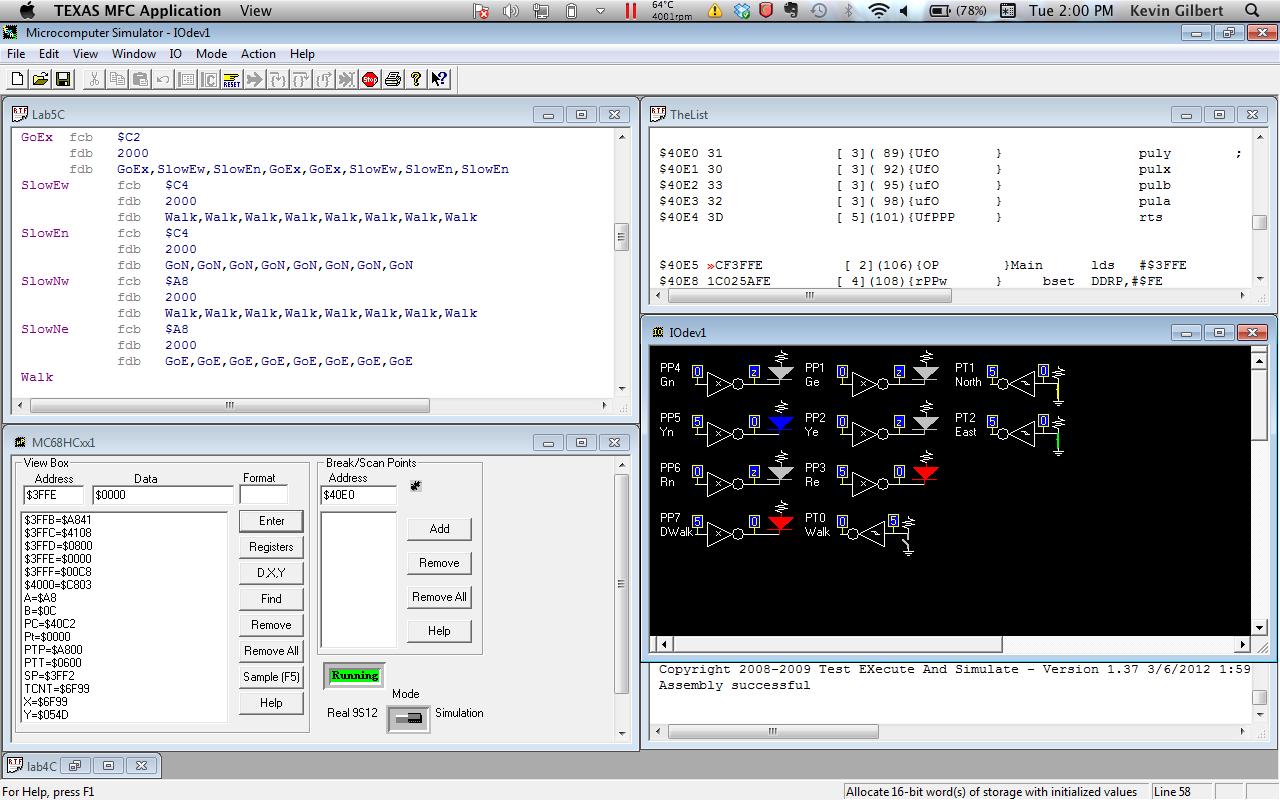
EE319K Gerstlauer Lab 4:30-4:45

Lab 5

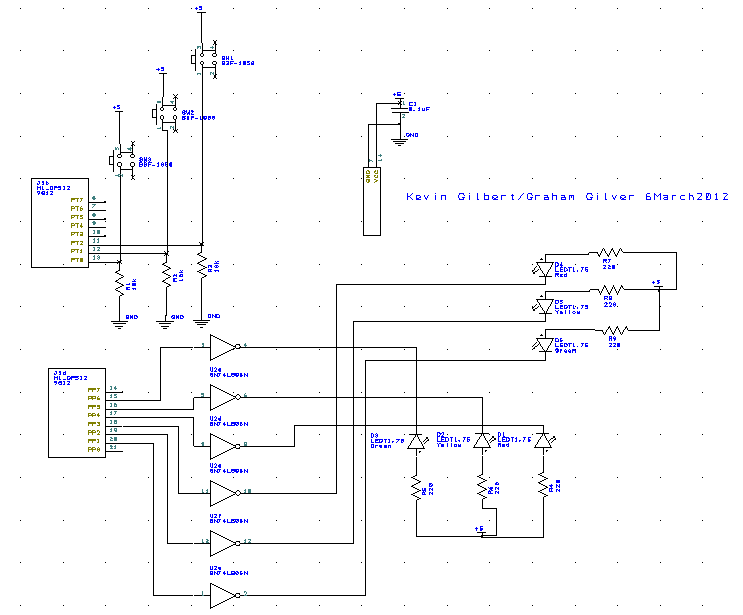
1.)



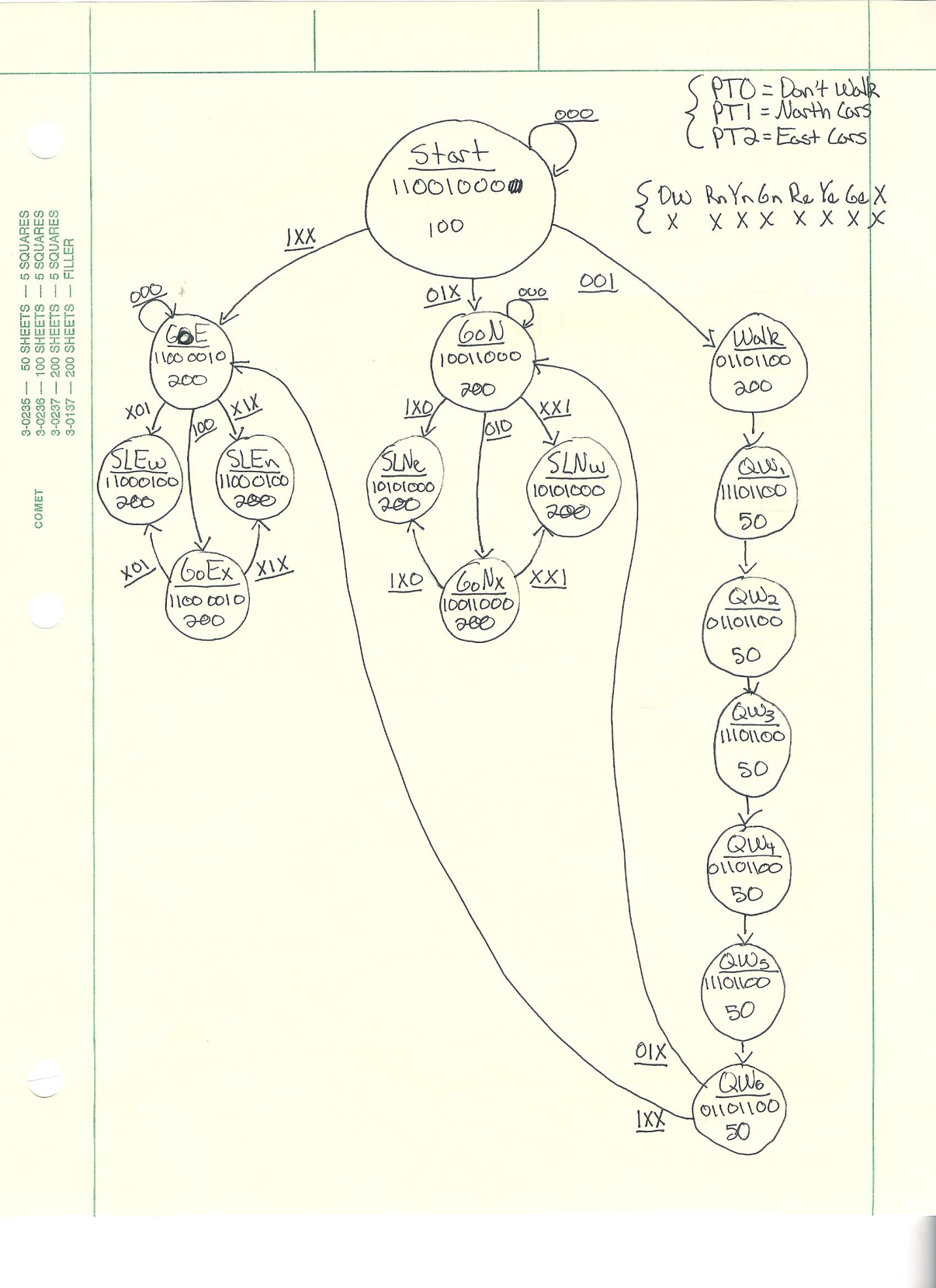




Gilbert 2

2.)

3.)



Gilbert 3

4.)

; \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* Lab5 \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

; Kevin Gilbert and Graham Gilvar

; Date created: 04 March 2012, 6:00 PM

; Last updated: 06 March 2012, 4:00 PM

; Tuesday 4:30-4:45 lab Gerstlauer

; Traffic light controller, FSM array programming

; I/O Directories

PTH equ $0260

DDRH equ $0262

PTP equ $0258

DDRP equ $025A

PTT equ $0240

DDRT equ $0242

TSCR1 equ $0046

TSCR2 equ $004D

TCNT equ $0044

out equ 0

wait equ 1

next equ 3

; RAM variables

Pt rmb 2

RegY rmb 2

TCNTo rmb 2

; \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* Main \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

org $4000 ; ROM State Array

Start fcb $C8 ; Output

fdb 1000 ; Delay value

fdb Start,Walk,GoN,GoN,GoE,GoE,GoE,GoE,GoE

GoN fcb $98

fdb 2000

fdb GoN,SlowNw,GoNx,SlowNw,SlowNe,SlowNw,SlowNe,SlowNw

GoNx fcb %10011000

fdb 2000

fdb GoNx,SlowNw,GoNx,SlowNw,SlowNe,SlowNw,SlowNe,SlowNw

GoE fcb $C2

fdb 2000

fdb GoE,SlowEw,SlowEn,SlowEn,GoEx,SlowEw,SlowEn,SlowEn

GoEx fcb $C2

fdb 2000

fdb GoEx,SlowEw,SlowEn,GoEx,GoEx,SlowEw,SlowEn,SlowEn

SlowEw fcb $C4

fdb 2000

fdb Walk,Walk,Walk,Walk,Walk,Walk,Walk,Walk

SlowEn fcb $C4

fdb 2000

fdb GoN,GoN,GoN,GoN,GoN,GoN,GoN,GoN

SlowNw fcb $A8

fdb 2000

fdb Walk,Walk,Walk,Walk,Walk,Walk,Walk,Walk

SlowNe fcb $A8

fdb 2000

fdb GoE,GoE,GoE,GoE,GoE,GoE,GoE,GoE

Walk fcb %01101100

fdb 200

fdb QW1,QW1,QW1,QW1,QW1,QW1,QW1,QW1

QW1 fcb %11101100

fdb 50

fdb QW2,QW2,QW2,QW2,QW2,QW2,QW2,QW2

QW2 fcb %01101100

fdb 50

fdb QW3,QW3,QW3,QW3,QW3,QW3,QW3,QW3

QW3 fcb %11101100

fdb 50

fdb QW4,QW4,QW4,QW4,QW4,QW4,QW4,QW4

QW4 fcb %01101100

fdb 50

fdb QW5,QW5,QW5,QW5,QW5,QW5,QW5,QW5

QW5 fcb %11101100

fdb 50

fdb QW6,QW6,QW6,QW6,QW6,QW6,QW6,QW6

QW6 fcb %01101100

fdb 50

fdb Start,Walk,GoN,GoN,GoE,GoE,GoE,GoE

Timer\_init psha ; Save Registers

pshb

pshx

pshy

movb #$80,TSCR1

movb #$07,TSCR2 ; Fast TCNT for lab simulation ($00), slow TCNT for actual board run ($07)

puly ; Restore Registers

pulx

pulb

pula

rts

Timer\_wait psha ; Save Registers

pshb

pshx

pshy

compare ldd TCNT

subd TCNTo

cpd #65000

blo compare

puly ; Restore Registers

pulx

pulb

pula

rts

Timer\_wait10ms psha ; Save Registers

pshb

pshx

pshy

loop2 ldx TCNT

stx TCNTo

jsr Timer\_wait

dbne Y,loop2

puly ; Restore Registers

pulx

pulb

pula

rts

Main lds #$3FFE

bset DDRP,#$FE

bclr DDRT,#$07

jsr Timer\_init

ldx #Start

stx Pt

bset PTP,#$C8

loop ldaa out,X ; Load outputs

staa PTP

ldy wait,X ; Wait routine

sty RegY

jsr Timer\_wait10ms

ldab PTT

lslb

abx

ldx next,X

bra loop

org $FFFE

fdb Main