

# Keiane Balicanta

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## EDUCATION

### Rowan University

Glassboro, NJ

*Bachelor of Science, Electrical & Computer Engineering*

May 2025

- Minor: Computer Science
- Certificate of Undergraduate Studies: Power Systems Engineering
- 3.64 GPA, Dean's List 2024

### Camden County College

Blackwood, NJ

*Associate of Science, Engineering Science*

Sept 2019 - Dec 2021

- 3.16 GPA, NJ STARS Scholarship

## SKILLS

<b>Programming Languages</b>	Python   C/C++   Java   MATLAB   Verilog HDL
<b>Web</b>	HTML   CSS   Flask
<b>DevOps</b>	GitHub/GitKraken   Git   VI   VIM
<b>Platforms</b>	Windows 2k   Ubuntu Linux   UNIX   MAC OS
<b>Hardware</b>	TI MSP430   FPGA DE10-Lite   Arduino
<b>Software</b>	VS Code   Eclipse   VS Studio 19/22
<b>Simulation</b>	Simulink   LTSpice   Altium Designer   Altera Quartus II   SolidWorks   AutoCad
<b>Communication</b>	Microsoft Office 2k/97   LaTeX
<b>Certifications</b>	Security Clearance   Common Access Card (CAC)

## TECHNICAL PROJECTS & RELEVANT COURSEWORK

### Fractional Visualization of Attribution Maps

Sept 2023 - May 2024

*Electrical & Computer Engineering | Junior Engineering Clinic*

Rowan University

- Investigated the impact of fractional differintegrals utilizing Riemann-Liouville and Grünwald-Letnikov methods of fractional calculus.
- Created visual interface using PyTorch and Gradio to visualize fractional methods using image inputs from CIFAR10 and MNIST databases.
- Implemented various Gradio components such as sliders, radios, buttons, and text inputs to give users deep customization with the model.

### LED Chess Board

Jan 2023 - May 2023

*Electrical & Computer Engineering | Embedded Systems, Electronics*

Rowan University

- Interfaced MSP MCU to mimic chess pieces on a prototype 4x4 LED matrix.
- Wrote C code and handled version control/repositories, and part of Altium PCB design with group mates.

### RISCV Computer Processor

Sept 2022 - Dec 2022

*Electrical & Computer Engineering | Computer Architecture*

Rowan University

- Designed a RISCV 32-bit CPU and testbenches using Quartus software and Verilog HDL.
- Input 32-bit instructions via ROM unit that was designed alongside a register file, ALU, RAM, program counter, and a control unit.

## WORK HISTORY

### Pepco Holdings Inc, Exelon

May 2024 - Present

*CO-OP, Smart Grid Project Execution*

Carney's Point, NJ

- Worked with a team of project managers on documentation, scheduling, forecasting, execution, and closeout of projects.
- Led the transition of project documentation from SharePoint to Oracle's Unifier Project Portfolio Management system for standardized documentation management and project tracking while also conducting training sessions for transition.

### Naval Surface Warfare Center Philadelphia Division (NSWCPD), NAVSEA

May 2023 - Aug 2023

*Engineering Intern, Software Service Agent*

Philadelphia, PA

- Developed code from design documents for sea water, hydraulics, and doors/hatches ship sub-systems.
- Worked with team in weekly meetings on criticisms, team updates, and individual status reports.