LOW-VOLTAGE H-BRIDGE IC

Check for Samples: DRV8837

FEATURES

- **H-Bridge Motor Driver**
  - **Drives a DC Motor or One Winding of a Stepper Motor or Other Loads**
  - **Low MOSFET On-Resistance: HS + LS 280 mΩ**
- **1.8-A Maximum Drive Current**
- **1.8-V to 11-V Motor-Operating Supply-Voltage Range**
- **Separate Motor and Logic Supply Pins**
- **PWM (IN/IN) Interface**
- **Low-Power Sleep Mode With 120-nA Maximum Combined Supply Current**
- **Dedicated $\overline{\text{SLEEP}}$ Pin**
- **2-mm × 2-mm 8-Pin WSON Package**

APPLICATIONS

- **Cameras**
- **DSLR Lenses**
- **Consumer Products**
- **Toys**
- **Robotics**
- **Medical Devices**

DESCRIPTION

The DRV8837 provides an integrated motor-driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion-control applications. The device has one H-bridge driver, and can drive one dc motor or one winding of a stepper motor, as well as other devices like solenoids. The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the motor winding. An internal charge pump generates needed gate-drive voltages.

The DRV8837 can supply up to 1.8 A of output current. It operates on a motor power-supply voltage from 1.8 V to 11 V, and a device power-supply voltage of 1.8 V to 7 V.

The DRV8837 has a PWM (IN/IN) input interface, which is compatible with industry-standard devices.

There are internal shutdown functions for overcurrent protection, short-circuit protection, undervoltage lockout and overtemperature.

The DRV8837 package is an 8-pin 2-mm × 2-mm WSON PowerPAD™ package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

ORDERABLE PART NUMBER	PACKAGE	TOPSIDE MARKING	SHIPPING
DRV8837DSGR	WSON – DSG	837	Reel of 3000
DRV8837DSGT	WSON – DSG	837	Reel of 250

(1) For the most-current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

FUNCTIONAL BLOCK DIAGRAM

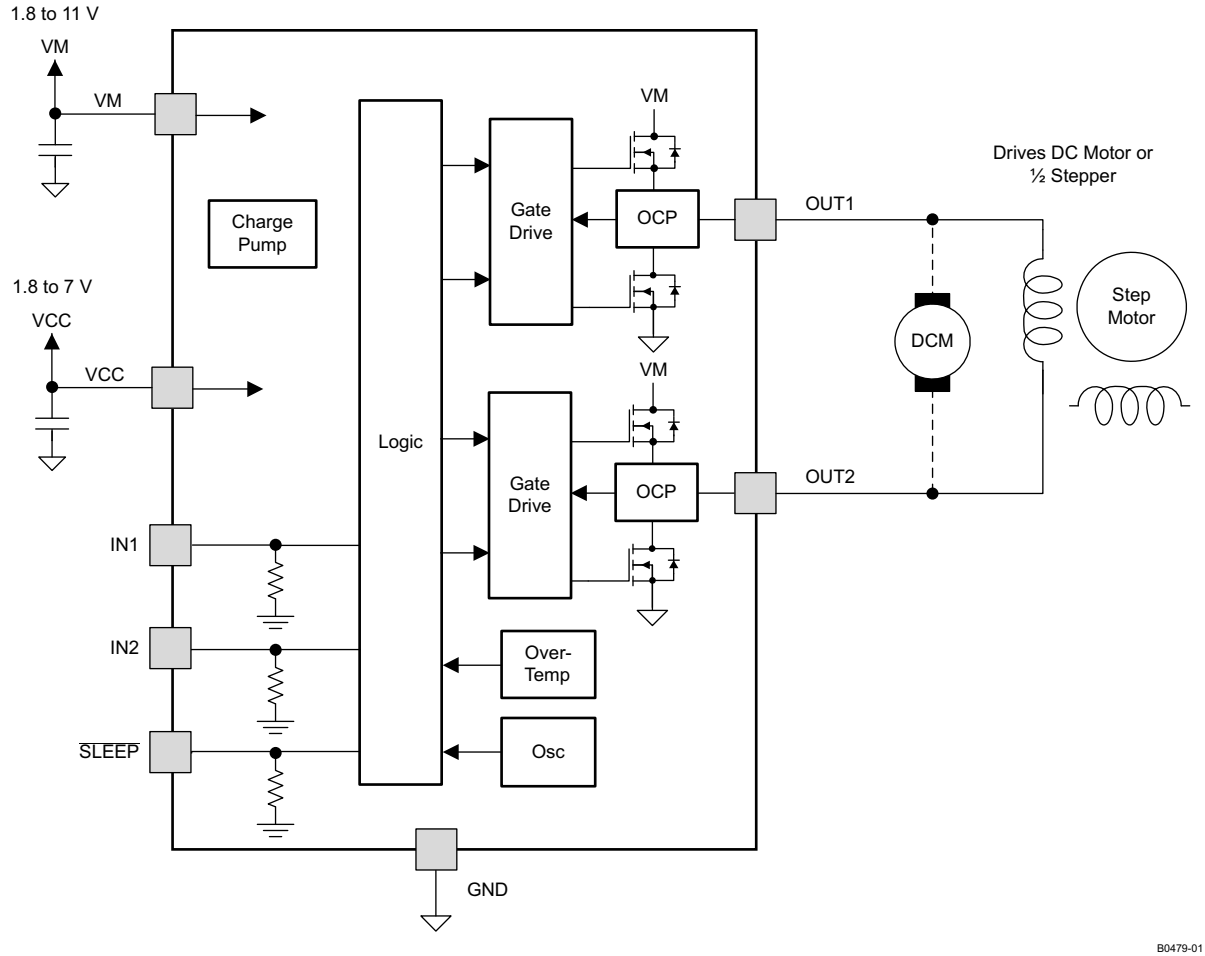
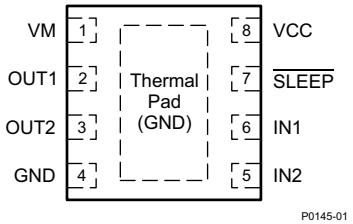


Figure 1. Functional Block Diagram

DRV8837
DSG Package
(Top View)



PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
Power and Ground				
GND	4	–	Device ground	
VCC	8	–	Device supply	Bypass to GND with a 0.1-µF 6.3-V ceramic capacitor.
VM	1	–	Motor supply	Bypass to GND with a 0.1-µF 16-V ceramic capacitor.
Control				
IN1	6	I	Input 1	Logic-high sets OUT1 high Internal pulldown resistor
IN2	5	I	Input 2	Logic-high sets OUT2 high Internal pulldown resistor
$\overline{\text{SLEEP}}$	7	I	Sleep mode input	Logic-low puts device in low-power sleep mode Logic-high for normal operation Internal pulldown resistor
Output				
OUT1	2	O	Output 1	Connect to motor winding
OUT2	3	O	Output 2	

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

		VALUE	UNIT
VM	Power supply voltage range	–0.3 to 12	V
VCC	Power supply voltage range	–0.3 V to 7	V
	Digital pin voltage range	–0.5 V to 7	V
	Peak motor drive output current	Internally limited	A
T_J	Operating virtual junction temperature range	–40 to 150	ºC
T_{stg}	Storage temperature range	–60 to 150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV8837 DSG 8 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	60.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	71.4	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	32.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	32.8	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	9.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Device power supply voltage range	1.8		7	V
V_M	Motor power-supply voltage range	1.8		11	V
I_{OUT}	H-bridge output current(1)	0		1.8	A
f_{PWM}	Externally applied PWM frequency	0		250	kHz
V_{IN}	Logic-level input voltage	0		5.5	V

(1) Power dissipation and thermal limits must be observed.

ELECTRICAL CHARACTERISTICS

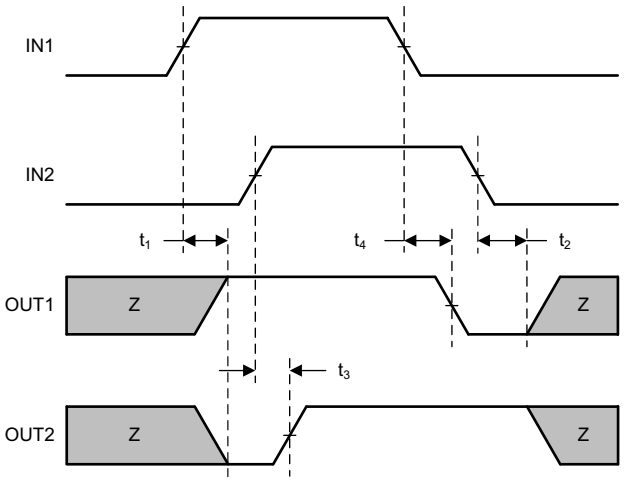
T_A = 25°C, V_M = 5 V, V_{CC} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supplies						
I_{VM}	VM operating supply current	V_M = 5 V, V_{CC} = 3 V, no PWM		40	100	µA
		V_M = 5 V, VCC = 3 V, 50-kHz PWM		0.8	1.5	mA
I_{VMQ}	VM sleep-mode supply current	V_M = 5 V, V_{CC} = 3 V, $\overline{SLEEP}$ = 0 V		30	95	nA
I_{VCC}	VCC operating supply current	V_M = 5 V, V_{CC} = 3 V, no PWM		300	500	µA
		V_M = 5 V, V_{CC} = 3 V, 50-kHz PWM		0.7	1.5	mA
I_{VCQ}	VCC sleep-mode supply current	V_M = 5 V, V_{CC} = 3 V, $\overline{SLEEP}$ = 0 V		5	25	nA
V_{UVLO}	VCC undervoltage lockout voltage	V_{CC} rising			1.8	V
		V_{CC} falling			1.7	
Logic-Level Inputs						
V_{IL}	Input low voltage		0.25 V_{CC}	0.38 V_{CC}		V
V_{IH}	Input high voltage			0.46 V_{CC}	0.5 V_{CC}	V
V_{HYS}	Input hysteresis			0.08 V_{CC}		V
I_{IL}	Input low current	V_{IN} = 0 V	–5		5	µA
I_{IH}	Input high current	V_{IN} = 3.3 V			50	µA
R_{PD}	Pulldown resistance			100		kΩ
H-Bridge FETs						
$r_{ds(on)}$	HS + LS FET on-resistance	V_{CC} = 3 V, V_M = 5 V, I_O = 800 mA, T_J = 25°C		280	330	mΩ
I_{OFF}	Off-state leakage current	V_{OUT} = 0 V			±200	nA
Protection Circuits						
I_{OCP}	Overcurrent protection trip level		1.9		3.5	A
t_{OCR}	OCP retry time			1		ms
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	ºC

TIMING REQUIREMENTS

T_A = 25°C, V_M = 5 V, V_{CC} = 3 V, R_L = 20 Ω

			MIN	MAX	UNIT
1	t_1	Output enable time		120	ns
2	t_2	Output disable time		120	ns
3	t_3	Delay time, INx high to OUTx high		120	ns
4	t_4	Delay time, INx low to OUTx low		120	ns
5	t_5	Output rise time	50	150	ns
6	t_6	Output fall time	50	150	ns



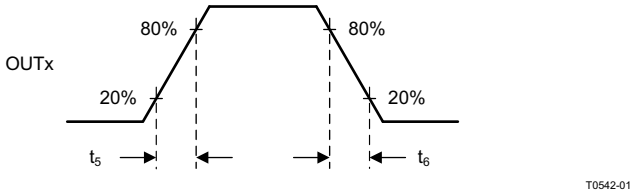


Figure 2. Input/Output Timing

FUNCTIONAL DESCRIPTION

Bridge Control

The DRV8837 is controlled using a PWM input interface, also called an IN/IN interface. Each output is controlled by a corresponding input pin.

The following table shows the logic for the DRV8837:

IN1	IN2	OUT1	OUT2	Function (DC Motor)
0	0	Z	Z	Coast
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake

Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the DRV8837 enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

Power Supplies and Input Pins

The input pins may be driven within their recommended operating conditions with or without the VCC and/or VM power supplies present. No leakage current path exists to the supply. There is a weak pulldown resistor (approximately 100 kΩ) to ground on each input pin.

VCC and VM may be applied and removed in any order. When VCC is removed, the device enters a low-power state and draws very little current from VM. If the supply voltage is between 1.8 V and 7 V, VCC and VM may be connected together.

Protection Circuits

The DRV8837 is fully protected against undervoltage, overcurrent, and overtemperature events.

OVERCURRENT PROTECTION (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge are disabled. After approximately 1 ms, the bridge is re-enabled automatically.

Overcurrent conditions on both high- and low-side devices, that is, a short to ground, supply, or across the motor winding all result in an overcurrent shutdown.

THERMAL SHUTDOWN (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. Once the die temperature has fallen to a safe level, operation automatically resumes.

UNDERVOLTAGE LOCKOUT (UVLO)

If at any time the voltage on the VCC pin falls below the undervoltage lockout threshold voltage, all circuitry in the device is disabled and internal logic is reset. Operation resumes when VCC rises above the UVLO threshold.

THERMAL INFORMATION

Thermal Protection

The DRV8837 has thermal shutdown (TSD) as described in the *Protection Circuits* section. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8837 is dominated by the power dissipated in the output FET resistance, or $r_{DS(on)}$. Average power dissipation can be roughly estimated by:

$$P_{TOT} = r_{DS(on)} \times (I_{OUT(RMS)})^2 \quad (1)$$

where P_{TOT} is the total power dissipation, $r_{DS(on)}$ is the resistance of the HS plus LS FETs, and $I_{OUT(RMS)}$ is the rms or dc output current being supplied to the load.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $r_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV8837DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	837	Samples
DRV8837DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	837	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

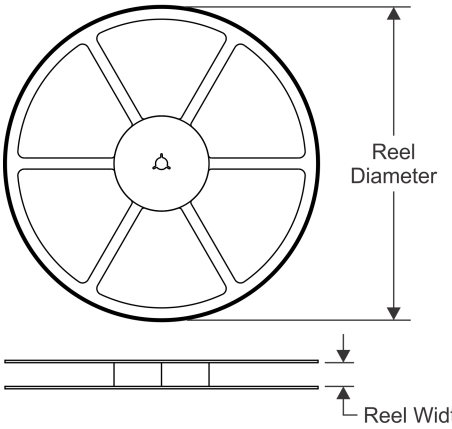
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

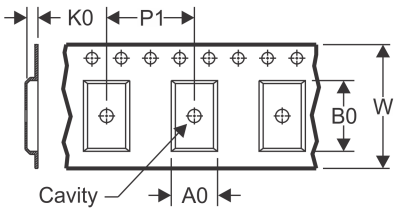
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

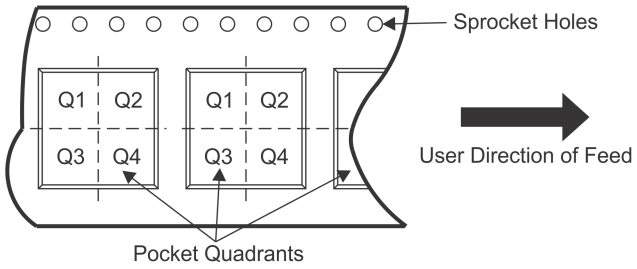


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

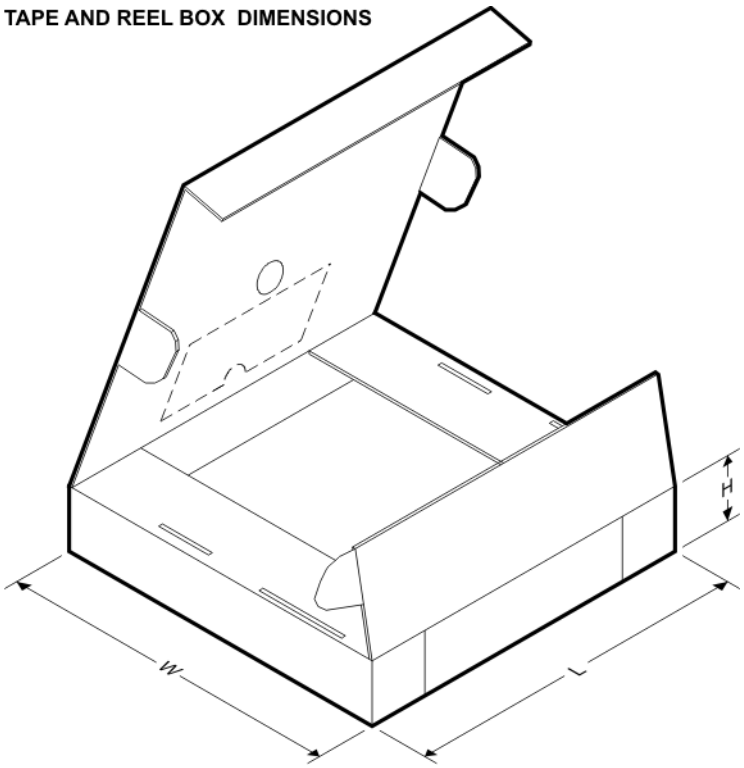
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8837DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8837DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

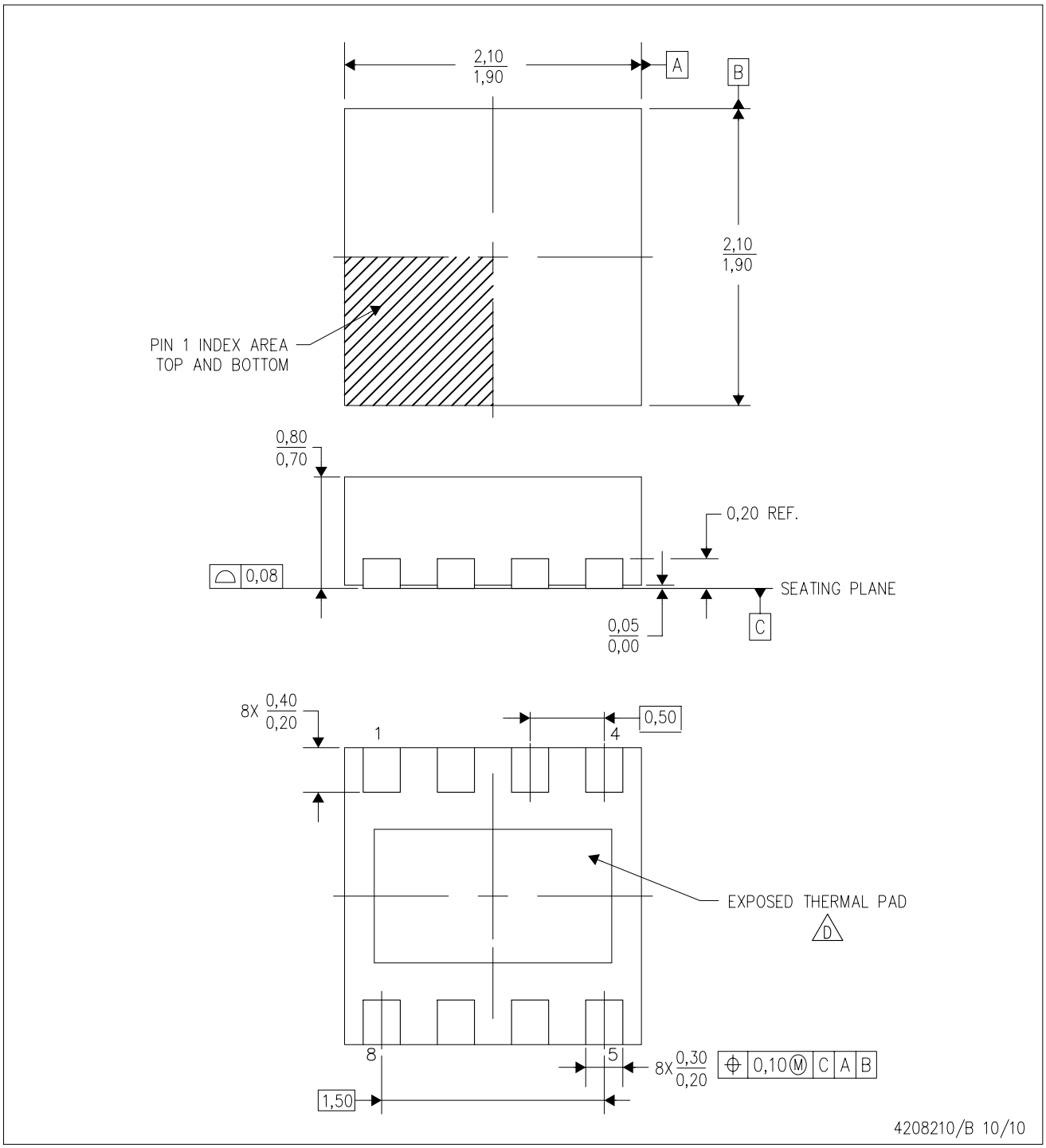
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8837DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
DRV8837DSGT	WSON	DSG	8	250	210.0	185.0	35.0

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

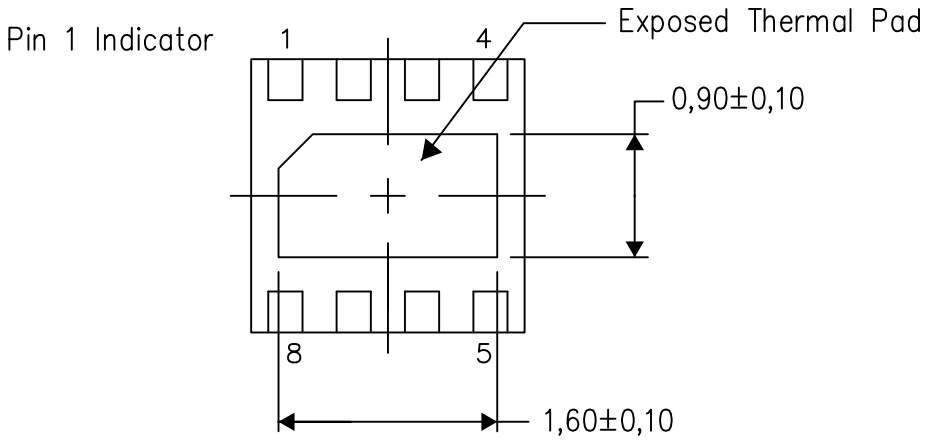
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



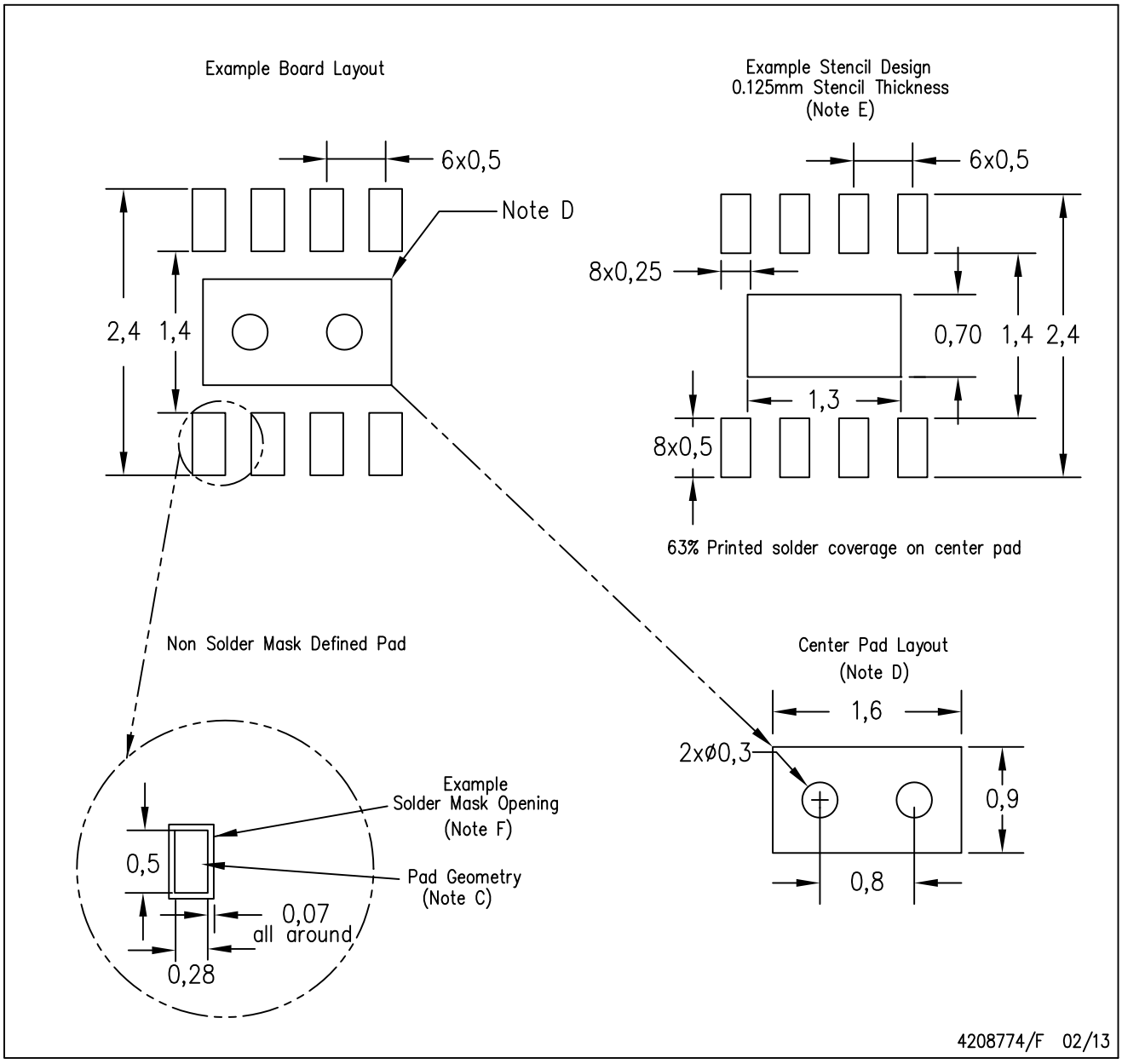
Bottom View

Exposed Thermal Pad Dimensions

4208347/G 08/13

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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