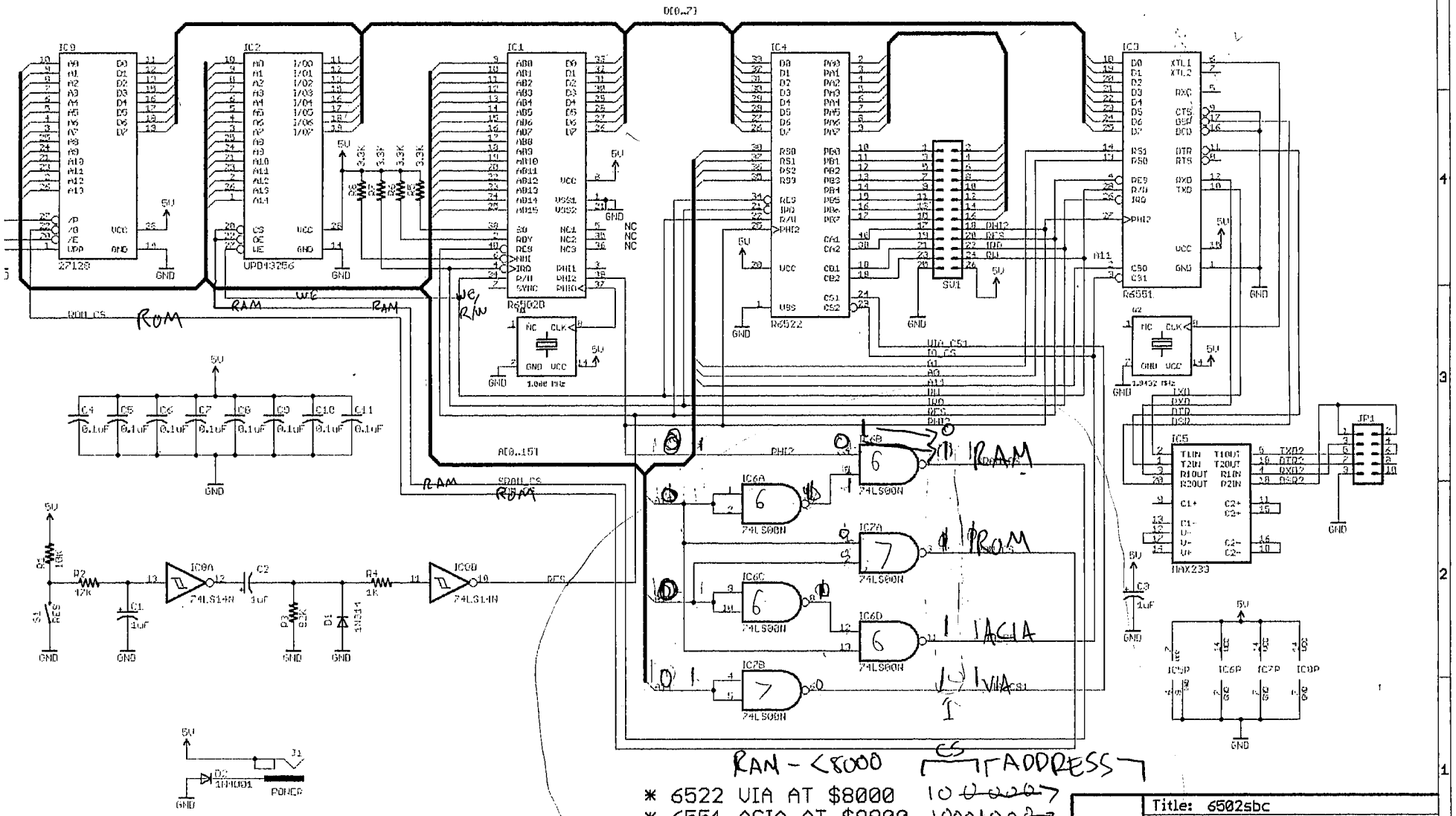
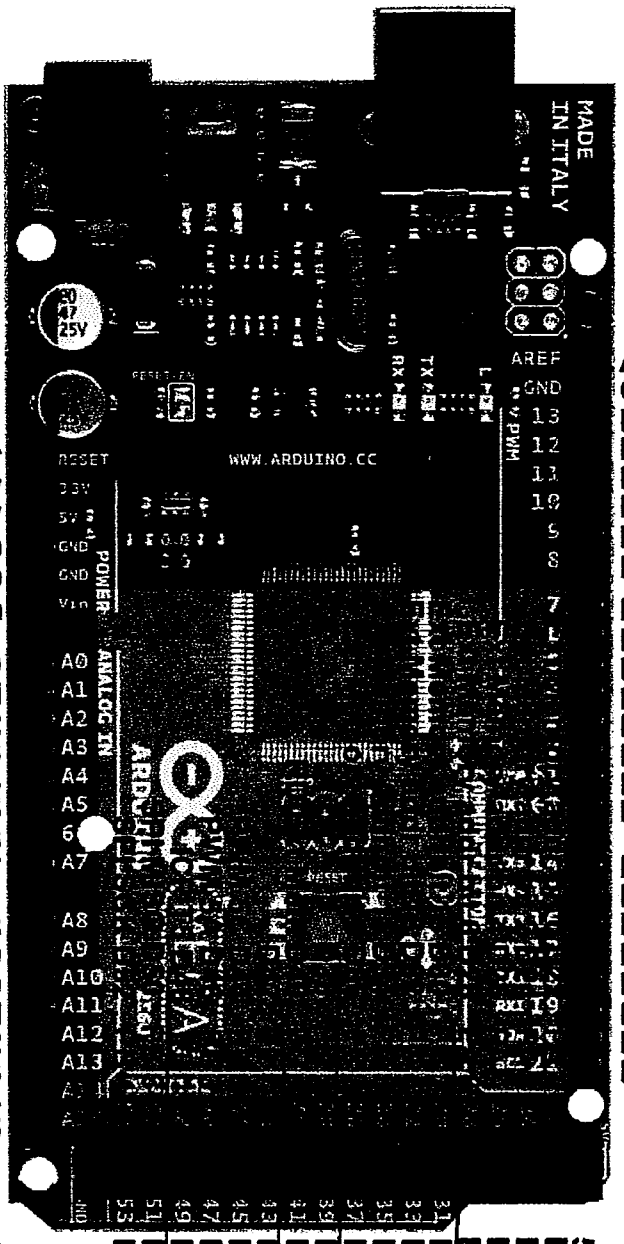
Loom Communications 6502 SBC, v. 1.0.4 (c) 2012



ram is on when A15 is low and Ø2 is low
rom is on when A15 high and A14 high -

Memory test

- $A9 (LDA) - $AA - 10101010
- $8D (STA) $05 $00 — Stor Acc. 0005
- $E6 (INC) $05 — Increment $0005
- $A5 (LDA) $05 — Load back to Acc.
-



AREF
GND
D13 : PB 7 | PWM T0A, Pin Int 7
D12 : PB 6 | PWM T1B, Pin Int 6
D11 : PB 5 | PWM T1A, Pin Int 5
D10 : PB 4 | PWM T2A, Pin Int 4
D9 : PH 6 | PWM T2B
D8 : PH 5 | PWM T4C

D7 : PH 4 | PWM T4B
D6 : PH 3 | PWM T4A
D5 : PE 3 | PWM T3A
D4 : PG 5 | PWM T0B
D3 : PE 5 | PWM T3C, INT5
D2 : PE 4 | PWM T3B, INT4
D1 : PE 1 | USART0 TX
D0 : PE 0 | USART0 RX, pin Int 8

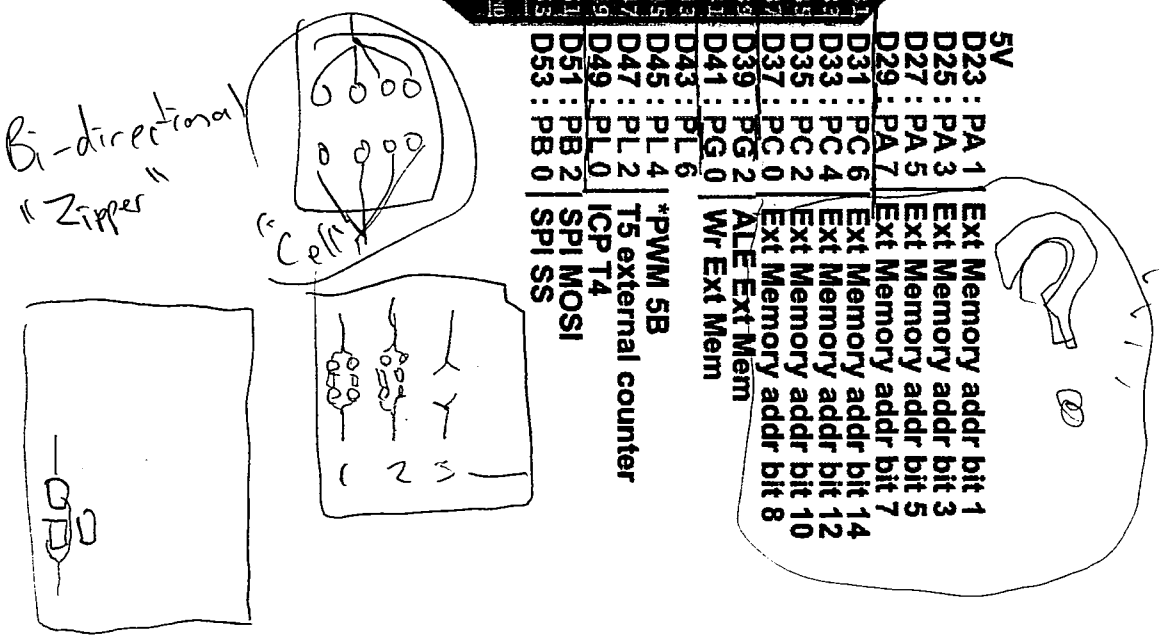
D14 : PJ 1 | USART3 TX, Pin Int 10
D15 : PJ 0 | USART3 RX, Pin Int 9
D16 : PH 1 | USART2 TX
D17 : PH 0 | USART2 RX
D18 : PD 3 | USART1 TX, Ext Int 3
D19 : PD 2 | USART1 RX, Ext Int 2
D20 : PD 1 | I2C SDA, Ext Int 1
D21 : PD 0 | I2C SCL, Ext Int 0

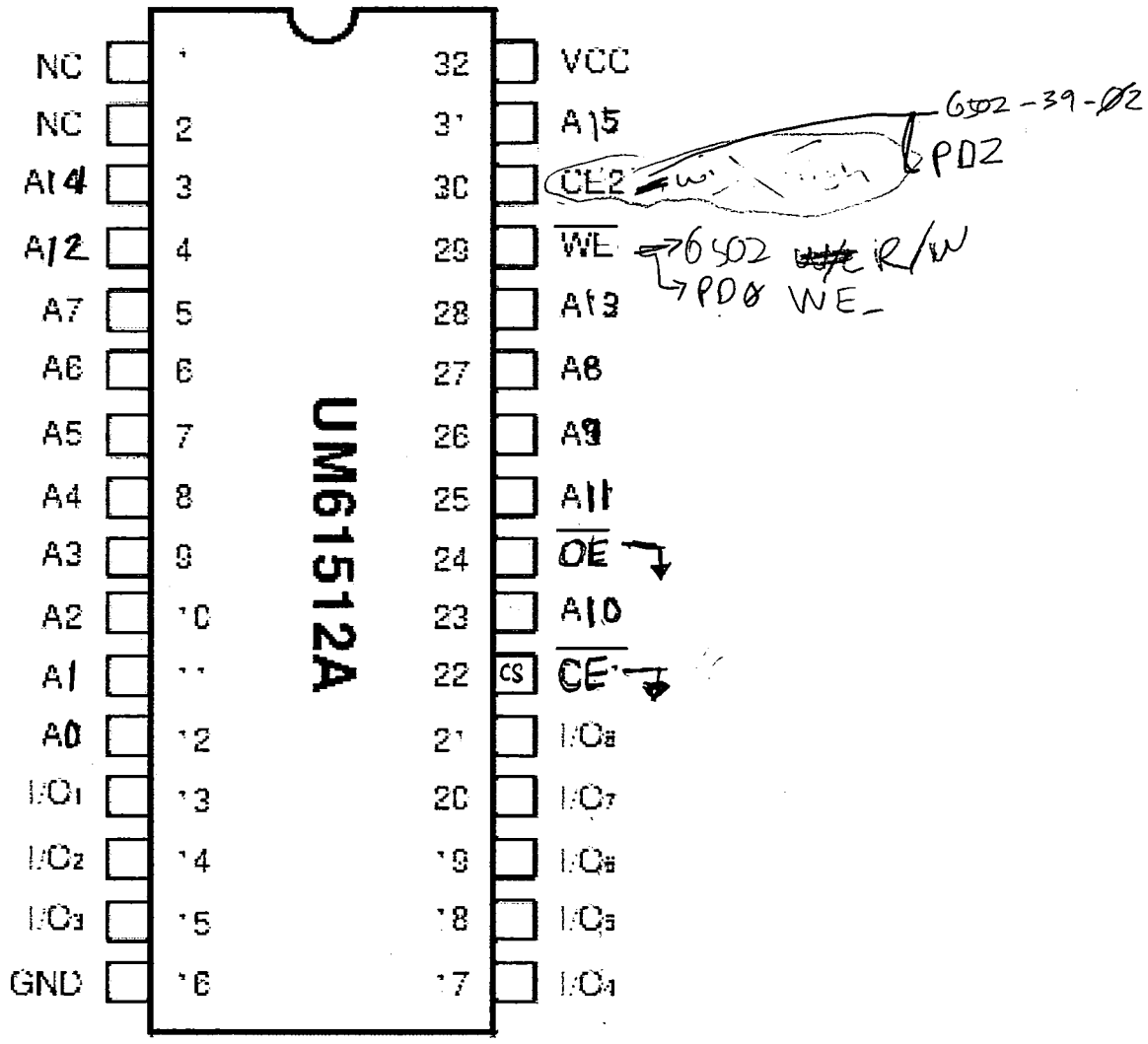
RESET
3.3V
5V
GND
GND
Vin

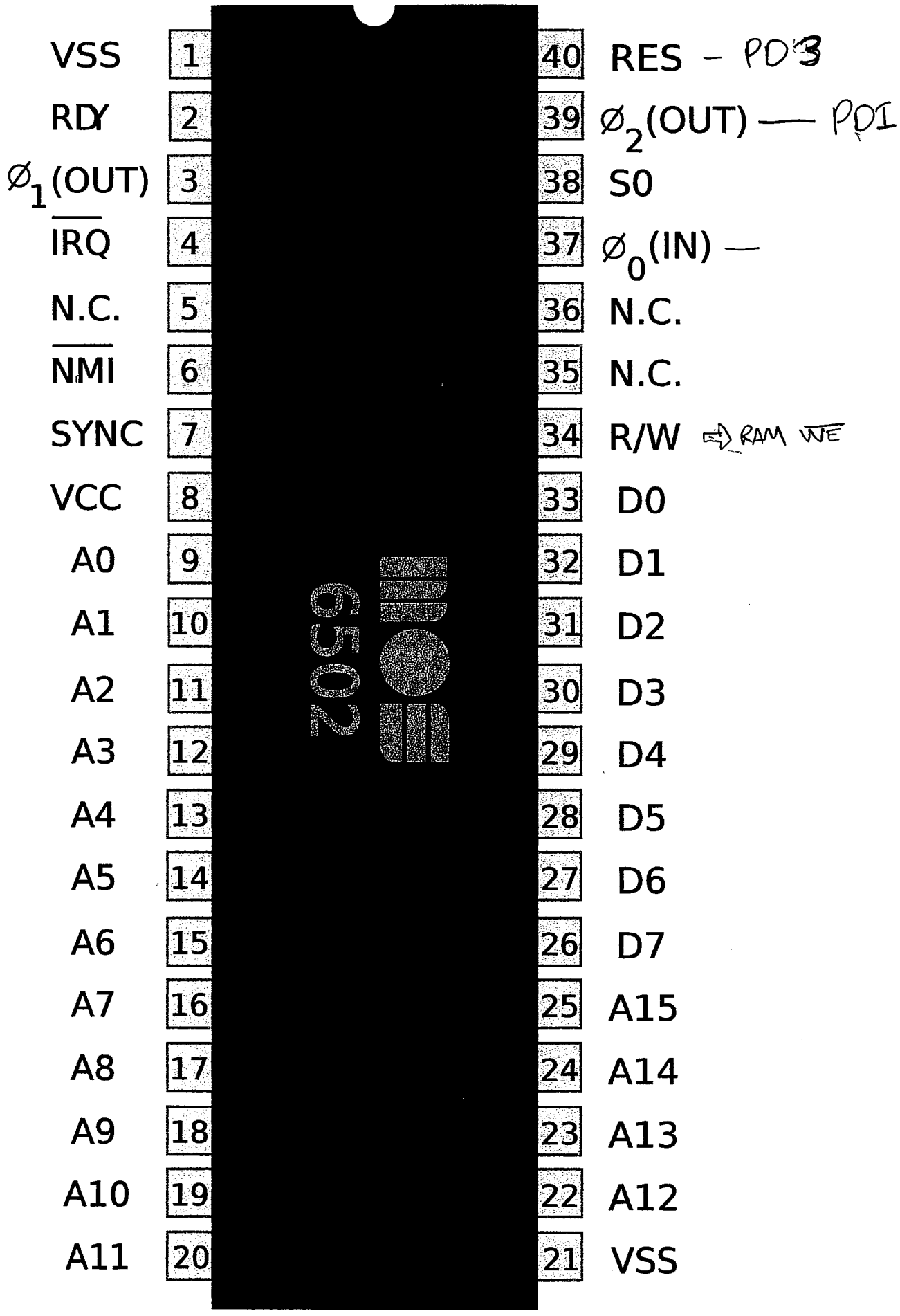
(D54) PF 0 : AIN0
(D55) PF 1 : AIN1
(D56) PF 2 : AIN2
(D57) PF 3 : AIN3
(D58) PF 4 : AIN4
(D59) PF 5 : AIN5
(D60) PF 6 : AIN6
(D61) PF 7 : AIN7

(Pin Int 16) (D62) PK 0 : AIN8
(Pin Int 17) (D63) PK 1 : AIN9
(Pin Int 18) (D64) PK 2 : AIN10
(Pin Int 19) (D65) PK 3 : AIN11
(Pin Int 20) (D66) PK 4 : AIN12
(Pin Int 21) (D67) PK 5 : AIN13
(Pin Int 22) (D68) PK 6 : AIN14
(Pin Int 23) (D69) PK 7 : AIN15

5V
D23 : PA 1 | Ext Memory addr bit 1
D25 : PA 3 | Ext Memory addr bit 3
D27 : PA 5 | Ext Memory addr bit 5
D29 : PA 7 | Ext Memory addr bit 7
D31 : PC 6 | Ext Memory addr bit 14
D33 : PC 4 | Ext Memory addr bit 12
D35 : PC 2 | Ext Memory addr bit 10
D37 : PC 0 | Ext Memory addr bit 8
D39 : PG 2 | ALE Ext Mem
D41 : PG 0 | Wr Ext Mem
D43 : PL 6
D45 : PL 4 | *PWM 5B
D47 : PL 2 | T5 external counter
D49 : PL 0 | ICP T4
D51 : PB 2 | SPI MOSI
D53 : PB 0 | SPI SS

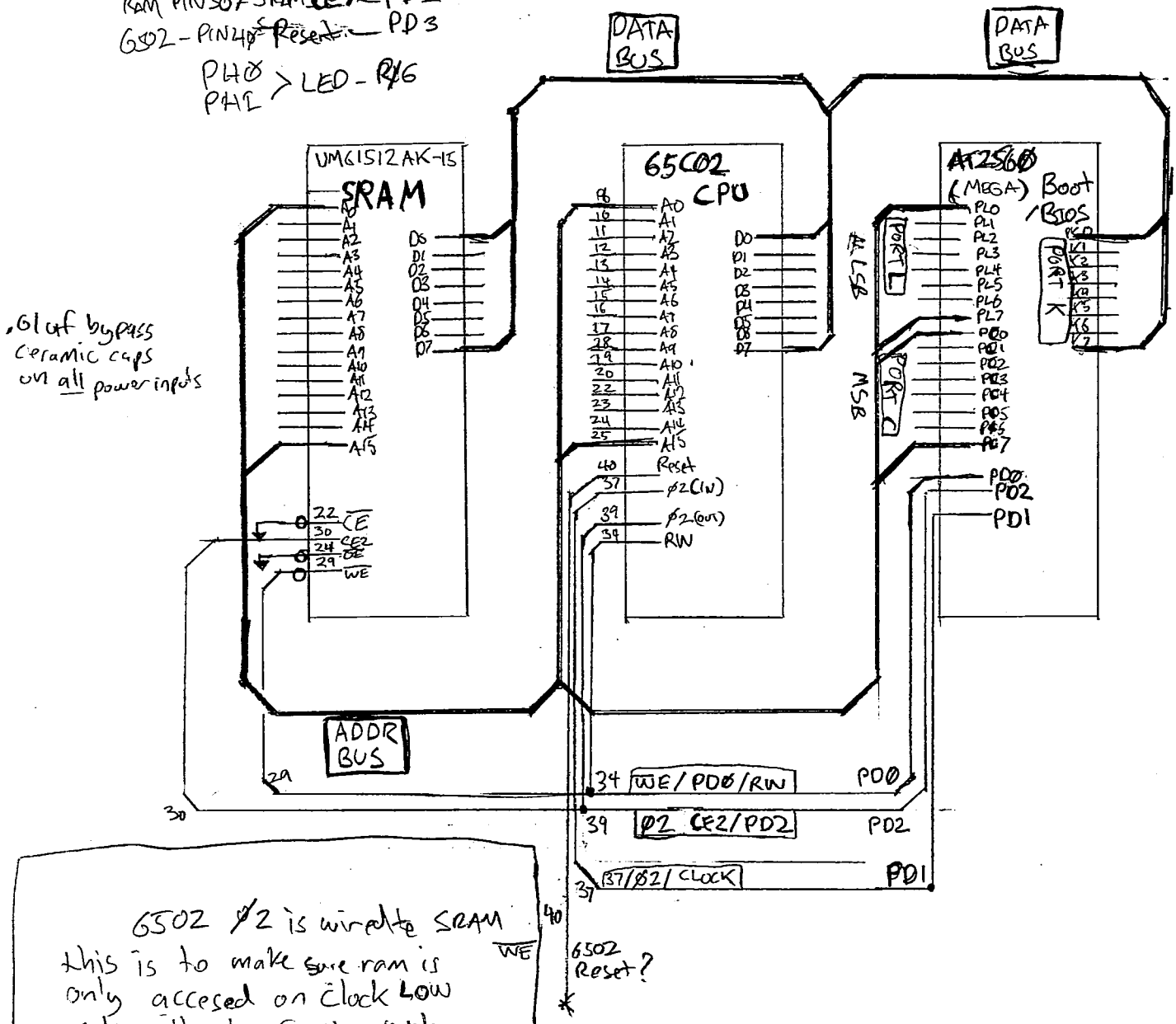



UM61512A
NC 1
NC 2
A14 3
A12 4
A7 5
A6 6
A5 7
A4 8
A3 9
A2 10
A1 11
A0 12
I/O1 13
I/O2 14
I/O3 15
GND 16
32 VCC
31 A15
30 CE2
29 WE
28 A13
27 A8
26 A9
25 A11
24 OE
23 A10
22 CS CE
21 I/O8
20 I/O7
19 I/O6
18 I/O5
17 I/O4
6502-39-02
PD2
6502 R/W
PD0 WE_


VSS 1
RDY 2
Ø1(OUT) 3
IRQ 4
N.C. 5
NMI 6
SYNC 7
VCC 8
A0 9
A1 10
A2 11
A3 12
A4 13
A5 14
A6 15
A7 16
A8 17
A9 18
A10 19
A11 20
40 RES - PD3
39 Ø2(OUT) — PD1
38 S0
37 Ø0(IN) —
36 N.C.
35 N.C.
34 R/W ⇨ RAM WE
33 D0
32 D1
31 D2
30 D3
29 D4
28 D5
27 D6
26 D7
25 A15
24 A14
23 A13
22 A12
21 VSS
6502

"Kernel Splatter Rev 0001"
Keith Legg, Dec 28, 2015

From bootloader.c -
RAM PIN28 WE — PD0
6502 CLK — PD1
RAM PIN30/SRAM ~~CE1~~ — PD2
6502 - PIN40 ~~Reset~~ — PD3
PH0 / PH1 > LED - R/G



6502 Ø2 is wired to SRAM ~~WE~~ this is to make sure ram is only accesed on clock LOW pulse. thanks Garth Wilson for that tip.

* reset is not currently controlled in software - the switch to Hi-Z seems to sufice but a better circuit is needed.