CS4110 Assignment 1 Report

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August 13, 2017

1 System Configurations

	System 1	System 2
Processor	2xCore i5-4200M @2.50Ghz	2xCore i5-4210U @2.70Ghz
L1d cache	32K	32K
L1i cache	32K	32K
L2 cache	256K	256K
L3 cache	3072K	3072K
RAM	16GB DDR3	8GB DDR3

Table 1: System Configurations

2 Observations

	Scenario #1		Scenario #2	
Event	System 1 Values	System 2 Values	System 1 Values	System 2 Values
Average Runtime(in ms)	9,521.99	10,956.67	563.62	606.04
CPU-cycles	28,309,836,428	27,619,082,088	1,746,565,867	1,646,140,523
No. of Instructions	7,606,471,119	7,616,154,025	4,174,417,418	4,129,854,611
branch-instructions	1,106,522,257	1,107,742,014	303,108,887	298,103,829
cache-references	102,350,340	95,237,452	16,970,863	24,531,642
cache-misses	76,696,819	67,074,605	10,415,072	10,746,780
L1-dcache-loads	3,233,709,007	3,252,081,137	835,800,684	842,473,119
L1-dcache-load-misses	1,686,239,462	1,686,087,796	70,760,708	70,676,397
dTLB-loads	3,211,014,395	3,241,702,482	831,961,558	839,799,886
dTLB-load-misses	1,053,525,175	1,052,939,970	1,513,147	1,378,370
LLC-loads	100,400,762	94,023,020	17,751,205	25,035,964
LLC-load-misses	76,246,912	66,716,165	11,089,960	10,954,286

Table 2: Observations for the two Scenarios

3 Conclusions

It is evident from the average runtime that scenario #2 is more efficient as the entire columns of the right operand matrix during multiplication is already loaded into the cache. Scenario #1 has around 70-75% cache misses whereas Scenario #2 has around 45-60% cache misses only.

Scenario #1 is more efficient for operations like matrix addition, matrix subtraction etc. where the operations are row-wise in both the operand matrices.

Scenario #2 is more efficient in matrix multiplication where the operation is row-wise in the left operand and column-wise in the right operand.

For both system configurations, Scenario #2 is more efficient.