Document on Assignment#2 Output

Opcode for Registers

R0 -- 0000
R1 -- 0001
R2 -- 0010
….
R15 -- 1111

Opcode for Instructions

ADD -- 0000
SUB -- 0010
MUL -- 0110
If an instructions has an immediate operand then set LSB of opcode is set to 1.
For example, opcode of the instruction **ADD R1, R0, #5** is 000**1**000100000101

LD -- 1000
SD -- 1010
JMP -- 1100 (unconditional jump)
BEQZ -- 1101 (conditional jump)
HLT -- 1110

Test Case #1: Swap the two numbers after doubling
//Register File initialization. $Register Name$Contents
$R2$600
$R3$800
// Memory initialization. $Memory Location$ Value
$600$55
$800$44
// Assembly Code
LD R4 R0[R2]
LD R5 R0[R3]
ADD R6 R4 R4
ADD R7 R5 R5
SD R0[R2] R7
SD R0[R3] R6
HLT

Output File(Test Case #1):
//Code Segment: // $Memory Location$opcode for the instruction

$000$1000010000000010 // LD R4 R0[R2]
$002$1000010100000011 // LD R5 R0[R3]
$004$0000011001000100 //ADD R6 R4 R4
$006$0000011101010101 //ADD R7 R5 R5
$008$1010000000100111 //SD R0[R2] R7
$010$1010000000110110 //SD R0[R3] R6
$012$1110000000000000 // HLT

//Data Segment : $Memory Location$Data
$600$0000000001011000 // 88
$800$0000000001101110 //110