CS4110 Assignment 2 Report

Rahul Kejriwal, CS14B023
Abinash Patra, CS14B032

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1 System Configurations

	System 1
Processor	2xCore i5-4200M @2.50Ghz
L1d cache	32K
L1i cache	32K
L2 cache	256K
L3 cache	3072
RAM	16GB DDR3
L3 Cache block size (B)	64 bytes
L3 No. of Cache Sets (N)	4096
L3 associativity (A)	12

Table 1: System Configurations

2 Observations

2.1 Address Translation Policy

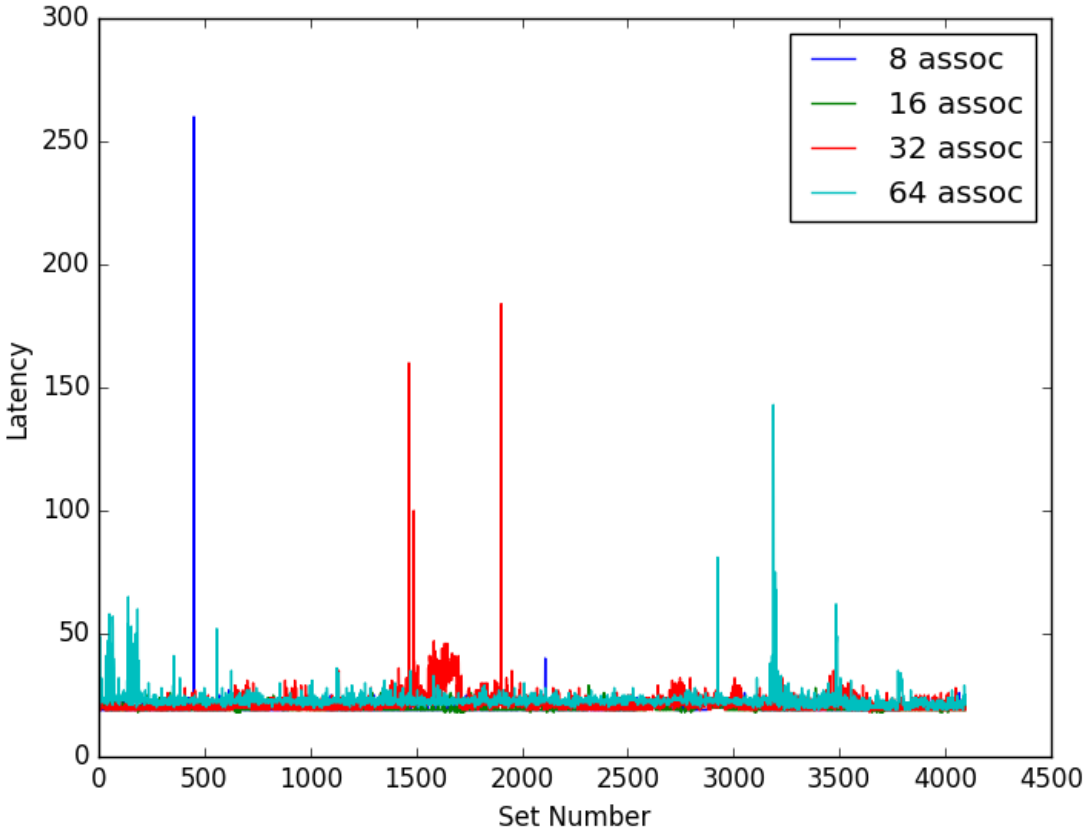

Figure 1: Latency vs Cache Set for different associativity

From the graph, we should have observed the curves for associativity above 12 in the around 200 cycles range. However, all of them appear to be in the same 20-30 cycles range with spikes in between.

From this we can conclude that the address translation policy **does not follow** the rule:

> **Rule 1:** *The addresses that differ by* $n * W$ *(n is nonzero integer) are located at the same set, different ways.*

The tag bits in our cache are not the MSB bits of the memory address. We need more information about the TAG bits from which we can get the appropriate W' size to repeatedly access same cache set.

Trying to find experimentally which bits are TAG bits and which are index bits is intractable for a 64-bit machine as we show now. Our cache block size (B) is 64 bytes meaning 6-bits from the 64-bit addresses are for offset. Of the remaining 58 bits, 12 bits are for index (since there are N=4096 cache sets). We are uncertain of the position of these 12 bits which can occur in $\binom{58}{12} = 8.91 * 10^{11}$. Each of these possible positioning of TAG bits, would give rise to a different value of W' (indeed multiple values of W' will exist for same positional configuration). In order to try out all these possible values where each such value would require around 5 seconds to execute is $5 * 8.91 * 10^{11}\ seconds = 1412\ centuries$ which is clearly intractable.

2.2 Cache Replacement Policy

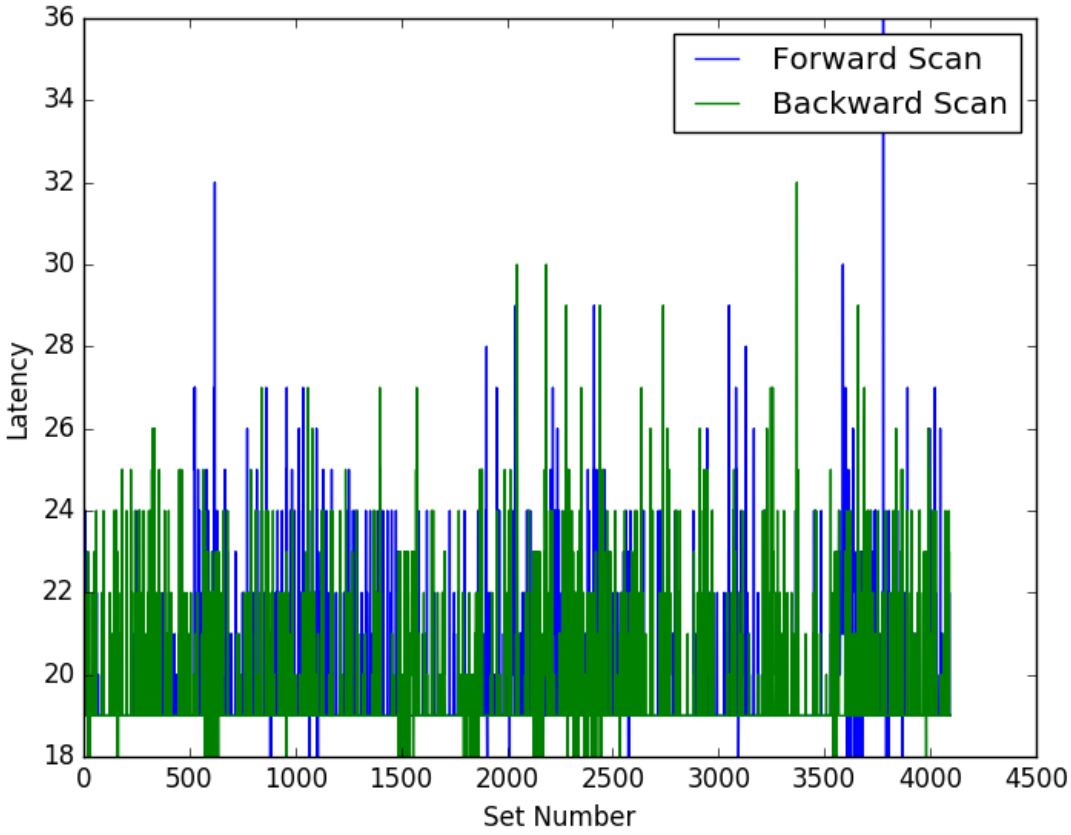

Figure 2: Latency vs Cache Set for forward and backward scans

Since, we do not know the correct value of W', this experiment is meaningless and cannot be interpreted.