ELEC ENG – 2EI4

Design Project #5

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Summary

The purpose of Design Project #5 is to design, simulate, and build a 3-bit Digital-to-Analog converter featuring a full-scale analog voltage, V_{FS} = 5 V. The design of the Digital-to-Analog converter features three digital input bits, the weights of these bits are determined from the ratio of full-scale analog voltage to the number of possible digital values for each of the bits. This allows for a proportionality between the output voltage and the sum of the input bits with their corresponding weights. The design features a network of transistors connected to a resistive network then, connected to an inverting unity-gain buffer.

Design

Circuit Diagram

In Figure 1 shown below, the circuit diagram is demonstrated.

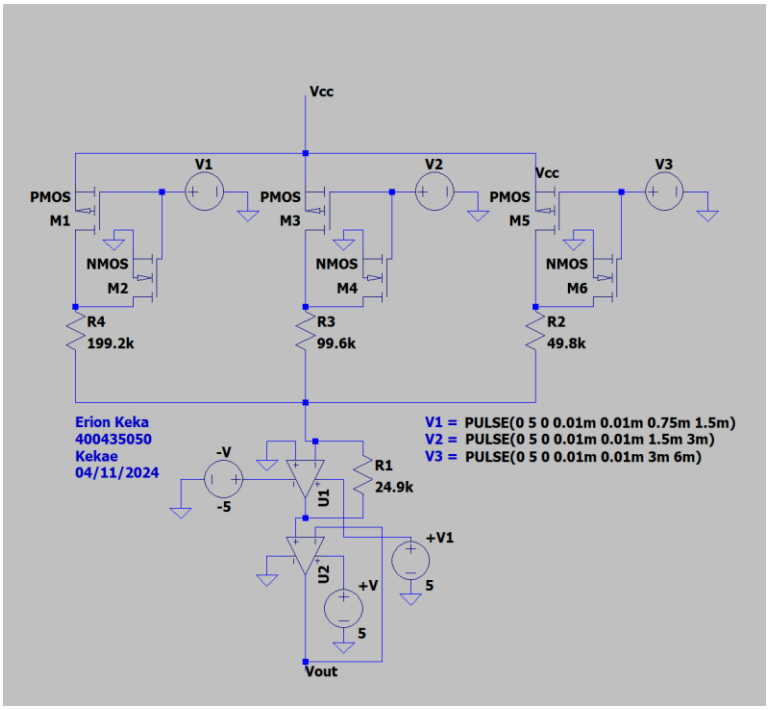

Figure 1: Circuit Diagram

Circuit Description

The Digital-to-Analog circuit diagram converts a digital input signal into an analog output voltage. In particular, the circuit is a weighted resistor Digital-to-Analog converter. This is done by creating a resistive network, the weights for these resistors are determined

as it being proportional to the binary value of the corresponding bit. This is expressed below in the calculations. When an input is inputted into the Digital-to-Analog circuit, the input is converted into an analog output, this analog output is proportional to the sum of the products of each of the input bits and the weights of the corresponding resistors. Within the circuit, there is also an inverting unity-gain buffer present. This is an op-amp circuit that can invert the signal output from the Digital-to-Analog circuit, it also provides a gain of one expressed in its name. The inverting unity-gain buffer works by isolating the output of the circuit. It prevents the effects of loading which occurs when a portion of the circuit draws more circuit in comparison to the rest of the circuit. By preventing these negative effects, we are improving the accuracy of the circuit. In short, the circuit takes a digital input then converts it to analog through the weighted resistor Digital-to-Analog conversion then, the output is buffered using the inverting unity-gain buffer.

Calculations

R_{REF} = 24.9k OHMs, this value was chosen arbitrarily to allow for higher resistor values within the circuit and such that the resistors are within the specified component kits.

$R_1 = 2^0(R_{REF}) = R_{REF}$ = 24.9k OHMs

$R_2 = 2^1(R_{REF})$ = 49.8k OHMs

$R_3 = 2^2(R_{REF})$ = 99.6k OHMs

$R_4 = 2^3(R_{REF})$ = 199.2k OHMs

References

[1] “Digital to analog converters - analog and digital electronics course,” s, https://electronics-course.com/digital-analog-converter#:~:text=A%20digital%2Dto%2Danalog%20converter,bits%20or%20its%20step%20size. (accessed Apr. 11, 2024).

[2] “Digital to analog converters,” Tutorialspoint, https://www.tutorialspoint.com/linear_integrated_circuits_applications/linear_integrated_circuits_applications_digital_to_analog_converters.htm (accessed Apr. 11, 2024).

[3] W. Storr, “Binary weighted digital to analogue converter,” Basic Electronics Tutorials, https://www.electronics-tutorials.ws/combination/digital-to-analogue-converter.html (accessed Apr. 11, 2024).

Measurement and Analysis

Physical Circuit

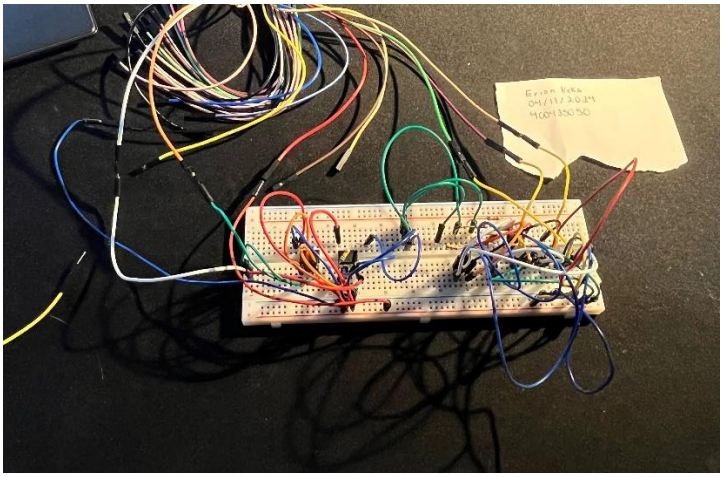

Figure 2: Physical Circuit

Digital Inputs

To test the circuit, digital inputs needed to be configured. To configure these inputs, the patterns functionality within the Waveforms software was utilized. The configuration for the inputs is demonstrated below. The supplies were also utilized to supply +/- 5 V to the operational amplifiers. In addition, the oscilloscope was utilized to measure the output of the Digital-to-Analog circuit.

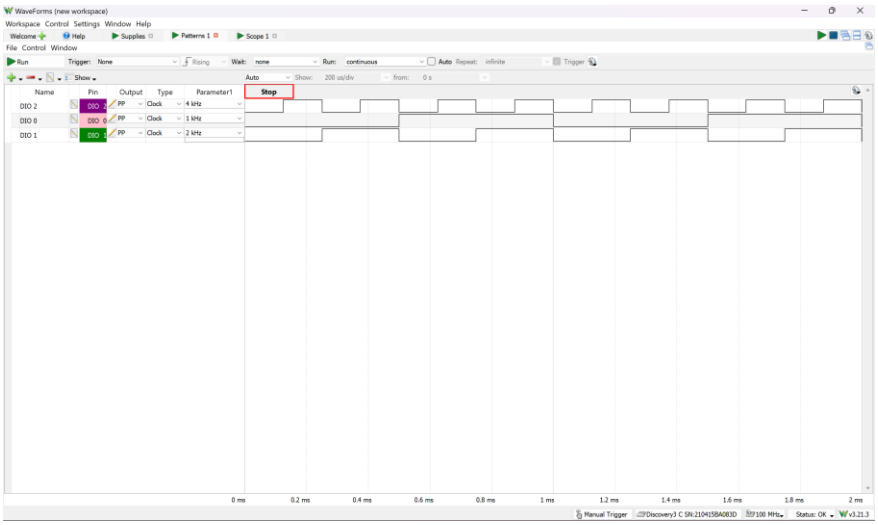

Figure 3: Digital Input Configuration (Pattern Generator)

Transfer Characteristics

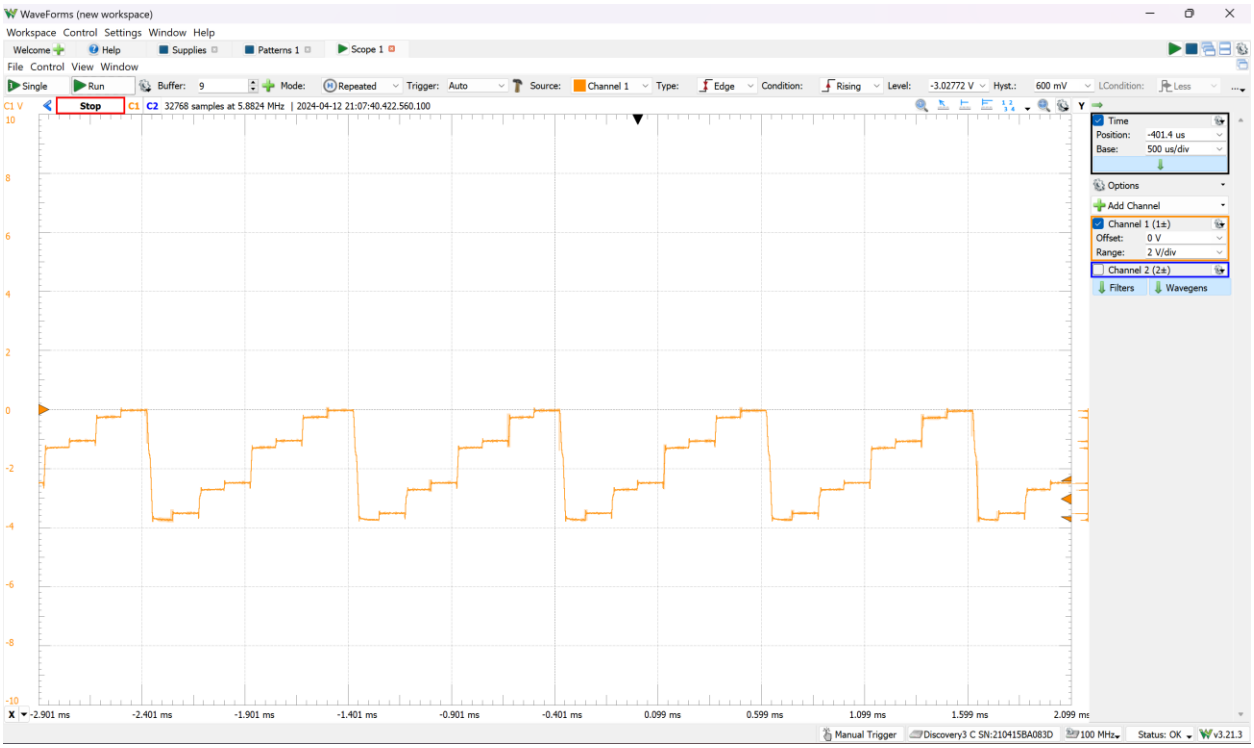

Figure 4: Transfer Characteristics – Digital-to-Analog Output (Orange)

From the graph shown above, we can see the transfer characteristics.

Gain Error

The gain error is the deviation of the experimental from the expected gain, it is a measure to indicate the accuracy of the amplification of the circuit. To calculate the gain error, we will determine the difference amongst the expected peak voltage and the measured peak voltage and dividing by the expected peak voltage. Since the graph is flipped, I will take the peak voltage to be the absolute value of the minimum voltage. This could be resolved by applying an offset to the output. From this knowledge, we can calculate the gain error to be $Error = \frac{V_{Expected} - V_{Measured}}{V_{Expected}} = \frac{5\ V - 3.95\ V}{5\ V} = 21\%$. This unfortunately does not pass the test, issues that caused this failure are discussed below.

Maximum Differential Non-Linearity

The maximum differential non-linearity is used to indicate how well the Analog-to-Digital converter can maintain an equal step size. To calculate the maximum differential non-linearity, we need to determine the ideal voltage. The ideal voltage is the voltage per step. This is calculated from the total voltage divided by the total number of steps, $V_{Ideal} =$

$\frac{V_{FS}}{\#\ of\ Steps} = \frac{5\ V}{8\ Steps} = 0.625\ V$. Now upon determining the ideal voltage, we can determine the maximum differential non-linearity by determining the difference between the ideal voltage and the measured step voltage divided by the ideal voltage. $MDNL = \frac{|V_{Ideal} - V_{Measured}|}{V_{Ideal}} = \frac{|0.625\ V - 0.767\ V|}{0.625\ V} = 22.7\%$. Once again, we are able to see that this error percentage is very large. There are many issues that can lead to this which are discussed below.

Offset Error

The offset error present in my circuit is found to be 4.89735 V. This was calculated by taking the known / given V_{FS} = 5 V and subtracting by the maximum voltage from the Waveforms output which is 0.10265 V. This gives the offset error. This value represents the accuracy of the output of the Analog-to-Digital conversion. It demonstrates the difference between output of Analog-to-Digital conversion and the expected value. This value must be minimized to ensure accuracy within the conversion.

Discussion

Origin of Various Errors

The origin of the errors that were found upon analyzing the output of the circuit were caused by many various factors. These factors can consist of faulty connections from the wires, output limitations from the AD3, and resistor values. The faulty connections from the wires within the circuit created noise that had an impact on the output of the circuit. In addition, the output limitations of the AD3, in specific, the output limitations of the Digital I/O is limited to 3.3 V which is not the 5 V input that is needed for the circuit as specified in the project manual. Subsequently, the limitation of only being allowed to use the 2CI4 and 2EI4 components kits created errors in the output. This limitation created an error because if we were not limited to these kits, I would have chosen values that are a lot higher to ensure that the output of the circuit is more accurate.

Different Implementation

Another method of implementing an Analog-to-Digital converter can be done without including a set of transistors as in my circuit. The Analog-to-Digital converter can solely be constructed with the operational amplifiers excluding the transistors. I chose my design over the design that excludes the transistors because by including the transistors, we can condition the analog input prior to it being transformed into a digital output. The group of transistors allows for a high input impedance and lower output impedance to help

preserve the integrity of the input signal. By eliminating the group of transistors, we will remove this conditioning and our output signal will be less accurate. A drawback of including the group of transistors is the augmented cost to build the circuit; however, this drawback is minor in comparison to the benefit. As a result, I have chosen to include the transistors in my design.