ELEC ENG – 2EI4

Design Project #4

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Circuit Schematic

To determine the circuit schematic for the MOSFET based XOR gate, Boolean algebra and DeMorgan's Theorem were applied. The final circuit schematic that was decided upon consisted of a total of 12 MOSFETs. These 12 MOSFETs consisted of 6 P-MOS and 6 N-MOS.

$$Y = A \oplus \mathrm{B}$$
$$Y = \bar{A}B + \bar{B}A$$
$$Y = \overline{\bar{A}B + \bar{B}A}$$
$$Y = \overline{(A + \bar{B}) \cdot (B + \bar{A})}$$
$$Y = \overline{AB + \overline{A}\overline{B}}$$

From the finalized equation, $Y = \overline{AB + \overline{A}\overline{B}}$, it is noted that the circuit schematic will be a pull-down network where A will be in series with B, $\bar{A}$ is in series with $\bar{B}$. Then, these two terms will be in parallel with one another. The pull-up network will be implemented by mirroring the pull-down network using P-MOS transistors, the parallel networks will be converted into series networks whilst, the series networks are converted into parallel networks. The finalized circuit schematic for the CMOS XOR gate circuit makes use of 12 MOSFETs. The pull-down network will make use of 4 N-MOS transistors and the pull-up network makes use of 4 P-MOS Networks. Two additional CMOS inverters must be included in the circuit for the inputs $\bar{A}$ and $\bar{B}$. Each inverter features one P-MOS and one N-MOS transistor. This takes us to a total of 12 MOSFETs, 6 P-MOS and 6 N-MOS transistors.

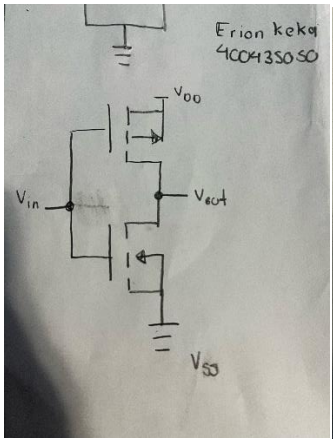

Figure 1: The CMOS XOR Gate

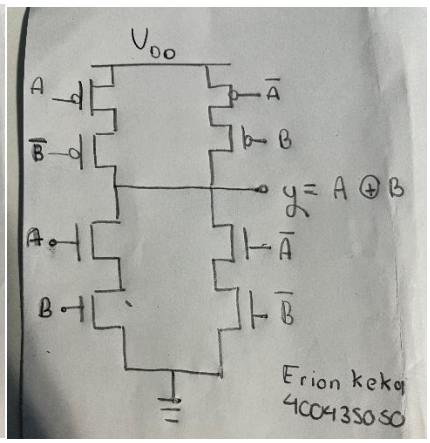

Figure 2: The CMOS Inverter

Ideal Sizing

It has been assumed that the average sizing for the P-MOS transistor is $(\frac{W}{L})_P = \frac{5}{1}$ and for the N-MOS transistor is $(\frac{W}{L})_N = \frac{2}{1}$ for all the MOSFETs. The conduction by holes performed in P-MOS transistors is substantially slower than the conduction by electrons performed in N-MOS transistors. The N-MOS transistors are faster by a factor of 2.5 — electron mobility ratio of electrons to holes. As we travel through the longest path in the circuit previously constructed, it can be noted the longest path in the pull-down network must travel through two MOSFETs whilst, the longest path in the pull-up network must also travel through two MOSFETs. In the pull-up network, R_{EQ} for the path is determined to be $\frac{p}{2}$ and in the pull-down network, R_{EQ} for the path is determined to be $\frac{n}{2}$. Making use of this information, we can conclude that the ideal sizing ratio can be determined to be $\frac{2(P-MOS)}{2(N-MOS)} = \frac{5}{2}$.

Circuit Feasibility

To determine whether the ideal sizing can be implemented within our hardware design, we must examine the circuit. From the circuit, we can deduce that the longest path that traverses from VDD to GND must pass through a total of 2 P-MOS transistors and 2 N-MOS transistors. From this, we can calculate the sizing for this circuit through $\frac{2(P-MOS)}{2(N-MOS)} = \frac{5}{2}$. Since this aligns with the calculated ideal sizing ratio, it is possible to implement the ideal sizing within the circuit.

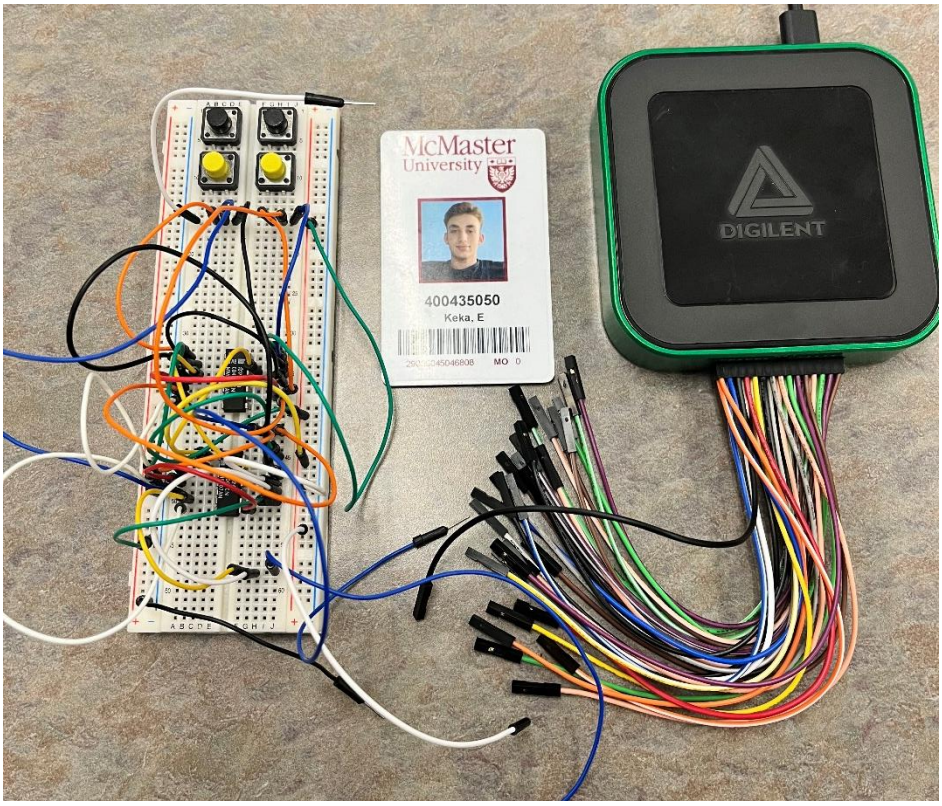

Figure 3: Physically Built Circuit

Functional Testing

Upon performing the functional testing utilizing the AD3 specifically the Digital IO pins, we can verify the truth table of the XOR gate as demonstrated below.

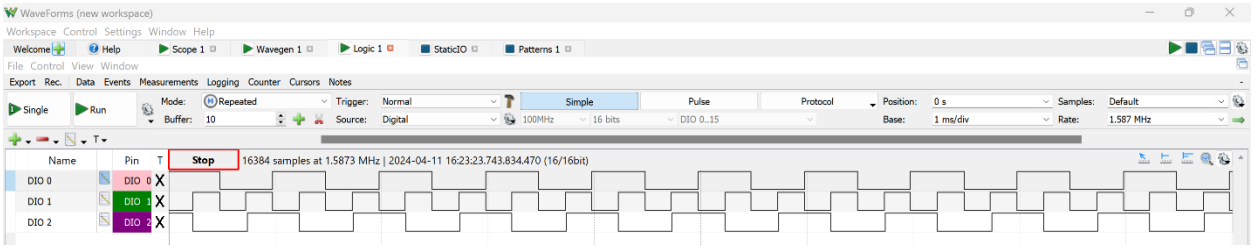

Figure 4: Functional Testing - Matches XOR Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Figure 5: Truth Table for XOR Gate

Static Level Testing

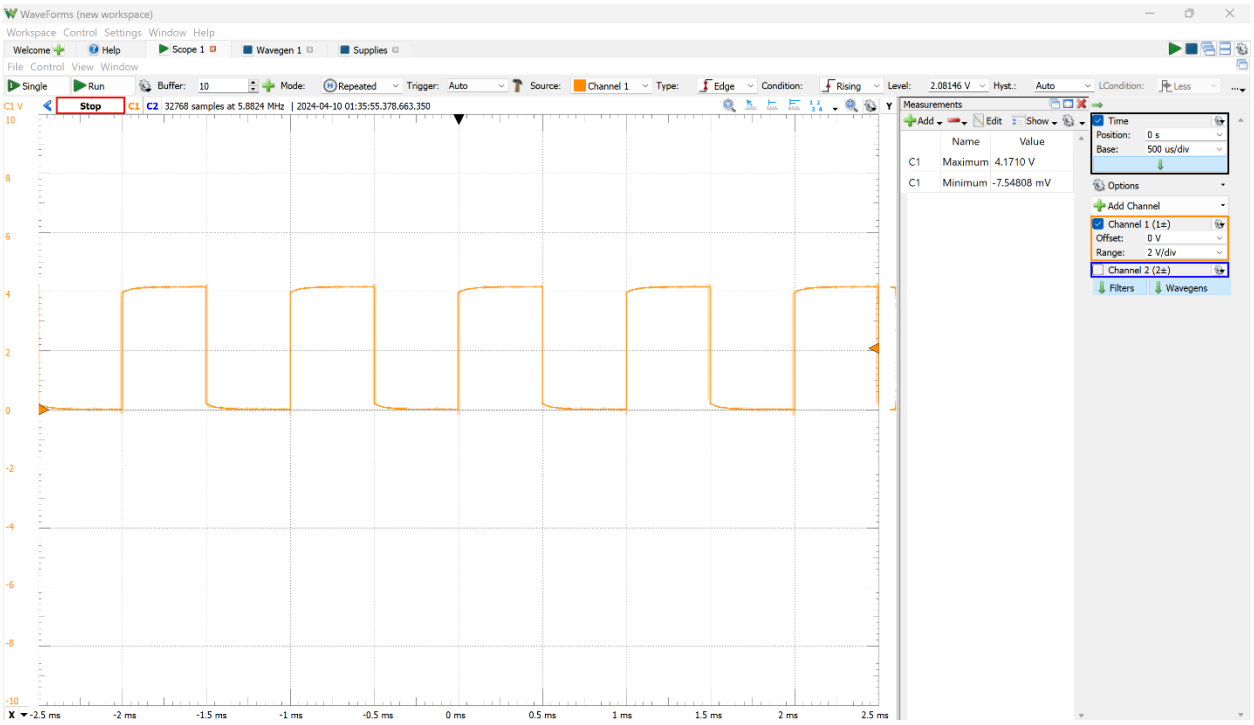

Figure 6: Initial Static Level Testing: Input A = 5 V, Input B = 0-5 V Square Wave

In the initial testing, we find $V_H = 4.1710\ V\ and\ V_L = -7.54808\ mV$.

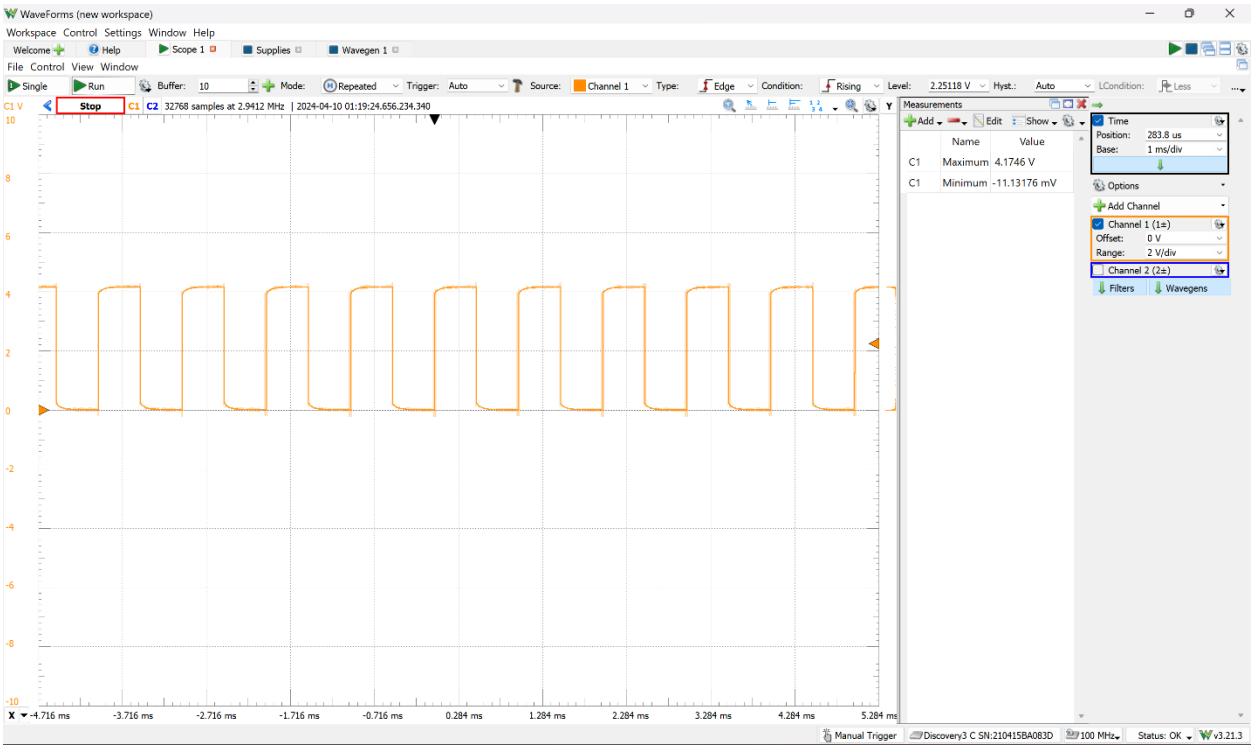

Figure 7: Secondary Static Level Testing: Input A = 0-5 V Square Wave, Input B = 5 V

In the secondary testing, we find $V_H = 4.1746\ V\ and\ V_L = -11.13176\ mV$.

The measurements from the two graphs are relatively similar. The value of V_H features a percent difference of approximately 0.086% whereas the value of V_L features a percent difference of approximately 38%. The differences present in V_L arise due to the poor connection of the wires utilized. The following formula was utilized to calculate the percent difference: $\%diff = \frac{|V_1 - V_2|}{[\frac{(V_1+V_2)}{2}]}$.

Timing

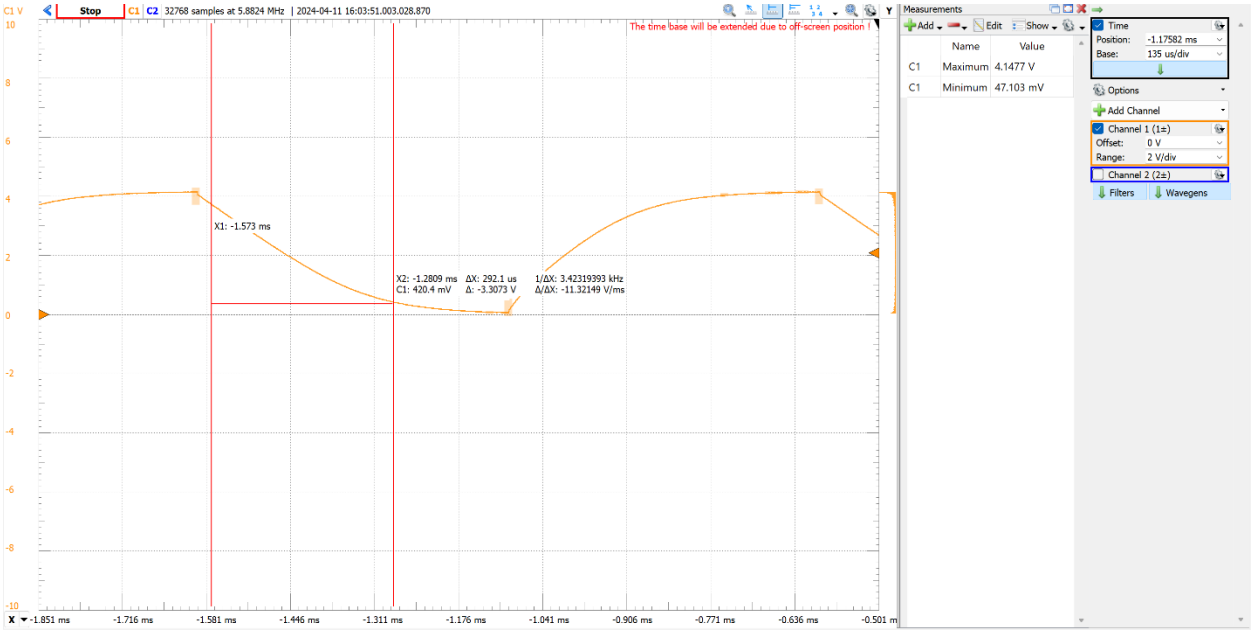

Figure 8: Graph of Fall Time

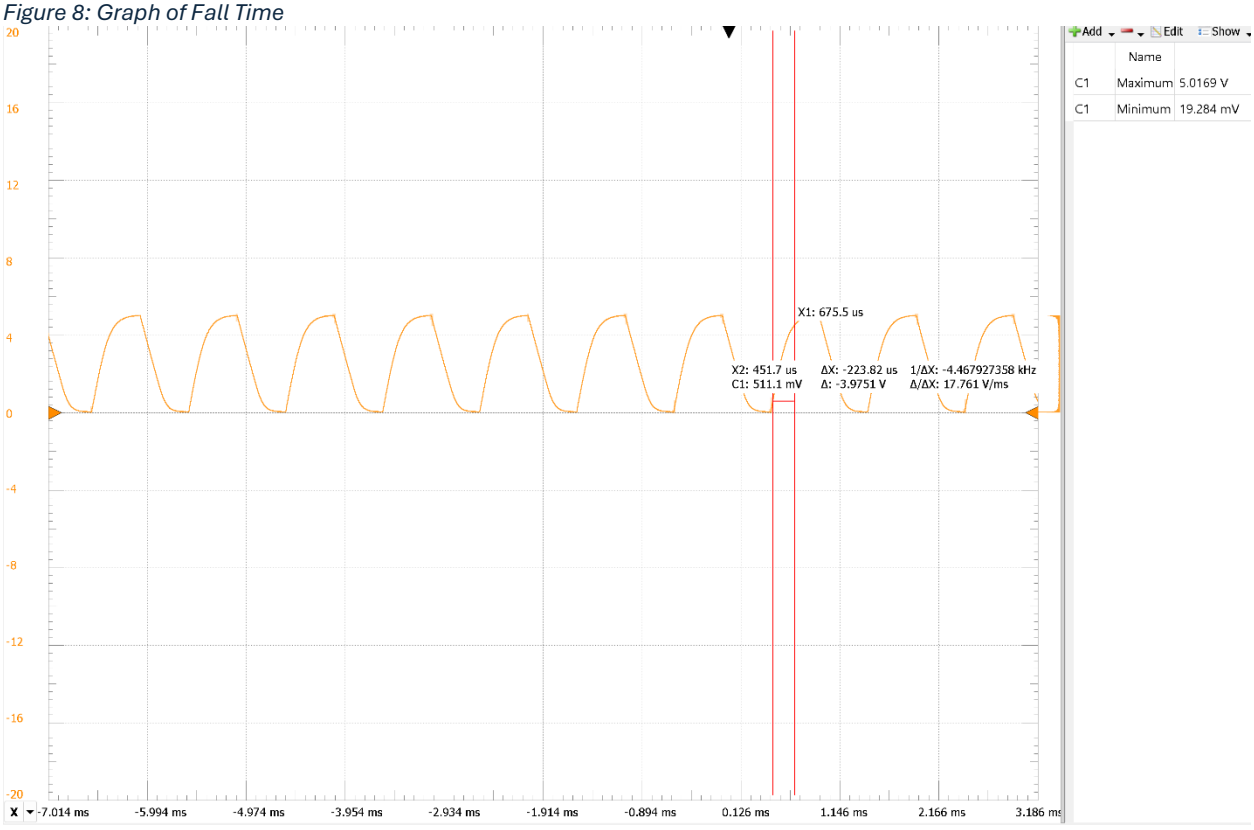

Figure 9: Graph of Rise Time

Making use of the cursors in the AD3, we can find the rise time and fall time of the XOR gate output by taking 90% of the maximum and 10% of the minimum then determining the difference between these points. Here the fall time is determined to be 292.1 us and the rise time is determined to be 223.82 us.

From these two graphs and values, we can determine the τ_{ref} = 4.16(100nF) = 4.16 x 10^{-7} s. Whereas τ_{PHL} = 0.5(223.8 us) = 111.9 us and τ_{PLH} = 0.5(292.1 us) = 146.05 us. From this, we can determine τ_P = 0.5(τ_{PLH}+ τ_{PHL}) = 128.975 us.

Bonus – Secondary Design

Circuit Schematic

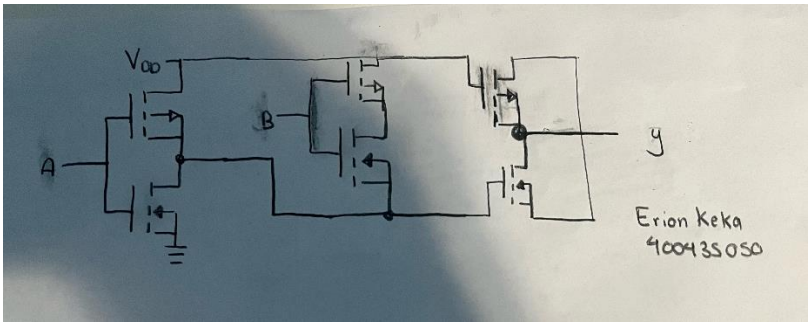

Figure 10: Circuit Schematic - BONUS

Physical Circuit

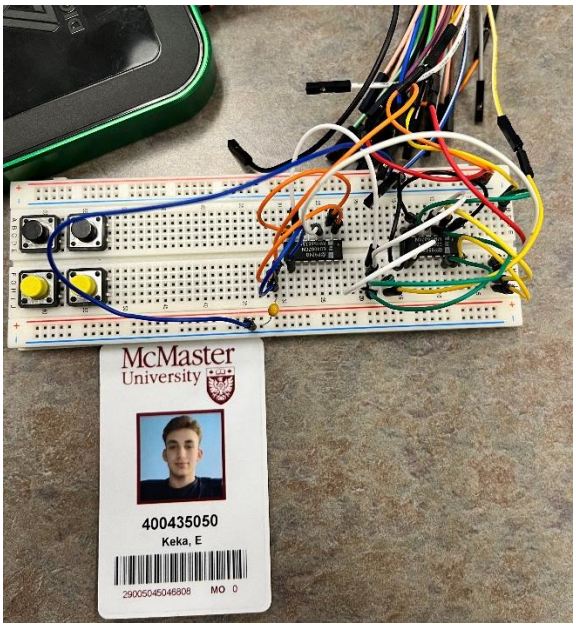

Figure 11: Physically Built Circuit

Functionality Testing

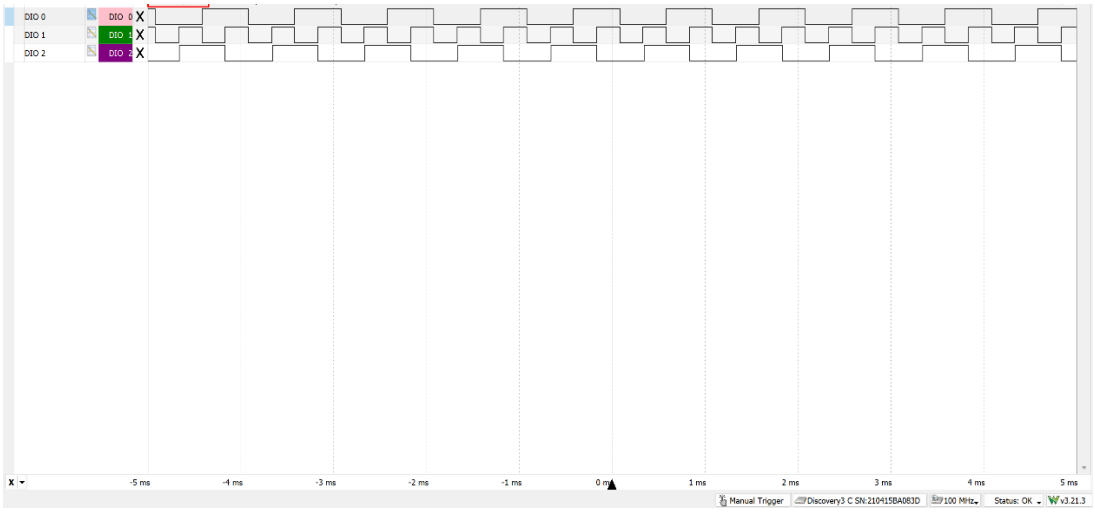

Figure 12: Functional Testing - Matches XOR Truth Table

Once again, upon performing the functionality testing using the Digital IO pins on the AD3, we find that the circuit matches the truth table of an XOR gate. This also matches the initial circuit design.

Static Level Testing

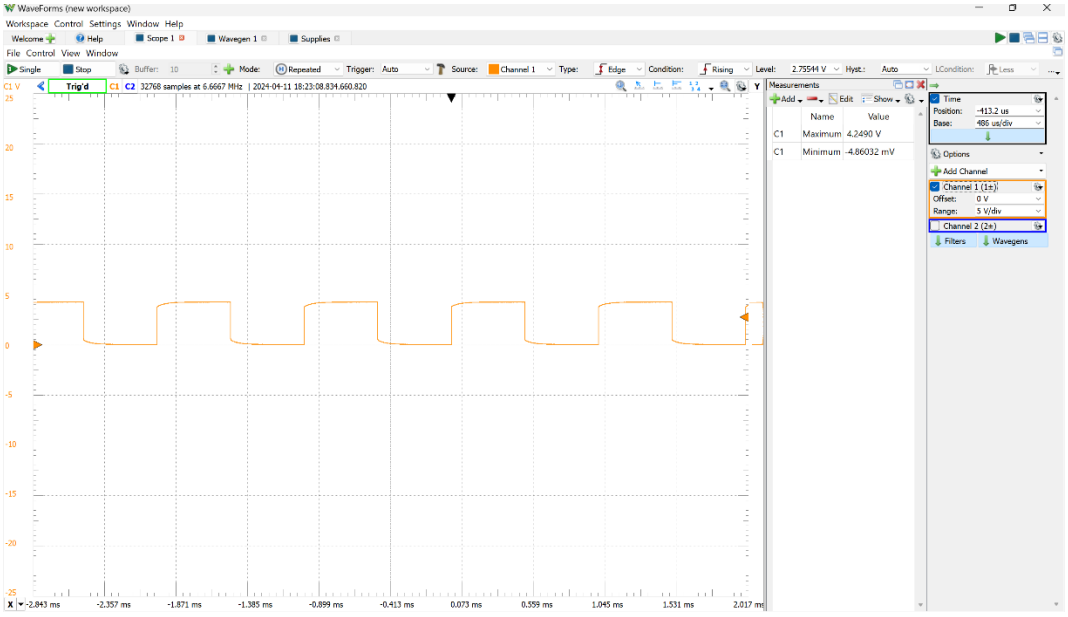

Figure 13: Initial Static Level Testing: Input A = 5 V, Input B = 0-5 V Square Wave – BONUS

In the initial testing, we find $V_H = 4.2490\ V\ and\ V_L = -4.86032\ mV$.

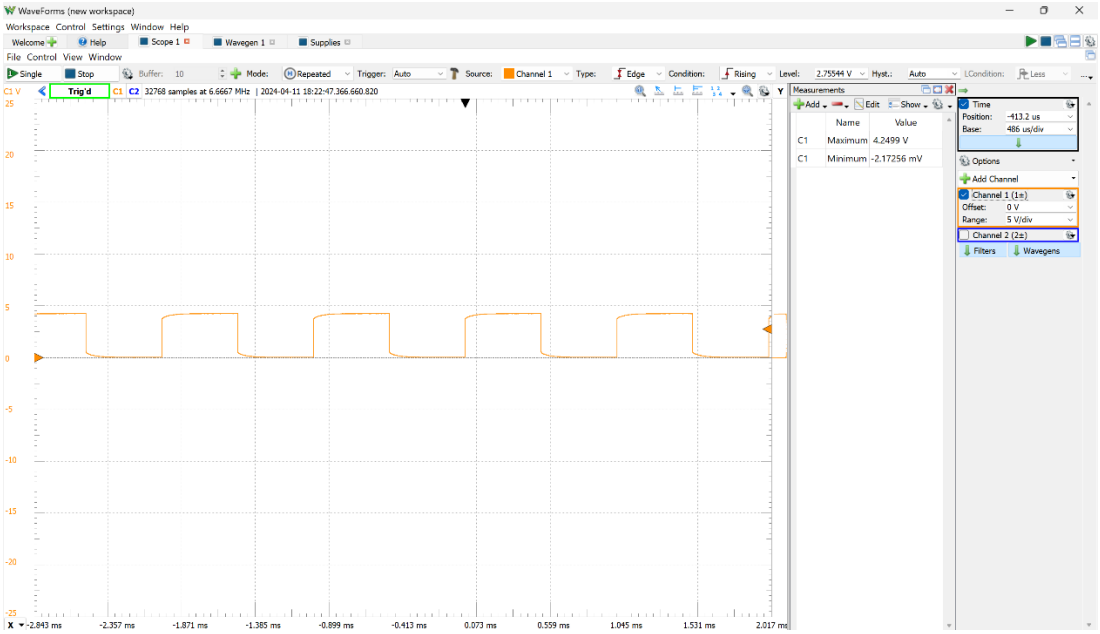

Figure 14: Secondary Static Level Testing: Input A = 0-5 V Square Wave, Input B = 5 V - BONUS

In the secondary testing, we find $V_H = 4.2499\ V\ and\ V_L = -2.17256\ mV$.

	Initial Design:	Bonus Design:	% Difference:
Initial Testing:	$V_H = 4.1710\ V$ $V_L = -7.54808\ mV$	$V_H = 4.2490\ V$ $V_L = -4.86032\ mV$	$V_H = 1.85\%$ $V_L = 43.32\%$
Secondary Testing:	$V_H = 4.1746\ V$ $V_L = -11.13176\ mV$	$V_H = 4.2499\ V$ $V_L = -2.17256\ mV$	$V_H = 1.79\%$ $V_L = 134.68\%$

Timing Performance

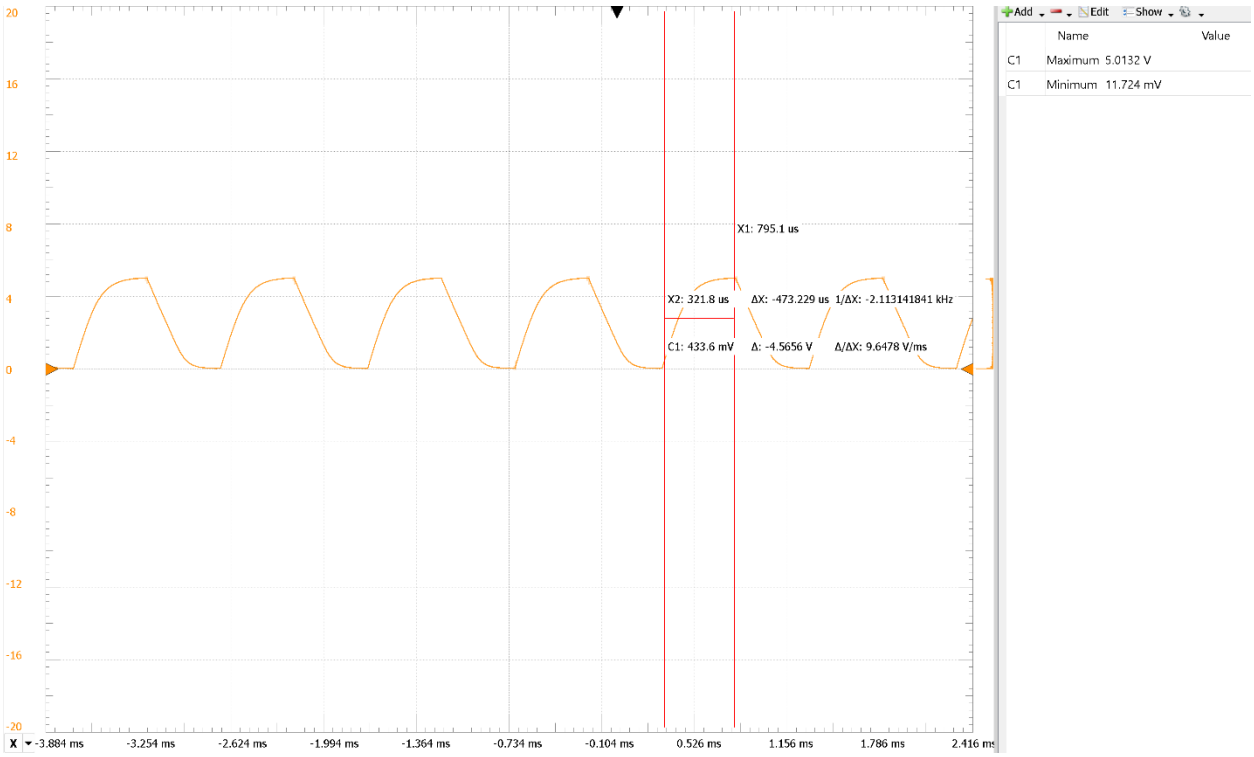

Figure 15: Graph of Rise Time – BONUS

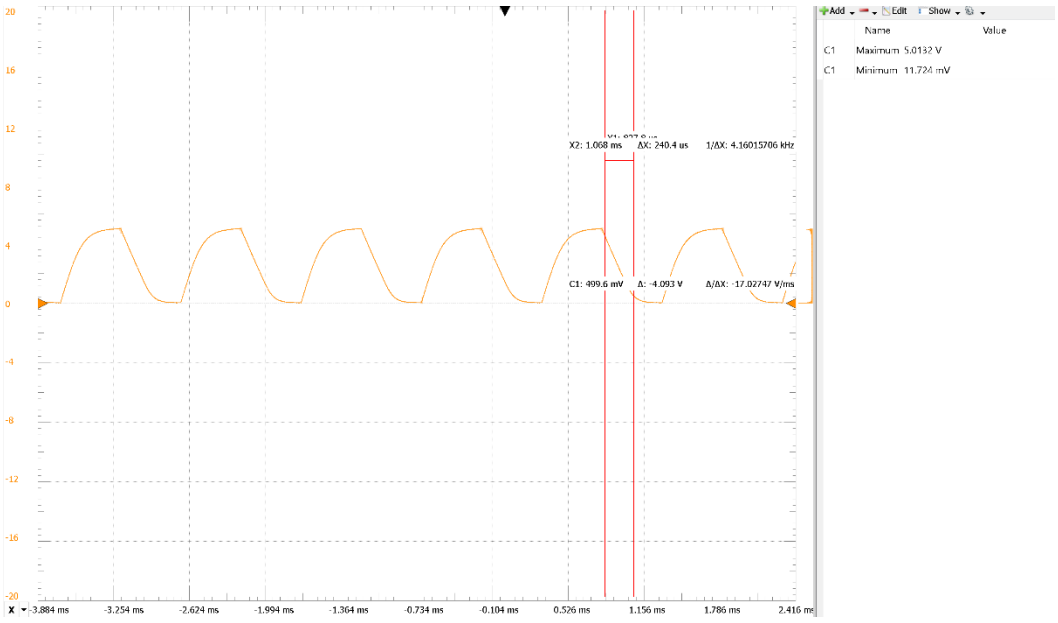

Figure 16: Graph of Fall Time - BONUS

From these two graphs, we can see that the rise time is 473.229 us and the fall time is 240.4 us. Now we can determine the τ_{ref} = 4.16(100nF) = 4.16 x 10^{-7} s. Whereas τ_{PHL} = 0.5(240.4 us) = 120.2 us and τ_{PLH} = 0.5(472.229 us) = 236.6145 us. From this, we can determine $\tau_P = 0.5(\tau_{PLH} + \tau_{PHL})$ = 178.40725 us. This value of τ_P features a percent difference of 32.16%. This error can arise due to the faulty wires previously mentioned. There was also an error that arose when calculating the value of rise time which is significantly larger than the other values found.