

Lab 4: Feedback Circuits

Professor: Dr. Chih-Hung (James) Chen

Name: Erion Keka

Student Number: 400435050

Submission Date: 2024-11-17

- 1. (10 Points)** (1) Based on the simulation data obtained in Step 1.2, what is the low-frequency (i.e., $f = 100$ Hz) voltage gain in dB for the first-stage differential amplifier Ad1, the second-stage CE amplifier Ad2, and the third-stage CC amplifier Ad3, respectively, for the differential-mode signal? (2) What is the overall voltage gain for the differential-mode signal? (3) Which input (V1 or V2) is the non-inverting input of the operational amplifier? (4) What is the upper 3-dB frequency f_H of the amplifier?
 - a.** Based on the simulation data obtained in Step 1.2, the low-frequency voltage gain in dB for the first-stage differential amplifier was found to be approximately 7.38 dB. The second-stage CE amplifier gain was found to be 70.05 dB and the third-stage CC amplifier gain was found to be approximately 0.00 dB.
 - b.** The overall voltage gain for the differential-mode signal was found to be approximately 77.43 dB.
 - c.** As V2 is in-phase with the output voltage, it is the non-inverting input of the operational.
 - d.** The upper 3-dB frequency of the amplifier is determined by finding when the initial phase, in this case, approximately 179.07 degrees falls by 45 degrees to approximately 134.07 degrees. This results in the upper 3-dB frequency of the amplifier being approximately 6338.41 Hz.
- 2. (5 Points)** Compare the simulated differential-mode gain Ad1 found in Q1 and the simulated gain Ad in Q5 of Lab 3. What causes these two gains to be so different from each other for the same differential amplifier?
 - a.** The simulated differential-mode gain in Q1 is found to be approximately 7.38 dB whereas, in Q5 of Lab 3, the simulated gain was found to be approximately 70.07 dB. When comparing these two gain values, we notice a percent difference of approximately 161.9%. This large percent difference arises due to the usage of a feedback stage within the circuit. The purpose of the feedback stage in circuits is to prioritize stability whilst, a significant hit to the gain is the draw-back.
- 3. (5 Points)** Based on the simulated results obtained in Steps 1.2 and 1.3, what are the input resistance R_{in} and the output resistance R_o of the Op-Amp?
 - a.** Based on the simulated results obtained in Steps 1.2 and 1.3, the input resistance of the op-amp is found to be approximately 81757.3 Ohms whereas, the output resistance is found to be approximately 460.9 Ohms.

4. (10 Points) (1) Based on the simulated and measured results from Steps 1.6 and 1.13, plot the simulated and measured output voltages V_o vs. time characteristics at 1 kHz. (2) Calculate the simulated and measured peak-to-peak voltage V_{pp} , the AC amplitude V_p , and the dc voltage V_{dc} of V_o , and compare the simulation and measurement results.

a.

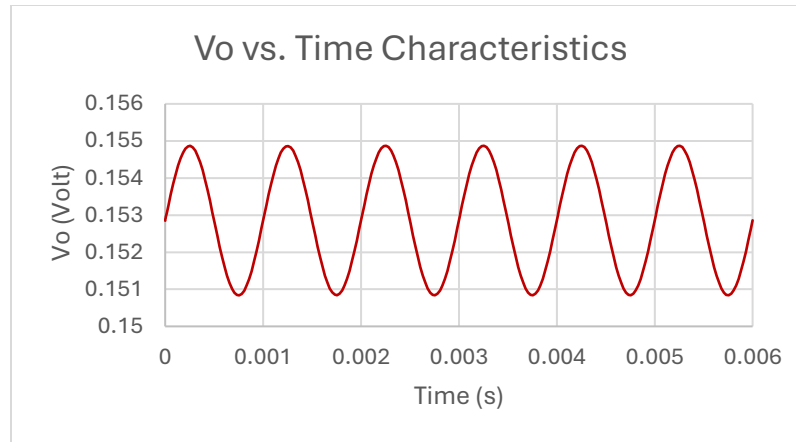


Figure 1: Graph of Step 1.6

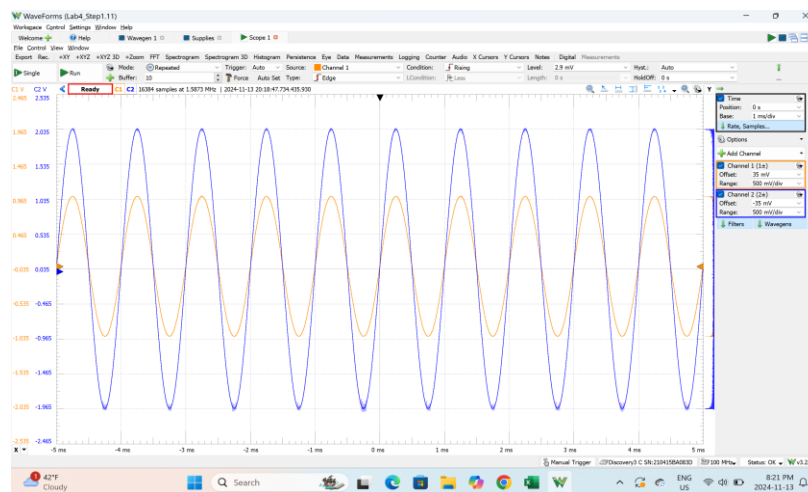


Figure 2: Graph of Step 1.13

- b. In Step 1.6,
 $V_{PP} = 0.1549 - 0.1508 = 0.0041 \text{ V}$
 $V_P = 0.0041 / 2 = 0.00205 \text{ V}$
 $V_{DC} = 0.1549 - 0.00205 = 0.15285 \text{ V}$

In Step 1.13,
 $V_{PP} = 2.035 - (-1.965) = 4 \text{ V}$
 $V_P = 4 / 2 = 2 \text{ V}$
 $V_{DC} = 2.035 - 2 = 0.035 \text{ V}$

Upon comparing the simulated and measurement results, the differences arise due to the utilization of an AC input amplitude of 1 V in Step 1.13 instead of the 1 mV amplitude used in Step 1.6.

5. (10 Points) (1) Based on the simulated and measured results from Steps 1.7 and 1.14, plot the simulated and measured voltage gain magnitude and phase vs. frequency characteristics. What is the low-frequency gain of this amplifier? (2) To operate this amplifier, what is its highest operating frequency to provide a constant gain as designed?

- a. Through the graphs below from both Steps 1.7 and 1.13, we can determine the low-frequency (at 1000 Hz) gain of this amplifier to be 2.0 V/V.

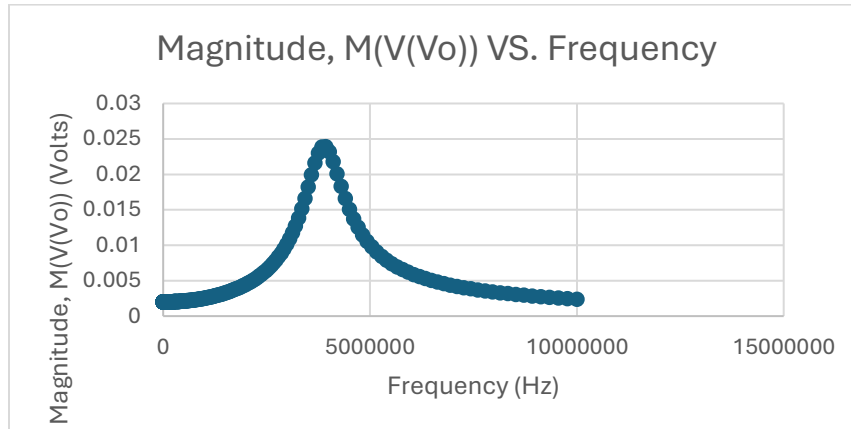


Figure 3: Step 1.7 - Magnitude VS. Frequency

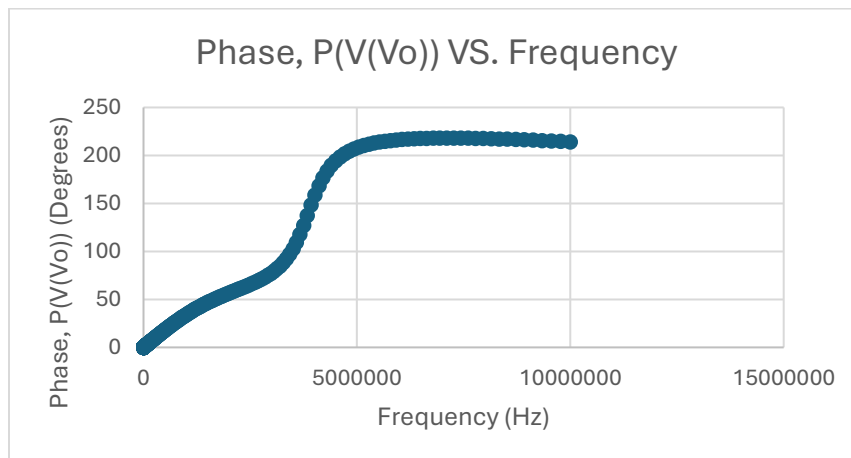


Figure 4: Step 1.7 - Phase VS. Frequency

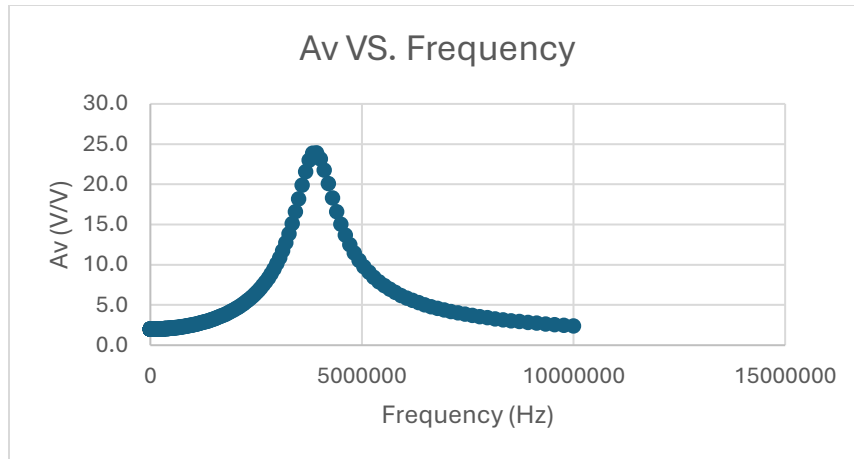


Figure 5: Step 1.7 - Av VS. Frequency

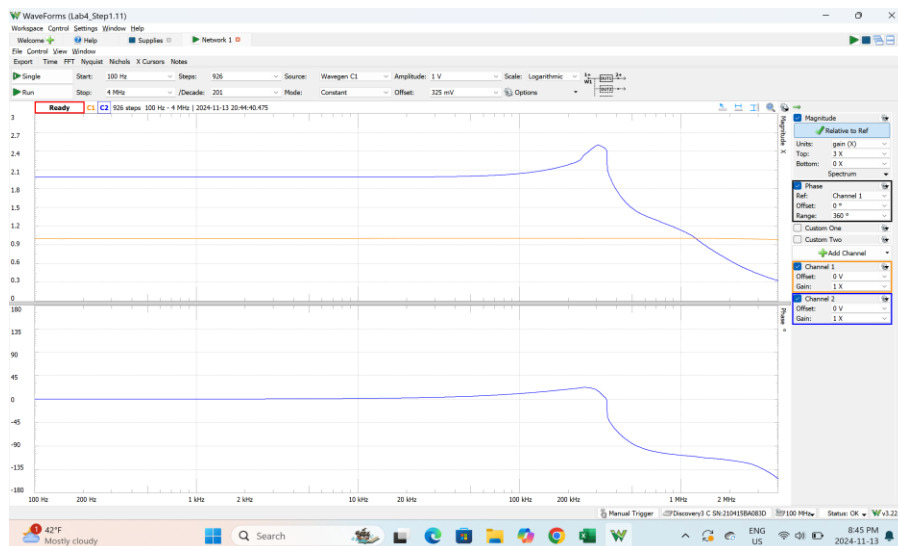
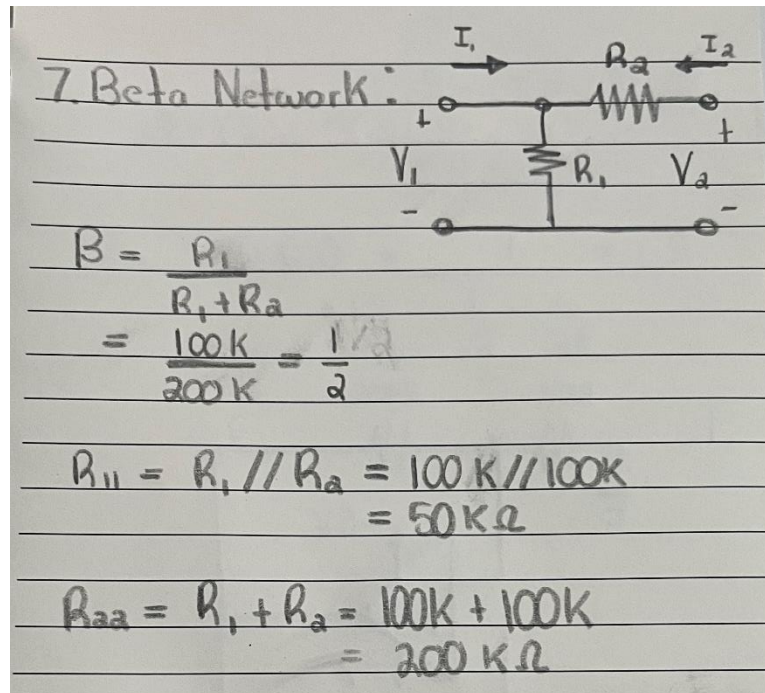


Figure 6: Step 1.14 - Magnitude and Phase VS. Frequency

- b. The highest operating frequency to provide a constant gain as designed within this amplifier would be approximately 100 KHz as demonstrated in Figure 6. This is the point where the gain begins to fluctuate.
6. (5 Points) What kind of feedback configurations (e.g., shunt-shunt) is it for the amplifier in Fig. 2?
 - a. The amplifier in Fig. 2 is in the series-shunt configuration.

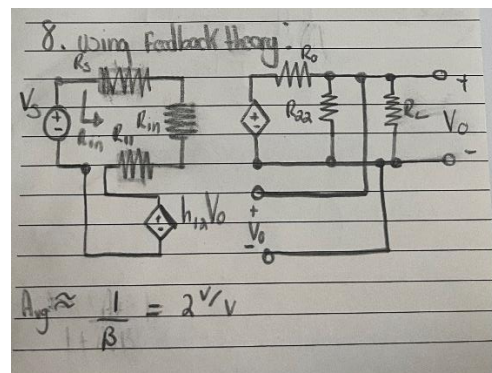
7. (10 Points) Find the beta network and the feedback components β , R_{11} , and R_{22} , respectively.

a.



8. (15 Points) Use the feedback theory and simulation results to find the amplifier's voltage gain, input resistance, and output resistance, respectively.

a.



8. $R_{in} = R_{ic}' - R_s$

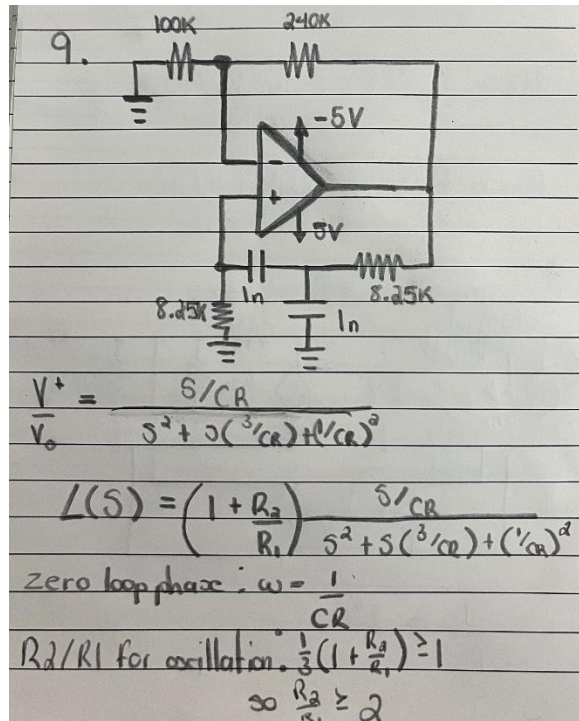
$$= (R_{in} + R_{11} + R_s)(1 + 0.5\beta) - R_s$$

$$= 303\text{ H}\Omega$$

$$R_{out} = \frac{1}{\frac{1}{R_{oc}'} - \frac{1}{R_e}} = 0.2\text{ }\Omega$$

9. (15 Points) For the oscillator circuit in Fig. 5, find its loop gain $L(s)$, the frequency for the zero-loop phase, and R_2/R_1 for oscillation.

a.



10. (5 Points) Based on the simulated results in Step 2.4, what are the settling times for $R_2 = 220$ k Ω , 240 k Ω , and 280 k Ω , respectively? What do you observe? Explain the observed trend.

a. Based on the simulated results in Step 2.4, the settling time for $R_2 = 220$ k Ω is found to be approximately 0.00177 s. The settling time for $R_2 = 240$ k Ω is found to be approximately 0.000924 s and for $R_2 = 280$ k Ω , we find it to be approximately 0.000618 s. From these values, we can observe that the resistance and settling time are inversely proportional. As the resistance value of R_2 increases, the value of the settling time is decreasing. This is a result of increasing R_2 thus increasing the loop-gain. When the loop-gain is increased, the dominant pole of the circuit is shifted to a higher frequency resulting in a decreased settling time.

11. (10 Points) (1) Based on the setup in Steps 2.3, 2.5, 2.8, and 2.9, plot the simulated and measured V_{out} . (2) Calculate the simulated and measured oscillation frequencies in each case. Compare and discuss them with the results from the theory.

a.

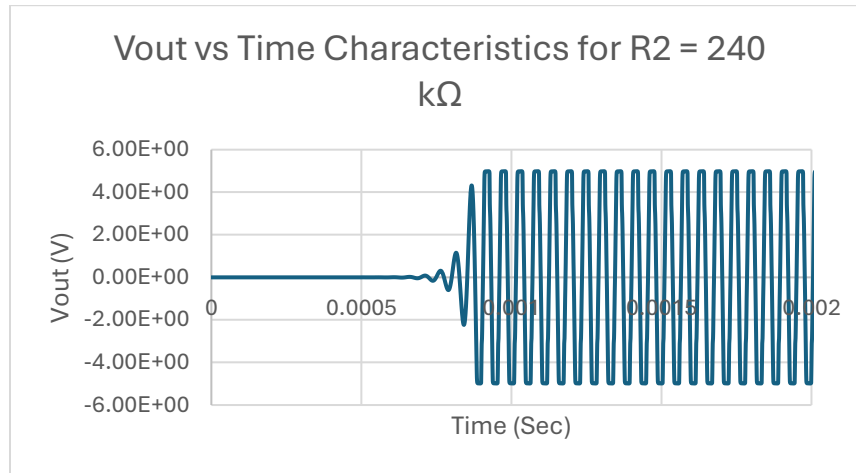


Figure 7: Step 2.3 - Simulated and Measured V_{out} Plot

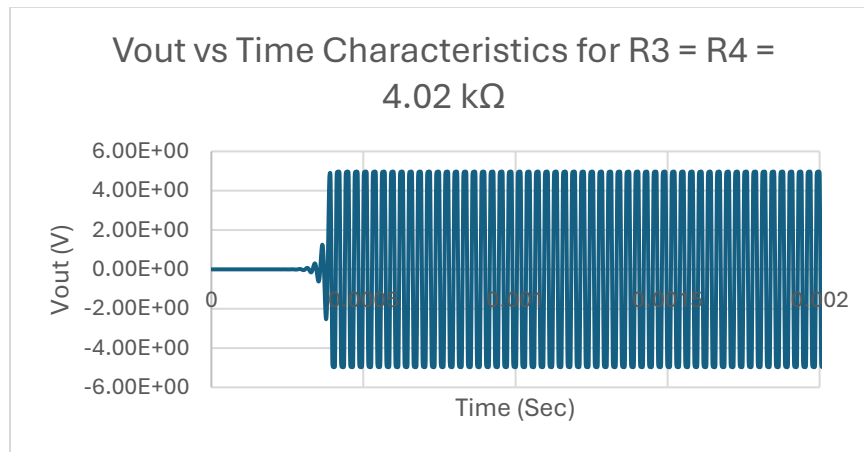


Figure 8: Step 2.5 - Simulated and Measured V_{out} Plot

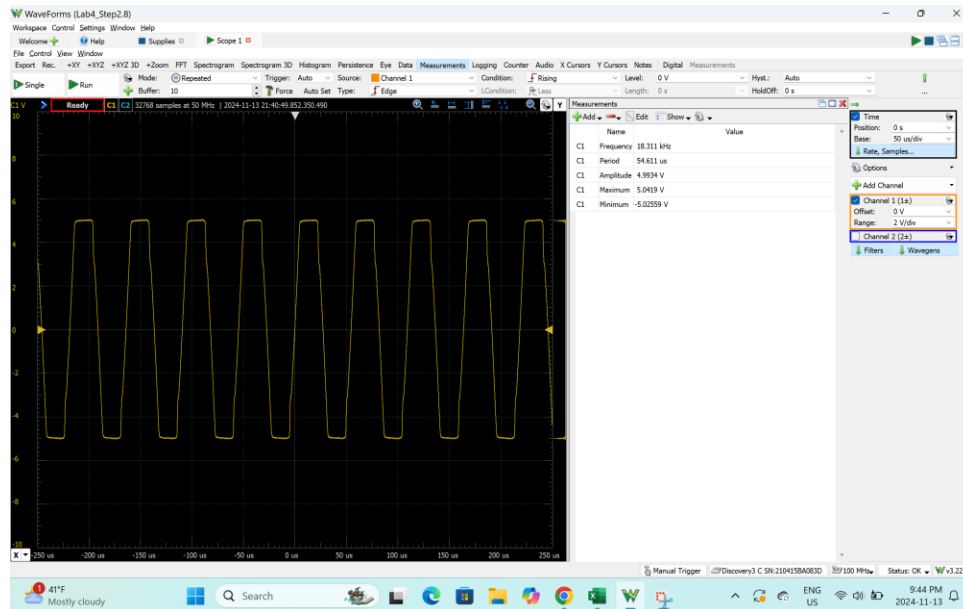


Figure 9: Step 2.8 - Simulated and Measured Vout Plot

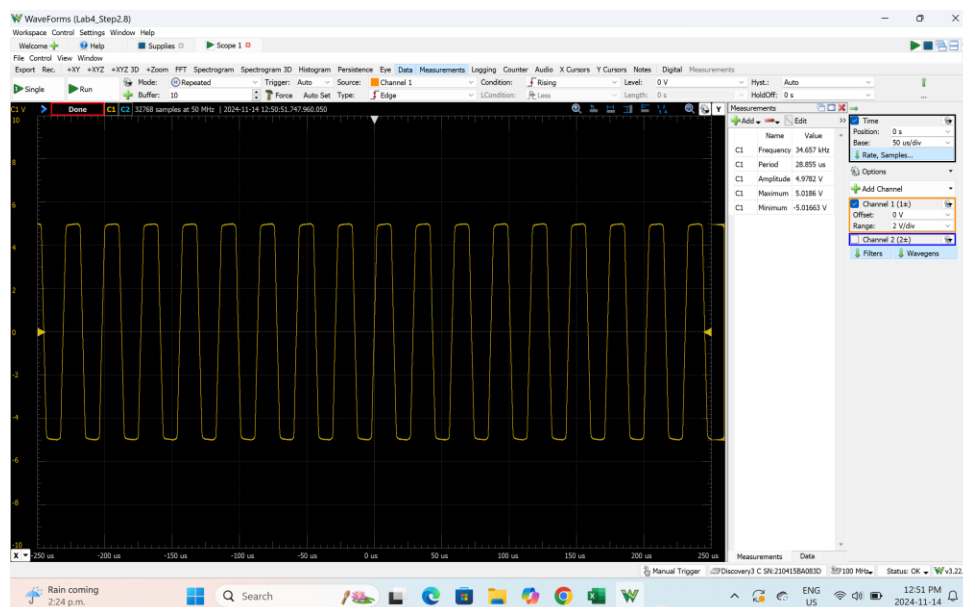


Figure 10: Step 2.9 - Simulated and Measured Vout Plot

- b. From Step 2.3, we find the simulated oscillation frequency to be 18 kHz whereas in the measured counterpart (Step 2.8), the frequency is found to be approximately 18.311 kHz. From Step 2.5, we find the simulated oscillation frequency to be 34 kHz whereas in the measured counterpart (Step 2.9), the frequency is found to be approximately 34.657 kHz. Our results align with the theoretical results. We previously noted that from $\omega = 1 / CR$, frequency is inversely proportional to the resistance. As we decreased the value of R in Steps 2.5 and 2.9, we note that the frequency increases matching the theory. In addition, we can notice both the measured and simulated frequencies are close to one another. (When comparing Step 2.3 to Step 2.8 and Step 2.5 to Step 2.9).