Lab 2: Single Stage Amplifiers

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Question 1:

1.

	Step 1.2	Step 1.10
$V_{o,min}$	-3 V	-3 V
I_o	0.000184825 A	0.0002043 A

2.

	Step 1.2	Step 1.10
R_o	$-2.41\text{x}10^6 \leq R_o \leq 4.07\text{x}10^6$	$-5.44\text{x}10^7 \leq R_o \leq 5.40\text{x}10^6$

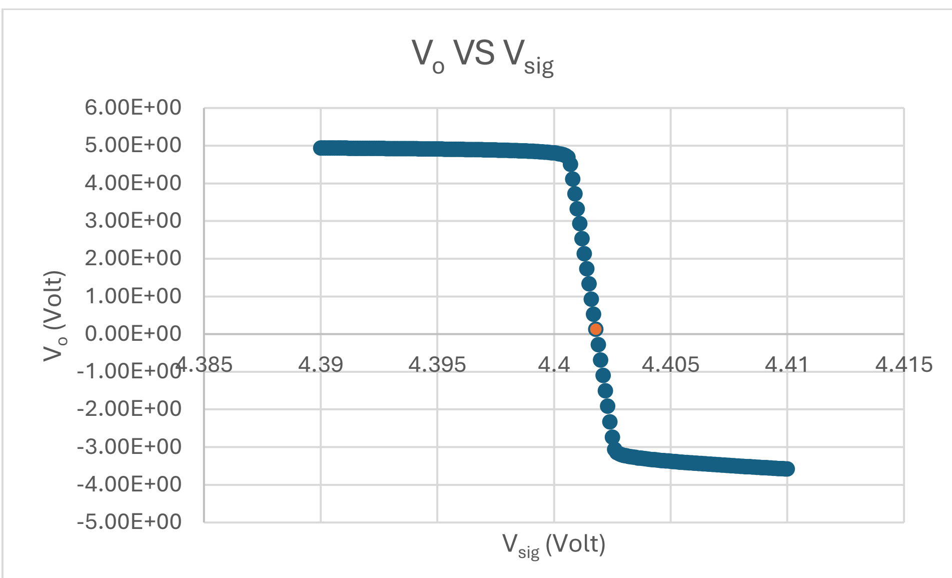
Question 2:

	Step 1.5
V_{o1}	4.940365198 V
V_{o2}	-3.578316473 V

For both cases, the value of V_{sig} lies outside of the voltage range in which the circuit acts as an amplifier. Thus, the values of V_{o1} and V_{o2} are the maximum and minimum output values for the circuit.

Question 3:

1.



As seen in the graph of V_o VS V_{sig}, the simulated characteristics are accurate. The orange highlighted point on the graph represents the point in which $V_{sig} = V_{BQ2}$ that results in $V_o \approx 0$.

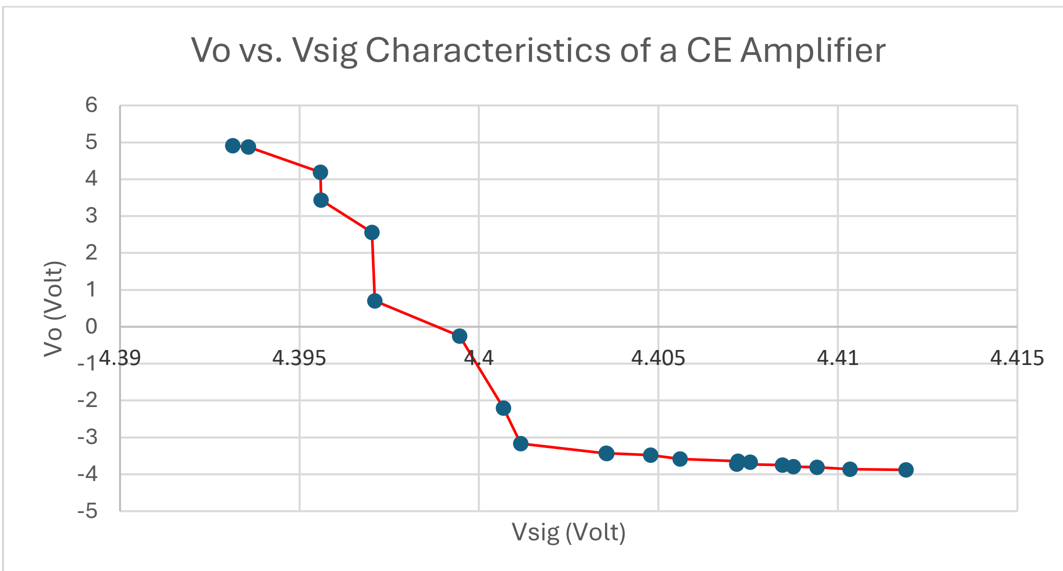
2.

	Step 1.6
Input V_{sig} Range	$4.4006\ V \leq V_{sig} \leq 4.4028\ V$
Output V_o Range	$-3.17529\ V \leq V_o \leq 4.4689481\ V$

3.

	Step 1.6
V_{sig}	4.4018 V
I_{C2}	-0.0001849 A
V_o	0.124312 V

4.



Question 4:

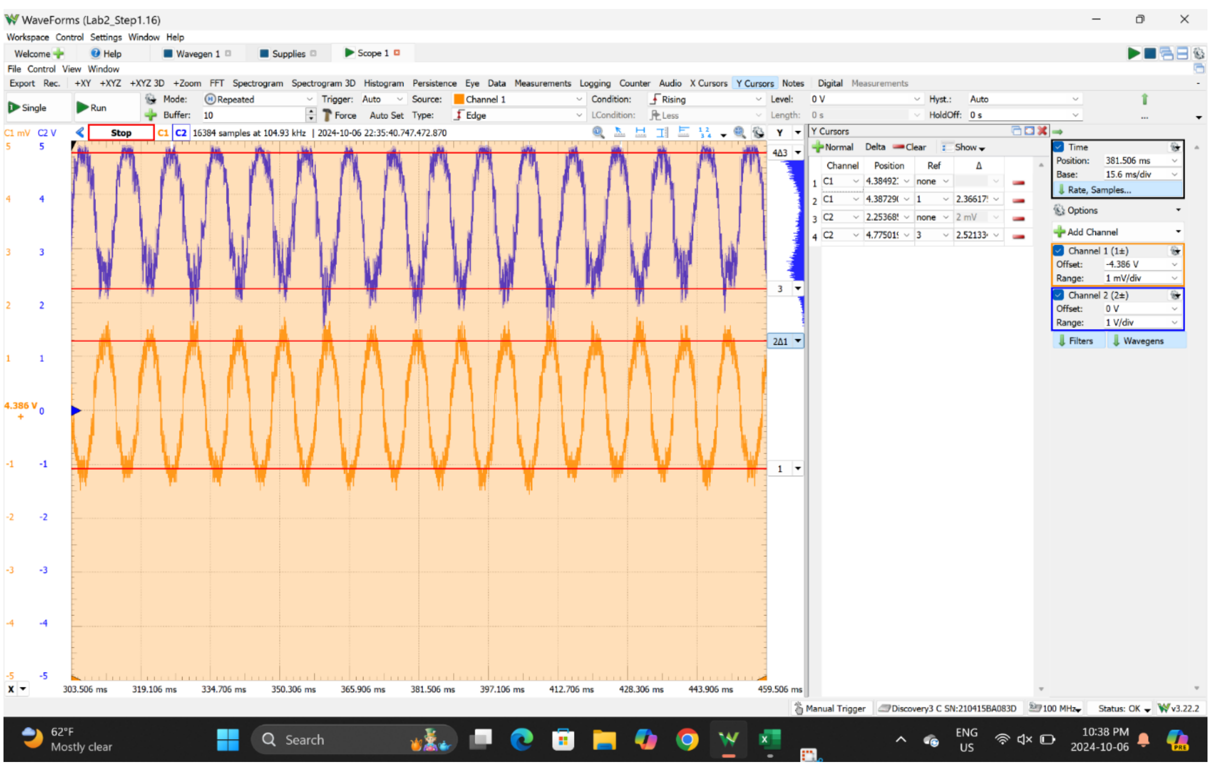
1.

	Lower Frequency (100 Hz)	Upper-3dB Frequency, f_{3dB} (14401.76903 Hz)
A_{vo}	$20\log\frac{V_O}{V_I} = 20\log\frac{4.047}{0.002}$ =66.1dB	$20\log\frac{V_O}{V_I} = 20\log\frac{2.839}{0.002}$ =63.04dB
Phase	179.5980977°	134.8646809°

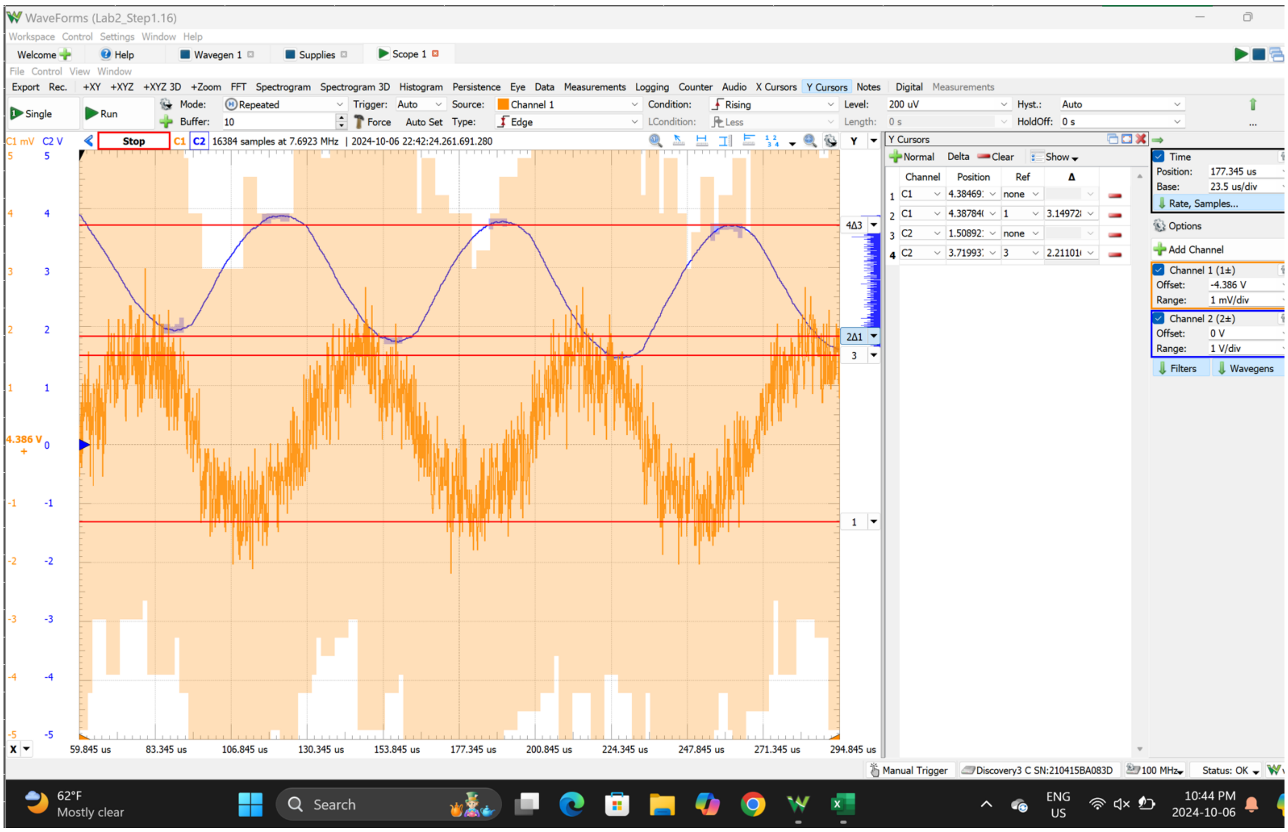
2.

	Step 1.18/19
ΔC1	2.37×10^{-3} V
ΔC2	2.52 V
Gain A_{vo}	60.6 dB

Through the measurement data, the voltage gain A_{vo} is found to be 60.6 dB. This is close to the simulated value of 66.1 dB. The difference amongst the values suggests a slight error occurred during the measurement. The Waveform screenshot is added below.



3. Upon setting the frequency to 14401.76903 Hz to match f_{3dB}. We achieve the output shown below. From the graph, we can calculate the gain to be 56.9 dB. About 0.707 of the low-frequency value obtained at 100 Hz is calculated to be 42.8 dB. These values are not close to each other. The percent difference between the two values is approximately 28.3%. However, a patten can be noted that with an increase in the frequency, the gain decreases.



Question 5:

1.

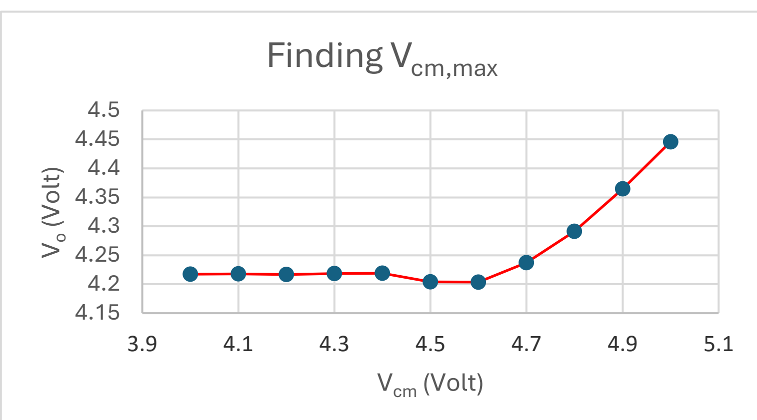
	Step 2.2
V_{CM}	0 V
V_E	-0.52537 V
V_o	4.249991 V
I_{C2}	9.1×10^{-5} A

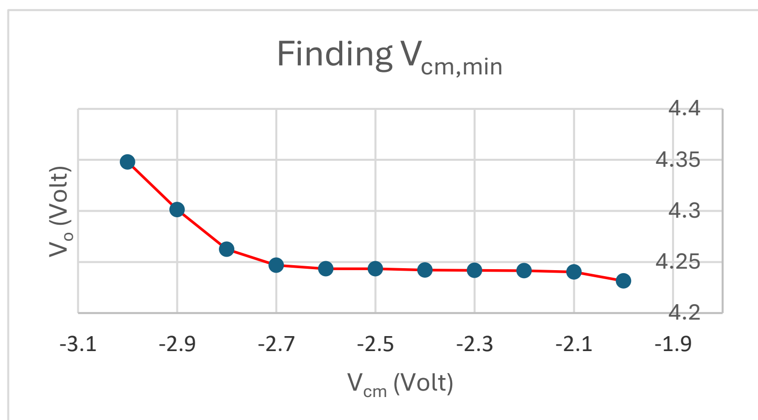
2.

	Step 2.2
For V_o to remain constant:	$-2.6\ V \leq V_{CM} \leq 4.6\ V$

3. The upper bound of the input common-mode range is bounded by the requirement of maintaining both the BJTs in the active region. The lower bound on the other hand is bounded by the requirement of keeping the constant current sink on – must keep the transistor of the constant current sink in the saturation operating region.

4. From the graphs shown below, we can see that $V_{cm,max}$ occurs at a point between 4.6 V to 4.7 V. It is also noted that $V_{cm,min}$ occurs at a point between -2.6 V to -2.5 V. This confirms the common-mode range found via the simulation.





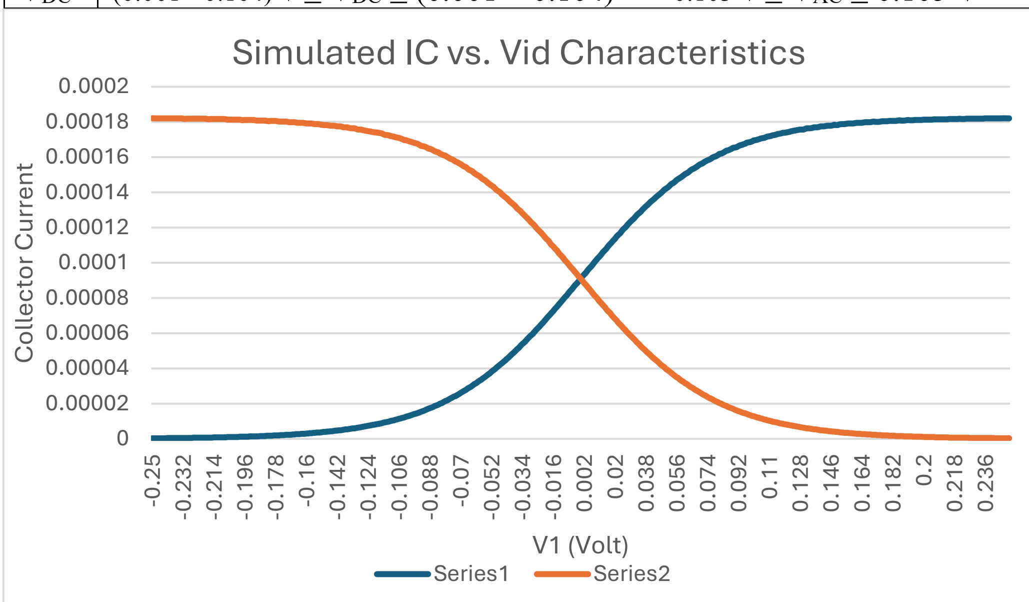
Question 6:

Frequency	$M(V(V_o))$	$P(V(V_o))$	Common-Mode Gain, A_{cm}
0.1 Hz	4.51783×10^{-8} V	-179.9767369°	-86.90 dB
100 Hz	4.87596×10^{-8} V	-157.9043648°	-86.24 dB

Question 7: (Parts 1 & 2 were combined)

From section 9.2.3 of the textbook, there is a limitation that exists with differential input. This limitation is given as $\pm\frac{V_T}{2}$ for the AC voltage whereas, it is $\pm 4\ V_T$. V_T for BJTs is found to be approximately 26 mV. The limitation is added / subtracted to the intersecting point of the graph of 'Simulated IC vs. Vid Characteristics' as this is ideal operation point.

	Step 3.2
V_{AC}	$(0.001 - 0.013)\ V \le V_{AC} \le (0.001 + 0.013) \rightarrow -0.012\ V \le V_{AC} \le 0.014\ V$
V_{DC}	$(0.001 - 0.104)\ V \le V_{DC} \le (0.001 + 0.104) \rightarrow -0.103\ V \le V_{AC} \le 0.105\ V$



Question 8:

1. Based on the results of the simulation data in 3.3, the voltage gain A_d for the differential-mode signal is found to be approximately 19.63 dB for the set of data. It begins at 19.63 dB and decreases to 16.98 dB at the highest frequency.
2.

	Upper-3dB, f_{3dB}
Frequency	8332821.508 Hz
Phase	-45.41565075°

$$Gain - Bandwith\ Product = Abs\ Gain * f_{3dB}, where\ Abs\ Gain = 10^{\frac{Voltage\ Gain}{20}}$$

$$\therefore Gain - Bandwith\ Product = (8332821.508)(9.58) = 79{,}828{,}430.04664\ Hz$$

3.

	Upper-3dB Frequency, f_{3dB}
Question 4	14401.76903 Hz
Question 8	8332821.508 Hz

Upon comparing these two f_{3dB} values, we can see that the differential amplifier in Question 8 features a significantly larger upper-3dB frequency than the common-emitter amplifier in Question 4. The percent difference calculated between these two values using the formula, $\frac{|V_1-V_2|}{[\frac{(V_1+V_2)}{2}]} * 100$, is found to be 199.31%.

4. Based on the measurement data obtained in Step 3.7 (actually 3.6), the measured low-frequency differential voltage gain, A_d, is found to be 21.2 dB.

Question 9:

Based on the simulation data, the CMMR can be calculated using the formula, $CMMR = 20log_{10}\left|\frac{A_d}{A_{cm}}\right| = 20log_{10}\left|\frac{19.63\ dB}{-86.9\ dB}\right| = -12.921\ dB.$