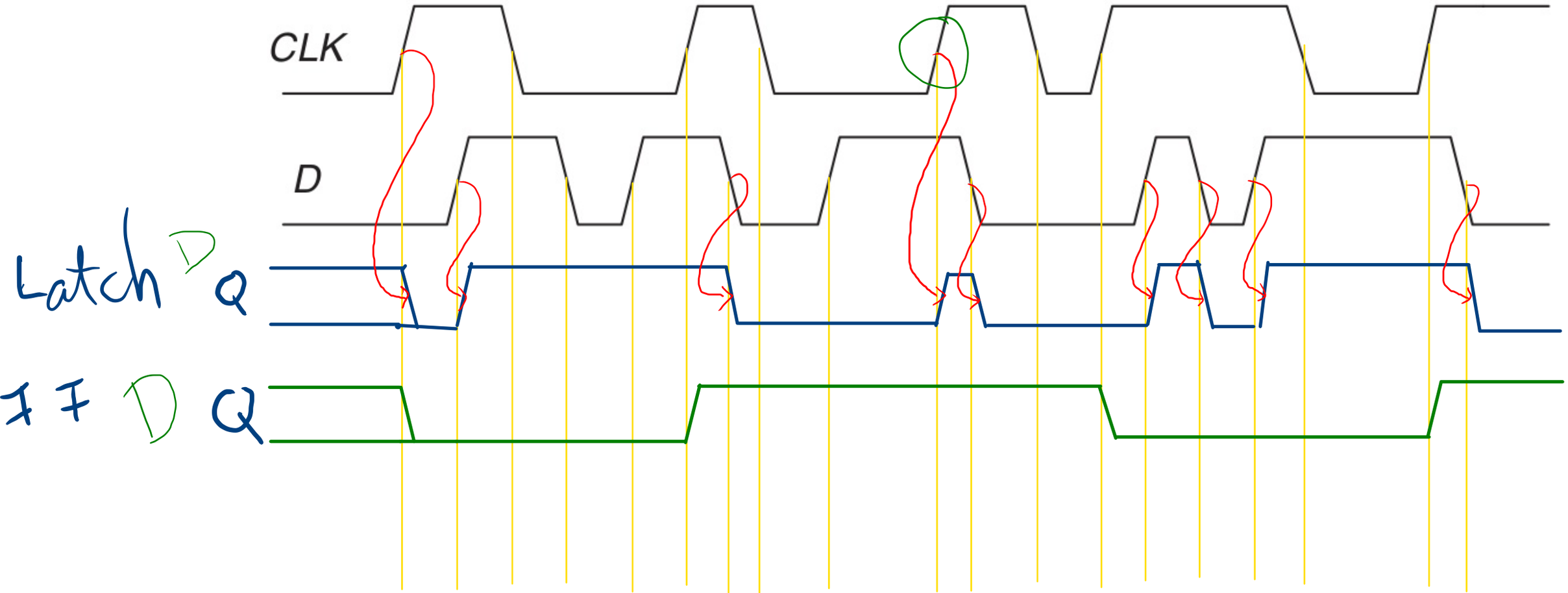
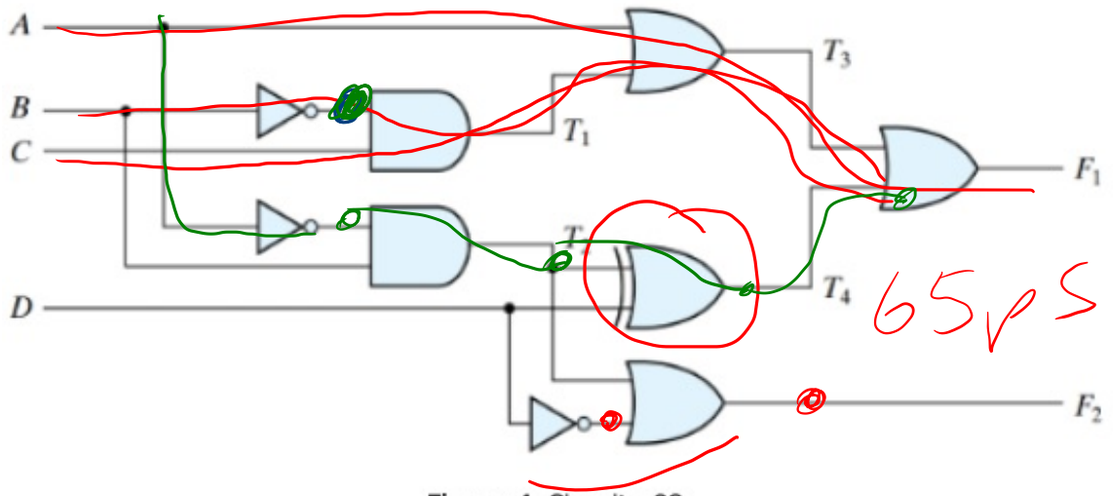

CLK
D
Latch
D
Q
FF
D
Q

2 OR

NOT AND 2OR

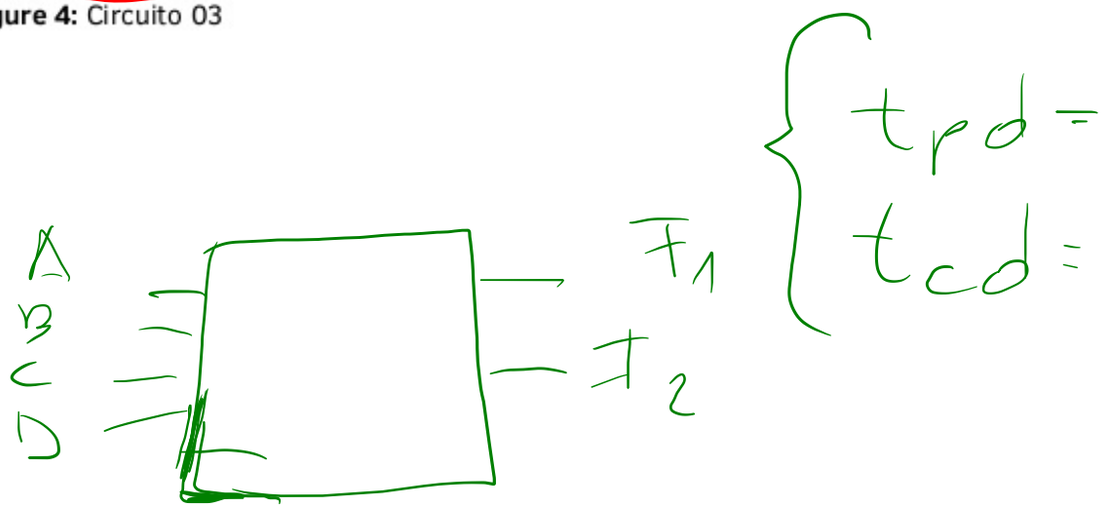


65ps

t_{pd}

t_{cd}

Figure 4: Circuito 03



32 16 8 4 2 1

→ 101101_2

↙ ↳ + x

− ↙

a) SS ⇒ $= -45_{10}$

b) S/M ⇒ $= -13_{10}$

c) 1's ⇒ $= -18_{10}$

d) 2's ⇒ $= -19_{10}$

$010010_1 = 18_{10}$

$+25_{10} \Rightarrow$ 11001_2 SS

→ $01\,1001_2$ 2's

$+25_{10}$

5bits $[0; 2^n - 1] \Rightarrow [0; 31]$

5bits $[-2^{n-1}; 2^{n-1} - 1] \Rightarrow [-16; 15]$

6bits $[-32; +31]$

-25_{10} 6 bits $[-32; +31]$

$01\,1001_2$ => magnitud

$10\,0110_2$

$+\quad\quad 1$

$10\,0111_2 \Rightarrow -25_{10}$

2's $10\,0111_2 \Rightarrow -25_{10}$

2's $\underline{-}\,110100_2 \Rightarrow \underline{-12_{10}}$

001100_2 magnitud = $\underline{12_{10}}$

$$\begin{array}{r} 10 \quad 2's \\ +\ (-5) \quad 2's \\ \hline 5_{10} \end{array}$$

4 bits $\quad [-2^{n-1};\ 2^{n-1}-1] \quad [-8;+7]$

5 bits

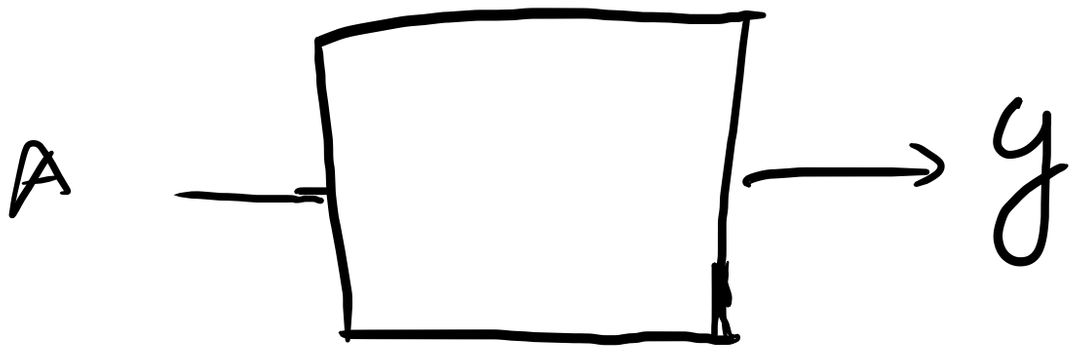
$$\begin{array}{r} 0\,1010_2 \quad +10 \\ +\ 1\,1011_2 \quad +(-5) \\ \hline 0\,0101_2 \quad +5_{10} \end{array}$$

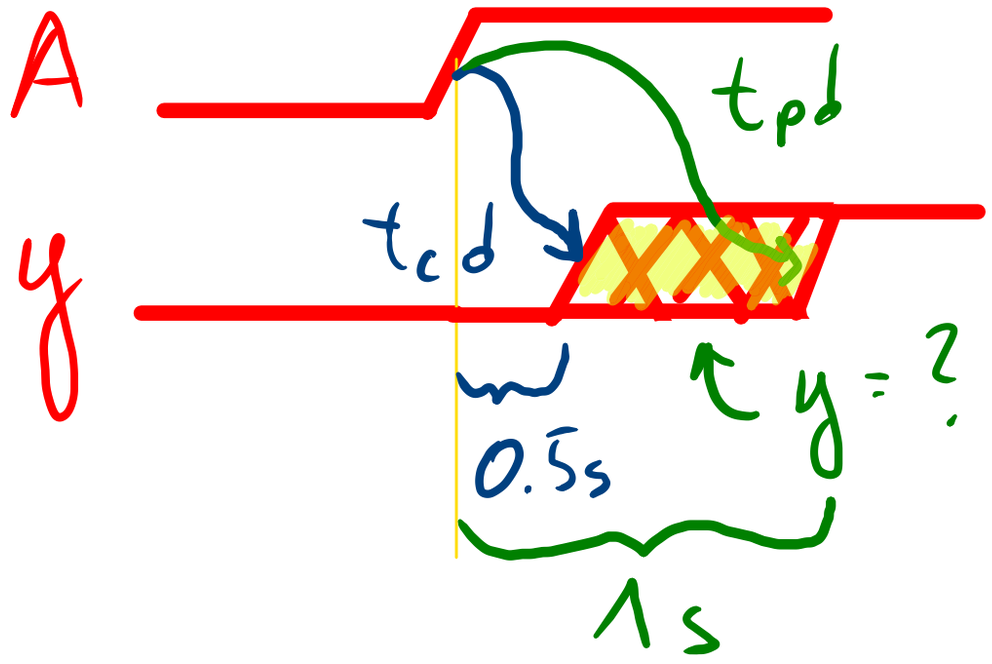
$0\ 0101_2$

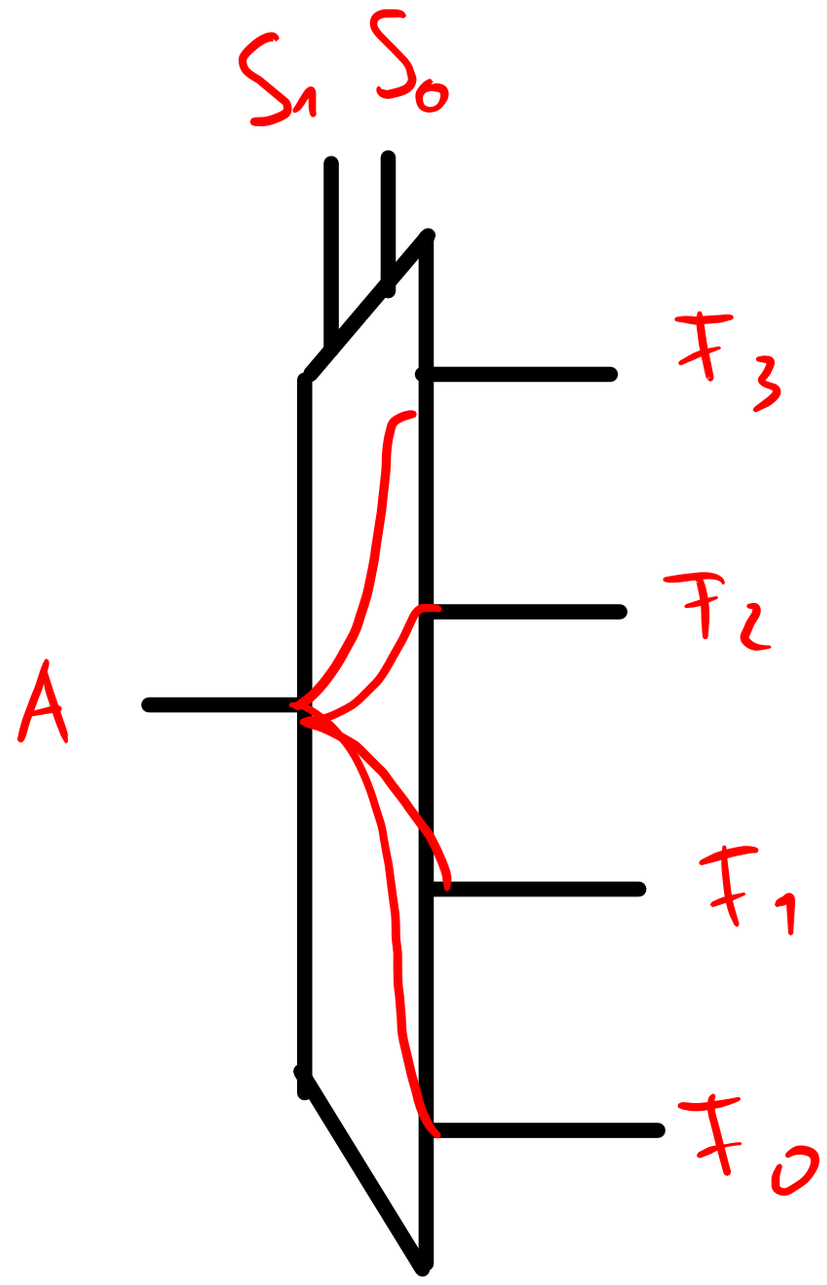
$1\ 1011_2 = -5_{10}$ 2's

$t_{pd} = 1s$

$t_{cd} = 0.5s$

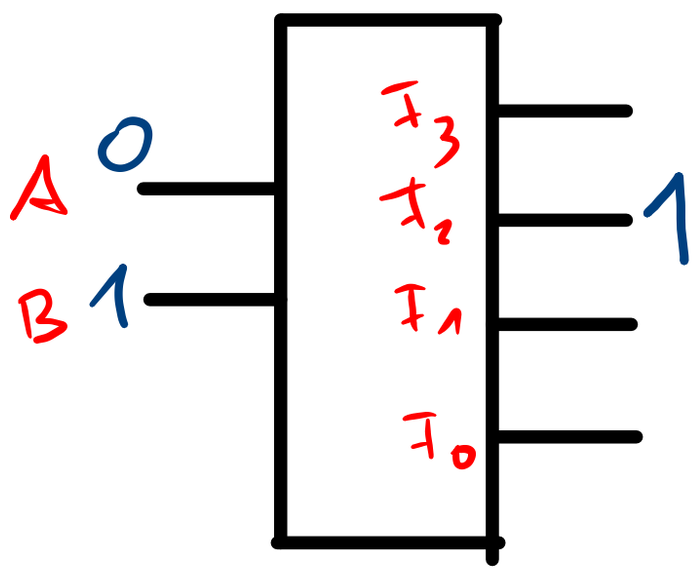







```
if (S1S0 == 00):
    F3 = A
    F2 = 0
    F1 = 0
    F0 = 0
elif (S1S0 == 01):
    F3 = 0
    F2 = A
    F1 = 0
    F0 = 0
elif (S1S0 == 10):
    F3 = 0
    F2 = 0
    F1 = A
    F0 = 0
```

DECODER



One Hot

```
if (AB == 00):
    I3 = 1
    I2 = I1 = I0 = 0
elif (AB == 01):
    I2 = 1
    I3 = I1 = I0 = 0
elif (AB == 10):
    I1 = 1
    I3 = I2 = I0 = 0
elif (AB == 11):
    I0 = 0
    I3 = I2 = I1 = 0
```

AB	Y	
00	0	$\bar{A}\bar{B}$
01	1	$\bar{A}B$
10	0	$A\bar{B}$
11	1	AB

$y = \bar{A}B + AB$ SOP

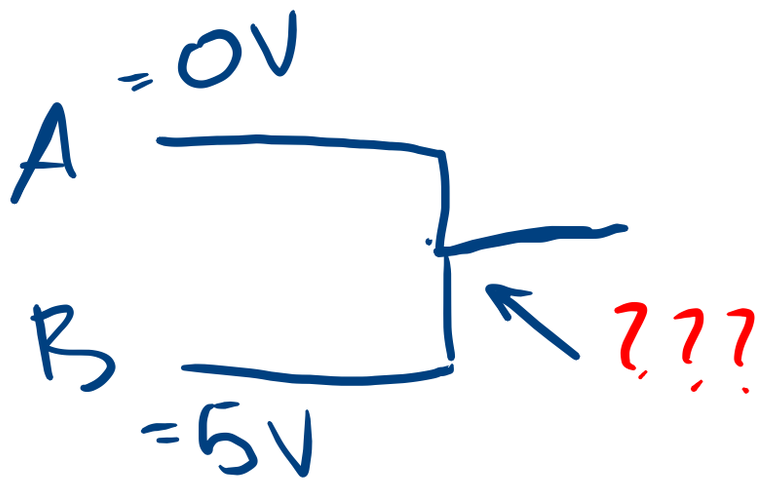
$1(\overline{BCD})$

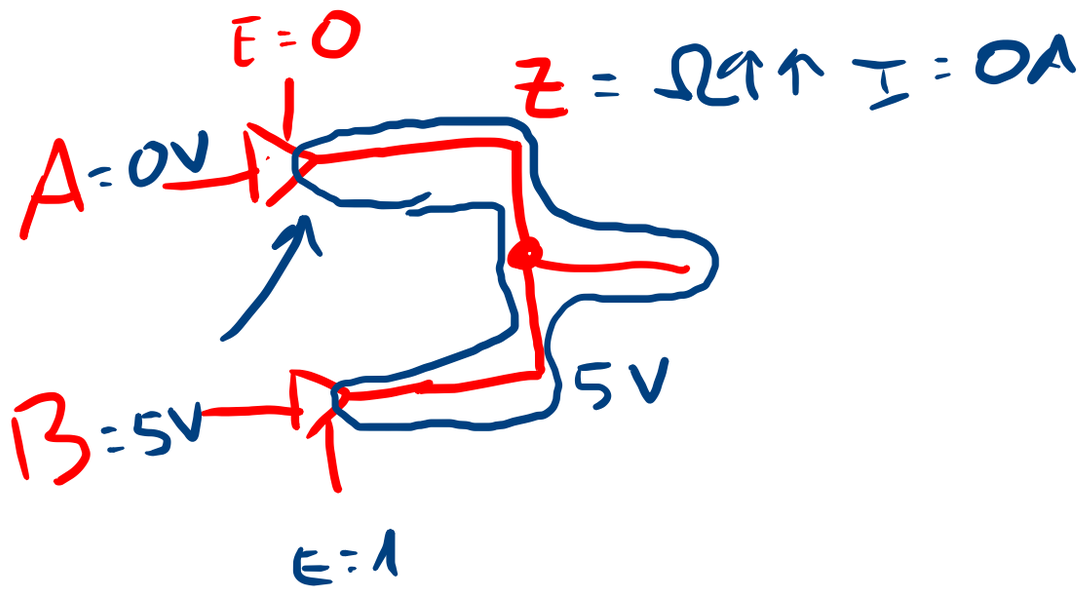
$$Y = A\cancel{B}\cancel{C}\overline{D} + A\overline{BCD} + \cancel{(\overline{A+B+C+D})}$$

A B C D	Y
0 0 0 0	1
0 0 0 1	0
0 0 1 0	0
0 0 1 1	0
0 1 0 0	0
0 1 0 1	0
→ 1 0 1 1	1
1 1 1 1	0

$1(\overline{11})$

$1(\overline{1}) = 1 \cdot 0 = 0$


A
=0V
B
=5V
???


E=0
Z = ΩΩ↑↑ I = 0A
A=0V
B=5V
5V
E=1

4:3

S[1] S[0]

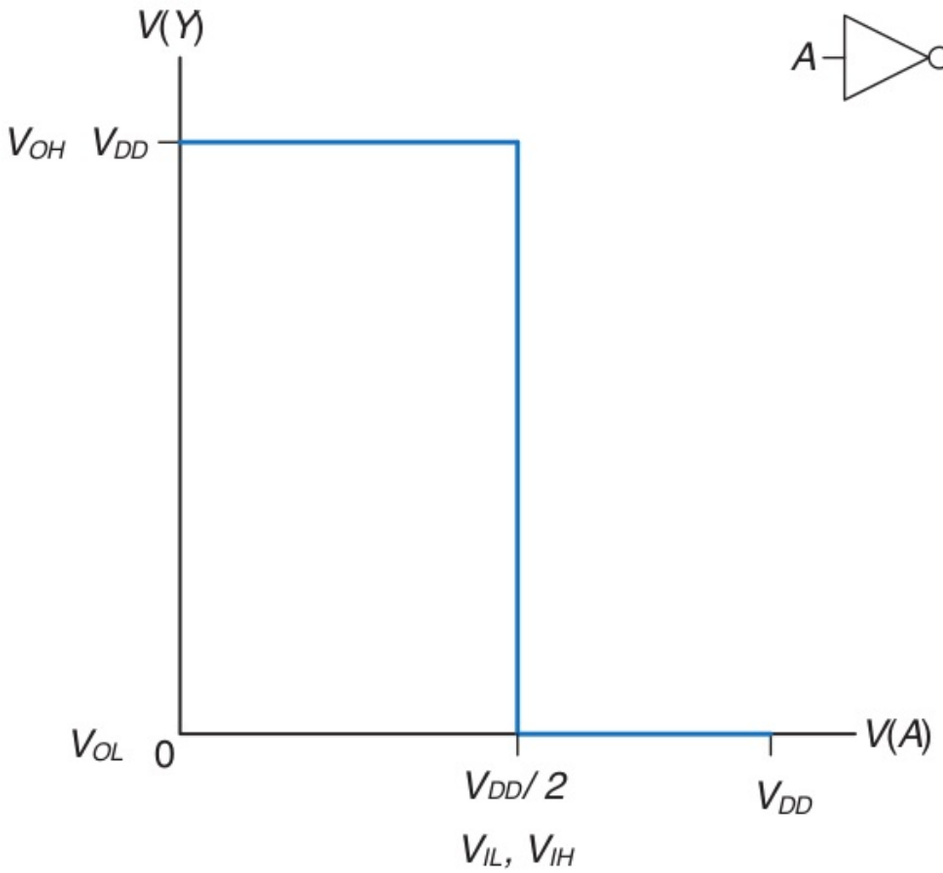
D[3] D[2] D[1] D[0]

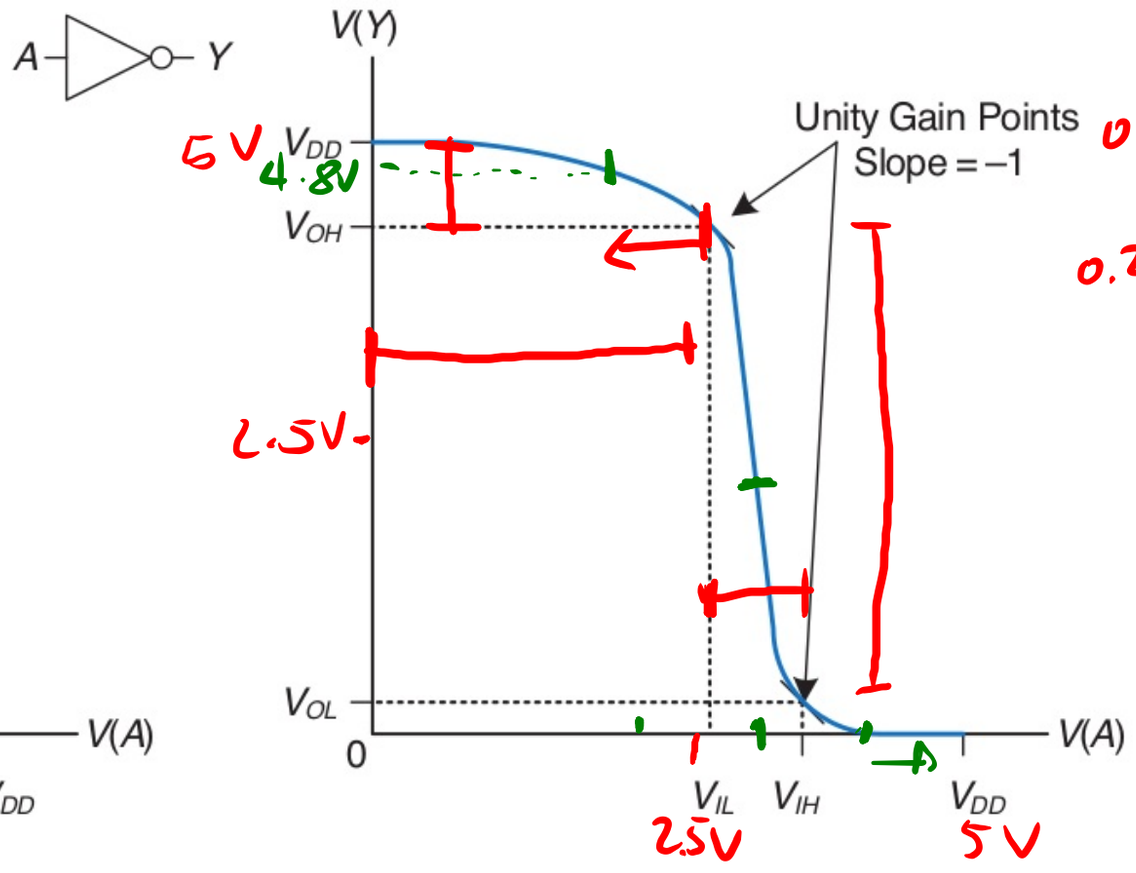
```
module mux4to1(input wire [1:0] S, input wire [3:0] D, output wire Y);

    assign Y = S[1] ? (S[0] ? D[3]:D[2]) : (S[0] ? D[1]:D[0]);
    /*
        if (S[1] == 1):
            if (S[0] == 1):
                Y = D[3]
            elif (S[0] == 0):
                Y = D[2]
        elif (S[1] == 0):
            if ((S[0] == 1):
                Y = D[1]
            elif (S[0] == 0):
                Y = D[0]
    */

endmodule
```

A → y

A → 1.3V
y → 4.8V

V_{OH} = 4V V_{IL} = 2.6V
V_{OL} = 0.8V V_{IH} = 3.0V





IN	out
2.5V	4.1V
2.6V	4.0V
2.8V	2.3V
3.0V	0.8V
3.5V	0.5V
4.0V	0.2V
4.5V	0V
4.8V	0V
4.3V	0V

0.1V
0.1V
0.2V
0.1V

- ¿Qué sucede cuando:
  - A = 0
  - C = 1
  - B = 1 -> 0

Y = 1

ΔBC = 011

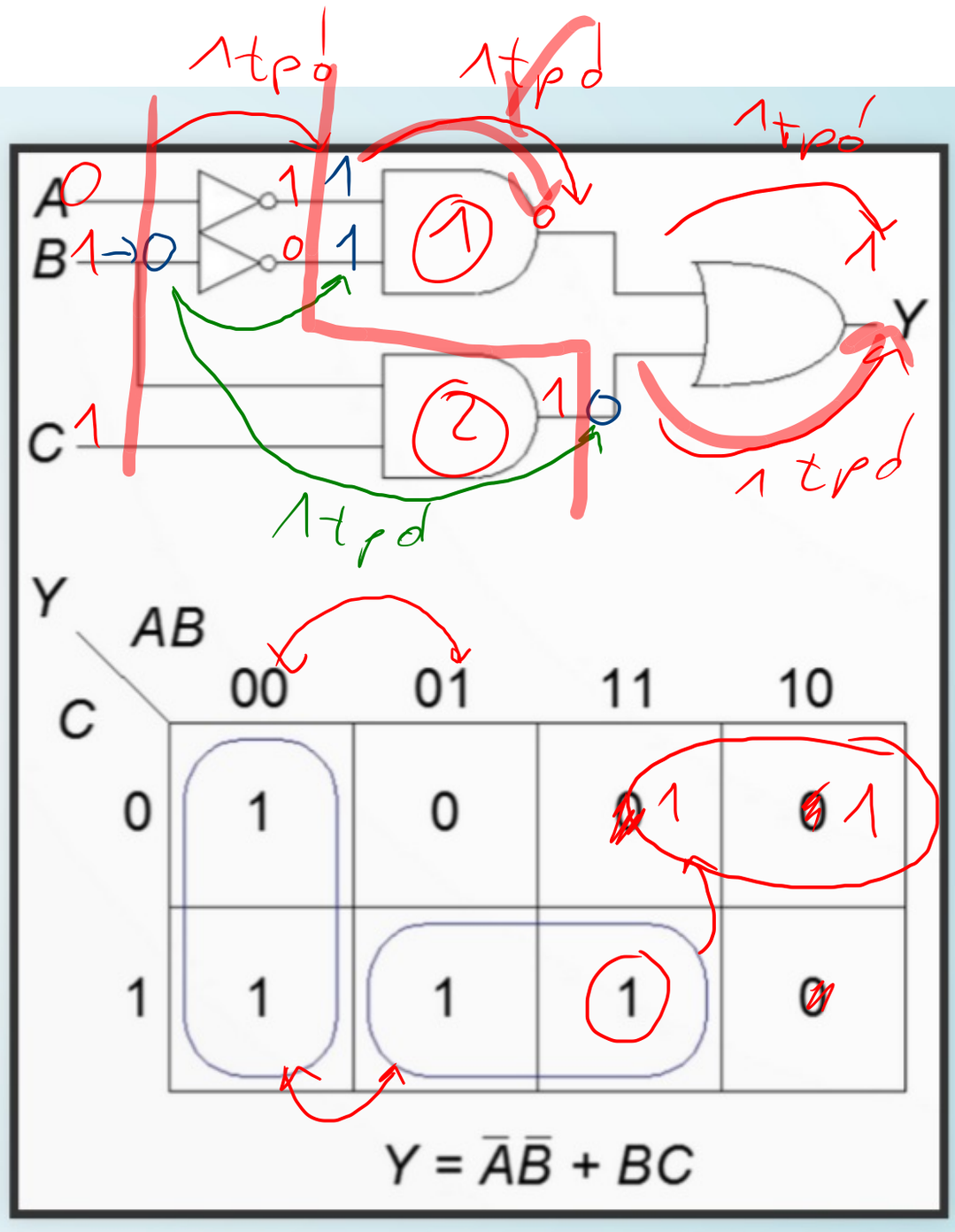
0
1
0

Y = 1

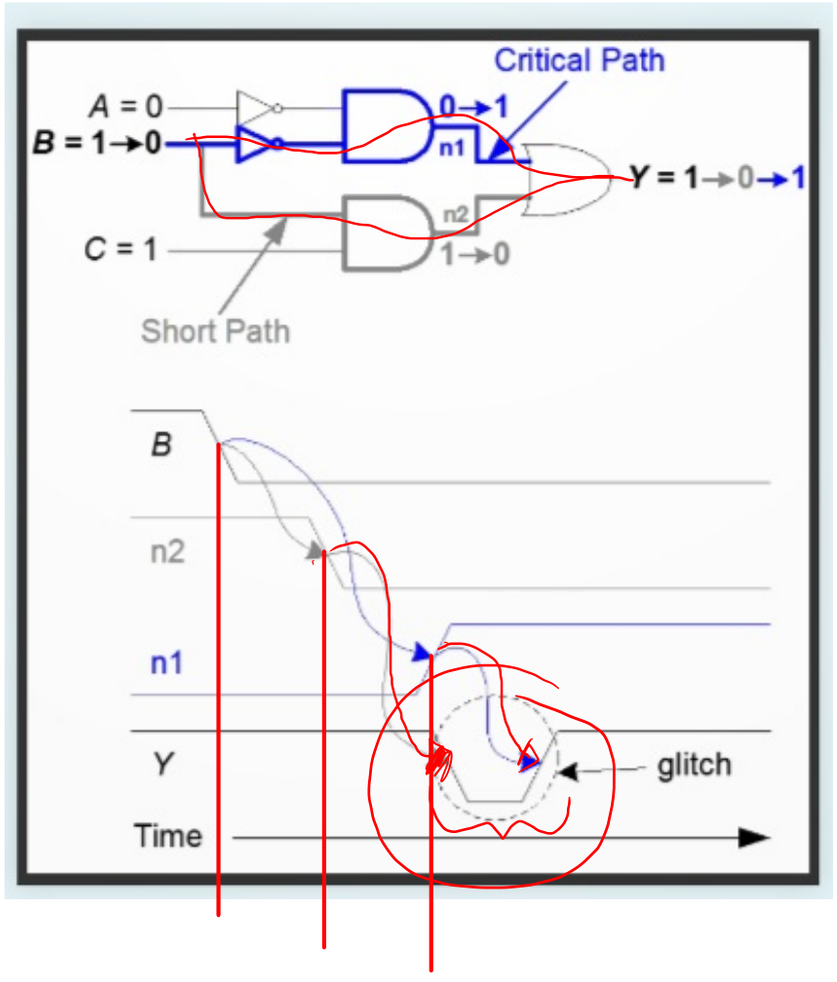
ABC = 001

ABC = 111

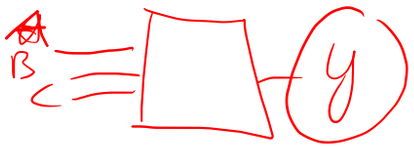
ABC = 110



Ejemplo Glitch


Critical Path
A = 0
B = 1→0
0→1
n1
Y = 1→0→1
n2
C = 1
1→0
Short Path
B
n2
n1
Y
glitch
Time

0 y
0 1
1


A
B
C
y

y 1→0→1