A 40 V 10 W 93%-Efficiency Current-Accuracy-Enhanced Dimmable LED Driver With Adaptive Timing Difference Compensation for Solid-State Lighting Applications

Dongkyung Park, Zhidong Liu, *Student Member, IEEE*, and Hoi Lee, *Senior Member, IEEE*

***Abstract*—This paper presents a floating-buck dimmable LED driver for solid-state lighting applications. In the proposed driver, an adaptive timing difference compensation (ATDC) is developed to adaptively adjust the off-time of the low-side power switch to enable the driver to achieve high accuracy of the average LED current over a wide range of input voltages and number of output LED loads, fast settling time, and high operation frequency. The power efficiency benefits from the capabilities of using synchronous rectifier and having no sensing resistor in the power stage. The synchronous rectification under high input supply voltage is enabled by a proposed high-speed and low-power gate driver with pseudo-digital level shifters. Implemented in a 0.35 μm 50 V CMOS process, experimental results show that the proposed LED driver can operate at 1 MHz and achieve peak power efficiency of 93% to support a wide range of series-connected output LEDs from 1 to 10 and a wide input range from 10 to 40 V. The proposed LED driver has only 2.8% current error from the average LED current of 345 mA and settles within 8.5 μs after triggering the dimming condition, improving the settling time by 14 times compared with the state-of-the-art LED drivers.**

***Index Terms*—Adaptive timing difference compensation (ATDC), average current regulation, floating-buck LED driver, floating-buck converter, high-voltage gate driver, LED driver, solid-state LED lighting.**

I. Introduction

In recent years, the rapid developments in high-brightness light-emitting diode (LED) technologies have enabled solid-state LED lighting to gradually replace the conventional incandescent and fluorescent lighting technologies because LEDs offer significantly better luminous efficacy, provide much longer lifetime and are environmentally friendly due to gas- and mercury-free construction [1], [2]. Higher luminous efficacy [i.e., larger ratio of the output luminous flux to the input electrical power (lm/W)] allows LED light bulbs to achieve the same brightness with much lower power dissipation, thereby achieving significant electricity saving. Since LED is a current-driven device and its brightness is proportional to the conduction current, a dc–dc-based high-current-accuracy LED driver is always needed to regulate current passing through LEDs for achieving constant luminous intensity under variations in input voltage and number of output LEDs in either ac- or battery-powered LED lighting systems as shown in Fig. 1. It should be noted that the ac-powered LED lighting systems typically involve a two-step approach: a pre-regulator shapes the input current to maximize the power factor, while the LED driver provides the current regulation and the dimming control of LEDs. To ensure proper operation of LED lighting systems, the design of the LED driver is crucial but challenging for concurrently satisfying many contradictory performance requirements.

For the traditional incandescent light bulb replacement, 1 W ($\sim$ 350 mA) white LEDs are commonly used based on luminous efficacy, color, and uniformity considerations. Since an individual 1 W LED can emit about 130 lumens of light as shown in Table I and a 60 W incandescent light bulb emits about 800 lumens, multiple LEDs should be used together to obtain the same brightness as the incandescent light bulb. Due to the circuit complexity of mitigating the LED current mismatch issue when driving several LEDs in parallel [3], [4], it is preferable to connect LEDs in series in high-brightness lighting applications. When LED drivers are either realized using buck or floating-buck topologies, they would have to support high input voltage due to the series connection of output LEDs and each 1 W LED having a typical forward voltage of 3 V. For robustness, the LED driver is essential to ensure the current accuracy in different LED lighting systems that may have different input voltages and various number of series-connected output LEDs. If the LED driver can also operate at a high switching frequency, the required value and volume of the off-chip inductor in the power stage can be reduced, allowing the converter to be compact enough to fit inside the Edison screw base of the light bulb. However, the difficulty of obtaining and regulating the LED/inductor current at high speed especially under high-input-supply voltage condition would limit the switching frequency of the LED driver. Due to the lack of the high-speed low-power high-side

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The authors are with the Department of Electrical Engineering, University of Texas at Dallas, Richardson, TX 75080 USA (e-mail: hoilee@utdallas.edu).

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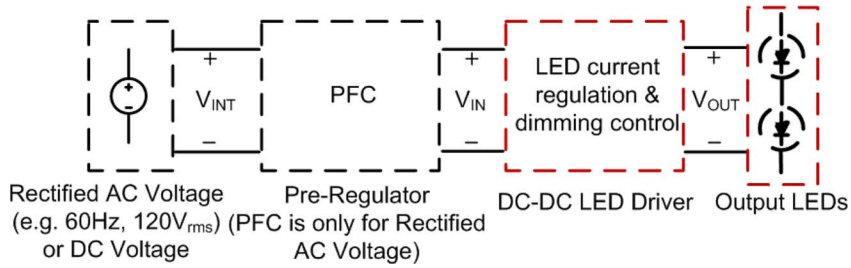

Fig. 1. Structure of a typical LED lighting system (note that the pre-regulator can be bypassed if input voltages of the system are obtained from a battery).

TABLE I
CHARACTERISTICS OF DIFFERENT LEDS FOR HIGH-BRIGHTNESS LIGHTING APPLICATIONS

LEDs			Lumens	Voltage	Power
Maker	Part Number	Color	@ LED current= 350mA	V_F (V)	(W)
Cree	XLamp XP-E	Cool White	130 (Typical)	3.00	1.05
Everlight	ELSW-F91CX	Cool White	90(Minimum)	2.95	1.03
LG Innotek	LEMWA33X75FW00	Daylight White	135(Typical)	3.00	1.05
Nichia	NS6W183B	White	143(Typical)	3.30	1.15
Osram Opto-Semi	LCW CQDP.EC	Cool White	121(Typical)	3.20	1.12
Philips LED	LUXEON LXML-PWC2	Cool White	135(Typical)	3.00	1.05
Samsung LED	SPHWHTL3D303E6R0H5	Daylight White	135(Typical)	3.10	1.09
Seoul Semi	SZ5-M0-W0-00	Cool White	142(Typical)	3.10	1.09
Sharp LED	GM2BB65QK0C	Cool White	50(Typical, @ 150mA)	2.95	0.44
Toyoda Gosei	E1SAP-YH0H4-0A	White	93(Typical)	3.35	1.17

gate driver and level shifters to enable on-chip synchronous rectification, an asynchronous power stage with a high-side power diode is commonly adopted in the high-input-voltage LED driver [5]–[8]. Off-chip high-voltage Schottky diodes could have a typical voltage drop of about 1 V that would decrease the power efficiency of the LED driver considerably especially under small number of series-connected output LEDs (small duty ratio of the converter due to low output voltage). Regarding dimming control, pulse-width-modulation (PWM) dimming is recommended by LED manufacturers to address the light color variation due to current amplitude modulation. High dimming frequency of a few kHz or above can mitigate the visible flickering issue caused by interaction between low dimming frequency and frame frequency of TVs [9]. To support high dimming frequency with a wide range of dimming duty ratios, the settling time of the LED driver should be sufficiently fast once the dimming condition is triggered in order to ensure the accuracy of the LED current especially in low dimming duty ratio conditions. The settling time depends on the controller design. The detailed relationship between the settling time and the LED current accuracy will be discussed in Section II. Tradeoffs among above performance requirements of the LED drivers on high current accuracy, high power efficiency, high operation frequency, and fast settling time would lead to suboptimal LED driver design.

Different control schemes have been previously reported in integrated LED drivers for regulating LED current in high-brightness lighting applications [5]–[8], [10], [11]. Peak-current control (PCC) [5], [6] and hysteretic-current control (HCC) [5], [7], [8] are two most accepted schemes to regulate the average LED current (I_{avg}). Fig. 2 shows these control schemes used in a floating-buck-based LED driver. Since the PCC scheme [Fig. 2(a)] can only provide the peak inductor/LED current information to the control loop, the value of I_{avg} would vary substantially under different input and output conditions due to the variations of the valley current [5]. The PCC scheme will also suffer from the subharmonic oscillation when the LED driver has a duty ratio larger than 0.5. Although the slope compensation can be applied to address the subharmonic oscillation in the PCC driver similar to the traditional peak-current-controlled voltage regulators [12]–[15], the LED current accuracy would be further degraded. By regulating both peak and valley LED currents, the HCC scheme can offer much better LED current accuracy than the PCC counterpart [5], [7], [8]. However, a sense resistor is needed in series with the inductor for detecting both peak and valley LED currents, as shown in Fig. 2(b). As large LED current flows through the sensing resistor for the entire switching period, the conduction power loss due to the sensing resistor in the HCC scheme is much larger than that in the PCC counterpart. Recently, adaptive off-time control [10], [11] was reported to approximate the valley bound of the LED current for achieving better current accuracy than the PCC offers and smaller conduction loss than the HCC provides. However, the reported SAR algorithm to implement the adaptive off-time scheme results in long calibration time and settling time of the LED current during dimming, limiting the current accuracy of the driver if the dimming frequency is high [10].

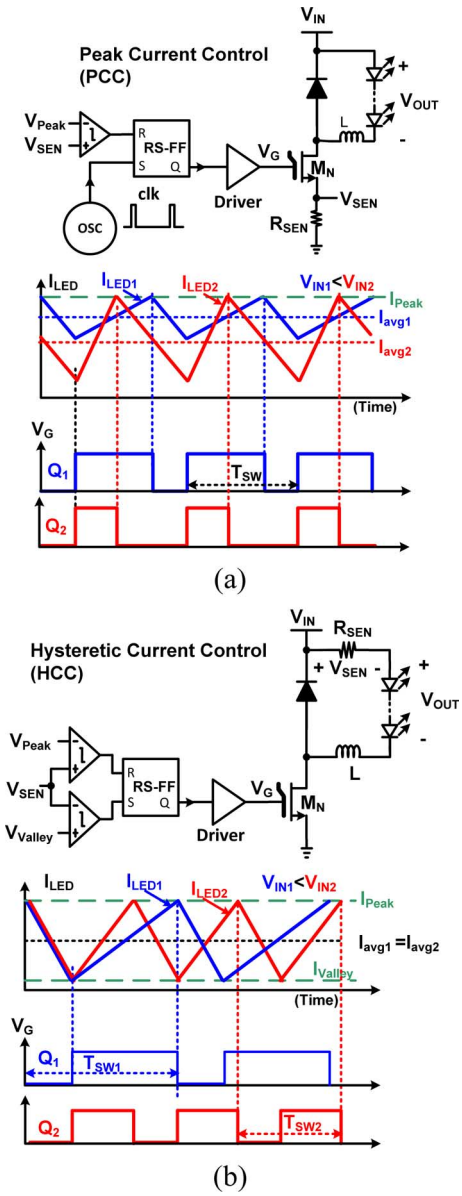

Fig. 2. Schematic and timing diagram of the control scheme under different input voltages for (a) PCC and (b) HCC LED drivers.

To mitigate above issues and concurrently achieve different performance requirements of the LED driver, a new control scheme: adaptive timing difference compensation (ATDC) is proposed to regulate $\mathrm{I_{avg}}$ for achieving: 1) high current accuracy; 2) fast settling time during dimming control; and 3) high converter operation frequency. A high-speed low-power synchronous gate driver is also developed to enable the proper operation of the synchronous rectifier in the driver power stage under high-frequency and high-input-voltage conditions. The proposed synchronous gate driver thus helps reduce the conduction power loss of the converter for better power efficiency. Adding to our prior literature [16], this paper details the design considerations and circuit implementations of the proposed ATDC LED driver. This paper is organized as follows. The operation of the driver, the control scheme, and the stability and settling time considerations are presented in Section II. Section III discusses circuit implementations of the proposed digital-based ATDC controller, gate driver and level-shifter designs, and the high-voltage current sensor design. Finally, measurement results and conclusions are given in Sections IV and V, respectively.

II. Proposed Dimmable ATDC LED Driver

A. Power Stage Architecture and Features

Fig. 3 shows the structure of the proposed LED driver. The power stage adopts the floating buck topology and consists of an on-chip synchronous rectifier with two high-voltage power transistors: low-side nMOS $(\mathrm{M_N})$ and high-side pMOS $(\mathrm{M_P})$ enabled by a proposed high-speed low-power synchronous gate driver. There exists a digital controller to realize the proposed adaptive timing-difference compensation (ATDC) for LED current regulation. The LED driver has also an on-chip low-side current sensor for detecting the peak LED current and adopts PWM dimming control. With on-chip synchronous rectifier and no sensing resistor in the power stage, significant conduction power loss can be saved in the proposed LED driver compared with the conventional high-voltage LED drivers shown in Fig. 2. Dead-time is introduced into the gate driving signals for power transistors $\mathrm{M_P}$ and $\mathrm{M_N}$ to minimize the shoot-through current during switching transitions and thus the short-circuit power loss of the LED driver. Although n-channel transistor is usually used as the high-side power device instead of p-channel counterpart because the n-channel device can be smaller in size for the same on-resistance, high dv/dt and di/dt noises at the switching node of the high-voltage power converter could couple to the high-side floating supply via the bootstrap capacitor and thus affect the reliability of the gate driver and the high-side n-channel power device [17]. The use of high-side power pMOS transistor can also save two additional off-chip components: a diode and a capacitor, which are needed to establish the floating supply in the high-side gate driver for the high-side power nMOS transistor [18].

For prolonging the lifetime of the LED driver, the proposed LED driver performs current regulation and does not require any electrolytic capacitor at the output terminal. Only a small-value ceramic output capacitor of 10 nF is used in the proposed LED driver. The proposed LED driver can also support high-frequency PWM dimming signal from "Dimming" input in Fig. 3 in order to adjust duty ratio of the dimming period for controlling brightness of output LEDs. In addition, the peak LED current information is needed in the ATDC scheme and it affects the power stage design. If a traditional buck topology is adopted as the power stage of the LED driver, sensing the low-side power nMOS [Fig. 4(a)] provides the valley current information. The peak LED current information can only be obtained through sensing the current passing through the high-side power pMOS as shown in Fig. 4(b). In high-input-voltage condition, the high-side current sensor would be difficult to achieve high sensing accuracy due to the supply noise coming from the crude PFC output in Fig. 1. In contrast, the floating-buck power stage enables the peak LED current information to be obtained by sensing the low-side power nMOS, simplifying the sensor implementation. In the proposed floating buck LED driver, a sensed voltage $\mathrm{V_{SEN}} = \mathrm{I_{SEN}} \times \mathrm{R_{SEN}} = (\mathrm{I_{LED}} \cdot \mathrm{R_{SEN}})/\mathrm{K}$,

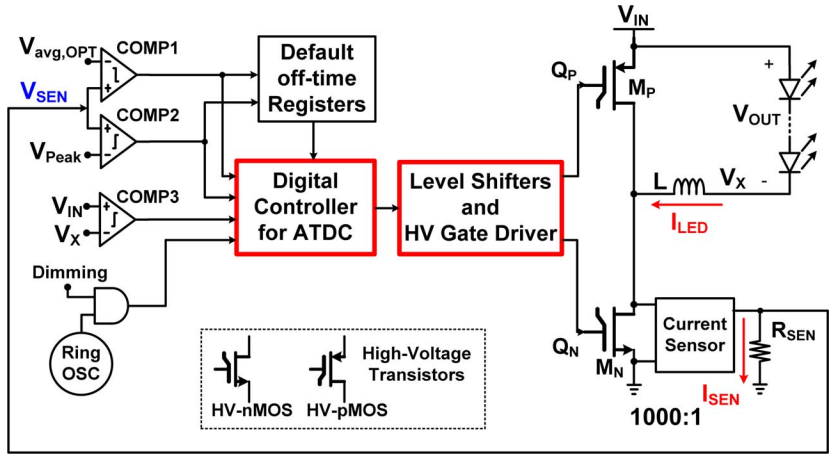

Fig. 3. Structure of the proposed dimmable ATDC LED driver.

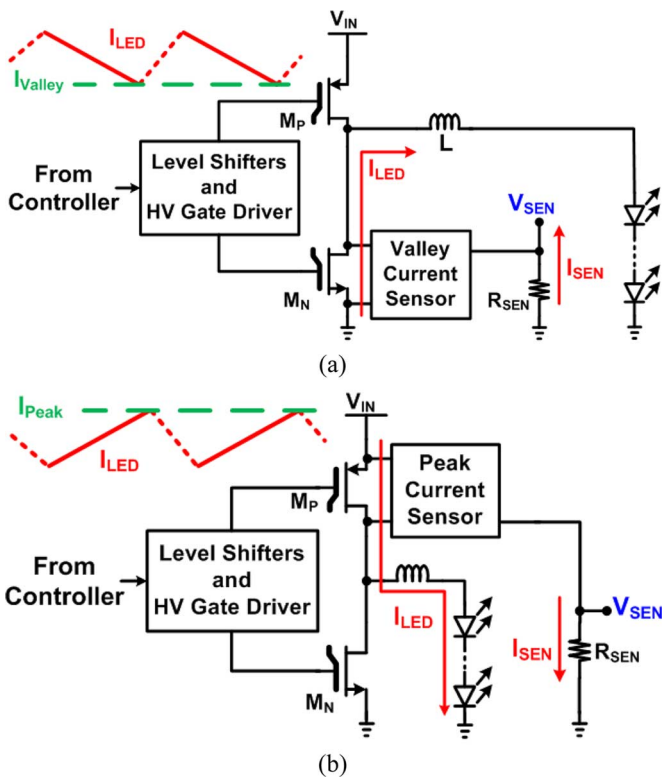

Fig. 4. Current sensing strategies in traditional buck converter for obtaining (a) valley LED current information through sensing low-side power nMOS $\mathrm{M_N}$ and (b) peak LED current information though sensing high-side power pMOS $\mathrm{M_P}$.

where $\mathrm{K} = 1000$ is used to provide the peak LED current information to the controller.

B. ADTC Control Scheme

The average LED current ($\mathrm{I_{avg}}$) in the floating-buck converter is given as

$$\begin{aligned} I_{\mathrm{avg}} &= I_{\mathrm{Peak}} - \frac{\Delta I_L}{2} \\ &= I_{\mathrm{Peak}} - \frac{V_{\mathrm{OUT}}}{2L} T_{\mathrm{off}} \\ &= I_{\mathrm{Peak}} - \frac{V_{\mathrm{IN}} - V_{\mathrm{OUT}}}{2L} T_{\mathrm{on}} \end{aligned} \tag{1}$$

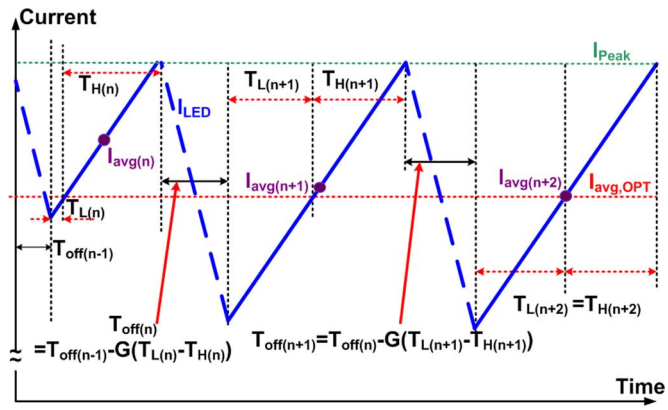

Fig. 5. Timing diagram of the inductor/LED current in the proposed ATDC scheme.

where I_{Peak} and ΔI_L are peak inductor/LED current and inductor/LED current ripple, respectively. L is the inductance used in the power stage, and T_{off} and T_{on} are off-time and on-time of power nMOS M_{N} in Fig. 3. From (1), if the input voltage V_{IN} of the driver changes or the number of output LEDs (thus output voltage V_{OUT}) varies, then the inductor current ripple ΔI_L and thus I_{avg} will be changed correspondingly, compromising the accuracy of the LED current. In order to maintain I_{avg} to a constant value for high current accuracy under variations of V_{IN} and V_{OUT}, T_{off} should be adjusted adaptively. Fig. 5 illustrates the proposed ATDC scheme to adjust T_{off} based on the timing diagram of the LED current. In Fig. 5, T_{H} and T_L are time durations that I_{LED} is higher and lower than the desired average current $I_{\mathrm{avg,OPT}}$, respectively. In order to achieve $I_{\mathrm{avg}} = I_{\mathrm{avg,OPT}}$, it needs to ensure $T_L = T_H$. The proposed ATDC scheme will thus adjust $T_{\mathrm{off(n)}}$ adaptively according to the following equation as

$$T_{\mathrm{off(n)}} = T_{\mathrm{off(n-1)}} - G \cdot \left(T_{L(n)} - T_{H(n)}\right) \tag{2}$$

where G is a gain constant dependent on the duty ratio of the driver and is selected by COMP3 in Fig. 3. As shown in Fig. 5, when $T_{L(n)} < T_{H(n)}$, it indicates that I_{avg} is larger than $I_{\mathrm{avg,OPT}}$ and the off-time $T_{\mathrm{off(n-1)}}$ of power transistor M_N in the previous switching cycle is smaller than the proper

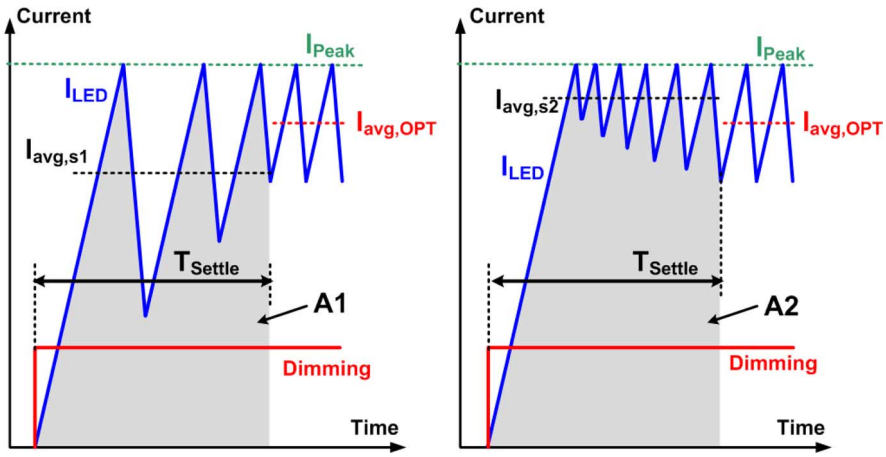

Fig. 6. Current offsets due to settling once dimming is triggered.

value. Therefore, the value $T_{\mathrm{off(n)}}$ of this switching cycle will be increased according to (2). Keeping on this process for a few switching cycles, the difference between $\mathrm{T_L}$ and T_H will be converged to 0 such that the off-time of power nMOS M_N settles to a constant value and I_{avg} reaches $I_{\mathrm{avg,OPT}}$. In case of $T_{L(n)} > T_{H(n)}$, $T_{\mathrm{off(n)}}$ will be decreased based on (2) and eventually results in $T_L = T_H$. It should be noted that the proposed ATDC scheme is realized by a digital controller with a typical clock frequency (dCLK) of 160 MHz. Since the maximum switching frequency of the proposed LED driver is 1 MHz, the digital controller is thus sufficiently fast to enable off-time calculation in every switching cycle (1 μs) of the converter under variations of input and output voltages. Additionally, the proposed ATDC scheme only needs a single low-side current sensor to detect the peak inductor/LED current for determining $T_H - T_L$.

C. Settling Time and Stability Considerations

Fig. 6 shows the settling behavior of the LED current once the PWM dimming signal is triggered. Fast settling time T_{Settle} is important not only to enable high dimming frequency but also to minimize the current difference between $I_{\mathrm{avg,s1}}$ (or $\mathrm{I_{avg,s2}}$) and $I_{\mathrm{avg,OPT}}$ during transient, where $I_{\mathrm{avg,s1}} = \text{shaded area A1}/\mathrm{T_{Settle}} < I_{\mathrm{avg,OPT}}$ and $I_{\mathrm{avg,s2}} = \text{shaded area A2}/\mathrm{T_{Settle}} > I_{\mathrm{avg,OPT}}$. Hence, fast settling time is important to improve the LED current accuracy especially under low dimming duty ratios of the short dimming period that give rise to larger current difference between $I_{\mathrm{avg,s1}}$ (or $I_{\mathrm{avg,s2}}$) and $I_{\mathrm{avg,OPT}}$.

To achieve fast settling time, the value of G in (2) should be maximized. However, if G is too large, the ATDC driver could suffer from the subharmonic oscillation due to too much increase or decrease in the next-cycle T_{off}. On the other hand, if the value of G is too small, it could take too long for the ATDC scheme to stabilize the average LED current to $I_{\mathrm{avg,OPT}}$ under perturbations of input or output voltages or sudden turning on the dimming signal, although the LED driver will be unconditionally stable. Therefore, the gain decision comparator (COMP3) is introduced in the proposed LED driver shown in Fig. 3 to simultaneously ensure stability and achieve the fast settling time under a wide range of input voltages and different

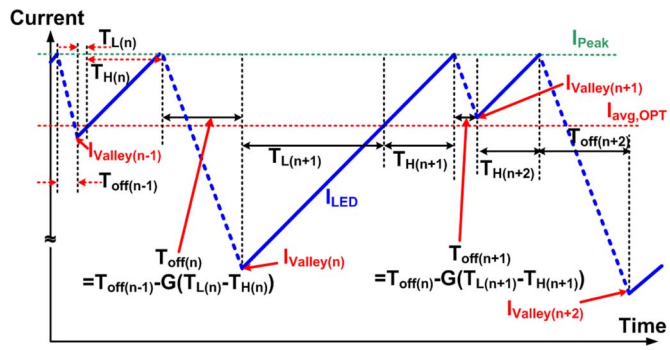

Fig. 7. Timing diagram of the LED current during subharmonic oscillation condition.

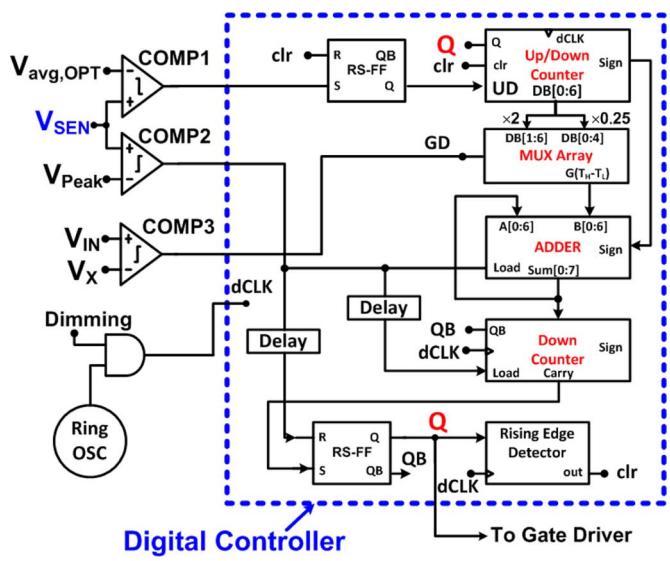

Fig. 8. Block diagram of the proposed ATDC scheme.

numbers of output LEDs. To design the appropriate value of G, the potential reason of instability in the ATDC scheme should be first understood and it is illustrated in Fig. 7. Assume that the output voltage ripple (ΔV_{OUT}) is much smaller than the value of V_{OUT} and the worst case $T_{L(n)}$ is about 0 in the steady state. If $T_{L(n)} = 0$ because off-time $T_{\mathrm{off(n-1)}}$ of the previous

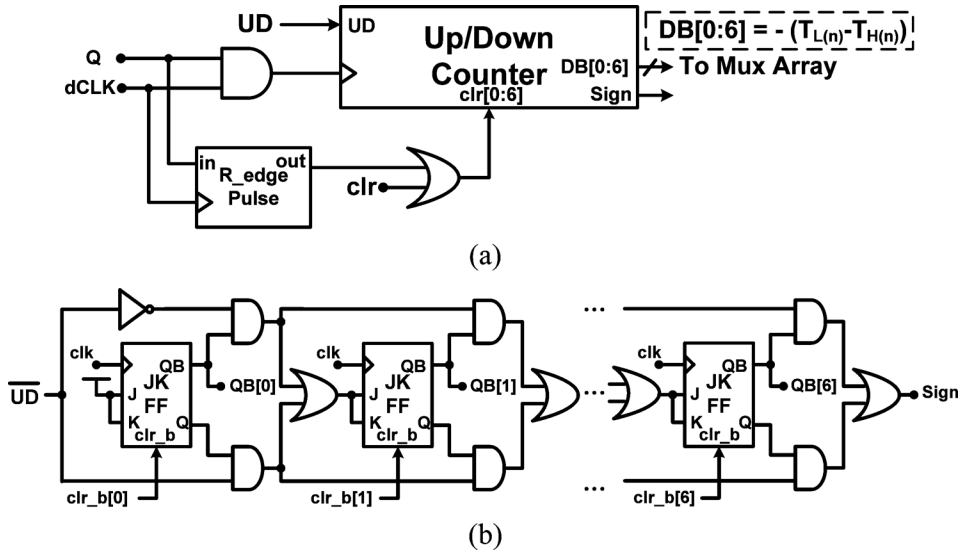

Fig. 9. (a) Structure and (b) schematic of the up/down counter.

cycle is too short, then next-cycle off-time will be set by the default off-time register in Fig. 3. Based on Fig. 7, $T_{\mathrm{off(n-1)}}$, $T_{H(n)}$ and $T_{H(n+1)}$ can be expressed as

$$\begin{aligned} T_{\mathrm{off(n-1)}} &= \frac{\Delta I \cdot L}{V_{\mathrm{OUT}}} \\ &= \frac{\Delta I \cdot L}{D \cdot V_{\mathrm{IN}}} \end{aligned} \tag{3}$$

$$\begin{aligned} T_{H(n)} &= T_{H(n+1)} \\ &= \frac{\Delta I \cdot L}{V_{\mathrm{IN}} - V_{\mathrm{OUT}}} \\ &= \frac{\Delta I \cdot L}{(1-D) \cdot V_{\mathrm{IN}}} \end{aligned} \tag{4}$$

where $\Delta I = I_{\mathrm{Peak}} - I_{\mathrm{avg,OPT}}$. By substituting (3) and (4) into (2), the off-time of the nth cycle is given as

$$T_{\mathrm{off(n)}} = \frac{\Delta I \cdot L}{V_{\mathrm{IN}}} \left(\frac{1}{D} + \frac{G}{1-D} \right). \tag{5}$$

Thus, the valley LED current $I_{\mathrm{Valley(n)}}$ at the nth cycle and $T_{L(n+1)}$ are given as

$$\begin{aligned} I_{\mathrm{Valley(n)}} &= I_{\mathrm{Peak}} - \frac{\mathrm{V_{OUT}}}{L} T_{\mathrm{off(n)}} \\ &= I_{\mathrm{Peak}} - \Delta I \left(1 + \frac{D \cdot G}{1-D} \right) \end{aligned} \tag{6}$$

$$\begin{aligned} T_{L(n+1)} &= \frac{L(I_{\mathrm{avg,OPT}} - I_{\mathrm{Valley(n)}})}{V_{\mathrm{IN}} - V_{\mathrm{OUT}}} \\ &= \frac{\Delta I \cdot D \cdot G \cdot L}{V_{\mathrm{IN}} (1-D)^2}. \end{aligned} \tag{7}$$

The valley inductor current $I_{\mathrm{Valley(n+1)}}$ at the $(n+1)$th cycle can then be derived as

$$\begin{aligned} I_{\mathrm{Valley(n+1)}} &= I_{\mathrm{Peak}} - \frac{D \cdot V_{\mathrm{IN}}}{L} T_{\mathrm{off(n+1)}} \\ &= I_{\mathrm{Peak}} - \frac{D \cdot V_{\mathrm{IN}}}{L} \\ &\quad \times \left(T_{\mathrm{off(n)}} - G \left(T_{L(n+1)} - T_{H(n+1)} \right) \right). \end{aligned} \tag{8}$$

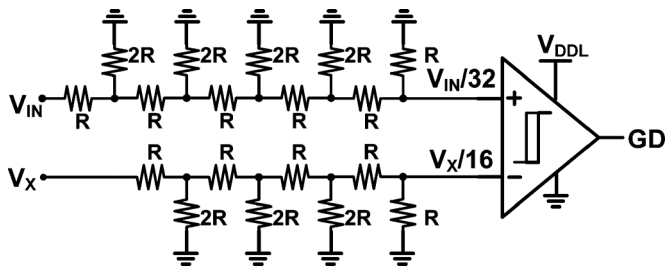

Fig. 10. Schematic of the gain decision comparator (COMP 3).

Substituting (4), (5), and (7) into (8), $I_{\mathrm{Valley}(n+1)}$ can also be expressed and simplified as

$$\begin{aligned} &I_{\mathrm{Valley}(n+1)} \\ &= I_{\mathrm{Peak}} - \frac{D \cdot V_{\mathrm{IN}}}{L} \left[\frac{\Delta I \cdot L}{V_{\mathrm{IN}}} \left(\frac{1}{D} + \frac{G}{1-D} \right) - G \right. \\ &\qquad \left. \cdot \left(\frac{\Delta I \cdot D \cdot G \cdot L}{V_{\mathrm{IN}}(1-D)^2} - \frac{\Delta I \cdot L}{V_{\mathrm{IN}} \cdot (1-D)} \right) \right] \\ &= I_{\mathrm{avg,OPT}} - D \cdot \Delta I \left(\frac{2G}{1-D} - \frac{\mathrm{DG}^2}{(1-D)^2} \right). \end{aligned} \tag{9}$$

From Fig. 7, if $I_{\mathrm{Valley}(n+1)}$ is larger than $I_{\mathrm{Valley(n-1)}}$ or $I_{\mathrm{Valley}(n+2)}$ is smaller than $I_{\mathrm{Valley}(n)}$, then the average LED current would diverge from the desired value, leading to the subharmonic oscillation in the system (the oscillation frequency is half of the switching frequency of the driver). By using (9), to guarantee system stability, the maximum value of G should be chosen by ensuring $I_{\mathrm{Valley}(n+1)} \leq I_{\mathrm{avg,OPT}}$ and is given as

$$\begin{aligned} I_{\mathrm{Valley}(n+1)} &= I_{\mathrm{avg,OPT}} - D\Delta I \left(\frac{2G}{1-D} - \frac{\mathrm{DG}^2}{(1-D)^2} \right) \\ &\leq I_{\mathrm{avg,OPT}} \\ &\Rightarrow G \leq \frac{2(1-D)}{D}. \end{aligned} \tag{10}$$

Since the duty ratio D can vary in a wide range from 0.15 to 0.825 under different input voltages and different numbers of

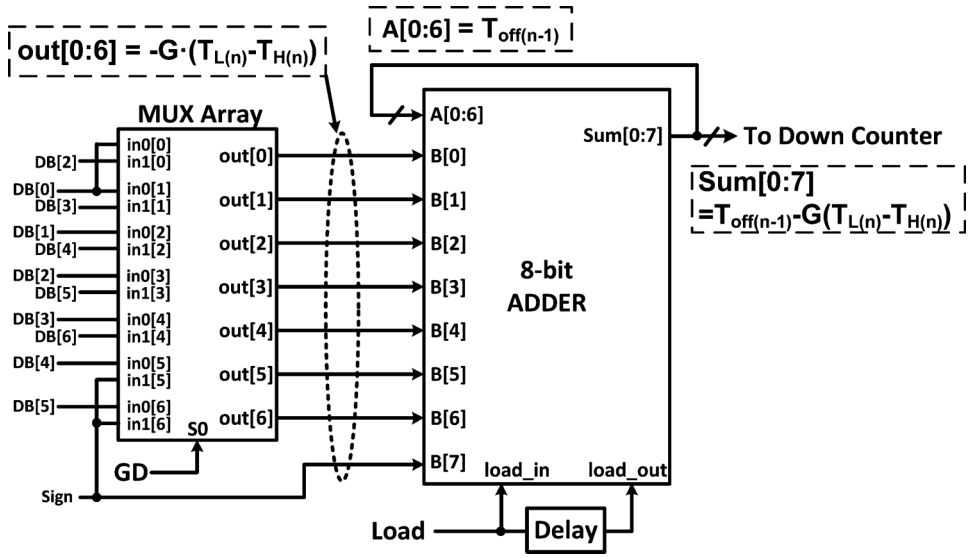

Fig. 11. Block diagram of MUX array and 8-bit adder.

output LEDs in this design, two separate values of G are designed corresponding to D larger and smaller than 0.5 in order to optimize the settling time. For example, the upper bound of G in (10) is 0.424 that corresponds to $D = 0.825$, so G is set to 0.25 in this design whenever D is detected to be larger than or equal to 0.5. Similarly, the upper bound of G becomes 2 at $D = 0.5$. The value of G is thus set to 2 to ensure the system stability for $D < 0.5$. Values of 0.25 or 2 will be selected automatically using the digital controller in Fig. 3 based on the output of COMP3. In this case, the proposed ATDC scheme can provide good settling time while always satisfying the worst-case stability condition.

III. Circuit Implementations

A. Digital Controller for Adaptive Timing Difference Compensation

Fig. 8 shows the block diagram of the digital controller that implements the proposed ATDC scheme. The controller mainly consists of an up/down (U/D) counter, a MUX array, an 8-bit adder, a down counter, and RS latches. When the dimming signal is asserted, Q becomes logic "1" and LED current $I_{\rm LED}$ ramps up while U/D counter starts counting up after resetting clr[0:6] register, as shown in Fig. 9(a). The U/D counter is implemented by using JK flip-flops with combinational logic circuits and its schematic is shown in Fig. 9(b). U/D counter is designed to count up for input UD $=$ ``0" and down for input UD $=$ ``1". When the comparator COMP1 detects the point at which the sensed voltage $V_{\rm SEN}$ becomes larger than $V_{\rm avg,OPT} (= I_{\rm avg,OPT} \times R_{\rm SEN}/1000)$, UD signal changes from "0" to "1", causing the U/D counter starts counting "down" while $\rm V_{SEN}$ keeps on increasing. When the comparator COMP2 detects the point at which $V_{\rm SEN}$ reaches $V_{\rm Peak}$ $(= I_{\rm Peak} \times R_{\rm SEN}/1000)$, the power nMOS transistor M_N is turned off and the register DB[0:6] in the U/D counter stores the information of $T_H - T_L$ in (2).

As discussed previously, the gain G will be selected to either 0.25 or 2 dependent on the duty ratio D of the LED driver. Fig. 10 shows schematic of the gain decision comparator, which consists of two R-2R voltage dividers and a hysteresis comparator. Since the hysteresis comparator is realized by using standard low-voltage CMOS transistors with their maximum gate-to-source voltage of 3.3 V, both $V_{\rm IN}$ and V_X are scaled down to below 3.3 V to prevent the input transistors of the hysteresis comparator from gate oxide breakdown. For chip area and device matching considerations, R-2R ladder dividers are used and the comparator compares $V_{\rm IN}/32$ with $V_X/16$ at its input terminals. When $V_{\rm IN}/32 > V_X/16$, it implies $D > 0.5$ and thus GD is set to logic "1" to make the value of G to be 0.25. On the other hand, the output of the gain decision comparator GD becomes logic "0" such that G is set to 2.

Fig. 11 shows the block diagram of the MUX array and the 8-bit adder to illustrate the mechanism of multiplication and addition for (2). Specifically, the multiplication of $(T_H - T_L)$ and G is performed by the shifted input connection of the MUX array instead of using any arithmetic logic unit that would occupy a large chip area and dissipate considerable power. The MUX array selects the value of G based on the input selection signal GD. When GD is "1", the MUX array makes a 2-bit LSB-side shifted connection of DB[0:6] to become DB[0:4] such that the output of MUX array (out[0:6]) is set to $0.25 \bullet (T_H - T_L)$. When GD is "0", 1-bit MSB-side connection is made to give out[0:6] $= 2 \cdot (T_H - T_L)$ as shown in Fig. 11. After that, the value $G \cdot (T_H - T_L)$ will be transferred to the 8-bit adder through the input B[0:6] when the load_in signal is asserted. The input A[0:6] that represents the previous-cycle off-time information $(T_{\rm off}(n-1))$ is an unsigned number and B[0:7] is a signed number with B [7] as the sign bit. After the summation of A[0:6] and B[0:6], the off-time at the nth cycle $({\rm Sum}[0:7] = T_{{\rm off}(n)})$ will be loaded to the down counter in Fig. 8 by the load_out signal. The down counter is implemented using the same structure as Fig. 9(b). While the value of the down counter is positive after Sum[0:7] value is loaded into

TABLE II
PERFORMANCE COMPARISONS OF DIFFERENT LED DRIVERS

	ZXLD1350 2011 [7]	ZXLD1350 2011 [7]	CAT4201 2011 [8]	TCAS I 2010 [10]	**This work**
Switching Frequency (kHz)	≤200 @ 7 LEDs	≤550 @ 7 LEDs	380	~188	**≤1000**
Input Voltage (V)	6 – 30	6 – 30	6.5 – 36	8 – 40	**10 – 40**
Max. LED Current (mA)	N. A.*	N. A.*	N. A.*	1500	**500**
Typical Average Current (mA)	350	350	300	720	**345**
Worst-Case Settling Time (μs)	N. A.*	N. A.*	N. A.*	120	**8.5**
Dimming Frequency (Hz)	N. A.*	N. A.*	N. A.*	500	**10,000**
Peak Efficiency (%)	95	92	90 (2 LEDs)	94.3	**93**
Current Error (mA)	32 (no. of LEDs: 1 – 7) @ V_{IN} = 30V	77 (no. of LEDs: 1 – 7) @ V_{IN} = 30V	N. A.*	14.5 (no. of LEDs: 5 – 8)	**9.6 (no. of LEDs: 5 - 10) @ V_{IN} = 40V 18.7 (no. of LEDs: 2 - 10) @ V_{IN} = 40V**
Inductor (μH)	100	47	22 – 56	33	**10 – 39**
Max. No. of Drivable LEDs	~ 8	~ 7	~ 9	8	**10**
Fabrication Process	N. A.*	N. A.*	N. A.*	UMC 0.35-μm HV CMOS	**AMS 0.35-μm 50V CMOS**

* N. A. stands for not available.

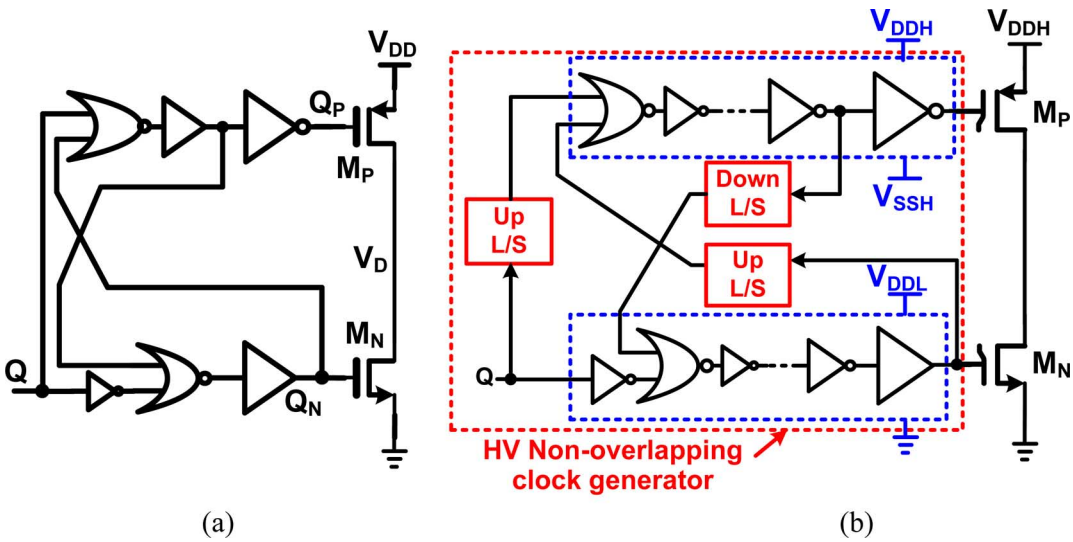

Fig. 12. (a) Traditional low-voltage gate driver design and (b) the proposed high-voltage gate driver.

the counter, power nMOS transistor M_N is turned off and the LED current is ramping down. When the Down counter output becomes "0", the LED current reaches its valley value, transistor M_N is turned on and signal Q in Fig. 8 becomes logic "1" again to repeat the same process described above. The operation of the digital controller will continue until $T_L = T_H$ (i.e., $I_{\text{avg}} = I_{\text{avg,OPT}}$).

B. High-Voltage Gate Driver and Pseudo-Digital Level Shifter

The short-circuit power loss increases with the switching frequency and the input supply voltage in the synchronous switched-mode power converters.

Therefore, the nonoverlapping clock generator (NOCG) that minimizes the shoot-through current of power transistors becomes more important in high-supply-voltage conditions. Fig. 12(a) presents the structure of a typical low-voltage NOCG to generate proper dead-time during switching transitions of power transistors for minimizing the short-circuit conduction loss. However, as the input supply voltage of the proposed driver can be as high as 40 V and the maximum gate-to-source breakdown voltage of HV CMOS transistors is only 3.3 V, the structure in Fig. 12(a) is not appropriate for generating a small differential high-side signal swing (1.5 V in this design) referenced to the high common-mode supply voltage V_{IN}. A high-voltage NOCG shown in Fig. 12(b), which includes three additional level shifters, is thus developed. It is crucial to ensure these level shifters to have fast speed for minimizing the propagation delay of the gate driver while dissipating low power.

Fig. 13(a) shows the structure of the proposed UP level shifter. The core circuit M_1–M_4 shifts up the input signal from $(\text{GND} - V_{\text{DDL}}: 0\text{–}3\text{ V})$ to $(V_{\text{SSH}} - V_{\text{DDH}} : (V_{\text{IN}} - 1.5\text{ V}) - V_{\text{IN}})$.

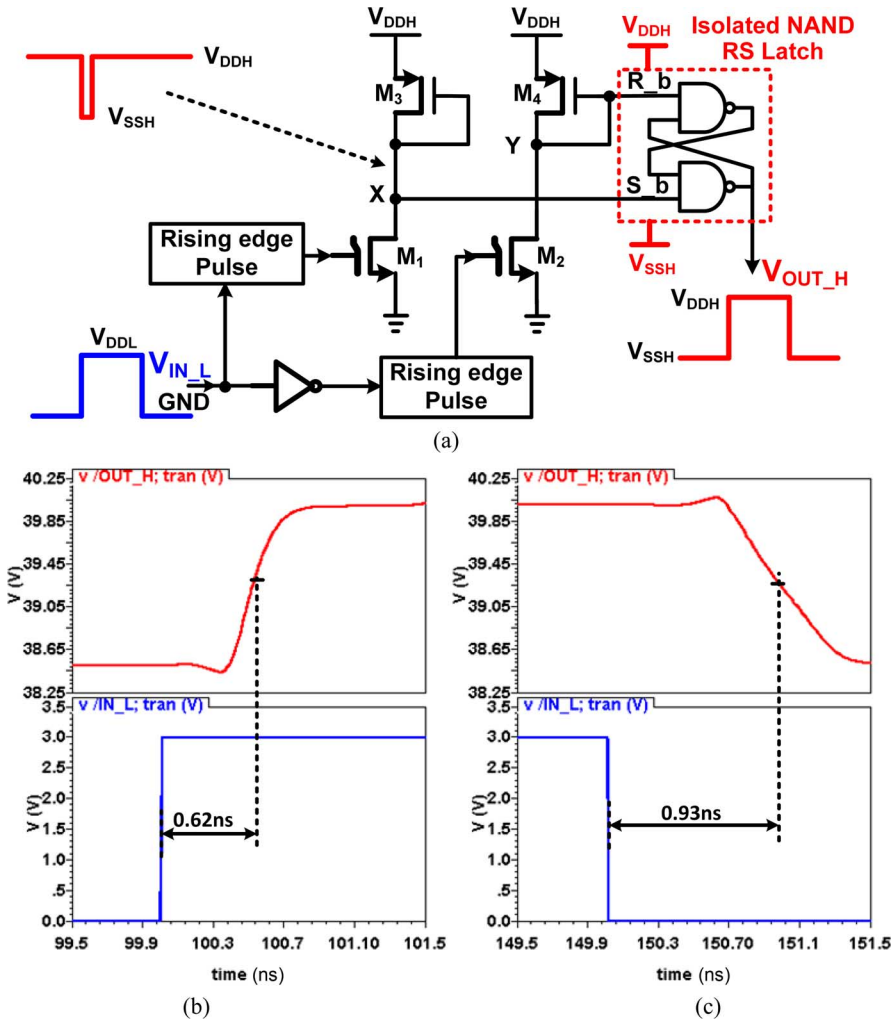

Fig. 13. Proposed UP-level shifter. (a) Schematic. (b), (c) Simulation results.

Transistors M_3 and M_4 are realized by low-voltage pMOS transistors in an isolated well, while transistors M_1 and M_2 are implemented by HV nMOS transistors to sustain high voltage. When transistor M_1 (M_2) is turned on, transistors M_1 and M_3 (M_2 and M_4) are all operated in the saturation region. By neglecting the channel length modulation, device sizes $(W/L)_{1,2}$ and $(W/L)_{3,4}$ can be designed to satisfy the following condition:

$$V_{\mathrm{DDH}} - V_{\mathrm{SSH}} = V_{\mathrm{SG3,4}} = \sqrt{\frac{\mu_{\mathrm{nH}} C_{\mathrm{OXnH}} (W/L)_{1,2}}{\mu_p C_{\mathrm{OXp}} (W/L)_{3,4}}} \times (V_{\mathrm{DDL}} - V_{\mathrm{thnH}}) + |V_{\mathrm{thp}}| \quad (11)$$

where μ_{nH}, μ_p, V_{thnH}, and V_{thp} are the mobility and threshold voltages of transistors $M_{1,2}$ and $M_{3,4}$, respectively. Diode-connected transistors M_3 and M_4 lower the output impedance of the level-shifting core circuit for delay minimization and make transistors M_1 and M_2 stay in the saturation region when either M_1 or M_2 is on. Two short-pulse generators are placed at inputs of the core circuit in order to reduce the conduction time of the core circuit to be much shorter than the on-time of the input signal. The core circuit is thus pseudo-digital in nature and the average current consumption of the level shifter can be significantly reduced. The rising edge of input signal $V_{\mathrm{IN\_}L}$ enables the generation of a short pulse at node X swinging between V_{SSH} and V_{DDH} through the branch involving transistors M_1 and M_3, while the falling edge of $V_{\mathrm{IN\_}L}$ generates a short pulse at node Y through transistors M_2 and M_4. The signal recovery circuitry using a NAND-based SR latch then converts up-shifted short-pulsed signals at nodes X and Y to signal $V_{\mathrm{OUT\_}H}$ that has the same on-time as the original input signal $V_{\mathrm{IN\_}L}$ for driving high-side power transistor M_P via logic gates and buffers. Simulation results in Figs. 13(b) and (c) show that the proposed level shifter achieves the worst-case propagation delay of 0.93 ns and only dissipates 2.7 μW/MHz for up shifting from low-voltage region (0–3 V) to high-voltage region (38.5–40 V). Compared with [19], both delay and power dissipation of the proposed level shifter are reduced by 2.3 times and 30%, respectively. The down level shifter in Fig. 12(b) is realized similar to the proposed Up level shifter by just flipping pMOS and nMOS transistors in the Up level shifter.

C. High-Voltage Peak Current Sensor

To sense the peak LED current, filter-based current sensing that senses current through the inductor ESR is possible but is

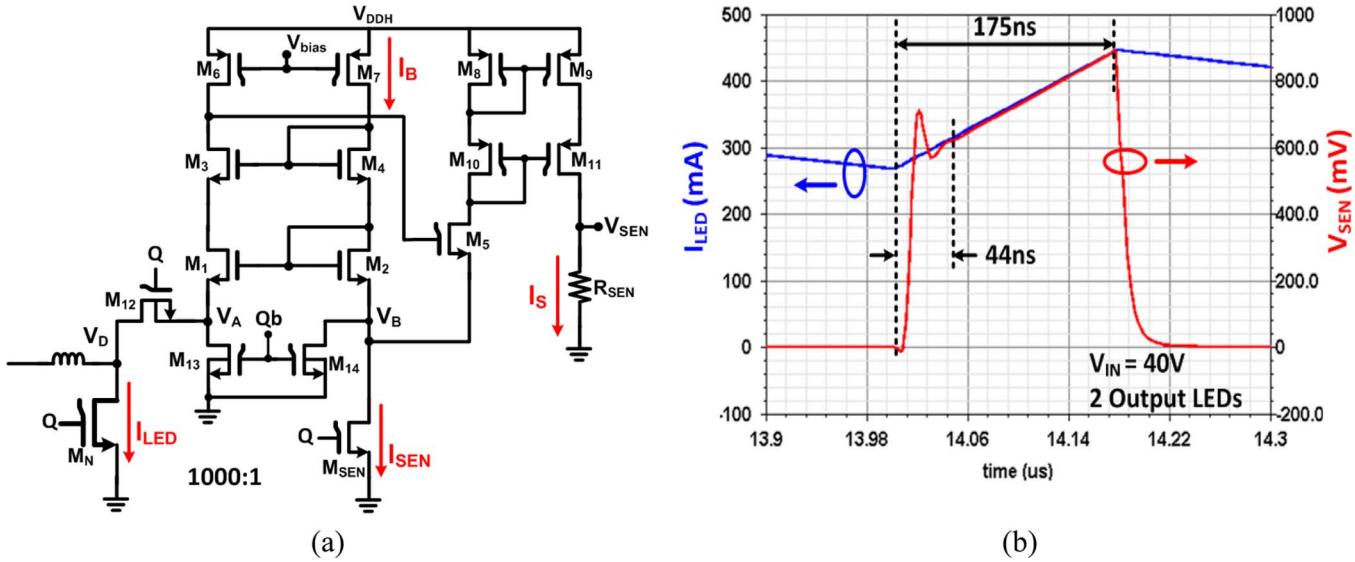

Fig. 14. (a) Schematic and (b) simulated performance of the high-voltage current sensor for sensing LED current.

susceptible to PVT variations of the filter components according to [20]. Hence, sense-FET approach is adopted for the current sensing. Fig. 14(a) shows the schematic of the on-chip HV peak current sensor for sensing current through nMOS power switch $\mathrm{M_N}$ in the floating buck converter. This current sensor is improved from the LV low-side valley current sensor in the traditional buck converter [15] by considering the reliability of transistors under high input supply voltages and the sensing operation difference between the ramp-up and the ramp-down portions of the inductor current. The proposed sensor consists of a HV sensing transistor $\mathrm{M_{SEN}}$ that is the same type as power nMOS $\mathrm{M_N}$ for better device matching. In the sensor, there are also a voltage mirror realized by isolated low-voltage nMOS transistors $\mathrm{M_1}$–$\mathrm{M_4}$ to force voltage at V_A equal to V_B; a current source realized by HV transistors $\mathrm{M_6}$ and $\mathrm{M_7}$ to provide bias current $\mathrm{I_B}$ for the voltage mirror; a source follower $\mathrm{M_5}$; a cascoded current mirror realized by HV pMOS transistors $\mathrm{M_8}$–$\mathrm{M_{11}}$; and a sense resistor $\mathrm{R_{SEN}}$ of 2 kΩ to convert sense current $\mathrm{I_S}$ to voltage V_SEN for the ATDC controller. When $\mathrm{M_N}$ is on, the current sensor monitors $\mathrm{I_{LED}}$ to provide the sensed voltage V_SEN for the current regulation. When $\mathrm{M_N}$ is off, HV transistor $\mathrm{M_{12}}$ is turned off to isolate $V_D = V_\mathrm{DDH}$ from V_A, while transistors $\mathrm{M_{13}}$ and $\mathrm{M_{14}}$ are turned on to establish a path for the biasing current I_B from the current source $\mathrm{M_6}$ and $\mathrm{M_7}$ and thus keeping the sensor active. The device aspect ratio of $\mathrm{M_{SEN}}$ is designed to be 1000 times smaller than that of $\mathrm{M_N}$ such that the drain current I_SEN through $\mathrm{M_{SEN}}$ will be equal to 1/1000 of I_LED if $V_\mathrm{B} = V_D$ when $\mathrm{M_N}$ is on. Voltage $\mathrm{V_{SEN}} = I_\mathrm{S} \times \mathrm{R_{SEN}} = (I_\mathrm{SEN} - I_\mathrm{B}) \times \mathrm{R_{SEN}} \approx I_\mathrm{SEN} \times \mathrm{R_{SEN}}$ then carries scaled I_LED information if $I_\mathrm{SEN} >> I_\mathrm{B}$. Similar to [14], the current sensing accuracy is determined by the matching between V_D and V_B in Fig. 14(a) and is in turn dependent on the loop-gain magnitude of the negative feedback loop realized by transistors $\mathrm{M_1}$–$\mathrm{M_5}$. The cascoded mirror $\mathrm{M_1}$–$\mathrm{M_4}$ increases the output resistance at the drain terminal of $\mathrm{M_3}$ and thus the loop-gain magnitude for better sensing accuracy. As the voltage difference between the drain terminal of transistor $\mathrm{M_5}$ and the node V_SEN is large, the cascoded current mirror structure realized by transistors $\mathrm{M_8}$–$\mathrm{M_{11}}$ minimizes the channel-length modulation of transistors to further improve the current sensing accuracy. Simulation results show that the current sensor consumes static current of 60 μA and settles within 44 ns in the worst-case condition when $V_\mathrm{IN} = 40$ V and the driver output has two series-connected LEDs as shown in Fig. 14(b). The sensing error of the peak value of V_SEN is only 0.79% compared with the desired value.

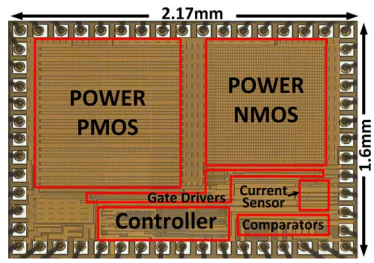

Fig. 15. Micrograph of the proposed dimmable LED driver.

IV. Experimental Results and Discussions

The proposed LED driver has been implemented in a 0.35 μm 50 V CMOS process. Fig. 15 shows the micrograph of the proposed driver whose total chip area is 3.47 mm^2 including all bonding pads. Most of the chip area is occupied by the large-size power transistors $\mathrm{M_P}$ and $\mathrm{M_N}$ and the area of ATDC digital controller is only about 27% of the power pMOS area. Cree XB-D white LEDs are used for the testing. The typical and maximum forward voltages of each Cree XB-D white LED are 3 and 3.5 V at 350 mA of LED current, respectively. The proposed LED driver was designed to support the input voltage V_IN ranging from 10 to 40 V and operate at a switching frequency of up to 1 MHz. The driver delivers a typical average current of 345 mA and can drive series-connected LEDs from 1 to 10.

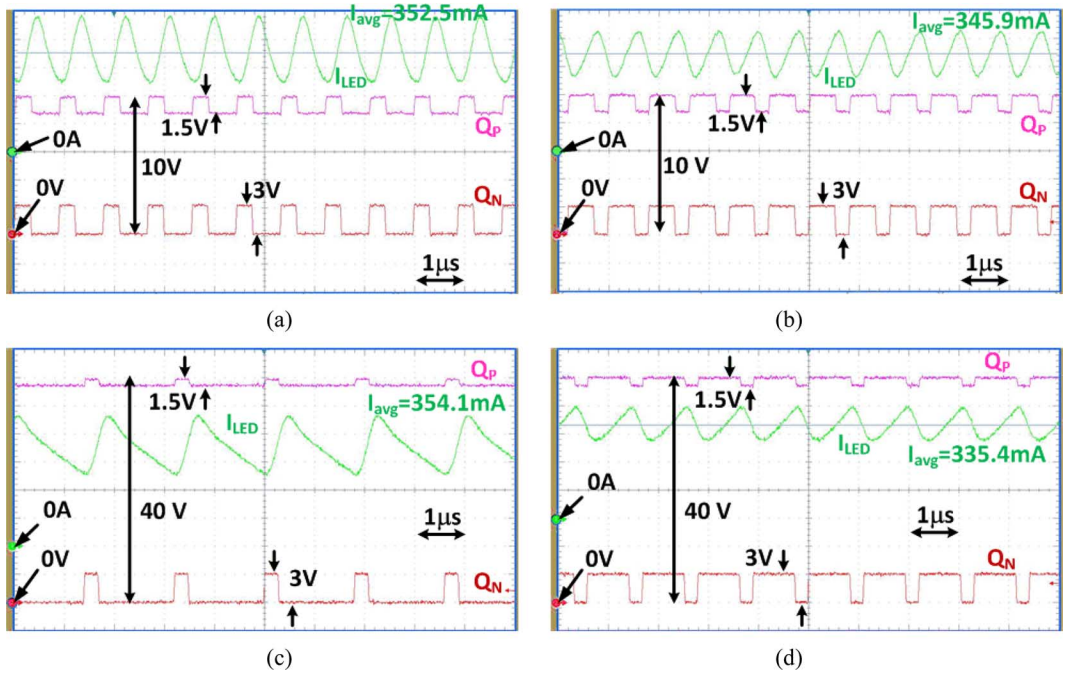

Fig. 16. Waveforms of the proposed LED driver under (a) $V_{\rm IN}$ = 10 V and one-load LED, (b) $V_{\rm IN}$ = 10 V and two-load LEDs, (c) $V_{\rm IN}$ = 40 V and two-load LEDs, and (d) $V_{\rm IN}$ = 40 V and ten-load LEDs.

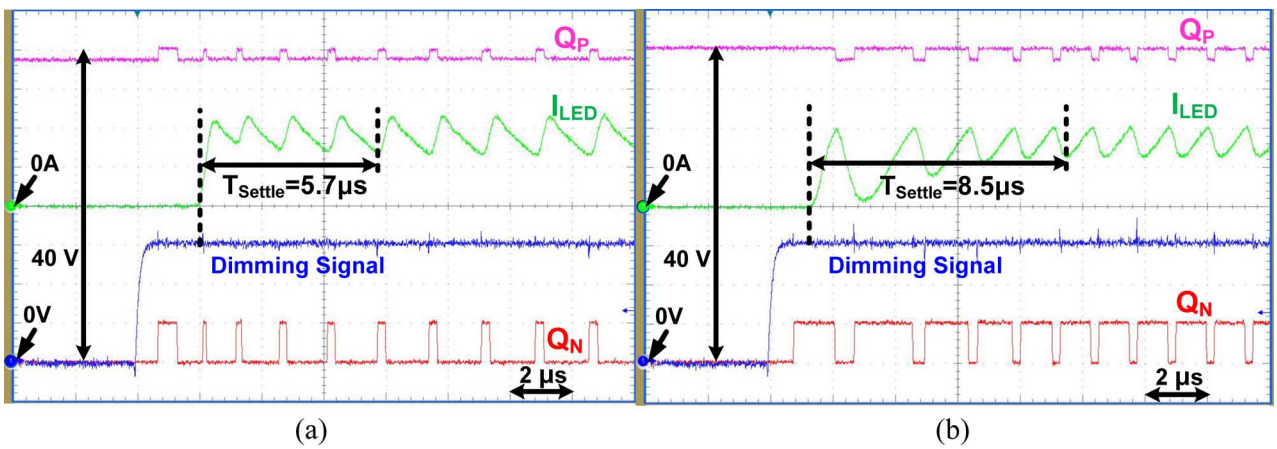

Fig. 17. Measured settling time after triggering dimming signal under $V_{\rm IN}$ = 40 V and (a) two-load LEDs or (b) ten-load LEDs.

Fig. 16(a)–(d) shows different measured oscilloscope waveforms under different input voltages and different number of output LEDs. The waveforms verify that the proposed driver functions correctly under different input voltages and duty ratios of smaller and larger than 0.5. It should be noted that the differential gate swings for driving power transistors $\rm M_P$ and $\rm M_N$ are 1.5 and 3 V, respectively. As the size of $\rm M_P$ and thus its input capacitance are much larger than those of $\rm M_N$, a smaller differential signal swing for $\rm M_P$ helps reduce its gate drive power loss that is proportional to the square of the differential gate swing. The measured waveforms further prove the proper operation of the proposed level shifter and gate driver.

Fig. 17 shows the measured settling behavior of the LED current in the proposed LED driver after sudden turning on the dimming signal. The settling behavior of the LED current is similar to the scheme shown in Fig. 6 with two extreme load conditions at the smallest number of LEDs (smallest duty ratio) [Fig. 17(a)] and the largest number of LEDs (highest duty ratio) [Fig. 17(b)]. The worst-case settling time is only 8.5 μs, which enables the fast dimming frequency of 10 kHz, supports a wide range of the dimming signal duty ratio, and minimizes the current error due to settling. Fig. 18 further shows the measured waveforms of the proposed LED driver under different duty ratios of the dimming signals. The range of the dimming duty ratio that controls the brightness of LED light bulbs is from 20% to 100%.

Fig. 19(a) shows the measured power efficiency of the proposed LED driver under different input voltages and different number of output LEDs. For the same number of output LEDs, the power efficiency is higher under a lower input voltage due to the larger duty ratio of the LED driver. Similarly, for the same input voltage, the power efficiency increases with number of output LEDs due to the increase in the output power level. The proposed LED driver can achieve the maximum power efficiency of 92.5% under $V_{\rm IN}$ = 40 V and ten series-connected

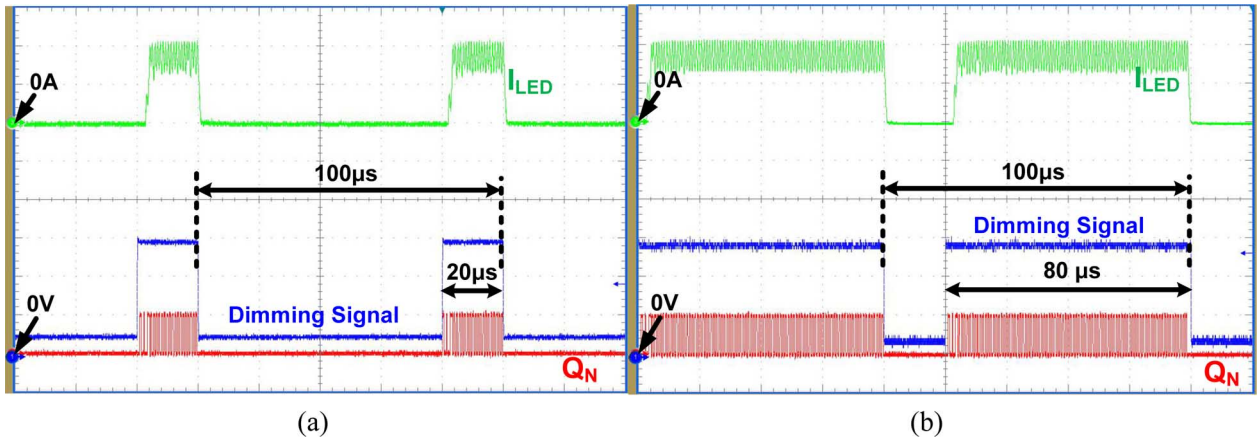

Fig. 18. Measured gate voltage of power nMOS Q_N and LED current under different duty ratios (a) 20% and (b) 80% of a 10 kHz PWM dimming signal.

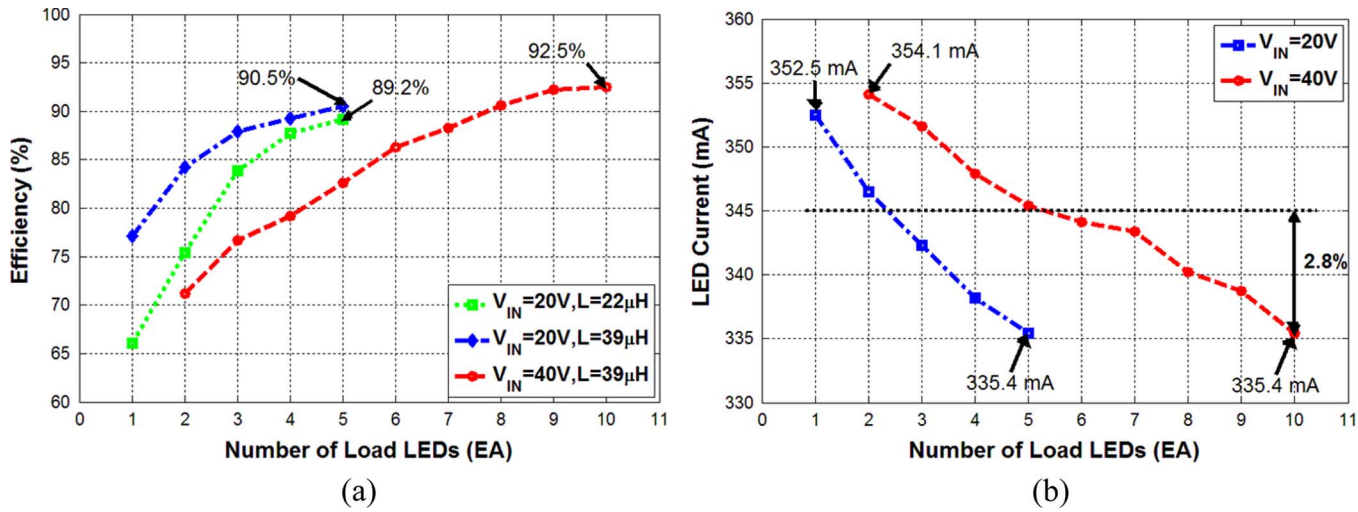

Fig. 19. Measured (a) power efficiency and (b) current errors of the proposed LED driver under different input voltages.

output LEDs at the switching frequency of 1 MHz. Fig. 19(b) shows the measured average LED current accuracy under different input and output conditions. The worst-case current error is 9.6 mA (2.8% of the average LED current of 345 mA) when $V_{IN} = 40$ V and the number of load LEDs changes from 5 to 10.

Table II provides the performance comparisons of different LED drivers. Based on [7], both the power efficiency and the current accuracy would be degraded when the switching frequency of the LED driver is increased. Compared with previous works from industry and literature, the proposed dimmable LED driver operates at a much higher switching frequency that enables smaller external components and achieves much smaller current error under different input and output conditions, while providing a comparable peak power efficiency. In addition, the proposed LED driver with the ATDC scheme reduces the settling time of the LED current by 14 times compared with the previously reported SAR-based adaptive off-time control [10].

V. Conclusion

A new dimmable LED driver has been introduced, discussed and verified in this paper. The proposed ATDC control scheme enables the driver to achieve fast settling time and high current accuracy over a wide range of input voltages and output LED loads. The power efficiency of the HV LED driver benefits from having no sensing resistor in the power stage and using the on-chip synchronous rectification via the high-speed low-power synchronous gate driver with pseudo-digital level shifters. The proposed LED driver can also operate at a high switching frequency due to high processing speed of the digital controller as well as high-speed low-power current sensor and synchronous gate driver. The proposed LED driver is verified experimentally and the performances of the proposed ATDC LED driver outperform those of state-of-the-art counterparts. The proposed dimmable LED driver is suitable for high-brightness solid-state lighting applications.

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Dongkyung Park received the B.S. degree from Korea University, Seoul, Korea, in 2000, and the M.S. degree from the University of Florida, Gainesville, FL, USA. He is currently working toward the Ph.D. degree in electrical engineering at the University of Texas at Dallas, Richardson, TX, USA.

From 2000 to 2004, he was with Samsung Electronics, Yongin, Kyungi-Do, Korea. In the summer of 2013, he was a Design Intern with Linear Technology, Tempe, AZ, USA. His research interests include low-power analog integrated circuits, integrated power management circuits, and LED driver for general lighting applications.

Zhidong Liu (S'13) received the B.S. degree from Nankai University, Tianjin, China, in 2007, and the M.S. degree from Peking University, Beijing, China, in 2010, both in electrical engineering. He is currently working toward the Ph.D. degree in electrical engineering at the University of Texas at Dallas, Richardson TX, USA.

He was an IC Designer with the Shanghai Research Institute of Microelectronics, Peking University, Shanghai, China, from 2010 to 2011. His research interests include low-power analog integrated circuits, high-voltage integrated hard-switching/soft-switching circuits, and high-voltage LED drivers for general lighting applications.

Hoi Lee (M'05–SM'09) received the B.Eng., M.Phil., and Ph.D. degrees in electrical and electronic engineering from the Hong Kong University of Science and Technology, Hong Kong, China, in 1998, 2000, and 2004, respectively.

In January 2005, he joined the Department of Electrical Engineering, University of Texas at Dallas, Richardson, TX, USA, where he is an Associate Professor. His current research interests include power management integrated circuits for ultra-low-power energy-harvesting systems, portable devices, and renewable energy systems, wireless power transfer for implantable microelectronic devices, and low-voltage low-power analog and mixed-signal circuit techniques.

Dr. Lee is an associate editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II—EXPRESS BRIEFS (TCAS-II) and serves on the Technical Program Committee of the IEEE Custom Integrated Circuits Conference and the IEEE Circuits and Systems (CAS) Analog Signal Processing Committee. He formerly served on the Technical Program Committee of the IEEE Asian Solid-State Circuits Conference and was an Associate Editor of the IEEE TCAS-II from 2007 to 2009. He was the recipient of the 2011 National Science Foundation CAREER Award and corecipient of the Best in Session Award at the 2013 SRC TECHCON Conference and Best Student Paper Award in the 2002 IEEE Custom Integrated Circuits Conference.