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Low power low noise high speed tunable CMOS radiation detection system

J. Galán [a,*], M. Sánchez-Raya [a], R. López-Ahumada [a], T. Sánchez-Rodríguez [a], I. Martel [b], R. Jiménez [a]

[a] Dpt. Ingeniería Electrónica, de Sistemas Informáticos y Automática, University of Huelva, Spain
[b] Dpt. de Física Aplicada, University of Huelva, Spain

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ABSTRACT

This paper presents a design of low power and low noise, high speed readout front-end system for semiconductor detectors. The architecture comprises a folded cascode charge sensitive amplifier with gain enhancement, a pole-zero cancellation circuit and a complex shaper circuit with Gm-C topology. A local feedback amplifier based on a wide swing gain boosting scheme with dc level shifting has been used. The system has been fabricated in a 0.13-μm CMOS technology with a single 1.2-V supply voltage. Experimental results show the flexibility of the system where the key parameters, such as decay time, charge gain and peaking time can be tuned. For a nominal peaking time of 150 ns the power consumption of the entire channel is less than 5 mW. A power consumption-low noise tradeoff will be considered to match a detector capacitance of 5 pF. The output pulse has a peak amplitude of 200 mV for a charge of 10 fC from the detector and achieves a linearity better than 1% up to an input charge range of 12 fC.

1. Introduction

The development of low noise low power readout front-end systems is of great interest today in several applications. Several sensors produce electrical charge in response to an external physical magnitude, such as piezoelectric sensors, photodetectors, pyroelectric sensors, particle detectors, and radiation detectors [1]. In particular, semiconductor detectors are extensively used for photon-counting imaging systems in medicine and for charged particle detection in nuclear physics applications. They are reverse-biased diodes that releases charge towards its electrodes when exposed to radiation. The energy deposited in these detectors is converted to an electric signal. To measure the deposited energy, which is proportional to the current pulse amplitude, a readout electronics is required. The analog front-end system is a conditioning channel that processes the information coming from the sensor and delivers it in a suitable form for further analog processing or digitalization. The trend to integrate the full electronic processing channel has become a priority due to high density and increased number of channels demanding low power, low noise and small area as well as the capability to include analog and digital circuits on the same chip. This approach replaces the conventional discrete and hybrid electronics [2–4].

The scaling down of the technology allows high speed front-end systems with small die area at the cost of low supply voltage and noise constraints [5]. The low supply voltage complicates the design requiring very efficient topologies. The design of operational amplifiers, which are the most important block in the front-end electronics, presents the additional difficulty of providing high gain and high output swing combining low-voltage operation with high power efficiency. Currently, gain enhancement techniques in combination with low voltage techniques are required to overcome the low intrinsic gain limitation in submicron technologies. Cascade structures that boost the gain with several amplifying stages need frequency compensation increasing the power consumption and limiting the bandwidth. The usual way to boost the gain is through cascode transistors but the design requires small overdrive voltages due to the output swing limitation.

This paper addresses the design of a readout front-end system for the radiation detection using silicon detectors. The aim of the work is to preserve or even to increase the system performance under low supply voltage operating conditions, optimum low power dissipation, and low noise. The use of a modern CMOS process requires a careful design where the analog transistor properties are worsened. This work uses a gain-boosting technique based on a local feedback amplifier with a wide-swing approaching.

* Corresponding author.
E-mail addresses: jgalan@uhu.es (J. Galán), msraya@uhu.es (M. Sánchez-Raya), ahumada@uhu.es (R. López-Ahumada), trinidad.sanchez@uhu.es (T. Sánchez-Rodríguez), imartel@uhu.es (I. Martel), naharro@uhu.es (R. Jiménez).

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The paper is organized as follows: An overview of the designed readout front-end system is given in Section 2. Section 3 discusses design considerations related to key parameters. Section 4 deals with the topology of the charge sensitive amplifier and the gain boosting scheme used. Section 5 presents the shaping circuit and simulation and experimental results are given in Section 6. Section 7 contains a summary.

2. Architecture of the designed front-end system

Radiation events hit a reversely biased semiconductor detector and the number of electron-hole pairs released is proportional to the energy of detected particles. The detector delivers a charge that must be amplified and shaped. Fig. 1(a) shows the architecture of the readout front-end channel designed in this paper for the radiation detection using silicon detectors. The system consists of a folded-cascode charge sensitive amplifier (CSA) with gain-boosting technique, a pole-zero cancellation circuit to eliminate undershoot, a shaper amplifier, and some integrators using Gm-C filter topology. The charge generated in the detector is fed to a charge sensitive amplifier (CSA) where the incoming current pulses are integrated by a feedback capacitor C_F and converted into voltage pulses. This kind of amplifier is commonly used due to the gain is insensitive to the detector capacitance C_{det} [6–8]. The CSA's output is a voltage step with amplitude proportional to the charge generated in the detector. This voltage pulse then slowly discharges by the feedback resistance R_F connected in parallel to C_F. The decay time must be adjusted to achieve a fast return to zero in order to prevent the pile-up of subsequent incoming current pulses in case of high rate experiments.

The voltage pulse is then amplified and shaped according to the time requirements of the application by a pulse shaping amplifier (shaper). The shaper also improves the signal to noise ratio of the signal by filtering the noise. It consists of a high pass section followed by several integrators. The CSA is dc coupled to the shaper. A pole-zero cancellation (PZC) circuit avoids the undershoot at the output of the shaper produced by the feedback pole of the CSA.

The back-end electronics processes the shaper's output signal in different ways depending on specific applications as shown in Fig. 1(b). The three main blocks that can be used for measuring the shaper's output are: a discriminator that uses a comparator to detect the signal amplitude and compares it with a threshold (counting), an analog to digital converter to measure the amplitude of the signal corresponding to each individual impinging particle (energy spectroscopy), or a time to digital converter for timing measurements (timing spectroscopy).The acquired information can be stored in the chip or sent out from it.

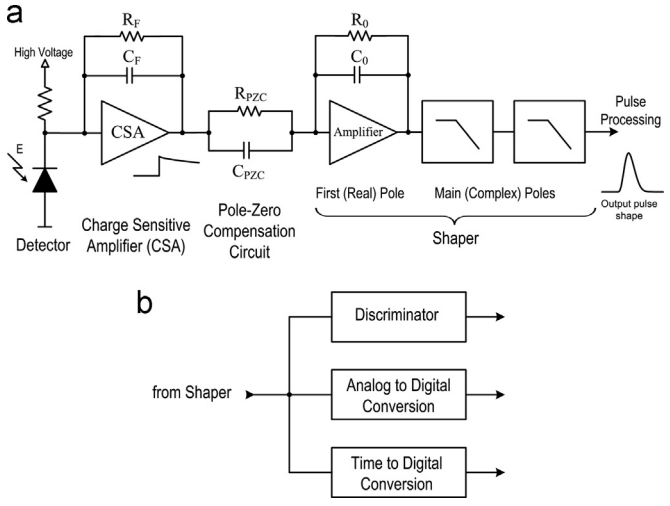

Fig. 1. (a) Architecture of the designed readout front-end system. (b) Back-end electronics.

3. Design considerations

The noise limit to the resolution of a radiation detection system is typically expressed in terms of equivalent noise charge (ENC). The ENC corresponds to the charge that must be delivered to the front-end in order to achieve an output signal to noise ratio equal to the unity. An equivalent definition for ENC is the ratio of total integrated rms noise at the output of the pulse shaper to the signal amplitude due to one electron charge, ENC$=v_{no,rms}/V_{out,max}$, yielding [5]

$$\mathrm{ENC}^2 = \frac{\int_0^\infty |v_{no}(j2\pi f)|^2 |H(j2\pi f)|^2 \, df}{qA^n n^n / C_F n! e^n} \tag{1}$$

where $v_{no,rms}$ is the total rms noise and $H(j2\pi f)$ is the transfer function of the shaper. In addition, n is the order of the shaper/filter, A is the dc gain of the integrators of shaper, and C_F is the feedback capacitor of the CSA. The final equation after solving is given as follows:

$$\mathrm{ENC}^2 = 4k_B T \frac{\gamma}{g_m} \frac{C_T^2 B((3/2), n-(1/2))n}{q^2 4\pi t_p} \left(\frac{n!^2 e^{2n}}{n^{2n}}\right) + \frac{K_f C_T^2}{C_{ox}^2 WLq^2 2n} \left(\frac{n!^2 e^{2n}}{n^{2n}}\right) \tag{2}$$

The first term is the contribution of the thermal noise and the second term is the flicker noise contribution. The meaning of the main parameters is as follows: k_B is the Boltzmann constant, T is temperature, g_m is the input transistor transconductance of the CSA, C_{ox} is the gate oxide capacitance per area, W and L are the width and length of the input transistor, K_f is the flicker noise coefficient, C_T is the total input capacitance consisting of detector, feedback and input transistor capacitances, B is the beta function defined in [5], t_p is peaking time, i.e. a measure of the speed of the detection system. Finally, $\gamma = 2/3$ for long channel MOS transistors and is approximately 1.5–2 in submicron technologies. There is another thermal noise source associated with the feedback resistance R_F. This noise contribution is inversely proportional to the value of the feedback resistance and proportional to the peaking time. The decay time of the CSA's output is proportional to R_F providing a tradeoff between noise and pile-up (overlap between successive input pulses).

Now that detector trends force a strong power constraint on the electronics, it is important to clarify the tradeoff between noise and power dissipation. The readout front-end system noise performance is strongly dependent on the input MOS transistor of the charge sensitive amplifier related to type, size and biasing. In a properly designed front-end the resolution should be limited by the noise of the CSA input transistor. Regarding the dominance of thermal and flicker noise in (2) for the input transistor, it is anticipated here that the thermal noise is the dominant noise source due to the low peaking time (150 ns). The peaking time specification defines the bandwidth of the shaper, and hence, determines the dominance of thermal or flicker noise. Therefore, in order to reduce the thermal noise, the transconductance g_m of the CSA's input transistor has to be increased, and g_m is directly related to the power consumption and the aspect ratio W/L. The flicker noise is inverse proportional to the gate area of the input transistor and strongly dependent on the technology process. Moreover, a p-channel MOS input transistor has been chosen

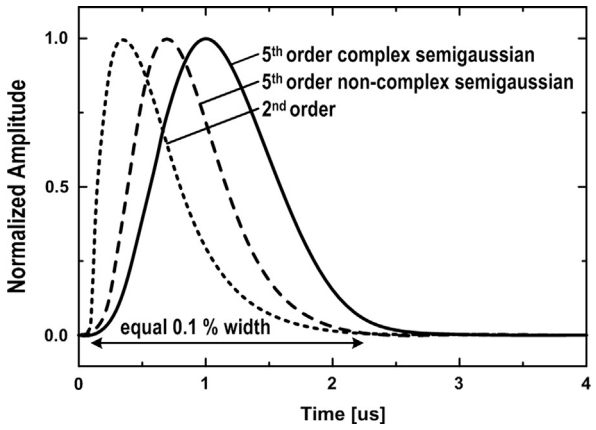

Fig. 2. Comparison of pulse shapes for filters with real and complex poles and the same return to baseline ($t_{0.1}$ is the width of the pulse to the fraction 0.1% of its peak height).

for the CSA in order to further reduce the $1/f$ noise contribution. In modern CMOS technologies the optimization of the input transistor becomes very challenging since these technologies are developed for digital design. Thus the optimization process relies on equations, models and parameters that can be strongly dependent on the technology.

Although noise originates in the CSA, the shaper order must be chosen correctly. Many monolithic front-end systems have low-order filters to provide the pulse shaping ensuring a simpler design with high power efficiency due to the reduced number of active blocks. For a given rate of the experiment, the shaped pulse must return to baseline within a fraction of the average interarrival time. By choosing the most symmetric shape that satisfies the baseline return requirement, a reduction noise is achieved. High-order shapers have more symmetric pulse shapes (best approximation to a Gaussian function) but the increased number of stages costs power. Fig. 2 illustrates the benefits of high-order complex pole filters comparing three filters with the same width and thus the same rate capability [9]. The symmetry is measured as the width to peaking time ratio. The pulse peaking time t_p is measured from 1% of the peak height to the center of the peak and is related to the time constant of the shaper. The constant time and the order of the shaper should be optimized for noise.

Finally, it is noteworthy that although the detector capacitance is a dominant parameter to low noise, the process optimization of the front-end electronics starts from the knowledge of C_{det}.

4. Charge sensitive amplifier

The performance optimization of the readout front-end system is not that simple in CMOS technologies so optimization of individual components has to be addressed. The charge sensitive amplifier or preamplifier is the first natural conditioning stage of the front-end to convert the electrical charge generated by detectors into voltages pulses, and it is the most critical block of the conditioning chain [10,11]. Architecture exploration and circuit techniques are required to meet the performance requirements for CSA in particular and for all other components in general by taking advantage of the specific technology and taking care of the technology driven constraints [12,13]. In general, the design of the CSA requires as main characteristics low noise, low power consumption, high open-loop gain, high gain-bandwidth (GBW) product and low rise time [14]. A careful design for the input transistor is mandatory for low noise and optimum power consumption.

The rise time of the output voltage should be smaller than the integration time of the charge over the feedback capacitor. The time constant $\tau_F = R_F \cdot C_F$ is responsible for slow signal decay and GBW determines the rise time at CSA output. Thus in order to transfer quickly the charge generated by the detector to the preamplifier, the *GBW* must be sufficiently large. Furthermore, as it has already been mentioned the CSA's open-loop gain should be high enough to ensure that the output is independent of the detector capacitor. The Miller's multiplication of the capacitor C_F by the CSA open-loop gain must be several times higher than the detector capacitance to guarantee that nearly the whole current pulse flows to the feedback capacitor and is integrated at the same time.

Telescopic, two-stage Miller and folded-cascode topologies with single-ended input and single-ended output are the most commonly solutions for CSA [15]. Fig. 3(a) shows the conventional folded cascode topology where a gain enhancement technique has been used for the charge sensitive amplifier. Folded-cascode topology is a single gain stage but with a quite reasonable gain achieved by the product of the input transconductance and the high output impedance due to the use of cascode techniques. A disadvantage in using a cascode scheme is that it reduces the maximum output swings possible before transistors enter the triode region. The bandwidth is proportional to the input transistor's transconductance. To enlarge the transconductance the bias current of the input transistor should be several times larger than the bias current of the output branch. This approach optimizes the power consumption further increasing the output resistance, and thus the dc gain ($g_{mi} \cdot r_{out}$). The very large transconductance of the input transistor reduces the thermal noise. The high contribution of flicker noise in modern technologies requires a PMOS input transistor instead of *N* MOS to reduce its effect.

The design in modern technologies reduces the output resistance of transistors and the low voltage environment limits the number of stacked transistors. This issue forces the use of gain-boosting schemes. The gain-boosting technique allows increasing the resistance seen at the drain of the cascode transistors. The basic idea in Fig. 3(a) is to use a local feedback amplifier [16] to keep the drain-source voltage across M_1 and M_4 as stable as possible, irrespective of the output voltage. This technique also known as regulated cascode, enhances the effective gain of the cascode transistors resulting in increased output resistance. If A_{GB} is the gain of the (inverting) local feedback amplifier in Fig. 3(a), then the output resistance is given approximately by the following:

$$r_{out} = A_{GB}(g_{m2} r_{d2} r_{d1} || g_{m3} r_{d3} r_{d4}) \tag{3}$$

where g_{mx} is the small-signal transconductance gain of M_x, and r_{dx}, is the small-signal output resistance of M_x. Hence, the gain A_{GB} allows compensating for the low value of r_{dx} in modern processes. Of course, the bandwidth of the additional amplifier must be higher than that of the main OTA for effective operation. Fig. 3(b) shows the local feedback amplifier using a wide swing gain boosting circuit with dc level shifting that does not limit the signal swing at the output of the CSA [17]. The biasing current I_{B1} is a cascode current source which ensures high output impedance and high A_{GB} of approximately $g_{m6}[(g_{m7} r_{o7} r_{o6}) || (g_{m8} r_{o8} r_{o9})]$, where M_8 and M_9 are the transistors used in the implementation of I_{B1}. Note as the scheme depicted in Fig. 3(b) corresponds to the gain boosting circuit for cascode M_2. A similar scheme for the cascode M_3 is easily derived.

Regarding the CSA reset system, its role is to discharge, discretely or continuously, the input node of the detection system. It also provides stabilization of the operating point for the charge sensitive amplifier. The reset system must be carefully designed because of it can generate additional noise since it is connected to the most sensitive input node of the detection system. The value of

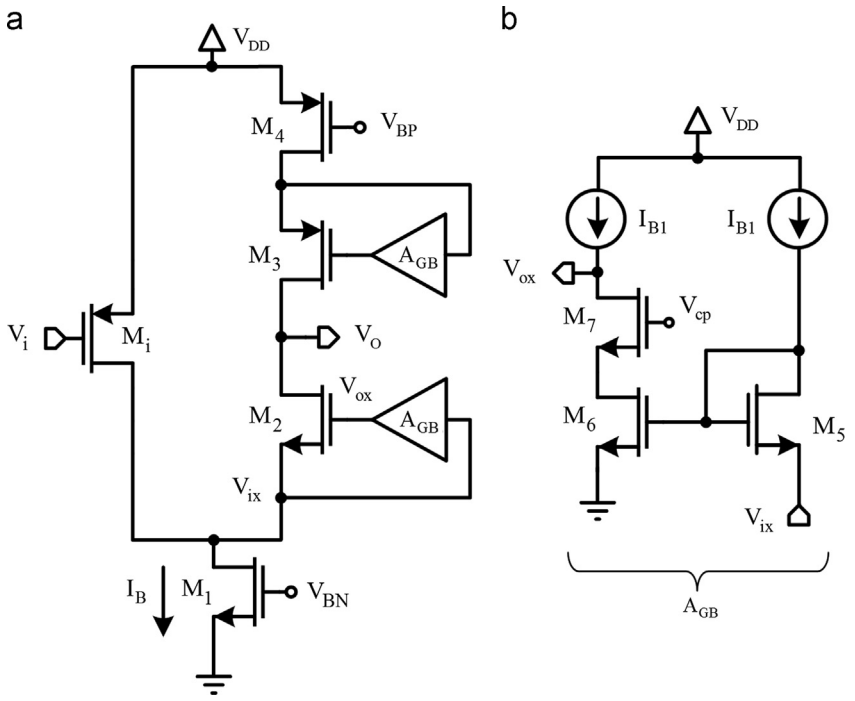

Fig. 3. Folded-cascode CSA with low-voltage gain-boosting scheme.

the feedback resistance R_F is a tradeoff between noise and dc voltage drop due to the detector's leakage current. The spectral density of the thermal noise due to R_F ($4kT/R_F$, measured in A^2/Hz) should be comparable to leakage noise ($2qI_{det}$) giving a large value of resistance difficult to implement in CMOS technology. The most common techniques to integrate this very large value are based on active devices. An active feedback transistor instead of a passive resistor allows improving parameters related to area, parasitic capacitances, speed and noise. The feedback resistor R_F has been implemented by a PMOS transistor following a scheme similar to [18] where a self-adaptive bias network was adopted to overcome the sensibility to process, temperature and bias conditions of the drain-to-source resistance. This ensures a stable value for the feedback resistance. The higher time constant $\tau_F = R_F\, C_F$ increases the decay time of the CSA's output step voltage as a compromise between noise and counting rate, since the relatively long discharge time constant of the CSA makes it vulnerable to pile-up, i.e. overlap of successive input charge pulses. For a variable bias gate voltage of the MOS-based feedback resistor, the decay time of the voltage step can be adjusted to fulfill speed constraints.

Using a pole-cero cancellation (PZC) circuit eliminates undershoots after the differentiating filter stage, which are the results of the long time decay of pulses at the CSA output. By adding an extra resistor R_{PZC} in parallel to capacitor C_{PZC} creates a zero in the transfer function which cancels the pole created by the charge sensitive preamplifier's feedback resistor. To achieve proper pole/zero cancellation, the condition $R_F \cdot C_F = R_{PZC} \cdot C_{PZC}$ is fulfilled. Resistor R_{PZC} directly couples the dc offset from the CSA output into the shaping circuit input and must be exact N times replica (N MOS transistors in parallel) of R_F. The gates of resistors R_F and R_{PZC} are connected together to change their effective resistance. The ratio C_{PZC}/C_F gives a charge gain or current gain at the output of the PZC circuit [19].

5. Pulse shaping amplifier

A band-pass filter, usually called as shaper, is applied to perform three main operations: (1) Provide an additional voltage gain enough to give required information about radiation detected. This facilitates accurate pulse amplitude measurements with A/D converters into the back-end electronics. The pulse shaping amplifier enhances the amplitude of the CSA output pulse from the mV range into hundreds of mV depending on the application requirement and the power supply range. (2) Improve the signal to noise ratio by filtering the noise out of a bandwidth. (3) Shape (shorten) the output signal to meet the time requirements, which is necessary to preclude the overlap between successive pulses in high rate experiments. With this aim the shaper introduces the dominant constant time, i.e lower than $\tau_F = R_F \cdot C_F$. Peaking time is the time at which the output of the pulse shaping reaches its maximum amplitude. Large peaking time is helpful in achieving the optimal energy resolution, whereas a short peaking time is essential for high counting rates.

A Gaussian shaped step response gives the optimal signal to noise ratio [8,11] and it is the most common pulse shaping technique employed in readout front-end systems. An ideal Gaussian pulse shaper is not physically realizable due to the need of a differentiator and an infinitely large number of integrators; instead an approximation of the Gaussian pulse can be made. A CR-$(RC)^n$ type semi-Gaussian pulse shaper becomes one of the most popular architectures in integrated circuits. This shaper consists of one differentiator (high pass section) followed of n integrators (low pass sections). In practice a CR differentiator followed by four RC integrators is usually considered adequate in this approach. The transfer function is characterized by the time constant of the differentiator and integrators, the dc gain of integrators and the number of integrators. Peaking time is proportional to the shaper time constant and to the number of integrators n. Increasing the order of the shaper results in an output pulse to be more closer to ideal Gaussian pulse but with larger delay. The simplicity of this topology makes it suitable for multichannel integrated circuits but the performance in terms of noise and timing is not the best solution.

Another option is a nearly true Gaussian filter obtained by the method proposed in [20] that can be realized using active filters with a limited number of stages. The design procedure uses a simple CR circuit as a differentiator with a real pole in cascade

with active filter sections with complex poles. There are several circuit configurations of active filters for realizing a complex pole pair. Filters employed for these applications are currently active RC topologies. They follow the classic method for designing stable linear active circuits by means of feedback amplifiers with passive linear components. They achieve very high linearity and high signal to noise ratio. However, due to the closed-open operation of the amplifiers the bandwidth is limited. Transconductance-C (Gm-C) filters usually feature higher operating frequencies due to their open-loop operation and thus also less linearity. Gm-C topologies can achieve better power efficient because the bandwidth of the active building amplifiers can be approximately equal to the filter bandwidth.

The designed Gaussian shaper is composed of a simple CR differentiator that creates a real pole given by $R_0 \cdot C_0$ (Fig. 1) followed by two cascade-connected second-order Gm-C sections with complex pairs of poles. The amplifier of the first stage (CR differentiator in Fig. 1) of the shaper is a down-scaled version of the CSA's folded cascode to reduce its power consumption. Fig. 4 shows the topology of the second-order Gm-C filter.

The transfer function of this second-order Gm-C section is given by the following:

$$H(s) = \frac{g_{m1}g_{m3}/C_1C_2}{s^2 + s(g_{m2}/C_1) + (g_{m3}g_{m4}/C_1C_2)} \tag{4}$$

A differential pair with resistive source degeneration has been used for the transconductors of Gm-C section as shown in Fig. 5. The transconductor also uses regulated cascodes based on the same gain boosting scheme shown in Fig. 3(b). The transconductance Gm is given by $G_m = g_{m1}/(2 + g_{m1} \cdot R)$ where g_{m1} is the transconductance of the input transistors M_1. Transistors M_4 and M_5 form a cascode biasing current source I_B. The circuit has been designed to achieve a linear dependence of $G_m \cong 1/R$ so that $g_{m1} \cdot R \gg 2$.

The shaper noise performance is defined by the choice of the cutoff frequency. Parameters of the frequency domain, such as, bandwidth, cutoff frequency and order set the shaper time domain behavior, i.e. the peaking time of the output pulse. A short peaking time is characterized by a higher cutoff frequency. The values of resistors, capacitors and transconductances must be set according to the peaking time and the dynamic range and the programmability of both.

The procedure of design follows the method proposed in [20] for a Gaussian filter. The simple CR differentiator in Fig. 1 realizes a real pole ($R_0 \cdot C_0$) which determines the time constant. The two complex conjugated poles obtained by the 4th order Gm-C topology are in the positions:

$$s_1 = \frac{g_{m2}}{2C_1}\left[-1 \pm j\sqrt{\frac{4C_1 g_{m3} g_{m4}}{C_2 g_{m2}^2} - 1}\right] \tag{5}$$

The relation between the time constant of the differentiator and the real pole is given by $R_0C_0 = \sigma_0\tau_x/A_0$, where $A_0 = 1.4766878$, $\sigma_0 = 1.0844$ and τ_x is the time constant of a CR-RC filter. For $\tau_x = 75$ ns, R_0 has been set to 100 kΩ yielding $C_0 = 550$ fF. The complex pole pairs are $p_i = -A_i \pm W_i$, where A_i and W_i are the real and the imaginary parts, respectively. From (5), they are given by

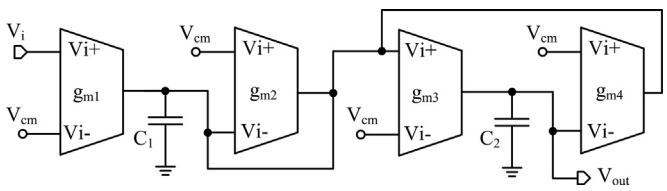

Fig. 4. 2th order low pass Gm-C filter block diagram.

the following:

$$A_i = \frac{\sigma_0\tau_x g_{m2}}{2C_1} \tag{6}$$

$$W_i = \frac{\sigma_0\tau_x g_{m2}}{2C_1}\sqrt{\frac{4C_1 g_{m3} g_{m4}}{C_2 g_{m2}^2} - 1} \tag{7}$$

The coefficients A_i, W_i are provided in [20] for each second-order stage of the filter. In order to simplify the design, all transconductances are set at the same nominal value $g_m = g_{m2} = g_{m3} = g_{m4} = 35$ μA/V. For the first stage: $A_1 = 1.4166647$, $W_1 = 0.5978596$, and for the second stage: $A_2 = 1.2036832$ and $W_2 = 1.2994843$. From (6), $C_{1a} = 1$ pF and $C_{1b} = 1.18$ pF. Applying the same procedure for the imaginary part in (7) yields $1 + (W_i/A_i)^2 = 4C_1/C_2$. As result, $C_{2a} = 3.41$ pF and $C_{2b} = 2.18$ pF. For $\tau_x = 75$ ns the peaking time of this Gaussian filter is about $t_p = 150$ ns.

The nominal cutoff frequency for the designed 4th-order low pass Gm-C filter is about 2 MHz. It can be noted in (4) that the gain can be varied by adjusting the transconductance g_{m1}, and this has no effect upon the location of the pole of filter. A passband gain of 12 dB has been set by including two transconductors in parallel for g_{m1}. The gain of the overall front-end system is related to the ratio C_{PZC}/C_F and the gain of the Gm-C filter.

6. Simulation and measurement results

The readout front-end system has been designed and fabricated in a 0.13-μm CMOS technology and powered from a 1.2-V supply. On the test chip, we included circuits having preamplifier output available for testing. The design procedure starts with the noise optimization in the CSA. The main contribution to the input noise is due to transistors M_i, M_1 and M_4. In (2), the term $1/g_m$ is an approximation of $(g_{mi} + g_{m1} + g_{m4})/g_{mi}^2$ if $g_{mi} \gg g_{m1}$, g_{m4}. The input transistor requires a large value of transconductance which, in turn, means that the transistor should have a large W/L ratio and be operated in a large quiescent current level. A very high transconductance of 10 mA/V and with non-minimum channel length for the input transistor M_i allows decreasing noise. The other secondary noise sources have been minimized. Once the conditions for the input transistor have been established, then the design methodology focuses on the output branch to achieve the required gain. The transistor dimensions and biasing conditions for CSA are shown in Table 1.

For the counterparts of M_5, M_6 and M_7 applied to cascode M_3 and not depicted in Fig. 3, the sizes are 3/0.13. The drain current of the input transistor is 1.1 mA. A practical upper limit on the ratio of the bias current of the input transistor to the currents of cascode output transistors is around four, giving output currents about 250 μA. The common-mode voltage V_{CM} is 0.8 V. The bias current for the local feedback amplifier is $I_{B1} = 30$ μA. The charge sensitive amplifier consumes 1.66 mW. The amplifier's GBW is 1.38 GHz for a load capacitor of 1 pF. GBW was set to meet the short timing requirements. Fig. 6 compares the open-loop frequency response of the CSA including the gain boosting scheme, with a conventional folded cascode op-amp without regulated cascodes. Note as the open-loop gain increases from 36 dB to 63 dB and the GBW value also increases from 1.1 GHz to 1.38 GHz. A g_m of 10 mA/V and an open-loop gain of 63 dB suggest than the output impedance is about 100 kΩ. This is sufficient to drive the nominal feedback resistor of 4 MΩ, so the CSA needs no buffer stage. We confirmed by circuit simulations that the circuit has enough gain to the frequencies necessary for the application.

The feedback elements were set at $C_F = 200$ fF and $R_F = 4$ MΩ. The generated charge Q from the detector is integrated into C_F giving at the output of the CSA an amplitude equal to Q/C_F.

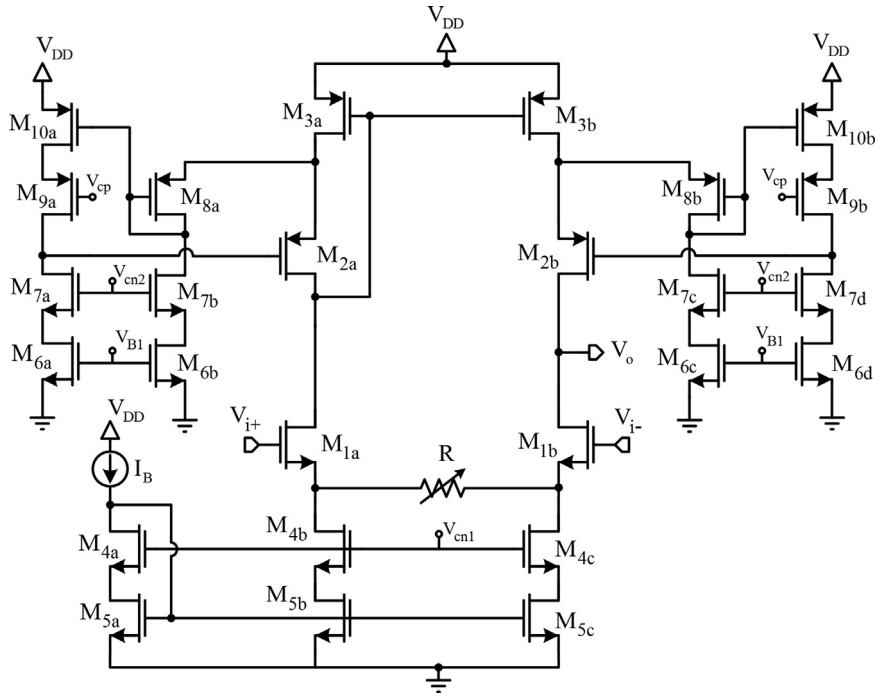

Fig. 5. Transconductor used in the Gm-C shaper section.

Table 1
Transistor dimensions and bias condition of CSA.

Transistor	*W/L* (μm/μm)	Bias condition	
M_i	100/0.26		
M_1	10/0.13	V_{DD}	1.2 V
M_2	8/0.13	I_B	1.35 mA
M_3	16/0.13	I_{B1}	30 μA
M_4	16/0.13	V_{CM}	800 mV
M_5, M_6, M_7	1/0.13		

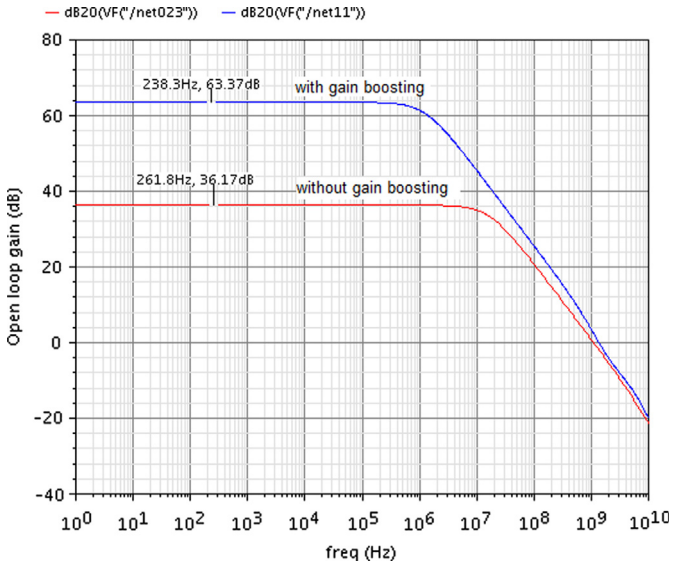

Fig. 6. Open-loop gain comparison of CSA.

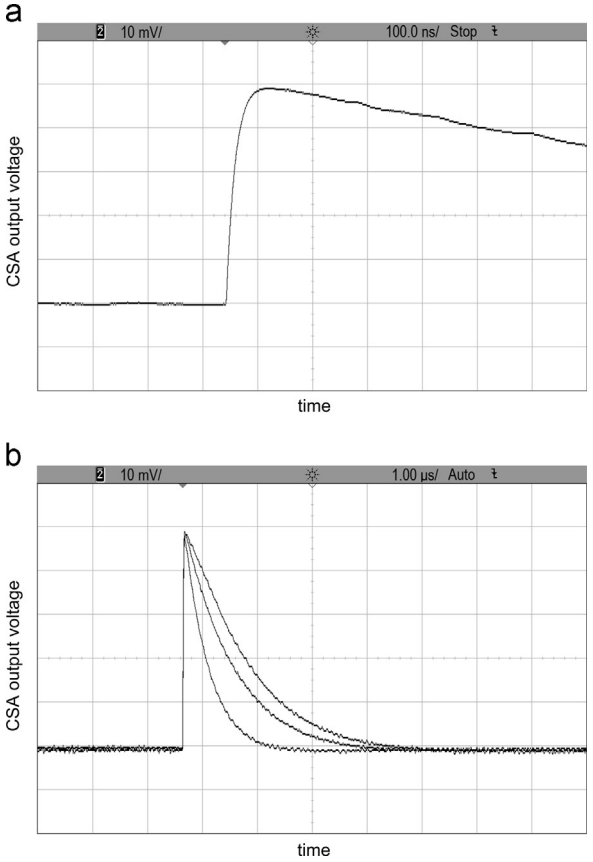

Fig. 7. Transient response of the CSA for a current input pulse of 10 fC. (a) Zoom to the rise time and (b) programmability of the decay time.

The charge gain of the CSA is given by $V_{out}/Q = 1/C_F$. For a feedback capacitor of 200 fF, the charge gain is 5 V/pC. Fig. 7(a) shows a zoom of the CSA's output voltage with a rise time (10–90% of the amplitude) of 32 ns for an input detector capacitor of $C_{det} = 5$ pF. The amplitude is near to 50 mV for an input charge of 10 fC. Fig. 7(b) shows the tunability for the decay time, which is suitable in high rate experiments, for values of R_F equal to 1.5 MΩ, 3 MΩ and 4 MΩ. Table 2 summarizes the performance of the CSA.

Concerning to the design of the shaping circuit, the same topology of CSA in Fig. 3 has been used for the first stage (real pole).

Table 2
Charge sensitive amplifier performance.

Parameter	Value
Input transistor gm	10 mA/V
V_{DD}	1.2 V
Power consumption	1.66 mW
Open-loop gain	63 dB
Gain bandwidth product	1.38 GHz
Charge gain	5 V/pC
Output swing	50 mV (for Q=10 fC)
Decay time	4 μs
Rise time	32 ns

Table 3
Transconductor of Gm-C section parameters.

Parameter	Value
M_1	20/0.13 (μm/μm)
M_2, M_3	10/0.13 (μm/μm)
M_4, M_5	7/0.26 (μm/μm)
V_{DD}	1.2 V
V_{CM}	600 mV
I_B	100 μA

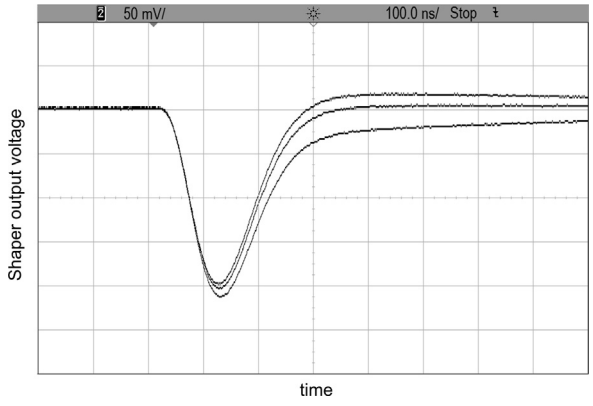

Fig. 8. Performance of the pole/zero circuit.

We have chosen a down-scaled version of the gain-boosted folded cascode amplifier where all transistor dimensions and the biasing current have been scaled by a factor of 10. Table 3 includes the transistor dimensions for the transconductors of Gm-C section shown in Fig. 5. Passive resistor R was switched to tune different values of transconductances. The power consumption of the overall shaping circuit is 2.73 mW. Thus the total power dissipation of the readout front-end system is 4.4 mW.

Fig. 8 shows the shaper's output signal applying the pole/zero cancellation. The nominal values of $R_{PZC}\cdot$ and C_{PZC} are 500 kΩ and 1.6 pF, respectively. To achieve proper pole/zero cancellation, the condition $R_F\cdot C_F = R_{PZC}\cdot C_{PZC}$ must be met. It can be seen the overshoot in the shaper's output signal if no cancellation is achieved. The decay time of CSA and the pole/zero circuit are controlled in a continuous-time way since the resistors have been replaced by active transistors where the values are set by the gate voltage.

In this kind of applications gain and peaking time are usually programmable using a discrete-time scheme based on an array of capacitors and/or resistors controlled by switches. The tuning used in this work includes the programmability of the first (real) pole of the shaper and the transconductors of the Gm-C section in order to adjust both mentioned parameters. A discrete-time approach has been chosen by means of switching the resistors instead of capacitors to save silicon area. The G_m tuning of the transconductor in Fig. 5 is performed by switching several polysilicon resistors R in parallel. In the shaper architecture, the constant time is half of the peaking time. Table 4 gives the values of shaper's elements for different peaking times.

Fig. 9(a) shows the peaking time programmability for an input charge of 10 fC and a detector capacitor C_{det}=5 pF. Fig. 9(b) shows the gain tunability.

Table 4
Shaper transconductances and capacitors.

Peaking time (ns)	R_0 (kΩ)	C_0 (fF)	$g_{m2}-g_{m3}-g_{m4}$ (μA/V)	g_{m1} (μA/V)
75	50	550	70	140
150	100	550	35	70
300	200	550	17.5	35

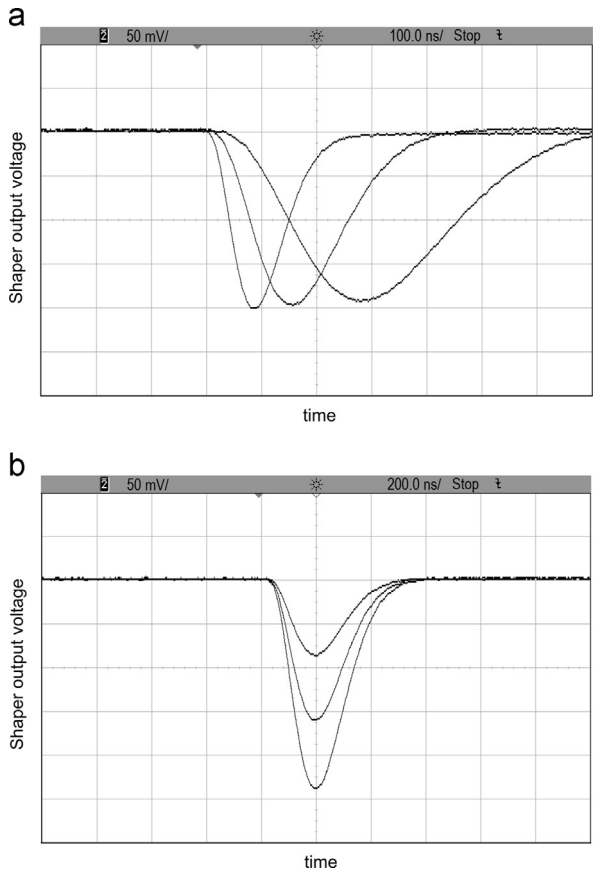

Fig. 9. (a) Peaking time and (b) gain tunability.

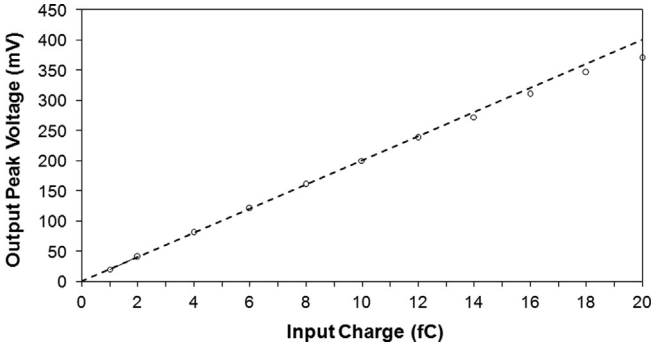

Fig. 10. Output peak amplitude versus input charge.

The peak amplitude of the output voltage of the front-end system must be linear for a charge range from the detector. Fig. 10 shows the energy response and the dynamic range obtained. The output pulse achieves a linearity better than 1% up to an input charge of about 12 fC.

For the nominal performance of the readout front-end system a theoretical equivalent noise charge of 61 e^- at $C_D=0$ pF has been achieved. The noise is proportional to the detector capacitor. The dependence on detector capacitor is about 122 e^-/pF. For $C_D=5$ pF noise is about 671 e^-.

7. Conclusions

The design and description of a readout front-end system for silicon detectors is presented. A charge sensitive amplifier and a shaper circuit with complex poles have been designed where the main parameters can be tuned. The implementation in a 0.13-μm CMOS technology suggests the use of gain boosting techniques. The design procedure follows a compromise between power dissipation and noise. The total power consumption is 4.4 mW and the noise is 671 e^- for a detector capacitor of 5 pF.

Acknowledgments

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