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144 Channel measurement IC for CdZnTe sensors with energy and time resolution ☆

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ABSTRACT

A 144 channel measurement IC for CdZnTe detectors, used for PET, is presented. Each channel consists of a charge sensitive amplifier, a fast and a slow shaper, a peak sampler for the energy acquisition and an event detector based on a time to digital converter to generate an accurate time stamp for each event. The channels are multiplexed to a fast pipeline ADC on demand. Measurement results for the ASIC showed a noise equivalent input charge of 800 e^- rms and a time resolution of 737 ps rms. Evaluation results with a CdZnTe detector yielded an energy resolution of 4.4% full width half maximum at 662 keV with a ^{137}Cs radiation source. The IC is implemented on a 180 nm CMOS process with a total chip size of 100 mm^2.

1. Introduction

The human body is by far the most studied object in the world. A lot of different methods and means are used to gather information about the internal structure, operation and function of the body. With the detection of X-ray in 1895 by W.C. Röngten, it was possible to have a look through the tissue and to study the bones and organs without surgery or dissection. Over 100 years of improvement, from the first X-ray bulb to complex multichannel X-ray receiver plates, yielded CT-systems, which give a detailed picture of the blood vessels and even of the heart in full function. A similar, maybe less detailed, however also less straining and cheaper method is the use of ultrasound systems. All these methods are passive methods, which are based on either different damping or reflection factors for the external applied energy. The image resolution is basically limited by the amount of energy, the texture of the tissue and the quality of the detector. While the X-ray-CT detector quality is still increasing, the possible resolution improvement is lowered by the demand for reduced energy delivered to the body. This way, modern CT-Systems show the potential to detect larger cancer spots. Unfortunately, it is not possible to find small spots down to a few cells in a quite texture less tissue like the brain. However, this would be a big advantage for early cancer detection and observation. Active systems, like Positron Emission Tomography (PET), may overcome these restrictions. A radioactive tracer substance is incorporated, which accumulates in the cancer cells due to the higher metabolic turnaround in this cells. Detection of the energy of a radioactive decay gives the possibility to back trace to the location of the decay and by this to the location of the cancer herd.

As depicted in Fig. 1, the decay of the injected isotope generates a positron, which converts into two gamma quanta by annihilation with an electron. These quanta travel in opposite direction. Measuring time and location of the two quanta in a detector around the source enables precise back tracing to the exact location of the decay. The energy detection is used to suppress interferences from scattered quanta and allows also to increase the spatial resolution by sub-pixel interpolation. While CT displays the structure of the tissue, PET is able to display metabolic processes.

2. System description

For the detection of X-rays scintillators are used, in most cases, which convert the energy of the photons into lower energy bands (e.g. visible light) to be detected by silicon based CMOS or CCD imagers. The main drawback of this solution is the degradation of the energy resolution, due to the statistical fluctuations of

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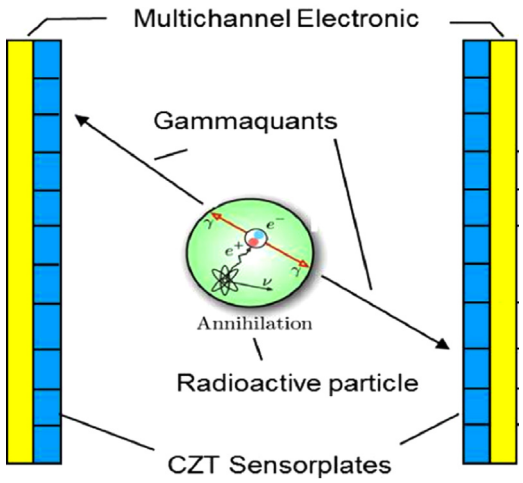

Fig. 1. Detection of radioactive decay.

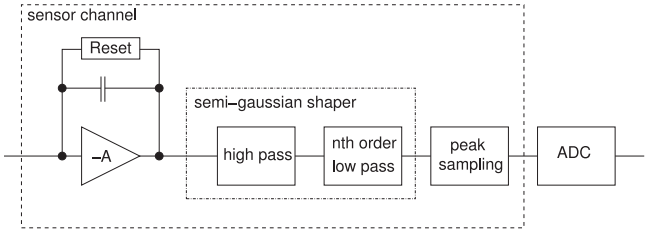

Fig. 2. Channel architecture (ADC can be shared by multiple channels).

scintillators. Therefore, means and materials for a direct conversion of the energy of a gamma quantum into an electrical charge are of high interest. However, the low moderating effect of Silicon reduces the ability of this material as a cost effective detector – at least not with the typical 300–600 µm thickness of CMOS Wafers. For an acceptable efficiency, silicon with a few centimeter thickness must be used. Therefore, materials with higher efficiency are applied, even though the advantage of a CMOS process integration is lost. Cadmium Zinc Tellurium (CdZnTe) is such a material. It combines the required high atomic number with an electron mobility of 1000 cm^2/Vs. Recently, it is increasingly proposed for the use in medical and scientific applications, because it exhibits a multiple higher efficiency at room temperature compared to silicon [1–3].

For PET imaging, positron emission radioactive tracers are used e.g. ^{18}F-FDG. The emitted positron annihilates with a free electron from the tissue. The products of interaction are two gamma quanta with an energy of 511 keV, which leave at almost strict opposite direction. Quantifying time and position of the impact of both quanta in a detector gives the possibility to calculate the trajectories. By superimposing different lines, the exact location of a hot spot is detected. Applying this method, radioactive tracers, which accumulate in small cancers spots, show the location more accurately and earlier than e.g. CT – as long as it is possible to detect the two quanta of a decay with high accuracy. Therefore, it is necessary to improve the energy, time and spatial resolution of the detectors and readout systems, continuously.

For CdZnTe, energy resolutions of 5.5 keV for an energy of 140 keV with 4% full width half maximum (FWHM) are reported [4]. The energy of 20–360 keV is of high interest for Single Photon Emission Computed Tomography (SPECT) due to the availability of biocompatible isotopes. For PET a higher energy range of up to 511 keV is required, due to the energy of the gamma quanta generated by annihilation.

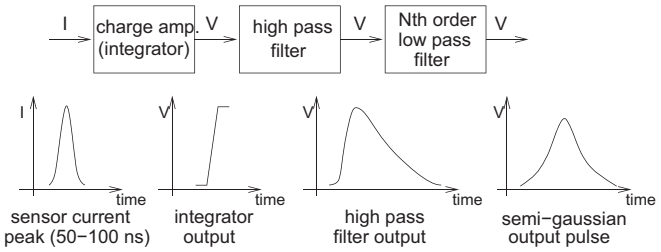

Fig. 3. Signal flow within one channel.

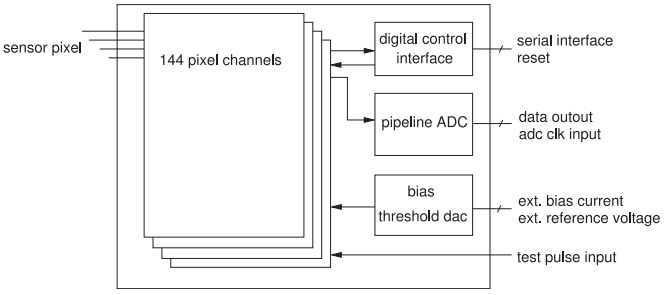

Fig. 4. Block diagram of the ASIC.

The developed ASIC is designed for PET mammography as well as detector research. The development focuses on an input referred noise below 1000 e^- equivalent noise charges (ENC). This ASIC is able to measure the amount of incoming charge, while most other implementations use only comparators to sort for one or two energy levels [5,6]. The measured value is stored within each channel and can be readout sequentially. Additionally, the acquisition in all surrounding channels can be activated if one channel is triggered. The charge measurement in combination with the charge acquisition of the surrounding channels allows us to achieve sub-pixel spatial resolution. For detector research, the output of each triggered channel can be automatically connected to a pipeline ADC to convert the whole waveform. A timing resolution of below 1 ns rms is projected to detect the coincidence of gamma quanta.

3. Circuit design

Readout channels for CdZnTe detector pixel arrays measure the induced charge in the pixel due to the drift of the electrons and holes within the CdZnTe crystal under an applied electric field. The electron–hole pairs are generated by ionization of the CdZnTe crystal. The readout circuits are mainly based on a charge sensitive amplifier followed by semi-Gaussian shaping of the signal, peak height detection and timing analysis in the analog domain. The semi-Gaussian shaping has been developed over many years and is used in most detector circuits. A typical detector channel as used in current developments [7] is depicted in Fig. 2.

Fig. 3 depicts the signal flow. The charge pulse emitted by the sensor is integrated and filtered. Peak sampling or timing analysis is done on the shaped pulses depending on the selected shaping time of the filter. The analog shaping filters in front of the sampling circuit are required to avoid aliasing of high frequency noise during the sampling process.

3.1. Channel architecture

The block diagram of the 144 channel readout ASIC is shown in Fig. 4. The configuration of each channel can be done independent of each other by a serial peripheral interface. This interface is also

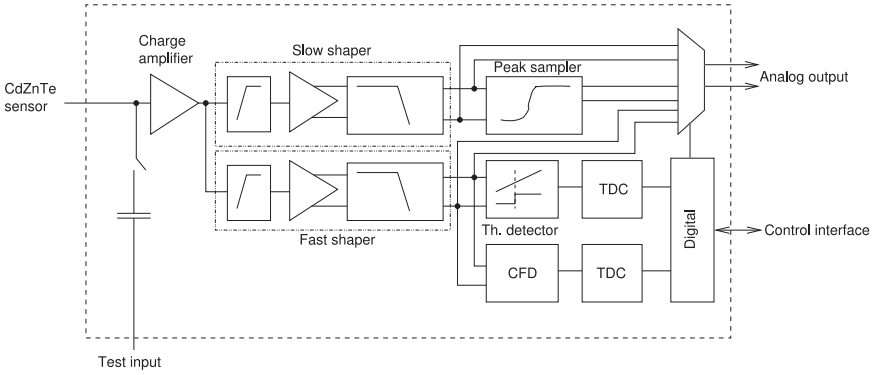

Fig. 5. Block diagram of one measurement channel.

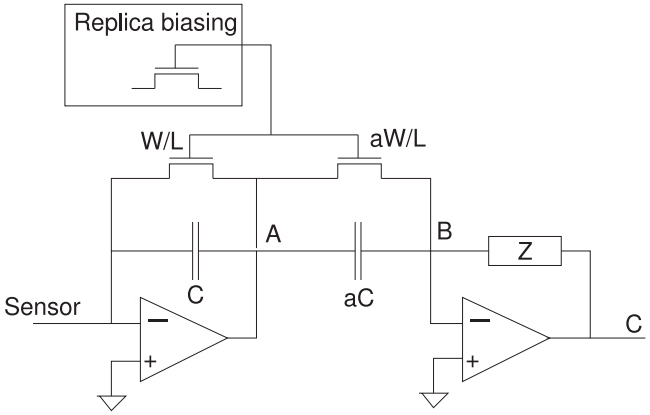

Fig. 6. Charge sensitive amplifier.

used to readout the timing data. The energy of each event is converted into digital. A 12 bit 50 MS/s pipeline ADC is implemented and shared by all channels.

Each channel, as shown in Fig. 5, has a test signal input for calibration and evaluation purposes. It can be used to characterize the analog channel, and for in-system non-linearity and mismatch correction of the TDC. The input charge generated by a gamma quantum is amplified by the charge sensitive amplifier and converted to voltage domain. After single-ended to differential conversion, two different 4th order shaping filters are used to generate semi-Gaussian shapes for energy and time acquisition. While the peak voltage is sampled and stored for analog to digital conversion, the event time is detected by a threshold and a constant fraction discriminator. The constant fraction discriminator triggers at a certain fraction of the pulse, which makes the event time independent of the actual pulse height. A digital time stamp is generated for each discriminator and can be read out. The output waveform of the slow shaper can be automatically redirected to the pipeline ADC if an event is detected in the channel.

3.2. Charge sensitive amplifier

The charge sensitive amplifier is the most critical part of the ASIC regarding the sensitivity of the signal detection. The resolution of the whole ASIC is limited by electronic noise generated by this amplifier. An ESD series resistance, typically used in integrated circuits, contributes to the overall system noise. It is, therefore, removed in this application.

The charge amplifier circuit, shown in Fig. 6, uses a compensated continuous reset system as proposed by [8]. The feedback device is biased to provide a equivalent resistance of more than 1 GΩ to limit its noise contribution. The pole introduced by the resistive feedback across the amplifier is compensated by a matching device across the differentiation capacitor between nodes A and B. The biasing of the continuous reset system is done by means of a replica structure. In contrast to the majority of integrated charge amplifiers in the literature, a cascoded symmetrical OTA is used. The differential input structure offers an improved power supply rejection ratio (PSRR) compared to the, often used, single input, folded amplifiers. This supports also the suppression of cross talk between readout channels. The PSRR advantage has to be paid by an increased power consumption for the same input referred noise power. The channel structure is designed for a maximum input charge of 25.6 fC, which corresponds to an input energy of approx. 800 keV [9]. The over range compared to the energy of one gamma quantum in PET applications allows to handle pile-up effects.

3.3. Fast and slow signal shaper

The output signal of the charge amplifier is connected to two parallel filters with different filter coefficients as shown in Fig. 5. These filters are also called semi-Gaussian shapers. Each consists of a high pass filter combined with a 4th order low pass. The shaping times are digitally selectable in 4 steps from 300 ns to 900 ns for the slow shaper and from 50 ns to 350 ns for the fast shaper. Single ended to differential conversions are implemented to increase power supply rejection and to reduce cross talk between channels. Due to the compensation scheme of the continuous time reset the conversion to differential has to be placed after the high pass filtering. A four step gain selection is included in this block, which allows us to adapt the circuit for different input energies during evaluation.

Baseline holders are not included in the design of the channel. The use of small pixel sizes reduces the leakage current per pixel down to below 200 pA. The offset caused by detector leakage and the amplifier offsets are sufficiently small to compensate them after filtering. The compensation is done in the energy and time acquisition blocks. The fast shaper for time acquisition includes a calibration DAC in the last filter stage. The comparator of the threshold detector is used to control the DAC based on a successive approximation calibration algorithm. The calibration can be applied during activation of the channel. The compensation strategy of the slow shaper is based on correlated double sampling. The baseline is sampled periodically during operation and stored in case of an event. Therefore, the baseline can be subtracted from the peak amplitude after analog to digital conversion. This approach filters for low frequency noise, too. The small pixel size reduces the detector signal to noise ratio, while the detector noise is still well below the noise of the electronics.

3.4. Event detection comparator and time stamp generator

For each event, a precision time stamp must be generated for coincidence detection of two quanta. Two different functions are implemented for the detection of the event time within each channel. The first one is based on a threshold detector applying a global threshold level for the whole ASIC. This level can be increased by 20% within each channel to reduce the event rate of noisy channels caused by detector crystal imperfections. Alternatively, these noisy pixels can be deactivated to prevent overloading of the readout interface. Each channel can also trigger the time and energy acquisition circuits of all surrounding channels. This feature is required to handle charge distribution across multiple channels. This is likely to happen by an askew incidence of the photons on the detector.

The triggering time of the threshold detector is converted into digital by means of a time to digital converter (TDC). The time to digital converter uses a CMOS inverter based ring oscillator as shown in Fig. 7. The ring oscillator is build-up by 11 current starved inverters. The bias current of the starved elements is set to 20 μA. During standby one inverter output is forced to ground. An incoming impulse sets PRESET to low and starts the oscillation. The current phase of the oscillator is saved to latches if the LOCK signal goes active. The number of oscillator periods during one measurement cycle is detected by a counter. The counter is working only during the transparent state of the latch, which avoids timing conflicts in case that the LOCK signal activates during counting [10]. During the falling edge of LOCK, the measured data are saved to registers. The unit delay of the ring oscillator depends on various parameters like supply voltage, process variations and temperature. Continuous trimming of the unit delay is not applied to lower the power consumption. Instead, the unit delay is measured after each conversion. The operation states of the TDC are shown in Fig. 8. After measuring the incoming pulse, the TDC restarts to measure its own oscillation frequency. The time of the event relative to one reference period can be calculated by

$$\tau_m = 1 - \frac{N_p * 22 + ph_p}{N_r * 22 + ph_r} \quad (1)$$

with the phase value ph_p and counter value N_p during impulse measurement and ph_r and N_r during reference measurement. The phase values have to be binary encoded. τ_m is normed to one period of the reference clock and aligned to the raising edge of the clock before the impulse.

There is also an 8 bit counter triggered by the reference clock to give a coarse time reference. The value of this counter is saved to registers if an event occurred. The counter is cleared by the global reset. This counter is implemented in the digital section of the channels.

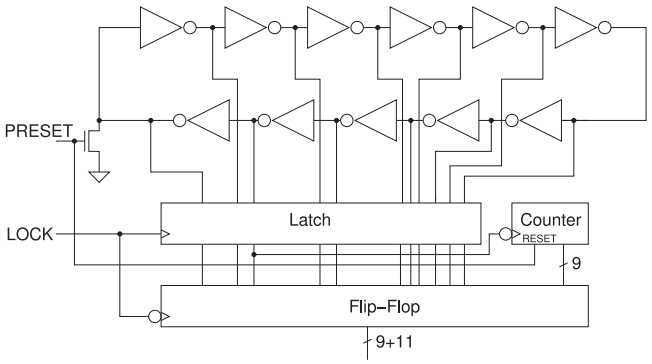

Fig. 7. Simplified schematic of the TDC.

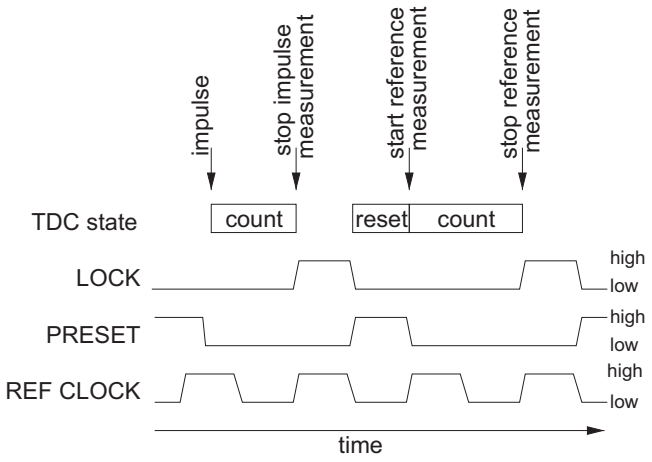

Fig. 8. TDC operation states.

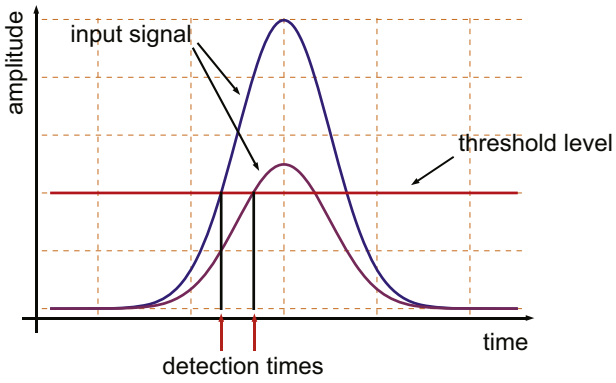

Fig. 9. Triggering time of a threshold detector for different pulse heights.

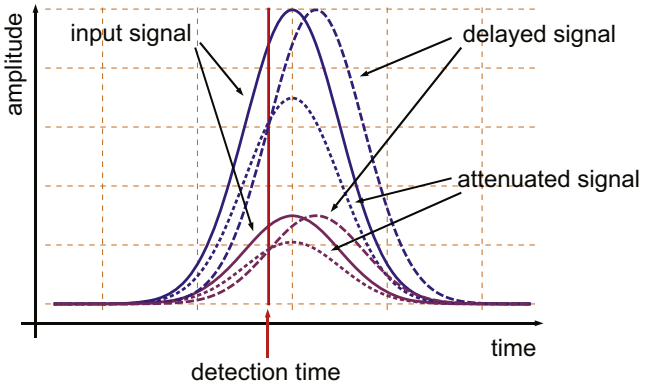

Fig. 10. Triggering time of a constant fraction discriminator for two different pulses (line: input pulse, dotted line: attenuated pulse, dashed line: delayed pulse).

The time stamp generated by a threshold detector depends on the energy of the event as shown in Fig. 9. An additional discriminator is required to generate an energy independent time stamp. The event detection output is also used to activate a constant fraction discriminator (CFD). This type of detector triggers at a certain fraction of the pulse to get timing information. Fig. 10 depicts this behavior for two different pulse heights. The CFD uses an attenuated version (dotted curves) of the input signal as threshold level. The input signal of the CFD comparator is a delayed version (dashed curves) of the pulse. The crossing point of these two curves is independent of the actual pulse height.

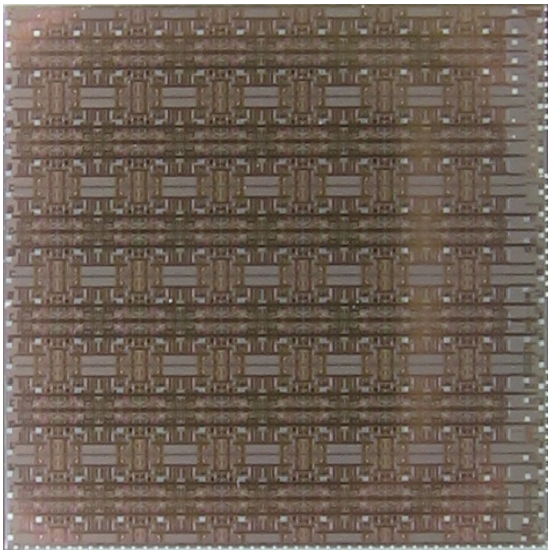

Fig. 11. Chip photo of the 144 channel measurement IC.

The time stamps generated by both TDCs are available via the serial interface.

3.5. Peak sampling

The peak sampling circuit at the output of the slow shaper is activated by the threshold detector. A differentiator followed by a comparator is used to detect the signal peak and to trigger the sampling circuit. The threshold detector and the peak sampling circuit are connected to independent shaping filters, which lead to different signal delays. Therefore, the activation of the peak detection circuit can be delayed between 100 ns and 700 ns using 100 ns steps to compensate for group delay differences between the fast and the slow shaper.

4. Implementation and measurements

A chip photo of the whole device is shown in Fig. 11. The IC is implemented in a 180 nm CMOS technology. Each channel occupies an area of 800 µm by 800 µm including the input pad with ESD protection to interface to the sensor by flip chip technology. Total chip size is 100 mm^2, matching the size of 12×12 sensor crystal. Large detector fields can be implemented by placing multiple sensor-IC modules.

A special test board was designed for laboratory evaluation. Test signals to the charge amplifier could be supplied either by bonded channel pads or through the channel test input. Full functionality of the channels could be verified. Fig. 12 shows the differential output of a slow shaper for a 1 V step test signal, corresponding to 25.6 fC charges at the input [11].

The measured pulse detection trigger levels across the channels are shown in Fig. 13 for 0.1 V and 0.4 V settings. The $\pm 25\%$ spread across the channels is sufficient for triggering the energy acquisition circuit. This trigger is also used to enable the constant fraction discriminator (CFD). A time stamp resolution of 737 ps could be measured, which is 25% better than the specified 1 ns.

Measurements with a CdZnTe-Sensor have been accomplished. The multipix CdZnTe detector from EI Detection & Imaging Systems[1] has been chosen for detector measurements. It consists of a 4×4 pixel matrix arranged in a monolithic block of $5.9 \times 5.9 \times 5.0$ mm^3. To obtain the preliminary results, 12 pixels from the detector are wire bonded to row 0 of the ASIC, and the cathode electrode of the detector is biased at -600 V, which gives an electric field of -1200 V/cm. A graphical interface, based on Labview, has been developed to generate the configuration data of the ASIC. The used test setup is presented in Fig. 14. The differential analog output of the ASIC is converted into single ended, and it is digitized using an APTEC multichannel analyzer (MCA). In order to calibrate the charge collection dependency with the photon interaction depth, the cathode electrode is sensed in ac-mode using an external circuitry. A CR-110 Cremat amplifier followed by an ORTEC 452 shaper is disposed in parallel to the pixel acquisition. Both cathode and pixel shaped signals need to be sampled in time coincidence. In that case, a two channel

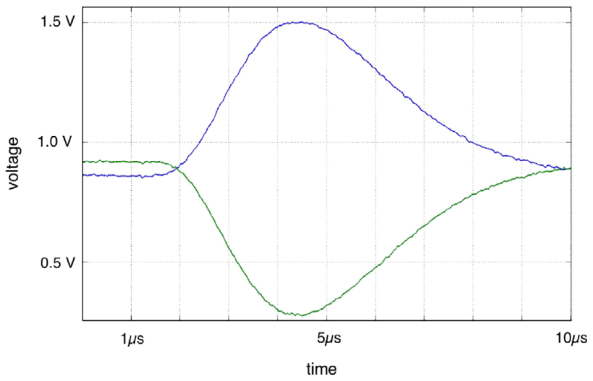

Fig. 12. Differential output signal of the slow shaper.

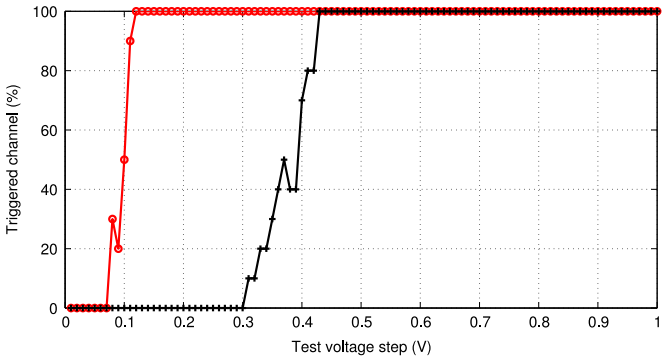

Fig. 13. Spread of trigger levels for two levels over all channels.

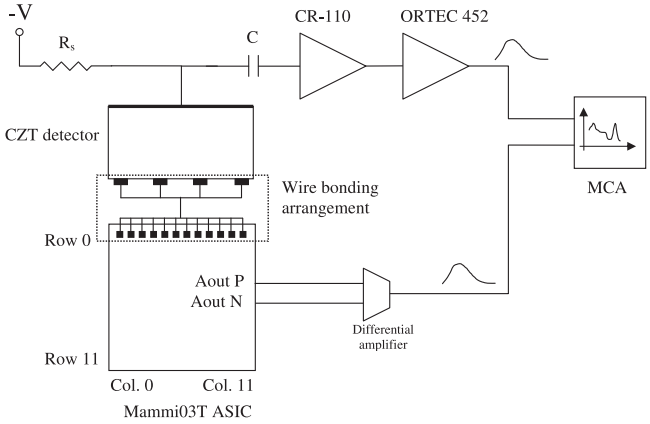

Fig. 14. Test setup used for detector measurements.

[1] EI Detection & Imaging Systems, 373 Saxonburg Blvd, PA 16056, USA.

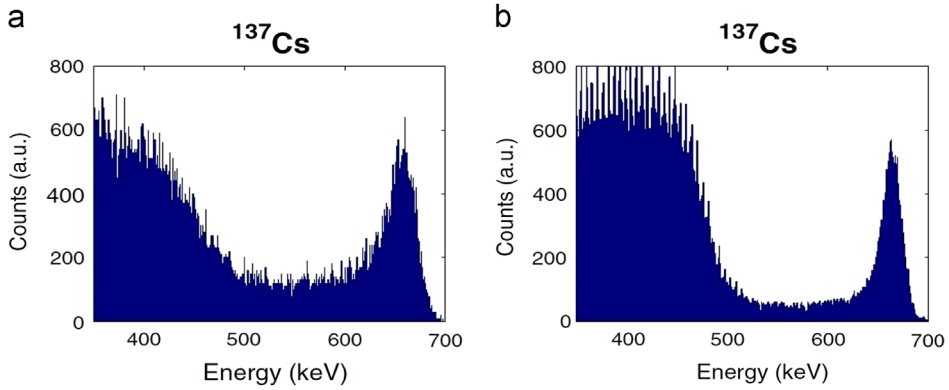

Fig. 15. Preliminary histogram for an uncollimated ^{137}Cs point source with and without interaction depth correction.

GaGe-CompuScope MCA is used. This measurement allows us to determine the cathode to anode signal ratio, which permit the restoration of the energy spectra [12]. The comparison of energy spectra – with and without the interaction depth compensation – permits the performance evaluation of the correction. The preliminary spectrum obtained with a ^{137}Cs uncollimated point source is presented in Fig. 15(a). The resolution measured, when the interaction depth is not taken into account, is around 4.4% FWHM at the 662 keV energy line. The improvement in the energy spectrum, when the interaction depth is considered, is shown in Fig. 15(b). The energy resolution measured when the correction is considered as 3.5%, which represents an improvement of approx. 20% compared to the uncorrected measurements. Such an important enhancement of energy resolution justifies the addition of a readout channel for the cathode signal in future revisions of the ASIC to facilitate the interaction depth compensation.

The power consumption of each channel is 25 mW during operation.

5. Summary

The design and measurement of a 144 channel measurement IC for CdZnTe detectors is presented. The design is projected for PET applications and to support the evaluation of future detector development. An energy resolution of 4.4% full width half maximum at 662 keV with a ^{137}Cs radiation source is achieved. A time resolution of 737 ps rms was measured. The ASIC provides a unique set of configuration options. This ASIC is able to measure the actual energy of each gamma quantum and the event time in parallel using CdZnTe detectors, which is unique compared to most other publications [5,6,13]. The time measurement is energy independent due to the use of a constant fraction discriminator.

Further work will concentrate on the improvement of the channel architecture to reduce the power consumption and area of the channels, while keeping the signal to noise ratio. The redesign concept is based on analog to digital conversion in each channel using a continuous time delta sigma modulator [14].

References

[1] M. Overdick, C. Baumer, K.J. Engel, J. Fink, C. Herrmann, H. Kruger, M. Simon, R. Steadman, G. Zeitler, Status of direct conversion detectors for medical imaging with X-rays, IEEE Trans. Nucl. Sci. 56 (2009) 1800–1809.
[2] N. Cesca, N. Auricchio, G.D. Domenico, G. Zavattini, R. Malaguti, R. Andritschke, G. Kanbach, F. Schopper, Silipet: design of an ultra-high resolution small animal pet scanner based on stacks of semi-conductor detectors, Nucl. Instrum. Methods Phys. Res. Sect. A: Accel. Spectrom. Detect. Assoc. Equip. 572 (2007) 225–227.
[3] H. Kim, L. Cirignano, P. Dokhale, P. Bennett, J.R. Stickel, G.S. Mitchell, S.R. Cherry, M. Squillante, K. Shah, CDTE orthogonal strip detector for small animal PET, in: Proceedings of IEEE Nuclear Science Symposium Conference Record, vol. 6, 2006, pp. 3827–3830.
[4] D. Meier, S. Chen, D.J. Wagenaar, G.E. Maehlum, B.E. Patt, B.M. Sundal, Y. Wang, B.M.W. Tsui, X-ray fluorescence study with pixellated CZT radiation sensors, in: Proceedings of IEEE Nuclear Science Symposium Conference Record NSS '08, pp. 1030–1034.
[5] R. Ballabriga, The Design and implementation in 0.13 μm CMOS of an algorithm permitting spectroscopic imaging with high spatial resolution for hybrid pixel detectors (Ph.D. thesis), Universitat Ramon Llull, 2009.
[6] E. Vernon, K. Ackley, G. De Geronimo, J. Fried, Z. He, C. Herman, F. Zhang, Asic for high rate 3D position sensitive detectors, in: IEEE Nuclear Science Symposium Conference Record (NSS/MIC), 2009, pp. 412–418.
[7] G. De Geronimo, G. De Geronimo, E. Vernon, K. Ackley, A. Dragone, J. Fried, P. O'Connor, Z. He, C. Herman, F. Zhang, Readout ASIC for 3D position-sensitive detectors, in: E. Vernon (Ed.), IEEE Nuclear Science Symposium Conference Record NSS '07, vol. 1, pp. 32–41.
[8] G. De Geronimo, G. De Geronimo, P. O'Connor, A CMOS fully compensated continuous reset system, IEEE Trans. Nucl. Sci. 47 (2000) 1458–1462.
[9] H. Spieler, Semiconductor Detector Systems, Oxford University Press, Oxford OX2 6DP, 2009, ISBN: 978-0-19-852784-8.
[10] M. Voelker, J. Hauer, A low power oscillator based TDC with in-system non-linearity correction, in: IEEE International Symposium on Circuits and Systems (ISCAS), 2012, pp. 1046–1049.
[11] M. Voelker, J. Carrascal, A. Soriano, J. Cela, J. Perez, F. Sanchez, J. Hauer, J. Benlloch, Design and preliminary performance of a readout ASIC for CZT based high resolution pet, in: Proceedings of IEEE Nuclear Science Symposium, Medical Imaging Conference and Workshop on Room-Temperature Semiconductor Detectors, 2011.
[12] A. Shor, Y. Eisen, I. Mardor, Spectroscopy with pixelated CdZnTe gamma detectors—experiment versus theory, Nucl. Instrum. Methods Phys. Res. Sect. A: Accel. Spectrom. Detect. Assoc. Equip. 458 (2001) 47–54 (Proceedings of 11th International Workshop on Room Temperature Semiconductor X- and Gamma-Ray Detectors and Associated Electronics).
[13] G. De Geronimo, E. Vernon, K. Ackley, A. Dragone, J. Fried, P. O'Connor, Z. He, C. Herman, F. Zhang, Readout ASIC for 3D position-sensitive detectors, IEEE Trans. Nucl. Sci. 55 (2008) 1593–1603.
[14] M. Voelker, H. Zhou, Continuous-time delta-sigma based readout concepts for CZT detector arrays, in: Proceedings of Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), 2010, pp. 1–4.