Jeer / mocacio

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#### **Course Announcements**

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  - Unfortunately the technical problems here were tougher than I expected, so I am changing how it works
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- Due to popular demand, I have changed PA4c1's specification to also allow the input to be a . cl-type file (originally was TAC)
  - PA4c1 is due April 28, and is mostly optional

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    - this happens when there aren't enough physical registers
  - Insert code to move values between registers and memory if needed ("spill code")
    - Typically we will re-run the instruction scheduler if we ever have to spill a register

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  - I recommend waiting until later in PA4 to try more complex schemes

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- Global register allocation via reduction to graph coloring
  - including a union-find algorithm for fun

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- By contrast, in a memory-to-memory model, register allocation is an optimization
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  - Hopefully, this is where you are after PA3. I will assume this memory model for the rest of this lecture.

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In this discussion of local allocation, I'm going to assume that all values must be stored in memory **between** basic blocks

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  - o any control flow (i.e., more than one basic block)

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Recall that a **reduction** is a proof that we could use an oracle for one problem to solve another, so for a problem to be NP-complete we need to prove both that if we can solve it, we could solve SAT and vice-versa

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- For both cases, we will assume that the input is a basic block that uses some number of virtual registers **v** 
  - our goal: create a semantically-equivalent block that uses some fixed number of physical registers k
- If k < v, there is another complication: spilling a register to memory may require more registers!
  - $\circ$  We have to account for this when we choose k

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- Big disadvantage: it dedicates a physical register to one virtual register for the entire basic block
  - even if the virtual register is only used in the first half!

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# Local Reg. Alloc.: Clean and Dirty Values

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  - this is part of why the register allocation problem is so hard!
- Let's see an example...

• Consider a two-register machine with this state:

phys. reg.	value/VR	clean?
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load x3
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but, if we spill **x1** instead, we get:

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This example suggests that it might be better to **preferentially spill clean** values. Unfortunately, it's not that simple...

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spilling the dirty value results in less spill code!

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- As an optimization, we can **not store to memory** any value that is dead after the block.
  - A global liveness analysis computes exactly this information
    - i.e., we can easily inspect its "live out" sets to determine which virtual registers (= temporaries/IR names) we don't need to store

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  - though it is NP-hard to produce optimal local allocations for single basic blocks, because of clean vs dirty values
  - frequency count allocator is simpler, but its allocations are usually worse
- If you are going to implement a local allocator in PA4, this greedy strategy is a good option
  - the textbook has a more-detailed version of this algorithm
  - if you want to do register allocation, I recommend building a local allocator first, regardless

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- Unfortunately, this is a bit of a **false hope**.
  - There are a lot of complications that arise at basic block boundaries! Let's take a look at some examples to see why.

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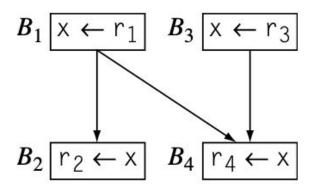
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    - note that this assumes we have a global liveness analysis!
  - For each successor of b, start the greedy register allocation algorithm in a state where the those virtual registers are already allocated to the same physical registers that we allocated them to in b

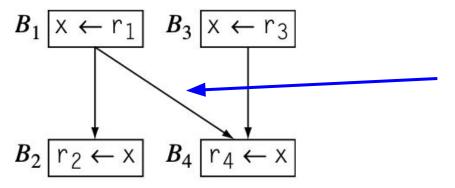
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- For each basic block b, in CFG order:
  - Run the greedy register allocation algorithm we just saw on b
  - Run a liveness analysis and compute a set (of virtual registers!)
     that are live when b exits
    - note that this assumes we have a global liveness analysis!
  - For each successor of b, start the greedy register allocation algorithm in a state where the those virtual registers are already allocated to the same physical registers that we allocated them to in b

Why won't this work?

 Consider this CFG (with some specific register allocations returned by the local allocator and values in the basic blocks):

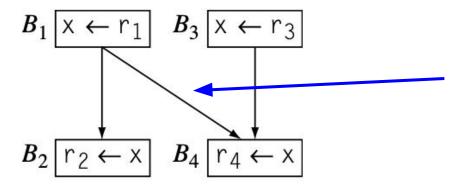


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 e.g., consider adding copy operations to keep x in a register. Where would they go?

 Consider this CFG (with some specific register allocations returned by the local allocator and values in the basic blocks):

$$B_1 \times r_1 B_3 \times r_3$$

this edge  $B_1 \rightarrow B_4$  is a *critical* 

Critical edges are just one reason that extending a local allocator beyond a single block is a bad idea. Instead, a global allocator should **coordinate** allocation decisions.

 it turns out that global allocators are fundamentally quite different than local allocators

tore x,

B<sub>3</sub>

Iding copy
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# Trivia Break: Popular Culture

This American science fiction media franchise began with a television show in the mid-1960s. The franchise is noted for its cultural influence beyond works of science fiction and for its progressive stances on civil rights; for example, in the 1960s, it was one of the first shows with a multiracial cast on American television. The franchise contains 11 spin-off television series and a film franchise; further adaptations also exist in several media. The series greatly influenced public interest in the U.S. Space Program and in education on the topic of space exploration. For example, NASA named one of its space shuttles (now on display at the Intrepid Museum in NYC) after something from this series.

# Trivia Break: Physics

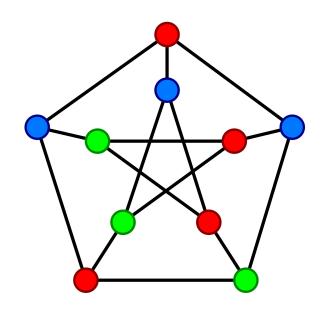
The creator of this speculative theory stated in an email to William Shatner (who played Captain Kirk in the Star Trek original series) that his theory was directly inspired by the term used in the show. The theory posits a speculative warp drive idea according to which a spacecraft could achieve apparent faster-than-light travel by contracting space in front of it and expanding space behind it, under the assumption that a configurable energy-density field lower than that of vacuum (that is, negative mass) could be created. The idea remains a hypothetical concept with seemingly difficult problems, although the amount of energy required is no longer thought to be unobtainably large.

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    - We will see an algorithm that takes advantage of a special property of our graph: we can spill registers to simplify it

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```
loadI \cdots \Rightarrow r_{arp}
      loadAI r_{arp},@a \Rightarrow r_{a}
     loadI
                              \Rightarrow r<sub>2</sub>
     loadAI
                  r_{arp}, @b \Rightarrow r_{b}
     loadAI
                 r_{arp}, @c \Rightarrow r_{c}
     loadAI r_{arp},@d \Rightarrow r_X
     mult r_a, r_2 \Rightarrow r_a
     mult r_a, r_b \Rightarrow r_a
     mult r_a, r_c \Rightarrow r_a
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Global Reg. Alloc.: Loc What are the live ranges for some of these (virtual) registers?

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loadI
                                 \Rightarrow rarp
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                   r_{arp},@a \Rightarrow r_a
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                                 \Rightarrow r<sub>2</sub>
      loadAI
                    r_{arp}, @b \Rightarrow r_{b}
      loadAI
                    r_{arp}, @c \Rightarrow r_{c}
      loadAI
                    r_{arp},@d \Rightarrow r_X
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                    ra, r<sub>2</sub>
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      mult
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```

	Register	Interval
1	rarp	[1,11]
2	ra	[2,7]
3	ra	[7,8]
4	ra	[8,9]
5	ra	[9,10]
6	$r_{a}$	[10,11]
7	$r_2$	[3,7]
8	$r_b$	[4,8]
9	$r_c$	[5,9]
10	$r_d$	[6,10]

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### Global Reg. Alloc.: Global Live Ranges

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  - Logically, a global live range is a closure of definitions and uses

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    - I will assume this from now on

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  - this data structure is a key component in other algorithms, such as Kruskal's (graph minimum spanning trees) and unification (for equation solving)

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    - That is, there is an edge from node n1 to node n2 if the values corresponding to n1 and n2 are simultaneously live
      - We can easily derive this information from the live ranges of the values for n1 and n2

x <- 1

y <- 2

z <- x + y

t <- y

u <- x + t

print z

print t

print u

	х	у	Z	t	u
x <- 1					
y <- 2					
z <- x + y					
t <- y					
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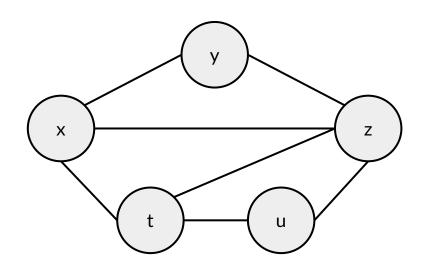
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  - We can map "spilling a value" back into the graph to simplify the interference graph (and therefore the graph coloring problem)
    - To be clear: this approach is heuristic (graph coloring is NP-complete). You could solve the graph coloring problem here using any graph coloring algorithm.

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- More formally, if the simplified graph is K-colorable, then so is G: since n has less than K neighbors, those use at most K-1 colors, and there is therefore at least one color available for n.

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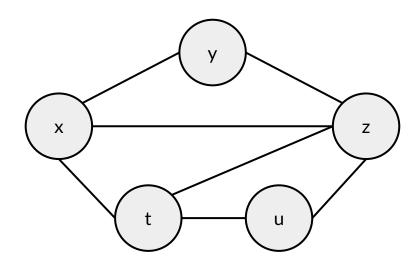
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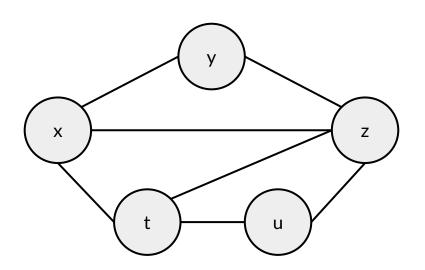
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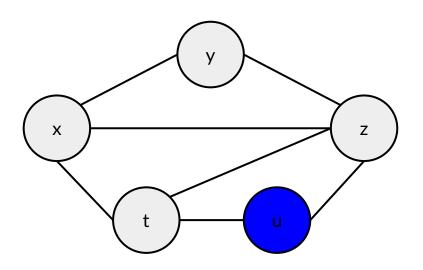


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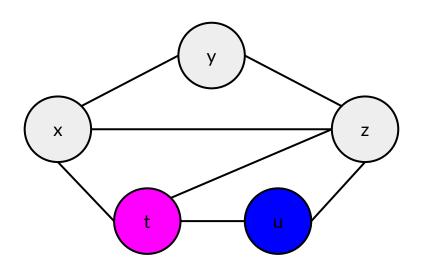
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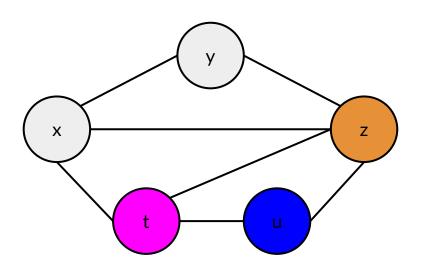
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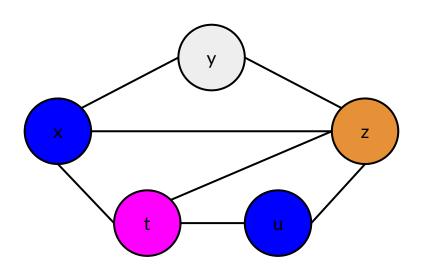
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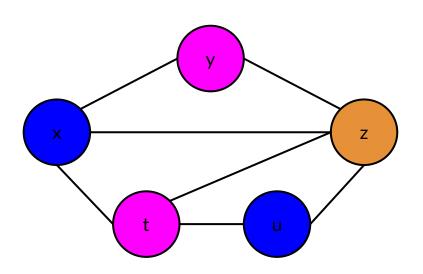
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- Implementing a global register allocator correctly is a challenge
  - I don't expect all (or even most) of you to succeed at this, and it is not required for PA4

#### **Course Announcements**

- The PA4 leaderboard is still Coming Soon™
  - Unfortunately the technical problems here were tougher than I expected, so I am changing how it works
    - More details to come in the next day or two...
- Due to popular demand, I have changed PA4c1's specification to also allow the input to be a . cl-type file (originally was TAC)
  - PA4c1 is due April 28, and is mostly optional