The Big MAC

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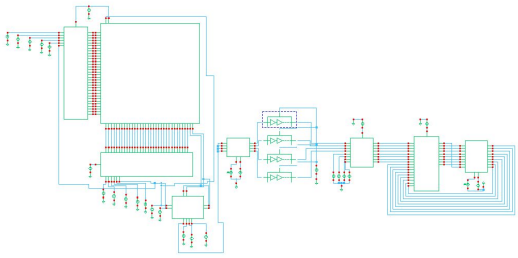
Introduction

We are interested in designing a system that to be a good balance of power and delay i.e. best power-performance ratio. Using deep learning technique of multiplication and accumulation (MAC) datapath for neural networks, we came up with a system with low power consumption and at the same time, less delayed. We more focused on low power consumption with power input of 950mV. To get the best results, we tried to use less transistors as possible because using more transistors mean more power consumption. That's why we we used 1 bit adder using transmission gate (TG) which has 20 transistors over CMOS full architecture which were using 28 transistors.

System Overview

For our system, we decided to go with low power consumption compared with high performance. We designed the different components to give us the least amount of power consumption with less delay possible.

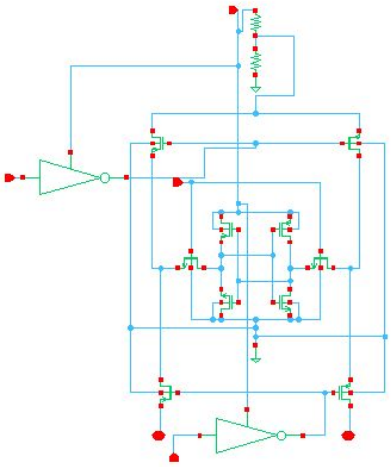


PIPO takes 4 bits from SRAM and forward them to inverter chain to reduce the delay. The inverter chain then forward these 4 bits to multiplier with 4 bits combinational input from user. The multiplier does the multiplication and forward the 8 bits result to adder. The 8 bits are forward to 9 bits PIPO which return 8 bits to adder and keep one bit space for carry.

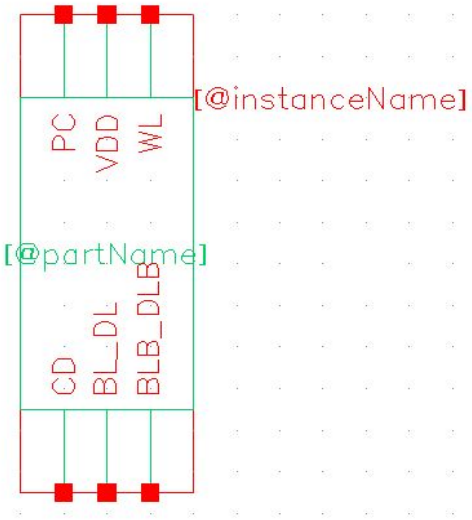
Component-Level Design Styles

SRAM which stands for Static Random Access Memory is a type of non-volatile memory which uses 6 CMOS transistors. It is the fastest memory type because of its fast switching compared to other memories.

Transistor level diagram of SRAM:

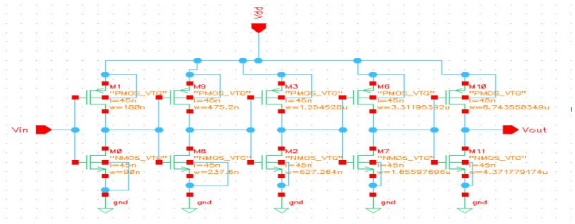


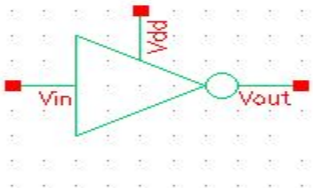
SRAM block diagram



To figure out the optimal number of stages in the Inverter Chain, we had to do some calculations and put it on the table. After seeing the stage that gave us the least amount of delay, we kept that in mind and tested every stage. From the results, we confirmed that the 5 Inverter Chain had the least delay which we then decided to integrate into the whole system.

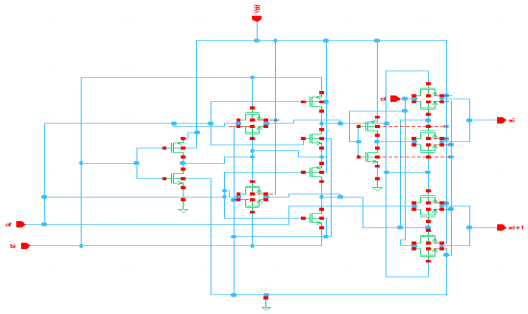
Inverter chain transistor and block diagram:



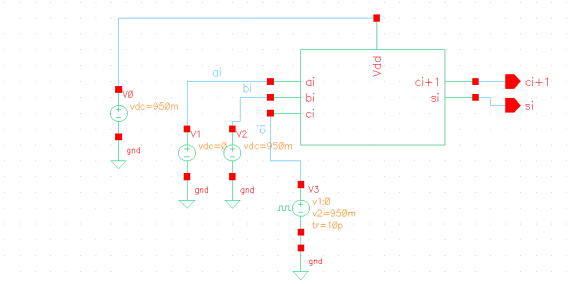


To design the 8-bit Carry Select Adder, we had to test the CMOS and transmission gate 1-bit full adders. Since we are going for low power consumption, we decided to use the transmission gate 1-bit full adder because TG uses less transistors compared to CMOS full adder architecture. Less transistor means, less power consumption and less area.

Transistor level 1-bit full adder using TG.

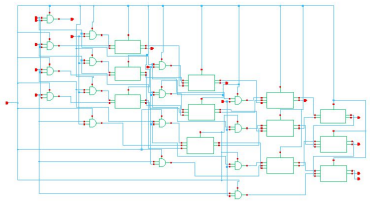


1-bit full adder using TG:

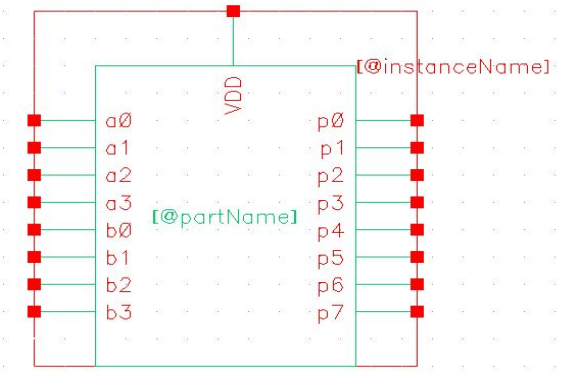


The multiplier composed of 16 AND gates, 4 half adders and 8 full adders to perform the multiplication of 4 bits from PIPO with combinational 4 bits from user.

Transistor level multiplier:

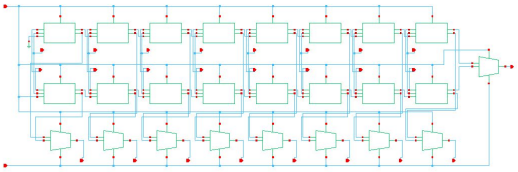


Block diagram of multiplier:

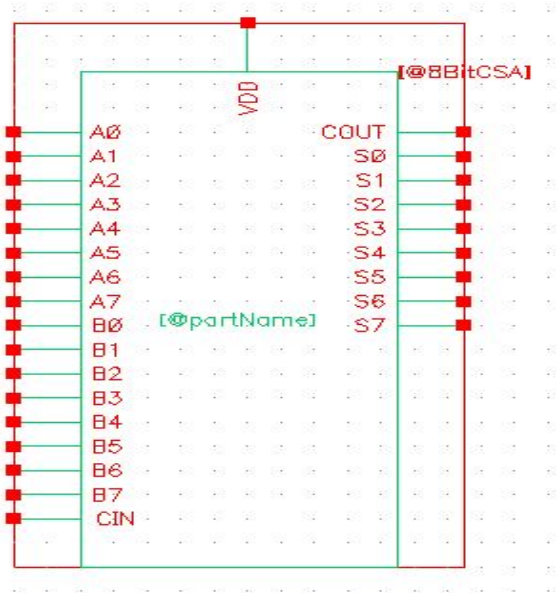


We chose the Carry Select Adder over the Ripple Carry adder because the Carry Select Adder has better performance even though it has a bigger area.

Transistor level diagram of Carry select adder:

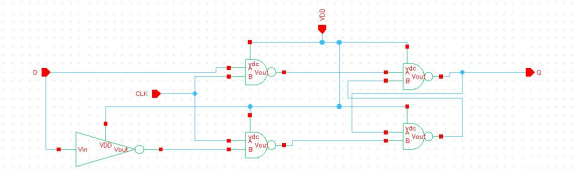


Block diagram of carry select adder

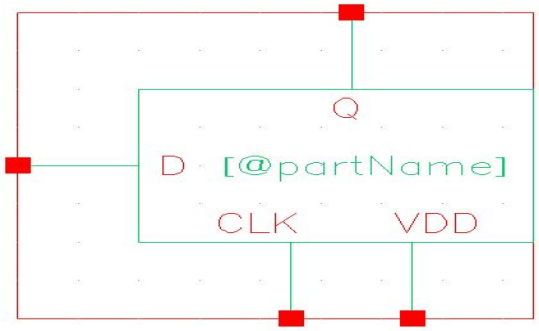


We used D-Flip-Flop for PIPO.

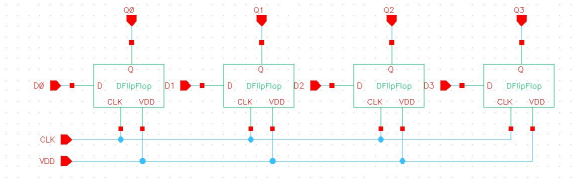
Transistor level diagram:

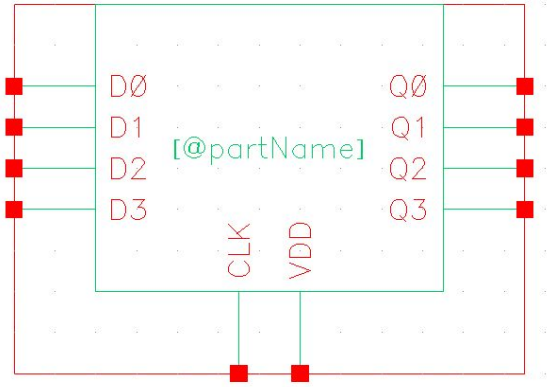


Block diagram of PIPO:



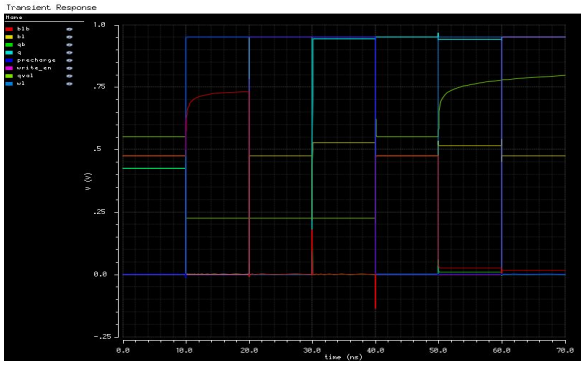
Logic level PIPO diagram:





System Characterization

SRAM characteristics:



Inverter Chain characteristics:

N	Delay(ps)
1	247.6485
2	253.954
3	222.885
4	186.502
5	162.0635

It is sized based on the table.

Number of Stages(N)	Upsizing Factor(u)	Propagation Delay(t_p)
1	1	128
2	11.31	22.62
3	5.04	15.12
4	3.36	13.44
5	2.64	13.2

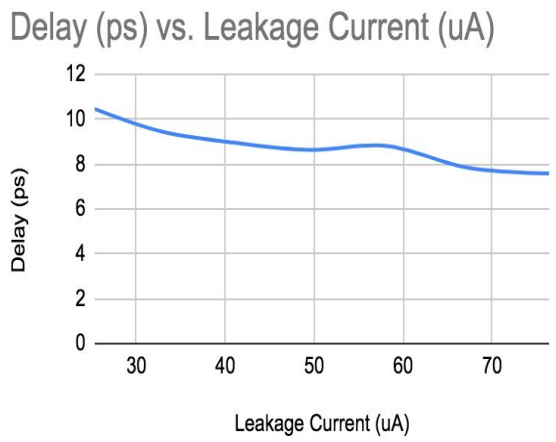
It is running on 950mV.

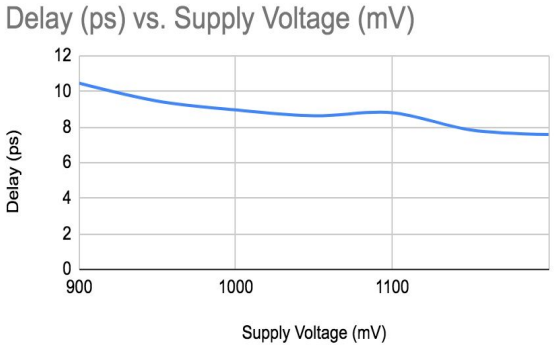
The 5 Inverter Chain consists of 5 NMOS and 5 PMOS.

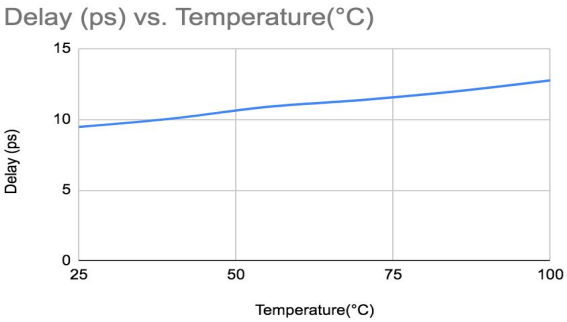
1-bit full adder using TG:

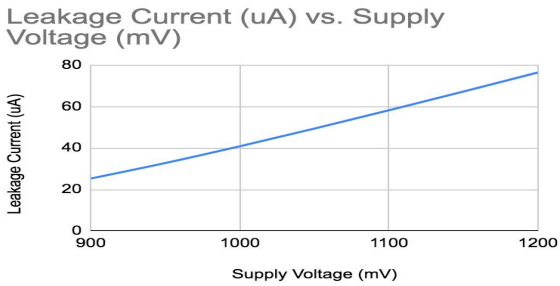
Supply Voltage vs Delay and Leakage Current

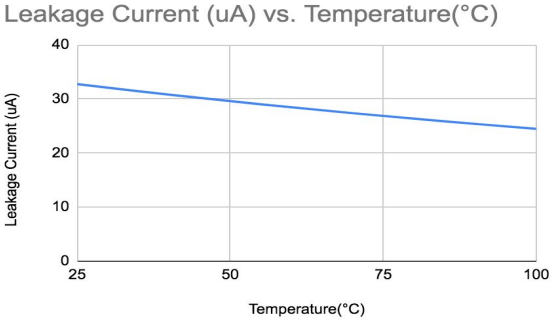
Supply Voltage (mV)	Delay (ps)	Leakage Current (uA)
900	10.4713	25.2961
950	9.4682	32.7623
1000	8.97	40.8472
1050	8.63935	49.3746
1100	8.81755	58.2083
1150	7.84765	67.2507
1200	7.5892	76.4350











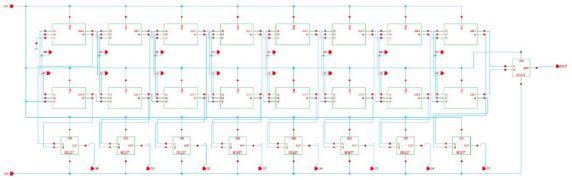
Delay Vs Temperature Vs Leakage

Temperature (°C)	Delay (ps)	Leakage Current (uA)
25	9.4682	32.7623
40	10.065	30.8141
55	10.8854	29.0275
70	11.3632	27.3869
85	11.97675	25.8784
100	12.75135	24.4903

Total number of NMOS are 10 and the total number of PMOS are also 10 in our 1 bit full adder using TG. We size the NMOS 45nm, 90nm and PMOS 45nm and 180nm, So the total area equal to 2700nm.

For delay, we added all the delays from 900mV to 1.2V using increment 50mV. The total delay we got 61.80325ps for our 1 bit full adder using TG.

8-bit Carry Select Adder



Supply Voltage (mV)	Delay (ps)	Leakage Current (nA)
900	1.305	628.91
950	1.365	772.74
1000	1.420	951.77
1050	1.475	1177.70
1100	1.525	1462.59
1150	1.560	1830.52
1200	1.585	2311.99

The 8-bit Carry Select Adder consists 187 NMOS sized at 90nm and 374 PMOS sized at 90nm
It is running on 950mV.

Task Organization

We tried our best to assign an equal amount of work based on difficulty level and each group member tried its best to put as much efforts as possible. We were holding group meetings twice per week and also online meetings when possible. We also helped each other when a group member needed help which equalized the workload among each group member. The most contribution of each group member is as following:
Patrick - Inverter chain, row decoder, Ripple Carry Adder
Karim - NOR gate, Multiplier, PIPO, SRAM
Afzaal - NAND gate, Transmission gate, 1 Bit Full Adder using TG
Evan - XOR gate, PIPO, Carry Select Adder, SRAM.

Conclusion

In conclusion, it was a great experience for each group member even though each one was introduced with cadence software for the very first time. On the positive side, we learnt using the cadence with a lot of techniques and shortcuts which help tremendously analyzing our MAC project and achieving our main goal of making our system low power consumption system with less delay time. The project was perfectly designed to master the students in cadence and analyzing each component of the required system. Ahish, our teaching assistant, was very helpful throughout the semester and went beyond in helping us. Overall, we achieved our goal of making low power consumption system with less delay and also with gain of real industry level experience using cadence software.