

OPEN-SOURCE MINIATURIZED TEST-BENCH DESIGN FOR
APPLICATIONS IN WEARABLE AUTONOMOUS ULTRASOUND
IMAGING

by

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**Open-Source Miniaturized Test-Bench Design for Applications in
Wearable Autonomous Ultrasound Imaging**

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*Dedicated to my great grandma, Rachel.
She always believed I could become an engineer.*

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Abstract

Open-Source Miniaturized Test-Bench Design for Applications in Wearable Autonomous Ultrasound Imaging

Abstract

by

GEORGE P. ENWIA

0.2 Abstract

Portable ultrasound systems are becoming more available and reliable. These systems are used for a variety of applications and research because they allow for innovations in beam-forming methods, imaging modalities, and visualization techniques. This thesis presents a low cost 64-channel portable ultrasound system based on System-on-Chip (SoC) architecture that will aid in the development of wearable autonomous ultrasound imaging applications.

Currently, the system features a multiplexer board, custom transceiver board, and SoC development board (Terasic DE-10). The transceiver features on-board high voltage (HV) pulse generation, analog to digital conversion (ADC) capabilities, and a 12V battery pack for power. The multiplexer board uses 64 solid state switches that allow for fast transmit (Tx) to receive (Rx) transitions. The SoC uses embedded software that runs the system autonomously. The system also allows for interchangeable front-end

probe circuitry by allowing for on- or off-board Tx/Rx switching. Presented here is the development and verification of this design.

1 Introduction

1.1 Motivation

Ultrasound is an attractive field because it is a well-established imaging method that is used widely for medical diagnosis and operations. It is non-invasive, portable, low-cost, and radiation-free. Traditionally, ultrasound has been a stationary tool used in medical establishments. As technology has improved, so have the prospects of having an ultrasound machine on the go^{11,6}. Recent research has explored designing application-specific integrated circuits (ASICs) to do the front-end beam-forming or analog to digital conversion of the system, while a field programmable gate array (FPGA) is used for the back-end processing^{5,12–15}. System-on-Chip (SoC) is another technology that has an FPGA and a hard processor system (HPS) in one package⁷. This means that there is no longer a need for a dedicated PC, like in medical applications. By combining these technologies, progress has been made into developmental applications that incorporate FPGA and ASICs together for front- and back-end functionality. This allows for more experimental applications that focus their functionality improvements in a specific way, such as imaging much smaller features in the body^{16,17}. These applications require higher signal-to-noise ratio (SNR) and also need to allow for the use of different imaging modalities.

The long term goal of this research is to develop a portable conformal ultrasound imaging system that is self-powered and able to locally display real time images^{18–20}. Before the work of this thesis, my previous colleagues (Alex Roman, Vida Pashaei, and Parisa Dehghanzadeh) demonstrated a test-bench ultrasound application that proves functionality of a portable system based on a system-on-chip (SoC) architecture^{21–23}. The SoC architecture combined front end circuitry and an ultrasound probe to demonstrate that the system could generate and output ultrasound pulses, then receive echoes and turn that data into an image using high-level languages such as Python (which can run locally on the SoC) or MATLAB (PC-based). This work is discussed further in the following papers: “An Open-Source Test-Bench for Autonomous Ultrasound Imaging” and “Conformal Ultrasound Transducer Array for Image-Guided Neural Therapy”^{21,22}. It is also described in depth in an M.S. thesis named “Open-Source Test-Bench Design for Applications in Autonomous Ultrasound Imaging”²³.

There is a lack of ultrasound systems that are suitable for low cost research. Currently, research based applications are either high cost, like the Verasonics systems (see Fig. 1.1), which cost at least \$50,000. These systems are meant for testing new imaging and beam-forming algorithms, because the software is programmable. Apart from cost, another problem is that these systems do not allow for innovation in hardware design. The ULA-OP research ultrasound system²⁴ is similar, in that the system allows for software innovation, while also having configurable hardware modifications. For example, different front-end circuitry can be used without changing any of the internal PCBs. The only issue with the ULA-OP system is that the hardware alone costs roughly \$60,000. The benefit of allowing for variable front-end circuitry means that a cheaper probe can

be purchased to counteract the high cost of hardware. But overall, these systems are not considered low-cost.



Figure 1.1. A picture of a typical medical ultrasound cart machine.

There are also consumer systems, like the Butterfly-IQ, that cost roughly \$2,000 for the probe and allows for image generation on phone. The system is very efficient, perfect for point-of-care applications, and very reliable for casual ultrasound usage²⁵. The problem with this system is that the hardware and software are fixed. There is no way to implement new or innovative techniques with this application, but it works reliably for what it is intended to do. Fig. 1.2 shows the probe and image generation on a cellphone.

To the best of my knowledge, there are no ultrasound systems that fall between these extremes. What is presented in this thesis is a system that aims to bridge this gap by being both i) low-cost, and ii) highly configurable in terms of front-end circuitry and back-end programming. Coming in at roughly \$1,000 for all the hardware, the system can be used for implementing neuro-modulation by using a custom ultrasound probe with pre-amplifiers built on-board to improve SNR (see Fig.(1.3)). The system can also interface with established probes, like the Blatek linear array probe used in this thesis. Because of the versatility of the system, the door is open to easy assembly and testing



Figure 1.2. A picture of the Butterfly-IQ system from their website: <https://www.butterflynetwork.com/>.

for hobbyists. This system also presents a very simple platform for people new to ultrasound. For example, using this system in ultrasound courses is possible because the front-end circuitry can be populated by hand while the back-end programming is also simple enough to modify, in order to understand the basic principles of the imaging modality.

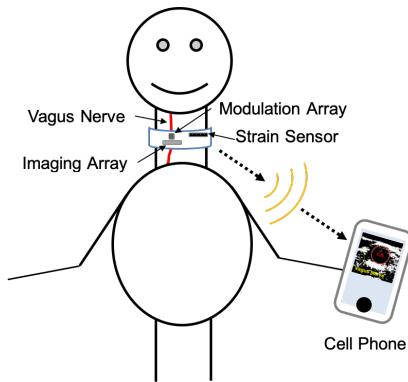


Figure 1.3. A diagram of the proposed wearable neuro-modulation array for vagus nerve therapy¹. Similar systems can be used for peripheral nerve stimulation.

The goal of this thesis was to develop the system discussed in the previous paragraph by advancing the work of the previous group. Specific advances include i) further

increasing portability and power efficiency, and ii) decreasing the footprint and complexity of the system. This thesis will discuss how these advancements were achieved and how the updated system compares to its predecessor.

1.2 Previous Work

To give a clear explanation of the goals of this thesis, it is necessary to understand the research that came beforehand. The test-bench system, discussed in the motivation, ran using an SoC architecture that controlled beam-forming, multiplexing, ADC functions, and data acquisition^{21 22 23}. This was done by using an SoC development board (Terasic DE-10), a HV pulser chip-set from Texas Instruments that consisted of the beam-former (LM96570), the high-voltage (HV) bipolar pulser (LM96551), and the duplexer or transmit/receive switch (LM96530). This transmitter also required eleven DC power supplies to function. The design uses a multiplexer board because the transmit and receive signals come in parallel. The receiver board used was an Analog Devices development board that has an eight channel ADC (AD9276) designed for ultrasound applications. Overall, this design employed one DE-10, a development board, four custom printed circuit boards (PCBs), and around thirty various connectors. Fig. 1.4 shows the old system with each of the modular portions labeled without connections, and a fully assembled version with the cables.

After the data was collected in the FPGA, it would be transmitted to the hard processor system (HPS) on the SoC and saved. The post-processing for this system happened after each set of data was acquired and then it was saved as a file. An image was then generated using Python (locally) or MATLAB (remotely on a PC). Note that MATLAB could not be run locally on the HPS because of its large footprint, memory requirements, and

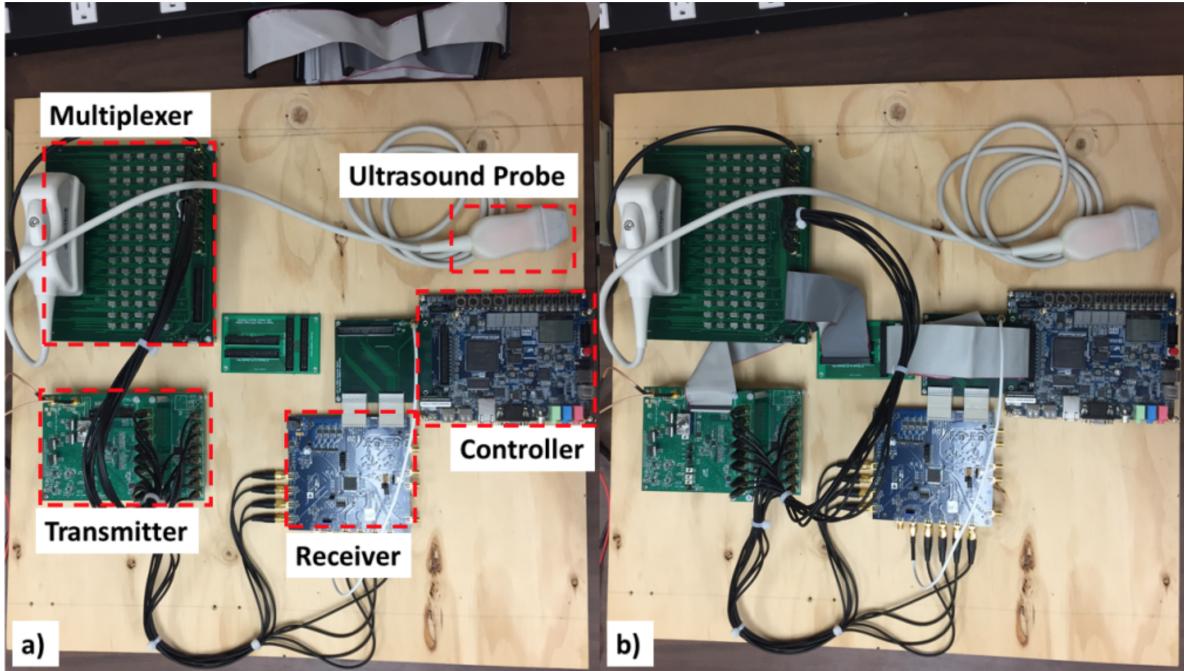


Figure 1.4. (a) The test bench system with each module labeled and no cable connections for clarity. (b) The test bench system fully assembled.

lack of support for the HPS's ARM architecture. On the other hand, Python does run on the HPS, thus enabling embedded image generation. However, the relatively slow HPS resulted in long image generation times (~2 sec), which limited the real-time ability of this system. Overall, the system did work well and reliably produced images. Although, since the majority of the effort was put into getting the system functional, there was a lot of room to improve the performance of the system.

While the previous work was done to prove functionality of the proposed SoC based ultrasound imaging system, the work of this thesis focuses intensely on optimizing the system and progresses the project towards being portable. As mentioned previously, the end goal of the research is a wearable system that is battery-powered and can display images locally. This work is first and foremost intended to be a stepping stone in that direction. The final results show promise that decreasing the size and complexity are

possible, but do not display the system in a fully portable state. There is much more work to do in terms of condensing the system into a portable unit, but as a jumping point, this thesis work serves as a start in the right direction towards full portability.

1.3 Background of Ultrasound

At its core, ultrasound is the acoustic equivalent of shining a flashlight through a medium to see what is concealed. Ultrasound has historically been used as a medical tool in order to get a glimpse of what is inside of the body using sound waves. The basic principle that drives ultrasound is the idea that energy, in the form of a mechanically generated sound wave, is sent into a medium and interacts with the particles of the medium. As these waves travel, they encounter changes in acoustic impedance, which represents the sound reaching a new material, such as soft tissue to bone. When the wave encounters a boundary, the energy of the wave can interact in a few different ways. Depending on the angle that the wave hits the boundary, energy is attenuated, reflected, refracted, or scattered in different ways. Fig 1.5 shows these interactions visually. Attenuation, reflection, and refraction happen as the wave travels through the medium. Scattering occurs when the wavelength of the sound waves strike objects that are relatively smaller than the size of the sound wave³. For the purpose of medical ultrasound, only reflection and scattering give useful information into what lies behind the surface. The reason being that reflection and scattering return some of that energy in the reverse direction of the wave, allowing that energy to be recaptured and turned into voltage that is recorded and eventually turned into images.

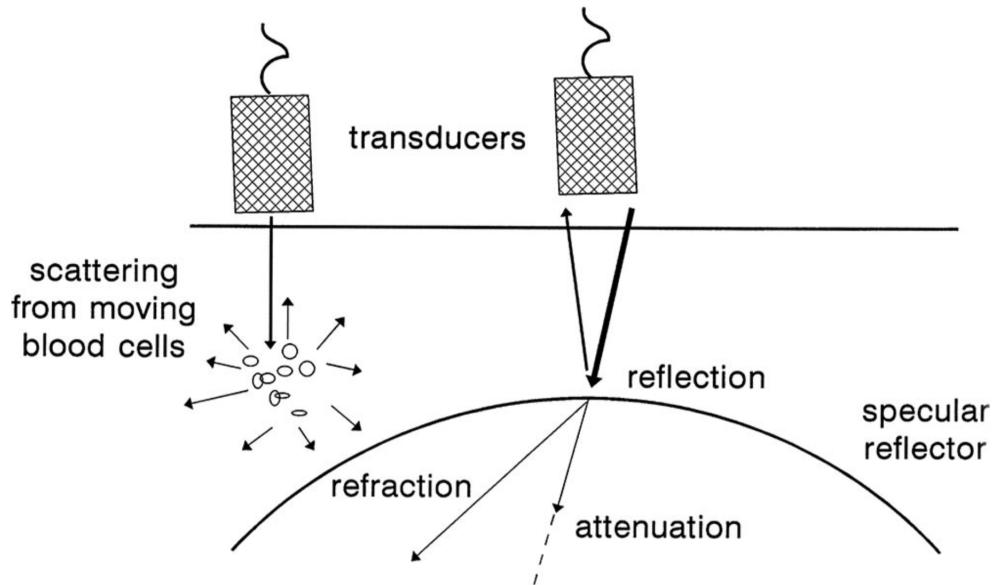


Figure 1.5. The four interactions ultrasound waves can have with biological material: attenuation, reflection, refraction, and scattering²

1.3.1 Pulse Generation and Acquisition

Originally discovered by the Curie brothers, the piezoelectric effect is a staple in the development of ultrasound technology². Piezoelectric crystals are generate electric charge when exposed to mechanical stress or conversely will experience stress when exposed to electricity (known as the reverse piezoelectric effect). This phenomenon is significant for ultrasound because it allows for a convenient method to electrically generate mechanical sound waves and receiving the reflected energy in the form of an electric potential (mechanical, meaning transferred through particles). Specifically, sound travels longitudinally, as seen in Fig. 1.6.

The sound waves generated have a few parameters that describe them quantitatively. Period describes the time required for one cycle. Frequency is the inverse of the period, but refers to the number of cycles completed per second. Amplitude refers to the maximum displacement delivered by the wave. Wavelength refers to the physical length of

Longitudinal Wave Particles move in the *same direction* as the wave:

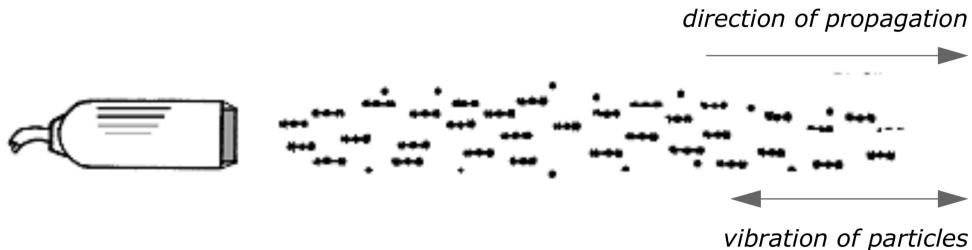


Figure 1.6. Longitudinal waves cause particles to vibrate in the same direction as the waves propagation³

one cycle of the wave, which is directly proportional to frequency. The last parameter that helps describe sound waves is propagation speed, which is the rate that the sound wave travels through a given medium. Propagation speed only depends on the properties of the medium, because no matter what frequency, sound travels at the same speed if traveling through the same medium. Table 1.1 displays the different densities, speeds of sound, and acoustic impedance of materials found in the body.

Table 1.1. Ultrasound Material Density, Speed, and Acoustic Impedance

Medium	Density (kg/m^3)	Speed of Ultrasound (m/s)	Acoustic Impedance ($kg/(m^2 * s)$)
Air	1.3	330	429
Water	1000	1500	1.5×10^6
Blood	1060	1570	1.66×10^6
Fat	925	1450	1.34×10^6
Muscle	1075	1590	1.70×10^6
Bone	1400 - 1900	4080	5.7×10^6 - 7.8×10^6

1.3.2 Operational Frequency and Wavelength

There is a fundamental trade-off that comes with choosing operation frequency for ultrasound. Higher frequency (shorter wavelength) ultrasound is attractive because it offers the best resolution, but penetration depth is much shorter. Conversely, with low frequency (longer wavelength) ultrasound, you obtain much higher penetration, while

losing resolution²⁶. Fig. 1.7 depicts this effect graphically, by showing that as wavelength decreases, penetration increases. Most medical ultrasound operational frequencies lie between 1-20MHz². The operational frequency of a specific application depends on the type of probe being used. The probe has a predetermined center frequency and bandwidth. For example, transthoracic probes function in the lower side of the frequency range, at 2-3MHz. These probes are usually used to image the motion of the heart, which is deep in the body and behind bone structures. The low center frequency is helpful here because those waves penetrate deeper into the body and although resolution is lower, returning echoes are large enough to be captured. Higher frequency probes are also available, but are mainly used to image structures closer to the surface of the skin. This is because, as mentioned before, the scanning depth is much shallower. For artifacts with shallow skin depth, the higher resolution makes high frequency probes attractive.

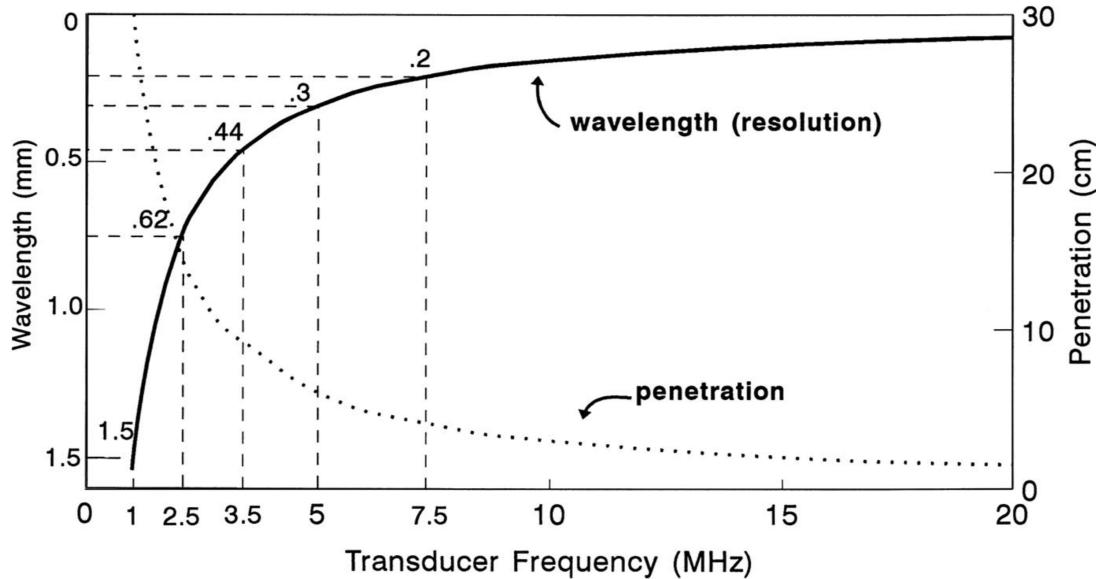


Figure 1.7. Relationship between resolution and penetration of ultrasound frequencies from 1-20MHz.

1.3.3 Ultrasound and the Body

The body is the main medium of transmission for ultrasound. In order to understand how ultrasound echoes give meaningful information into what lies under the skin, we must understand how the waves interact within the body. Fig. 1.8 visually displays the areas of compression and rarefaction as a wave travels through tissue. Since the body is made up of many materials of differing composition, we need a way to classify the way sound interacts with them all. Acoustic impedance is the main method of characterising materials in the body, with regards to ultrasound transmission. Acoustic impedance is related to the density of a material and the propagation speed within that material. The equation $Z_0 = \rho \times c$ describes this relation, where Z_0 is the acoustic impedance, ρ is the density, and c is the propagation speed. As mentioned earlier, sound waves experience refraction, reflection, and attenuation as they travel through changes in medium or tissue. There are a few conditions that determine how these interactions occur. When there is a large change in density between the two regions, like in the case of a sound wave traveling from soft tissue into bone, a few things happen. During the impact, some energy is refracted into the bone material, but because the acoustic impedance varies so much (1.6 vs. 7.8), a majority of the energy is reflected. This means a strong echo is returned in the direction of the probe. The angle of incidence matters though, because if the echo strikes at the wrong angle, it may be sent back in a direction that is missed by the probe. A similar occurrence happens at the boundary of two mediums of similar density, like soft tissue to fat. Because the transition is not as stark, most of the energy is refracted as it travels into the new medium. When the energy is refracted, the direction of travel is changed. This happens to compensate for the change in the speed of propagation when it enters the new medium⁴. In this example, the speed would change

from 1540 m/s to 1450 m/s . Unfortunately, since most of the energy is transmitted at this boundary, a smaller echo is reflected back towards the probe.

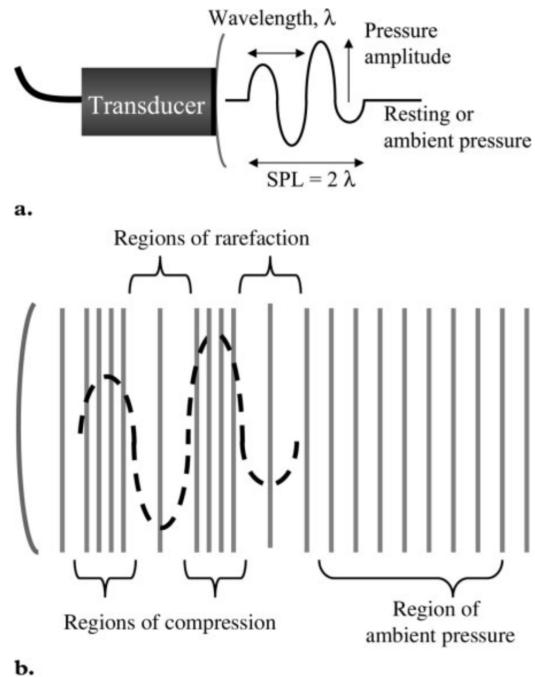


Figure 1.8. (a) Shows an ultrasound pulse being generated from a transducer with wavelength, spatial pulse length (SPL), and pressure depicted. (b) Shows tissue elements in the form of grey lines to illustrate the effects of the ultrasound wave traveling through the tissue⁴.

As implied in the term “acoustic impedance”, the further the sound waves travel in a medium, the more energy it expends. The concept is similar to friction, but the particles that are being moved, absorb some of the energy passing through. The deeper an artifact or region of interest is, the more energy is needed to overcome the attenuation in order to get an echo back to the transducer.

1.4 Literature Review

As mentioned earlier, recent ultrasound systems have been developed around ASIC, FPGA, and SoC architectures. Here we will discuss some of these systems and their specifications, strengths, and weaknesses to get a better idea of what other systems there are on the market, how these systems function, and what they have to offer.

1.4.1 FPGA-Based Portable Ultrasound Imaging System for PoC Applications

The first system we discuss was designed by Gi-Duck Kim *et.al.*⁵. They use a mobile processor that runs Linux. The processor interfaces with the FPGA to directly transfer the ultrasound image data. This avoids using a video processing unit and thus saves time during the transition. The system is able to achieve 30 frames per second, showing that their application does provide real time images.

Their hardware design uses a Spartan-3 FPGA chip to interface between the front end circuitry (pulse driver, pulser, ADC) and back end circuitry (CPU with Linux kernel and LCD screen). The FPGA is in charge of beam-forming for both transmission and reception, mid processing, and back end processing. Because the FPGA takes care of the beam-forming, they output directly to pulse drivers that interfaces with 16 pulsers, as their system has 16 channels, and their center frequency is $3.5MHz$. The receive path consists of HV multiplexers and an ADC that runs at $40MHz$ and uses low voltage differential signaling (LVDS) to transfer the data back to the FPGA. The FPGA then goes through and runs the mid and back end processing , where DC canceling, time gain compensation, low pass filtering, envelope detection, and down-sampling all occur. After this, the data is transferred to the CPU module.

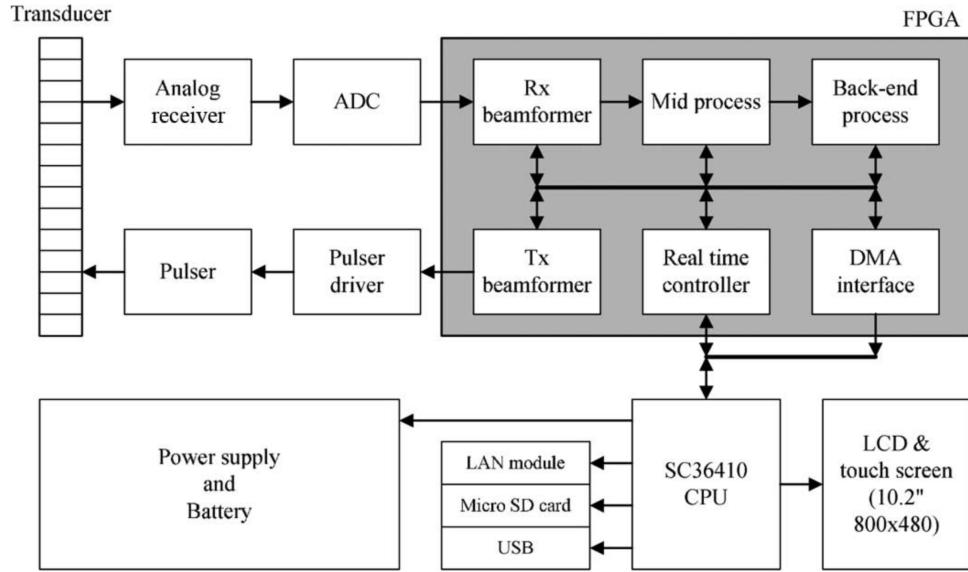


Figure 1.9. Block Diagram of Portable Ultrasound system described in ⁵.

The Samsung S3C6410 is used to control all the sub-systems and display images to the LCD screen. Having the dedicated CPU allows for many peripheral features like USB and SD card interfaces. The more important aspect for their application is the digital video interface that allows them to constantly display to the LCD screen. In order to ensure that this system is portable, they also provide power to it with a power supply module. This consists of 4 Li-ion batteries that can support the system for about 1.5hrs. All of their necessary voltages are generated from this battery pack. Fig. 1.9 shows the block diagram for their system and the breakdown of tasks for the FPGA. Their system does a good job at exhibiting what it means to be truly portable by powering and generating all their power sources on board, laying everything out on interfacing PCBs, and using a dedicated LCD screen for image display. Although, this system does lack the robustness of most medical ultrasound systems which usually have anywhere from 32 - 256 channels. This system has 16, which works for their application, but in order to get better resolution, more channels are needed.

1.4.2 FPGA-Based System for High Frequency Ultrasound Imaging

This next system, designed by Jeeun Kang *et.al.*⁶, uses a Virtex-7 FPGA by Xilinx Inc., but their application focuses more on intravascular ultrasound (IVUS). IVUS is mainly used to gain information about blood flow, which in turn gives insight into the artieries. This type of system allows for the detection of arterial calcification, which if caught early, can prevent strokes. The system utilizes high frequency ultrasound, which uses much higher frequencies that typically lie in the $20\text{-}50\text{MHz}$ regime.

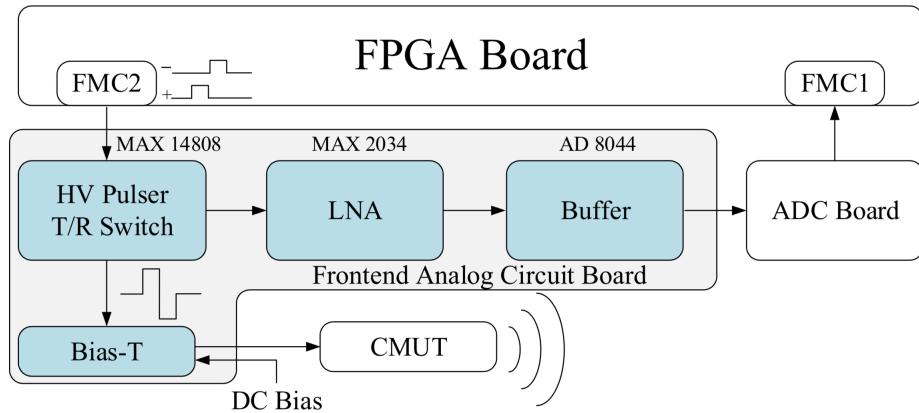


Figure 1.10. Block Diagram of the front end circuitry described in⁶

The system consists of a dedicated PC that is connected via peripheral component interconnect express(PCIe) that acts as the direct data link between PC and FPGA that samples at 125MSPS. Because they have higher imaging frequency, they also use higher operating frequencies, namely 20MHz for their transmit path and 60MHz for their receive path. They are able to achieve 170 frames per second for this ultrasound system, but like the previous system, this one only has 16 channels. Fig. 1.10 shows the block diagram of the front end design of the system described in⁶. As mentioned earlier, the FPGA is connected back to the dedicated PC through the PCIe board.

The group thoroughly breaks down the system from the a second block diagram in Fig. 1.11. This figure shows the different clock domains and the transmit versus receive paths. It also depicts that all of their clock domain transitions are located in the FPGA. This design choice is beneficial because clock transitions are very difficult to handle in a PC system. This system also benefits because it has on-board DDR3 memory, which ensures that storage size is not an issue. The group uses a FIFO buffer to read and write data into the memory, before it gets sent over to the PC for image processing and display. The system presented in this paper provides a great platform to develop and test imaging algorithms, but it falls short in terms of image resolution. This is a trade off that comes with being limited by cost.

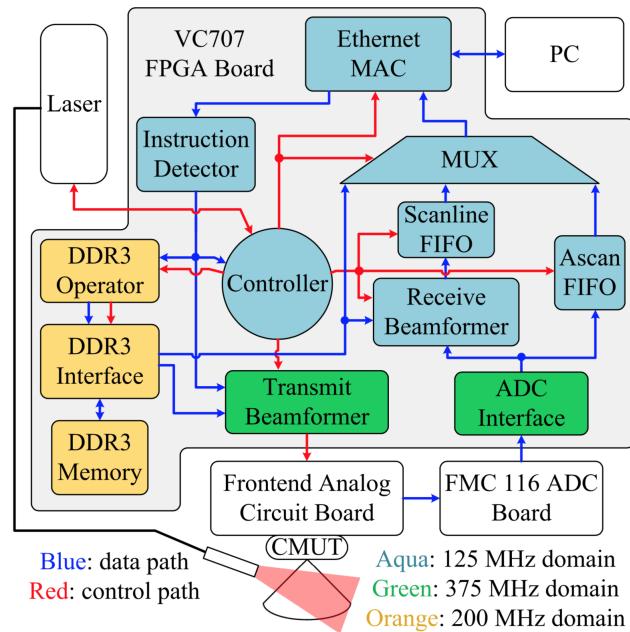


Figure 1.11. Block Diagram of the full system described in⁶

1.4.3 System-on-Chip solution with ASIC implementation

The last system we talk about here takes a slightly different approach to solving the portable ultrasound problem. Jeeun Kang *et. at.* describe a comparable system that employs an ASIC that includes all of the front end circuitry, including pulse generation, receive beam-forming, mid processor, and Doppler processing, all in a single package. They specify that it is a $27 \times 27\text{mm}^2$ chip that consumes 1.2W . Their system was developed around this ASIC and implemented into a compact $200 \times 120 \times 45\text{mm}^3$ package that is fully-portable and battery-powered. Their system has 32 channels, but is designed for scalability of up to 128-channel operation. This is done by cascading up four chips.

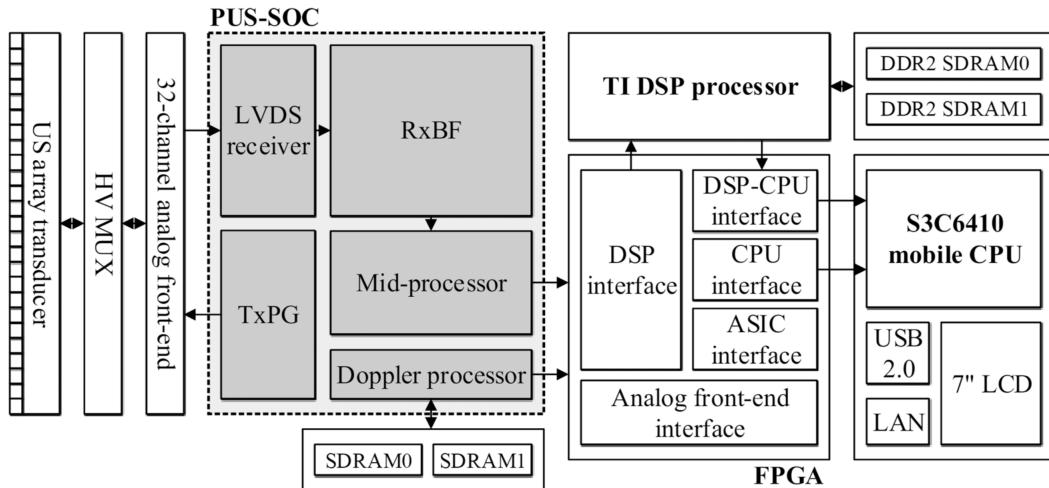


Figure 1.12. Block Diagram of Portable Ultrasound system described in ⁷

Fig. 1.12 shows the block diagram for their ultrasound system. As mentioned before, the ASIC is used for front end transmit and receive, while the FPGA is implemented between the front end circuitry and CPU. The FPGA takes care of sending the incoming data to the DSP and relaying it to the CPU for image display. The group has achieved

30 FPS (frames per second) with the system and is able to run it for roughly three hours on the battery pack.

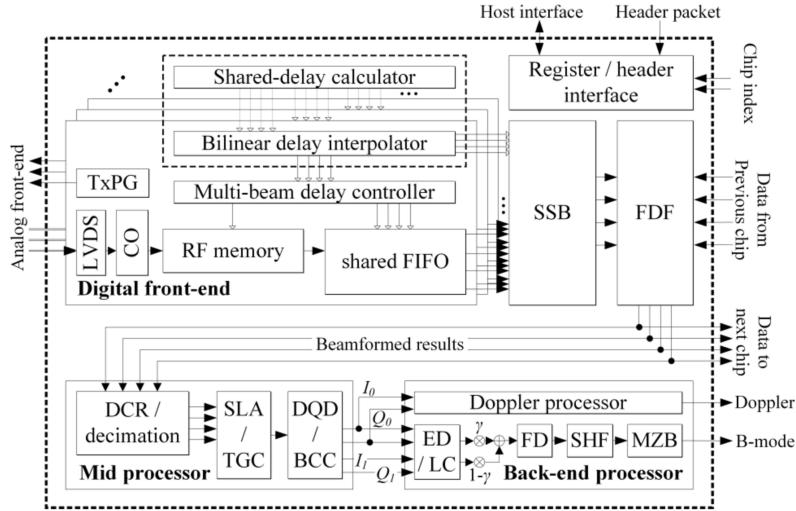


Figure 1.13. Block Diagram of SoC ASIC designed in ⁷

The system has a lot of flexibility designed into it, as the pulse shape and sequence are user defined parameters, this allows for different imaging algorithms to be tested. The other benefit is that by allowing the cascading chips, they are able to achieve much higher image resolution. The group also has extended aperture capability, which can effectively double the number of elements. For these reasons, this system is very impressive and can be used in a wide number of applications.

1.5 Thesis Structure

The rest of the thesis is structured as follows: Chapter 2 discusses transceiver design, probe board design, and updates to components since the last groups work. Chapter 3 discusses imaging methods. Chapter 4 discusses the merging of the old system's software with the changes in the new system. Chapter 5 discusses the experimental and

verification results of the system. Chapter 6 concludes the thesis, and Chapter 7 discusses potential next steps for the project.

1.6 Published Works from this Research

Two works were published as result of this research:^{1,9}. The first is a conference paper with me as the first author, while the second is a journal paper with me as a co-author.

2 System Hardware

2.1 Overview

The system contains four main parts: the controller, the transceiver, the ultrasound probe board, and the ultrasound probe. The controller, which consists of a DE-10 Standard Development board, is programmed to generate signals, receive signals, and do the back-end processing through a single High Speed Mezzanine Card (HSMC) connector. The HSMC connector plugs the transceiver board directly from the transceiver into the DE-10.

The transceiver board generates all supply voltages locally, produces high voltage (HV) pulses, and converts incoming analog echo voltages from the probe into digital signals that are fed back into the DE-10 for storage and processing. To do this, the transceiver employs a few integrated circuits, namely the SN74LV4T125, MAX14808, AD-9276, LT8362, and LT1763 chips. The reasoning behind why these ICs were selected and how they all work will be discussed in this section.

The ultrasound probe board multiplexes the transmitted and received signals to the ultrasound probe. The ultrasound probe contains the 64 channel transducer array which outputs the ultrasound pulses and receives the returning echo voltages. The MAX14866 is the IC used to multiplex our eight channel system to the 64 elements. The choices and

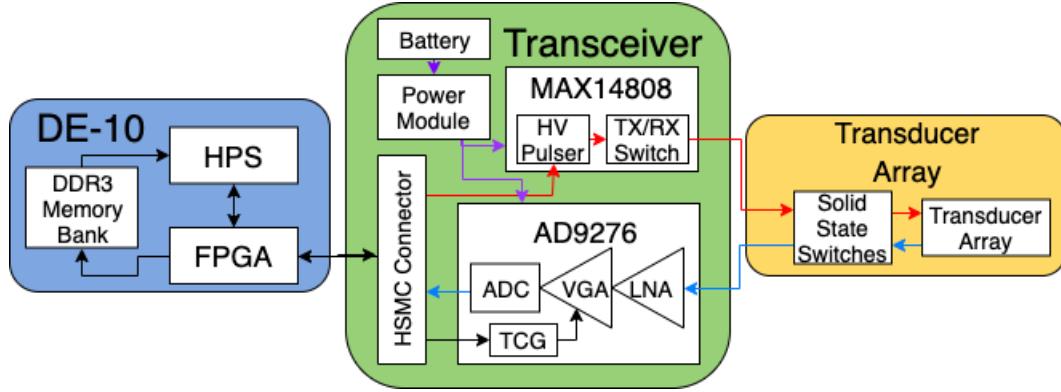


Figure 2.1. Simplified block diagram of the system, including SoC, custom transceiver, breakout board, and ultrasound probe.

design of this board will be discussed at the end of the section. Fig. 2.1 contains a block diagram of the design to make the process easier to visualize.

In order to directly compare the original system developed in²³ with the new version, Table 2.1 shows specifications of both systems. Clearly the new system is smaller, consumes less power, and can be reprogrammed much faster (due to replacing reed relays with solid-state switches).

Table 2.1. Comparison between previous system and current system

Configuration	Previous	New
Footprint	$30 \times 30 \text{ in}^2$	$7.5 \times 18 \text{ in}^2$
Active Consumption	2.35 W	2.184 W
Passive Consumption	795mW	336 mW
MUX Reprogram Time	200 μs	4 μs
Component Cost	\$-	\$700
DE-10 Cost	\$300	\$300
Ultrasound Probe	\$ 4,000	\$4,000

2.2 Transceiver Design

The custom transceiver condenses the bulk of the system hardware onto a $5.6 \times 6.7 \text{ in}^2$ size PCB. This advancement was suggested by the previous group for good reason. By implementing the transmit and receive circuitry on one board, the size, complexity, and

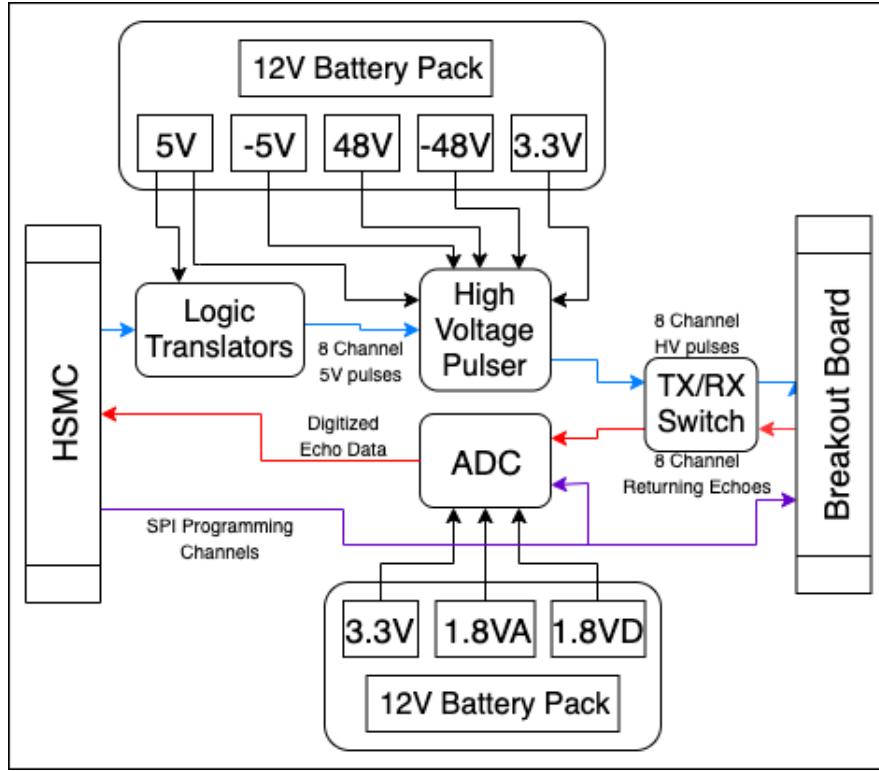


Figure 2.2. Simplified block diagram of the custom transceiver.

power efficiency all improved. The custom transceiver eliminated roughly twenty five connectors, four PCBs, and cut the footprint by about half. There are only four connectors needed for the custom transceiver: one HSMC connector, 12 V power connections from a battery pack, and two sixteen-pin LX connectors that plug into the ultrasound probe board. Because of the number of analog connections, digital connections, and power planes, this board is six layers. We will now discuss the way this board was designed and what is actually on it. For clarity, this section will be broken up by the main ICs on the board: LT8362, LT1763, SN74LV4T125, MAX14808, and AD9276. All circuit schematics and layouts can be found in Appendix A. Fig. 2.2 shows a simplified block diagram of the custom transceiver PCB. Some peripherals discussed in this section are removed for conciseness.

LT8362. The LT8362 is a very versatile power supply. It can be configured to be a boost converter, SEPIC (single-ended primary inductance converter), or inverting converter. The input voltage range is 2.8 V-60 V, which covers our 12 V input. The LT8362 is used to generate the 5 V supply using a SEPIC topology, 48 V using a boost topology, then 5 V and -48 V from an inverting topology. The LT8362 also features an output enable pin, which is tied back to the SoC to allow for better power management.

LT1763. The LT1763 series of low drop out (LDO) regulators covers a large variety of logic level voltages. In this application, one 3.3 V and two 1.8 V regulators are used to supply logic level voltages to the MAX14808, AD9276, and SPI conversion circuitry. These ICs also feature very low shutdown current, under $1 \mu\text{A}$, which helps keep standby power consumption lower. These are all fed from the 5 V power supply as well, in attempt to lower the voltage drop across these LDOs. This also decreases power consumption by not having the conversion from 12 V down to 3.3 V and 1.8 V, respectively.

SN74LV4T125. In the first version of the transceiver board, this chip was not utilized. It was only after initial testing did the need for these arise. There was a discrepancy between the voltage output from the FPGA and the voltage requirement for the input of the MAX14808. The FPGA can output 1.8 V, 2.5 V, or 3.3 V. Unfortunately, the MAX14808 needs 5 V logic for the pulse inputs and settings. The SN74LV4T125 remedies the situation, because this IC is a logic translator. It can take 1.2 V-3.3 V and translate it up to 5 V. This is done by supplying the chip with a V_{CC} , in our case 5 V, and it will take the incoming signal and output the same signal with translated voltage up to 50 MHz. Fig. 2.3 shows an example translation from the data-sheet of 1.8 V to 3.3 V. It is also worth noting that this translation only takes around 3 ns, so the chip does not introduce any timing concerns.

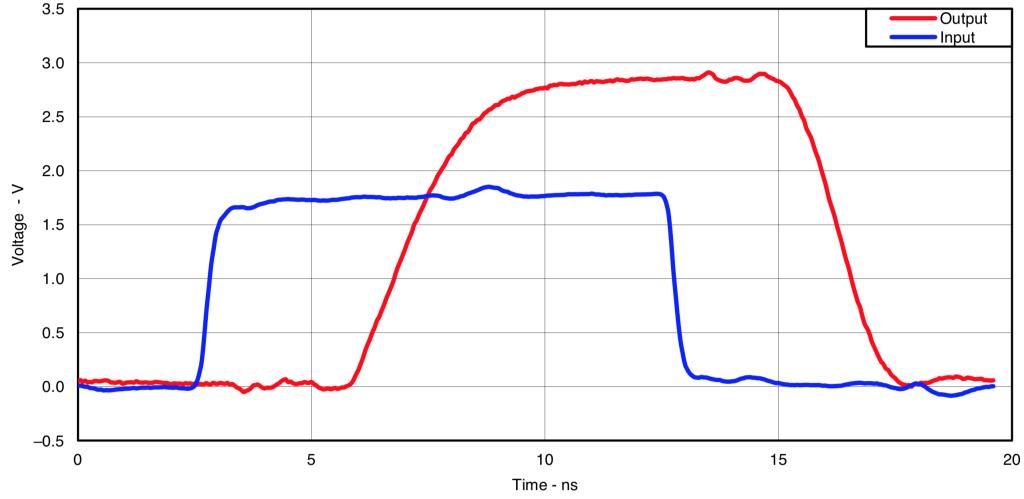


Figure 2.3. SN74LV4T125 translation of 1.8 V logic to 3.3 V logic.

MAX14808. The MAX14808 is by far the biggest contributor to the decrease in hardware and software complexity of the system⁸. The previous group used at least three different ICs to do what this IC does. In this application, the MAX14808 used as an octal three-level high-voltage pulser⁸. It is designed specifically to drive piezoelectric transducers for ultrasound imaging. The MAX14808 comes with many features, such as disable transmit mode, current settings, mode selection, low power integrated TX/RX switches, and low propagation delay. All of these features help decrease the complexity and power consumption of the transmitter.

Implementation of this chip is detailed in the data-sheet, and best practices were followed. Although the MAX14808 is extremely helpful, it was not as easy to implement as it would seem. The inputs seem differential, but they are not. Fig. 2.4 shows the inputs necessary to achieve the desired output for this application. The DINP and DINT signals act as enables for generating the HV pulses. The input voltage for these pulses ranges from 0-100 V. For this application we use ± 48 V supplies to get around a 96 V_{PP} pulse

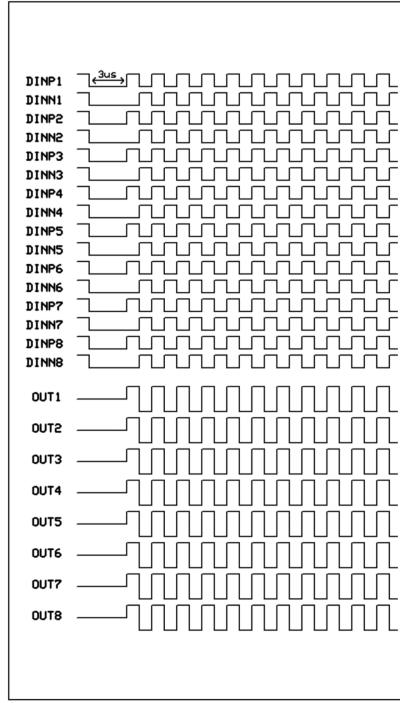


Figure 2.4. Diagram for desired MAX14808 input and output pulses⁸

out. The pulser bandwidth is 20 MHz, which also works well for this application, as this uses a center frequency of 8 MHz with a bandwidth of about 6 MHz.

In attempt to make the board design as user-friendly as possible, all of the customizable settings were routed to the FPGA and can be set in the SoC. The truth tables for the all these settings are in the data-sheet. For our testing, we set the mode settings to Octal Three-Level pulsing, which means *MODE0* is held high and *MODE1* is held low. The MAX14808 also features current limiting by setting *CC0* and *CC1* high or low, depending on the truth table. For our application, we left these alone and used the *2A* setting. The chip also features an over-heat protection pin that will send a low-enabled signal to the SoC if the chip reaches an internal temperature of 150°C. We also hold the *SYNC* pin low, which disables the use of an external clock. For this application, that is fine, but if any phase delays are to be used in the system, this function should be utilized. The

last settings we will discuss regard the internal TX/RX switches. When both inputs are low, the TX/RX switches take about 650ns to turn on and about 20ns to turn off. After the pulse, there is a damping circuit that fully discharges the output of the pulser to not leave any voltage offsets as the received echoes come back. In our application, this damping period also sets the chip in "transmit disabled" mode. The typical power consumption of the MAX14808 is about 73 mW per channel during Octal-Three Level mode, which puts the chip at about 600 mW during active mode. This power consumption drops to about 17 mW per channel during standby, which puts the standby power dissipation at 136 mW. Discussion on programming input pulses and measuring outputs is in the Experimental Setup and Results section.

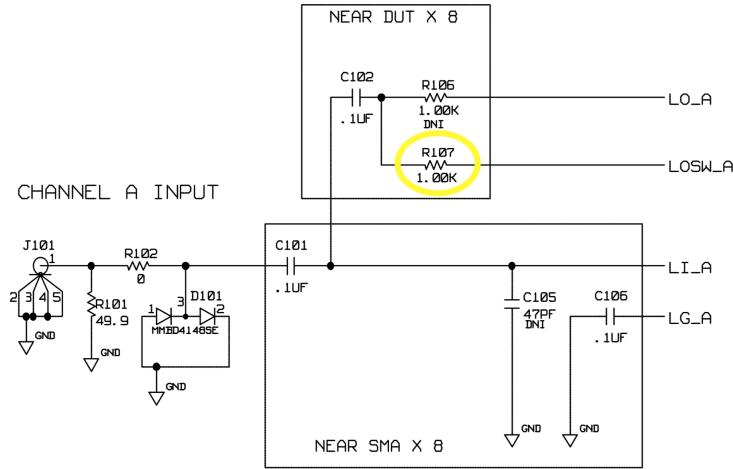


Figure 2.5. Input Circuitry to AD9276 with R107 highlighted to show change

AD9276. The AD9276 is an eight channel ADC (12 bits at 10-80MSPS, SNR 70 dB) with integrated LNA (Gain = 21.3 dB), VGA (Gain = -42 dB to 0 dB), and uses SPI programming. The AD9276 is the same ADC used in the previous system. This IC is specifically designed for ultrasound applications. The only difference in implementation is that this system no longer uses the development board. This system is optimized to function

without all the peripherals that come with the development board. This decision decreases both the overall footprint and the number of connectors needed.

Some layout changes that were made to implement the AD9276 on the custom transceiver include changing the input impedance to better match in output impedance coming from the MAX14808, which is around a 200Ω . As described in the data-sheet, we changed the feedback resistor value in Fig. 2.5 to $1k\Omega^{27}$. Previously, this resistor was 348Ω , which set the input impedance to match the 50Ω from the SMA connectors on the development board. For visual reference, Fig. 2.6 shows the full transceiver board populated with the power connections in place.

2.2.1 Ultrasound Probe Board Design

In order to interface with the transceiver board, a breakout board was developed to incorporate the solid state switches and ultrasound connector together on one PCB. Fig. 2.7 shows the populated PCB. The largest advancement this connector PCB has to offer is that it drastically decreases the amount of time taken between transmitting and receiving, which directly decreases the amount of time each pulse cycle takes. The reason we were able to decrease the programming time was because of the multiplexer design.

This system employs the MAX14866 for multiplexing. The MAX14866 is a 16 element solid state switch chip that offers low R_{ON} (7Ω), excellent isolation (-75 dB), and great cross-talk performance (-62 dB). This chip also features t_{ON} and t_{OFF} times of $4 \mu s$, while using SPI programming to set each switch to the desired setting. The MAX14866 also features a bank programming option that allows us to program all 64 switches using one SPI channel, which reduces software complexity. The switch to the MAX14866 also

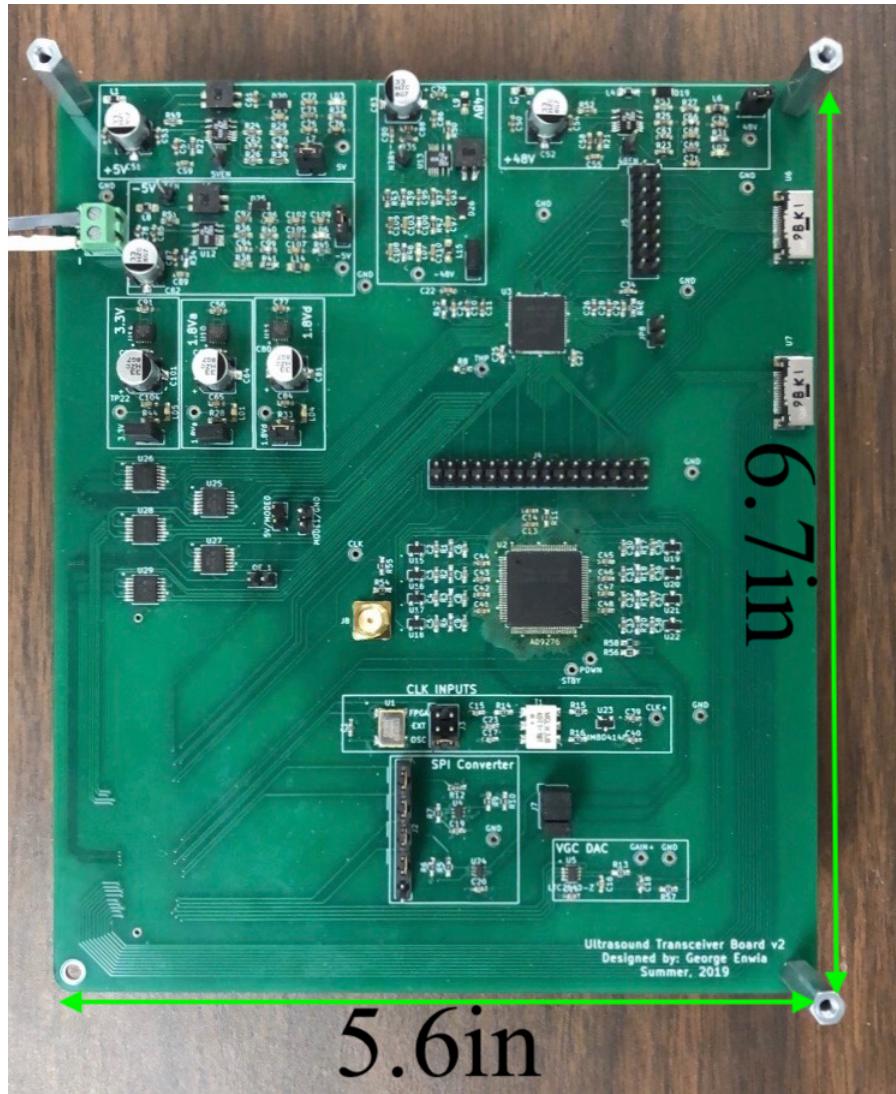


Figure 2.6. Fully populated custom transceiver board with HSMC underneath

decreases the footprint of this board significantly, as instead of having 82 reed relays, we have four $7 \times 7 \text{ mm}^2$ chips.

A layout issue that should be noted stems from fact that the output pins on the LX connectors and the input pins on the MAX14866 are so close together. The way this board was laid out, the system is unable to receive from adjacent channels. This is because when laying out, I was not able to tie each of the eight channels to either side of

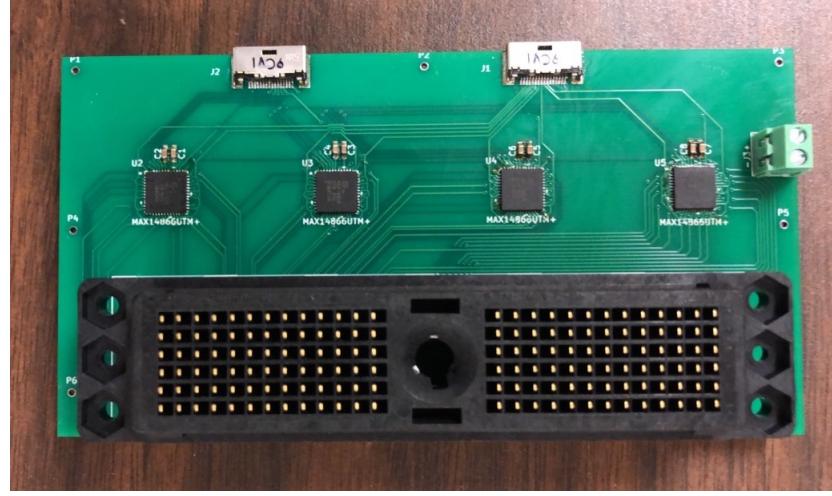


Figure 2.7. Breakout board with four solid state switches and Blatek probe connector

each MAX14866²⁸. If the board was laid out in that way, there would have been no feasible way to fit all the overlapping traces. The solution that was proposed to me after fabrication was to adjust the traces from the outputs of the MAX14866s to the ultrasound probe. By arranging which elements were tied to what output pins, the system could have been configured to receive from adjacent elements.

The system is designed with the idea that we could implement variable front end circuitry allowing for multiple applications from the same transceiver/SoC build. One such application involves a wearable array that employs on probe pre-amplifiers. The benefit of this design is that the signals coming from the transducers are immediately amplified, before any noise affects the incoming echoes. By pre-amplifying all incoming signals, we are thus able to increase our overall SNR. But to do this, we must use off board Tx/Rx switches, which is accounted for in the design. This implementation opens the door for a wide array of imaging modalities because of the improved SNR^{1,9}.

3 Imaging Methods

There are many different ways in which ultrasound imaging can be done. Most common is what's called B-Mode imaging. Our system previously used this mode of imaging. This system introduces the transition towards a plane wave imaging method in an attempt to gain some added features that will be discussed in the following section.

3.1 B-Mode Imaging

B-mode imaging functions by emitting a pulse and receiving echoes back from the medium. This is done by using piezoelectric elements to transmit pulses and receive echoes. The received echoes are more or less powerful depending on how reflective artifacts are. Fig. 3.1 shows the traversal of the ultrasound wave through the body and how echoes are generated.

The attractive part of B-mode imaging is that it is simple and versatile. There are many methods of beam-forming. Beam-forming allows focal depth to be changed, improvements in lateral resolution, and phased pulsing can give angled beams. One of the main problems with B-mode imaging is that there is increased beam spread, because only a fraction of the elements are active at a time. This causes worsened lateral resolution, which is important in trying to image smaller artifacts in the body. B-mode imaging

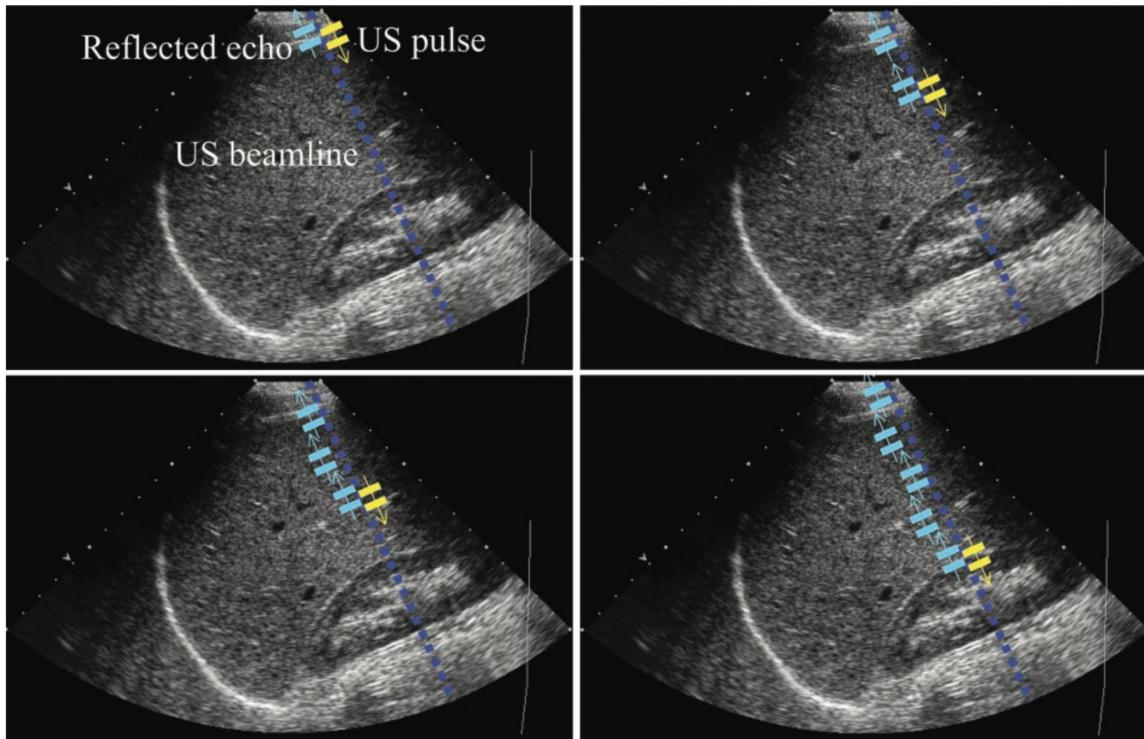


Figure 3.1. Step-wise illustration of B-Mode (Pulse-Echo) Imaging⁴

is also not the best method if an application requires any information about motion. For that, Doppler and plane wave imaging are employed.

3.2 Plane Wave Imaging

Plane wave imaging is a method that is derived from an imaging method often used in optical imaging. For ultrasound, the method translates very well. By exciting all of the elements on the transducer array, we are able to get a much more uniform beam and thus a much higher lateral resolution. This is evident in the FOCUS simulations displayed in Fig. 3.2, where we compare the beam spread and lateral resolution of the previous group's B-mode imaging method with our new plane wave imaging method. In our application, we generate the plane wave pulses in the FPGA. Similar work is done

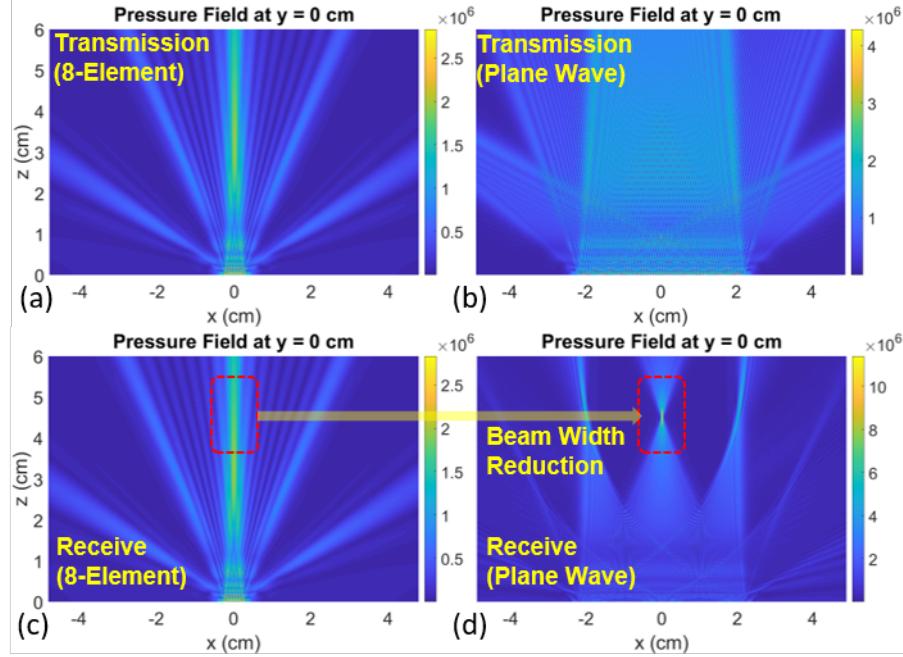


Figure 3.2. Focus Simulation of previous B-Mode imaging vs. Plane wave imaging. (a) Transmission 8-element (b) Transmission Plane Wave (c) Receive 8-element (d) Receive Plane Wave⁹.

in²⁹, where they create a low-cost system that allows them to run any imaging modality by implementing an “app” that takes the data and processes it. By doing this, they are able to collect raw echo data and perform all of their conditioning in software. Our current system is moving towards interfacing with a wearable transducer array that has on-board pre-amplifiers. For that application, it is beneficial to be solely software based because it allows us to do all of our post-processing and receiver beam-forming on the DE-10. By directly amplifying the incoming echoes, we minimize noise injection and by doing the receive beam-forming in software we decrease footprint, complexity, and power consumption because of the removal of unnecessary beam-forming hardware. This versatility allows the system to be used in a variety of applications, instead of being locked into one.

Not only do we get better lateral resolution in the system, but plane wave imaging also presents a possible way to save on the number of pulse cycles we need per image. With plane wave imaging, we acquire eight times for a full image. This is roughly three times less cycles than the previous group needed for their eight element scan with 25% overlap. The previous system was not able to do this because there were timing concerns, as the reed relays on their application took roughly $200\ \mu s$ to reprogram. Since we have the solid-state switches on board, we are able to quickly reprogram these multiplexer to allow for higher speed plane wave imaging, while saving on power consumption.

With plane wave imaging, Doppler imaging is also possible. This can be implemented by adding a phase delay to all the elements and acquiring at high speed. Even further benefits can be gained by compounding the results from multiple plane wave images acquired at various transmit angles θ . The compounding process averages out unwanted speckle in the image (caused by localized scattering within tissue), thus increasing the final contrast-to-noise ratio (CNR). Fig. 3.3 shows this method. Not only will this make for more pronounced features from objects of interest, but also remove incoherent sources such as speckle that will never be the same for different transmit angles.

This scheme was tested using the same FOCUS simulations as in Fig. 3.2, but this time we added a delay between elements to create an angled plane wave. This was done in order to see how the ultrasound beam would look in the medium. Fig. 3.4 shows the elements of the Blatek ultrasound probe created by the FOCUS simulations to show what the simulated transducer elements looked like. The parameters used to create the

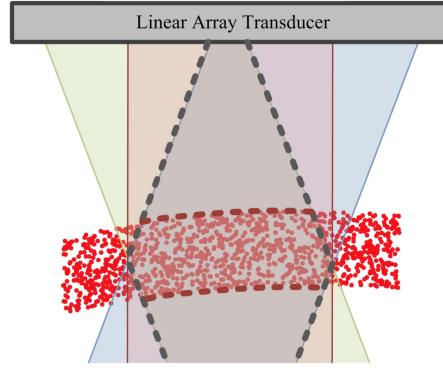


Figure 3.3. Phased plane wave imaging with a linear array¹⁰.

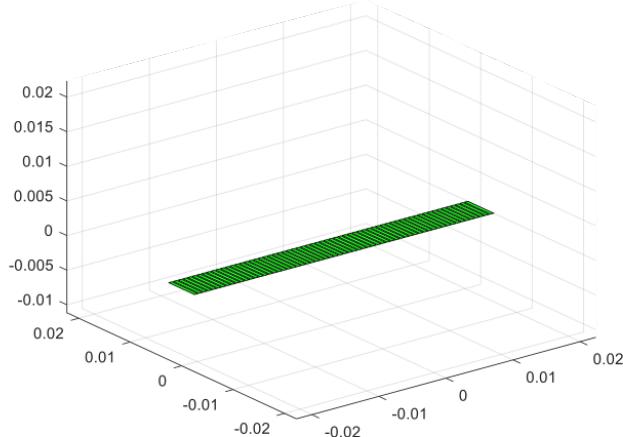


Figure 3.4. View of the Blatek linear array probe generated using FOCUS simulations.

array were taken from the Blatek probe's datasheet. Two sets of simulations are presented. The first outputs all 64 elements with a linear delay. This allows for a much wider range of angles that can be created. Unfortunately, with our system being limited to 8 channels, we can only transmit the linear delay across 8 channels at a time.

This problem can be partially overcome by repeating an 8-element linear delay profile across the array, thus allowing only 8 transmitters to cover the entire 64-element aperture. This method works since phase is a periodic function of time delay (modulo

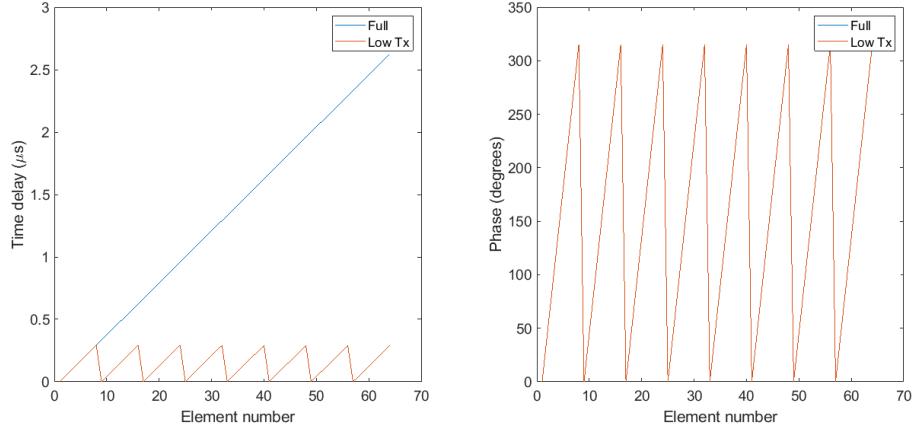


Figure 3.5. On the left are the time delays across the elements throughout the aperture for a full transmit array (Blatek 64-element linear probe, element pitch = 0.3 mm) and a “low-Tx” array where the delay profile is broken into eight repeated segments of eight elements. A particular transmit angle has been assumed. On the right are the phase delays in the two cases for a center frequency of 3 MHz.

2π); thus, applying a periodic time delay profile results in the same phase profile as the linear delay profile used by a conventional “full” system with 64 transmitters. Fig. 3.5 shows the delay in time for a full array and the “low-Tx” repeated array for a particular steering angle, as well as the phase delays in the two cases (as expected, they are perfectly matched). The conditions under which such matching can occur are discussed in the next paragraph.

Fig. 3.6 shows the simulations for the low-Tx arrays for various values of beam angle θ . These results were generated over a small set of angles, but it is clear that the results are very promising. These profiles almost exactly match those of the uniform-delay plane wave from the full array, but the trade-off is that we are limited in the range of angles we are able to generate. In fact, it can be shown that the low-Tx array can only

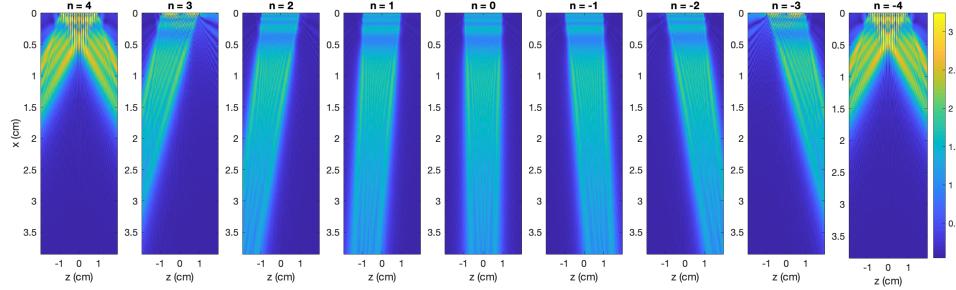


Figure 3.6. This figure shows the FOCUS simulation of the transmitted plane wave from the “low-Tx” transmitter as the beam angle θ is varied. The simulation assumes a 64-element linear array probe with $\Delta x = 0.3$ mm, $c = 1500$ m/s, and a frequency of 3 MHz.

generate distortion-free plane waves at angles that satisfy the following condition:

$$\sin(\theta) = \left(\frac{n}{N_W} \right) \frac{c}{f\Delta x}, \quad (3.1)$$

where $N_W = 8$ is the number of transmitters available, $n = \{-N_W, \dots, N_W\}$ is an integer, c is the speed of sound in the medium, and Δx is the element pitch (equal to the sum of transducer width and inter-element spacing or kerf). This result shows that a maximum of $2N_W - 1 = 17$ steering angles are available in our case. In practice the larger angles (corresponding to larger values of $|n|$) are not useful since they result in inter-element phase shifts larger than π , which generates spatial aliasing and unwanted “grating lobes” in the output pressure profile. One such grating lobe is visible for the $n = \pm 4$ cases in Fig. 3.6.

Once the FPGA code is developed, this system could support plane wave imaging that supports this angled plane wave generation strategy, which combined with compounding would vastly increase the capabilities of the system.

Plane wave transmission must be combined with receive-mode focusing to generate ultrasound images. Note that the received data can be acquired over multiple scans, making it possible to operate with a limited number of physical receive channels (8 in

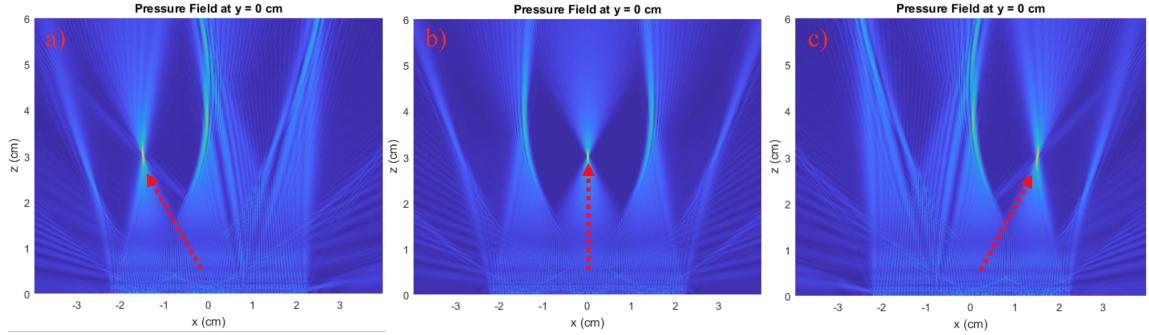


Figure 3.7. FOCUS simulations of the a) left, b) center, and c) right focused beam with angles of $+26.57^\circ$, 0° , and -26.57° respectively.

our case). Figs. 3.7 a)-c) show the results of using all 64 received channels for true-time delay beam focusing, with the focal point set at $z = 3$ cm and $x = +1.5$ cm, 0 cm, and -1.5 cm, respectively. For sub-figure a) the left-most element has zero time delay, with the delay increasing to the right; for sub-figure b) the delay is uniform across the aperture; and for sub-figure c) the right-most element has a delay of zero that increases to the left. A series of such focal points can be created during post-processing of the data to create an image of the zx plane.

4 System Software

In this chapter, we will discuss the changes made to the software from the previous group's work²¹. The same code was used with changes in both the Verilog and C programming. These changes were made to incorporate the HV pulser (MAX14808), the solid-state switches (MAX14866), controllable power supplies, and single HSMC connector interface. By adding finite state machines (FSM) for the MAX14808 and MAX14866, we were able to easily implement these two additions into the system. The HSMC connector was implemented by reassigning pins to interface with the custom transceiver board.

4.1 HSMC Implementation

Incorporating the HSMC as the one and only contact from the SoC to the rest of the front-end circuitry allowed for a small managerial change³⁰. Pins were reassigned to allow the SoC access to all the front end circuitry. The power supplies, pulser, logic translators, solid-state switches, and ADC chips feature settings that require simple high/low logic to implement special operations. For example, some of these settings are standby mode, current control, mode select, variable gain input, and output enable. These are all set in the C programming, and thus are user controlled. By routing everything through

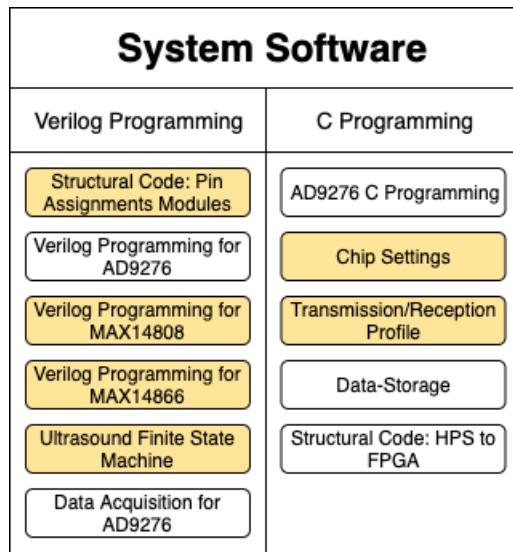


Figure 4.1. The different software blocks, split into Verilog or C Programming. Yellow modules were added or updated, white modules were not touched.

the HSMC, the system cuts down on many connectors and removes a significant amount of complication. Not only does it make the system less complex, but it also removes potential noise sources, as this change removes long cables running from board to board. Fig. 4.1 depicts the software modules in the system and which were added, updated, or left as is.

4.2 Programmable Pulse Profile

Previously, the HV pulses were generated by using the beam-forming chip set. In this application, the HV pulses are generated through the SoC directly. The MAX14808 allows for this by taking FPGA outputs and converting them directly into HV pulses of a desired voltage range. This was achieved by adding a state machine for the pulse pattern generation that outputs a user-controlled number of pulses at a user-controlled frequency.

The pulse frequency is generated off of an generic PLL block in System Builder, but the output frequency is tied to a register in the C programming.

Fig. 4.2 shows the FSM for the pulse generation code. The state machine for the HV pulse generation starts in State 0 where it initializes all the inputs, parameters, and outputs. It then waits for a START signal from the SoC. When this signal is asserted, an initial delay counter begins. This counter is to ensure that the pulser is ready to receive a transmission profile. The next state is when transmission occurs. TX_EN is asserted and outputs a user-defined number of pulses. These outputs are generated from an Altera PLL module, that also has a user-defined frequency, and directed to the input pins of four SN74LV4T125 that are then translated and sent to the pulser. The final state then is for "Damping Mode". This state counts a user-defined number of CLK cycles and allows the MAX14808 to transition the TX/RX switches from Transmit mode to Receive mode in order to decrease leakage. Once the damping stage is over, the outputs return to zero and the state machine returns to its first stage and awaits the next START signal. To fully implement the pulse generation FSM and make it fully user-controller, we added all the parameters to be defined in the C program.

4.3 MAX14866 SPI Programming

This system uses solid-state switches (MAX14866) in order to multiplex the 8 channels with the 64 probe elements. These switches are much faster than the reed relays used in the previous system and cuts down on time needed to reprogram between images. The MAX14866 has 16 channels per IC and allows for bank programming. This feature is attractive because it allows for the use of one SPI channel instead of four. When chained together, the ICs function like a shift register, allowing for one 64 bit chunk to program

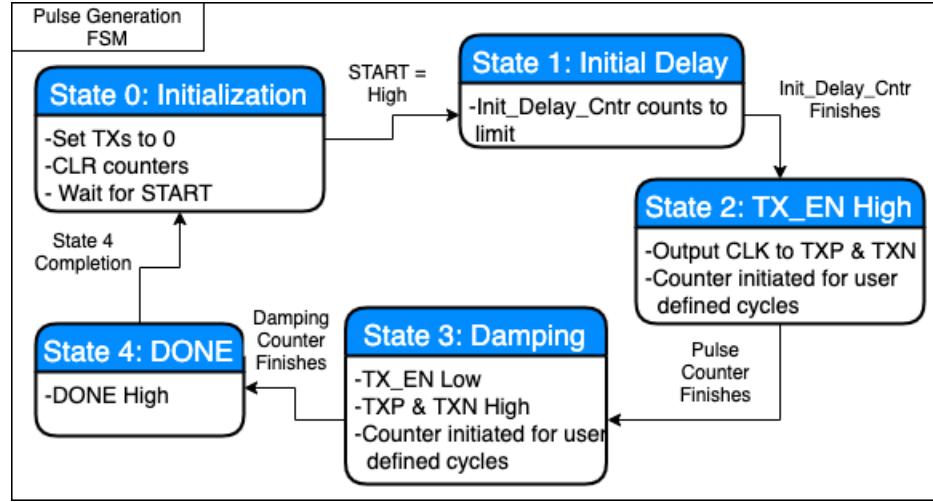


Figure 4.2. Pulse profile generation FSM.

all 64 switches. For our application, this is done twice. Once before the transmission of the pulse and once after. This is to select what channels are outputting pulses and what eight channels are reading back echo data.

These solid-state switches are also attractive because they allow for different imaging methods to be used. For example, Fig. 4.3 shows 32 elements in the array after turning all switches on for transmit and then receiving from eight of them. This imaging method is called plane wave imaging, as described in the previous chapter. During later processing, these chunks would be stitched together to form a whole image.

In order to attempt to recreate the results from the previous group and display the functionality of the miniaturized system, a pattern similar to that of the previous group was used. Eight channels were transmitted from at a time, but for this system, only one was received from per pulse. The only discrepancy between the previous system's imaging method and ours is, because of the layout of the ultrasound probe board, this system could only collect data from one channel at a time. An oversight in layout impeded us from being able to collect data from eight adjacent channels. This oversight

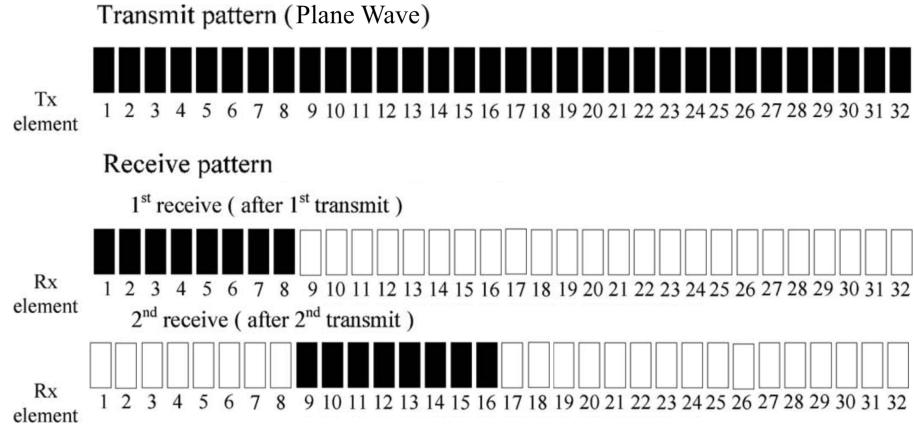


Figure 4.3. An example transmission pattern for plane wave imaging.

caused imaging to take eight times longer, as each of the 64 elements had to be received individually.

4.4 Ultrasound FSM updates

Changes to the hardware of the system caused some incompatibility in the code. To fix this, we had to reincorporate the pulser and multiplexer programming modules into the system FSM in place of the beam-forming code that the previous system used. This section discusses these changes and how the new FSM works. Fig. 4.4 is a block diagram of the updated FSM. Starting at State 0, we will walk through the states and note what each state does and what changes were made, if anything.

4.4.1 State 0

This state is used to initialize the system. It sets everything high/low depending on necessary initial conditions. When the START signal is asserted, the system moves to State 1. Changes to this state include updated controls for MAX14808 and MUX.

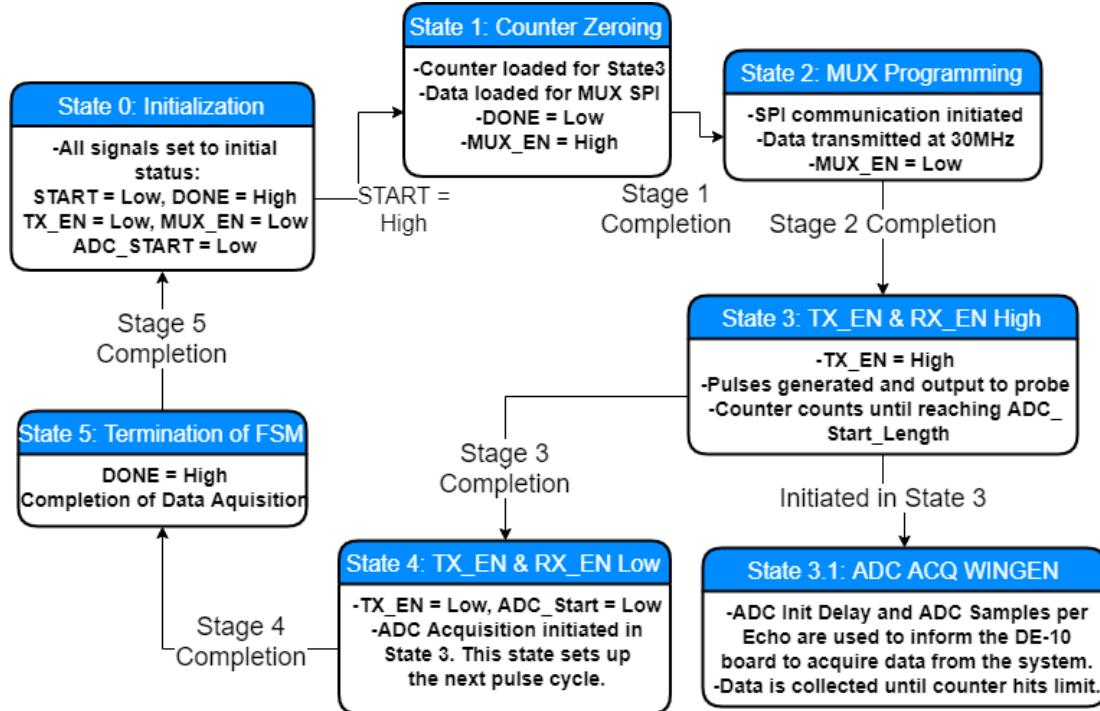


Figure 4.4. FSM for Ultrasound system code.

4.4.2 State 1

This state zeroes all counters and loads the MUX programming profile. This state also changes the DONE signal to LOW. When MUX EN is asserted, the system transitions to State 2. The only changes made here regard adding the MUX load step and changing the transition condition to MUX EN.

4.4.3 State 2

This state is the added MUX programming module. The MUX must be configured before the transmit and receive modes, so this step was added here. One MUX programming is complete, MUX EN is switched LOW and the system transitions to State 3.

4.4.4 State 3

This state is the pulse transmission state. This module produces the pulse profile and transmits it to the transceiver and outputs the pulses to the medium. At this point as well, the acquisition window generator (ADC ACQ WINGEN) is initialized. This module was switched in for the previous beam-forming module. When the pulses are done transmitting, the system transitions to State 4.

4.4.5 State 4

This state is responsible for turning the ADC acquisition window off and sets the system to be ready for the next pulse cycle. No changes were made in this state. When this is complete, the system transitions to State 5.

4.4.6 State 5

State 5 is just to separate the DONE signal transition from State 4. Once this state is reached, DONE is switched HIGH and the system transitions back to State 0 and is ready to be initiated again.

5 Experimental Setup and Results

5.1 Overview

In this section we will discuss the testing and verification for each stage in the system. This will consist of power distribution, logic translators, HV pulser, ADC, multiplexer, and lastly discuss the functionality of the system as a whole.

5.2 Power Supply Verification and Characterization

In total, this application uses the seven power supplies mentioned earlier: 1.8 V_d , 1.8 V_a , 3.3 V , 5 V , -5 V , 48 V , and -48 V . In order to characterize the power supplies individually, I went through all the data sheets to get an idea of the maximum load of each power supply. Table 5.1 shows the results of this investigation. Figs. 5.1 and 5.2 show the schematics for these power supplies in LTSPICE.

Table 5.1. Maximum current requirements for each power supply.

Power Supply	1.8 V_d	1.8 V_a	3.3 V	5 V	-5 V	48 V	-48 V
Tested Current Rating	1 A	1 A	1 A	2.1 A	1 mA	300 mA	300 mA
Typical Current Draw	80 mA	400 mA	120 mA	600 mA	67 mA	186 mA	157 mA

The next step was to verify that these power supplies could supply the maximum load without failing. The seven power supplies were all tested using a digital multi-meter (DMM) and electronic load.

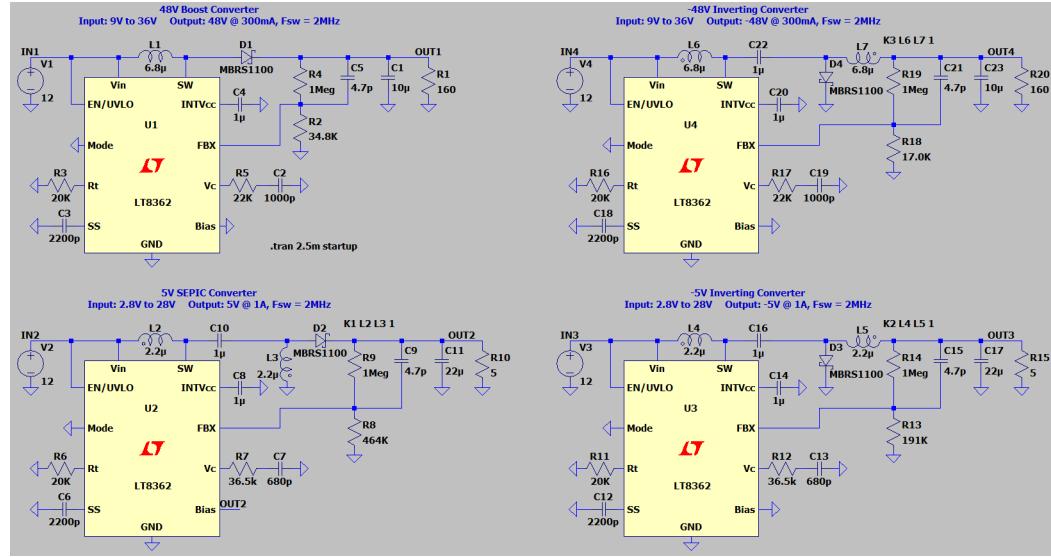


Figure 5.1. Schematics of all four switching power supplies in LTSPICE.

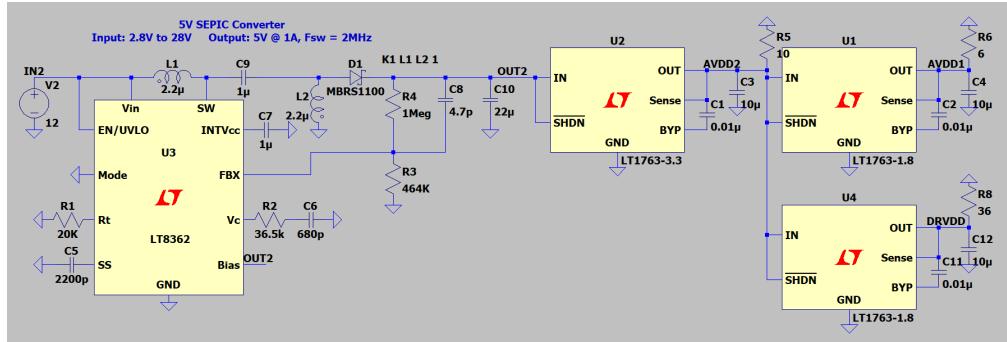


Figure 5.2. Schematics of the three LDO regulators fed off of the 5 V supply in LTSPICE.

We'll start with the 1.8 V_a , 1.8 V_d , and 3.3 V , because these regulators are generated off of the 5 V supply. The system requires that the 1.8 V_a , 1.8 V_d , and 3.3 V regulators must be able to supply 1 A each²⁷. Because these three are generated off of the 5 V supply, they were confirmed to work individually at 1 A, but not all three at the same time. Fig. 5.3 shows simulation results of the three LDO voltage regulators.

The 5 V power supply powers the 1.8 V_a , 1.8 V_d , 3.3 V regulators, and the HV pulser. At worst-case, it must be capable of driving a maximum of 3.1 A. The data sheet shows that

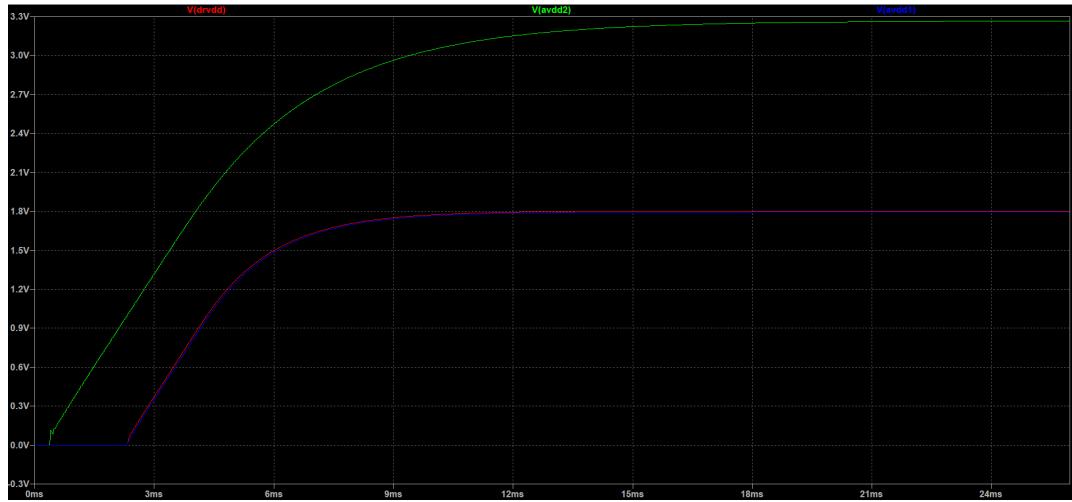


Figure 5.3. Transient simulation results of the LDOs in LTSPICE.



Figure 5.4. Transient simulation results of the +/-5 V switching power supplies in LTSPICE.

the 5 V supply is rated at a typical maximum of 2.5 A and an absolute maximum (with over-current mode enabled) of 3.1 A. To avoid damaging the IC, the 5 V power supply was confirmed to function under 2.5 A load, but was not verified to function under a 3.1 A load.

The last three supplies are the -5 V, 48 V, and -48 V. The -5 V power supply has a maximum load of 67 mA, which it is more than capable of. The 48 V supply must support

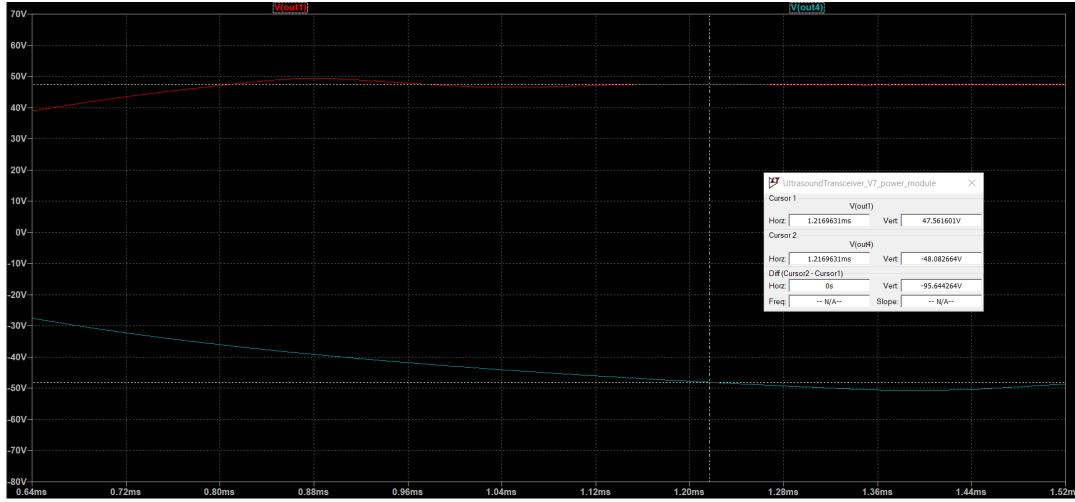


Figure 5.5. Transient simulation results of the +/-48 V switching power supplies in LTSPICE.

a maximum of 186 mA during 2 A operation of the HV pulser. When testing this, I used 200 mA as a load. The output of this power supply does droop as the load time increases, but in short pulses, the power supply is more than capable of supplying enough current. The -48 V power supply works quite similarly, as it must be capable of driving a 157 mA load. This supply is more than capable of supporting this load at short load times, but again as load time increases the output falls to around -24 V. Fig. 5.6 shows the back end of the system with all seven supplies being powered by a 12V battery pack. The 1.8 V supplies can not drive a green LED, so they do not have the optical feedback. Fig. 5.4 shows the simulation results for the +/-5 V supplies, while Fig. 5.5 shows the transient simulation results of the +/-48 V supplies.

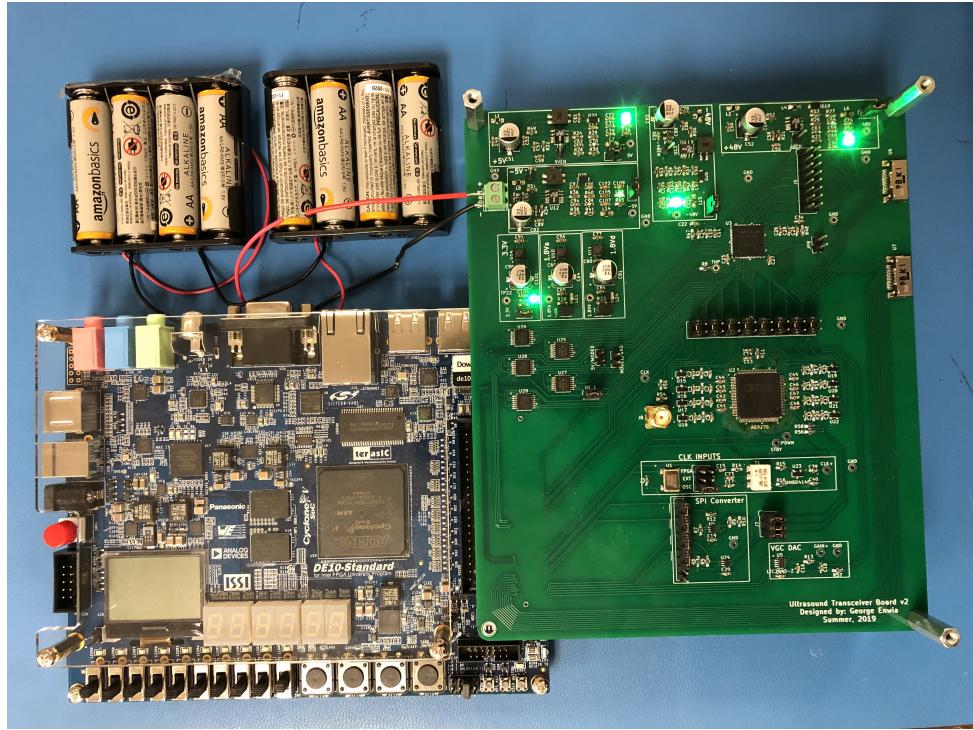


Figure 5.6. Back end of the system without the ultrasound probe board, being powered off of a 12 V battery pack.

5.3 MAX14808 Verification

Since the discussion of functionality has already been covered in an earlier section, we will skip straight to the discussion of the testing done to verify the MAX14808's functionality. The most simple way to test the pulser was to have the FPGA generate the 5 MHz DINP and DINT signals shown in Fig. 2.4. To fully power the HV pulser during this testing, we also had the SoC enable the 5 V, -5 V, 48 V, and -48 V. We also added the jumper to activate the 3.3 V regulator, so when the 5 V output is on, so is the 3.3 V. Fig. 5.7 shows the 2.5 V signals output by the FPGA and translated to 5 V signals by the SN74LV4T125. This translation shows some oscillation at the beginning of the pulses. This is believed

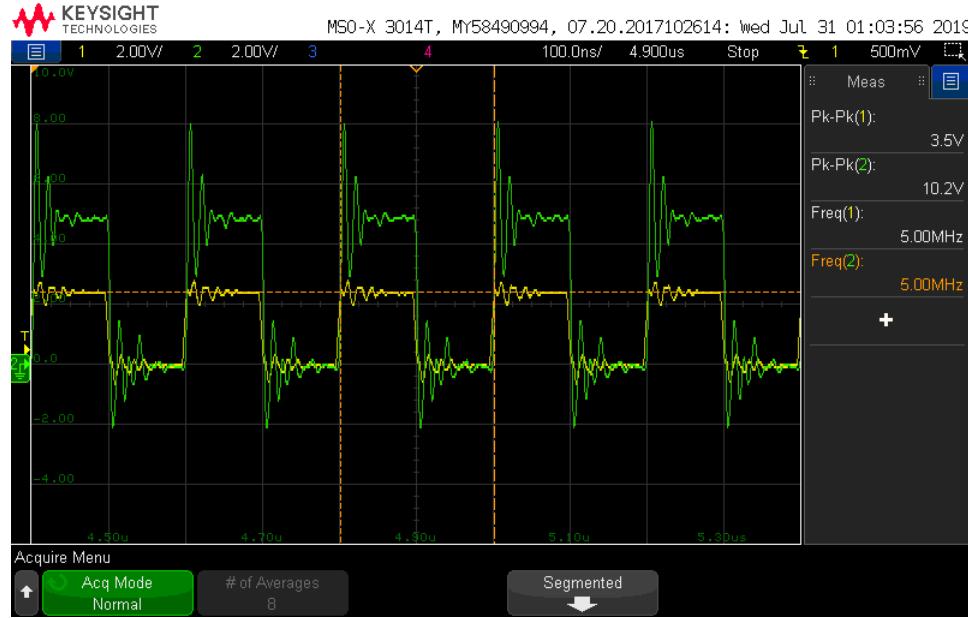


Figure 5.7. Output pulses from the FPGA being translated from 2.5 V to 5 V by the SN74LV4T125. The harmonics here are due to this not being driven by a single pulse but a continuous pulse train, this has since been fixed in the code.

to be due to the output signals being continuous and not single pulses, and insufficient bypass capacitance during initial testing (the issue has since been fixed).

The next stage in the pulse testing is ensuring that the inputs to the MAX14808 are translated into pulses of the correct amplitude and frequency. Fig. 5.8 shows both DINP (yellow) and DINN (green) at the input pins of the MAX14808. Fig. 5.9 and Fig. 5.10 show the positive and negative enable pulses and the output pulses. These pulses were generated using the ± 48 V power supplies, and as we can see in the scope traces, the output V_{PP} is 100 V, which lines up exactly with what we would expect from these pulses. We can also see that both input and output signals remain at 5 MHz, ensuring there is no frequency change from the output of the FPGA to the ultrasound probe board.

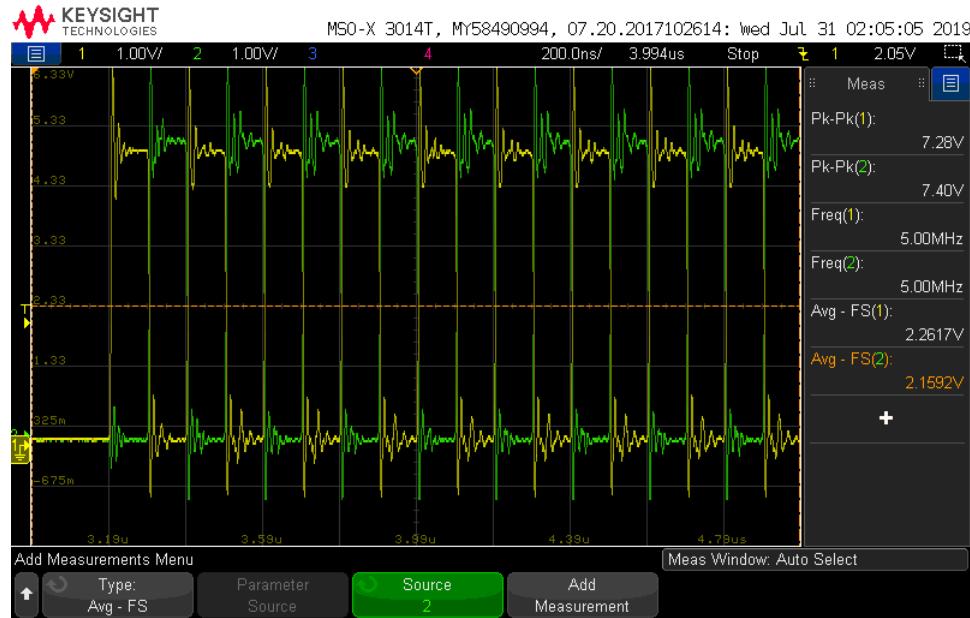


Figure 5.8. Positive and Negative inputs to MAX14808 showing alternating pulses to create high voltage pulses.

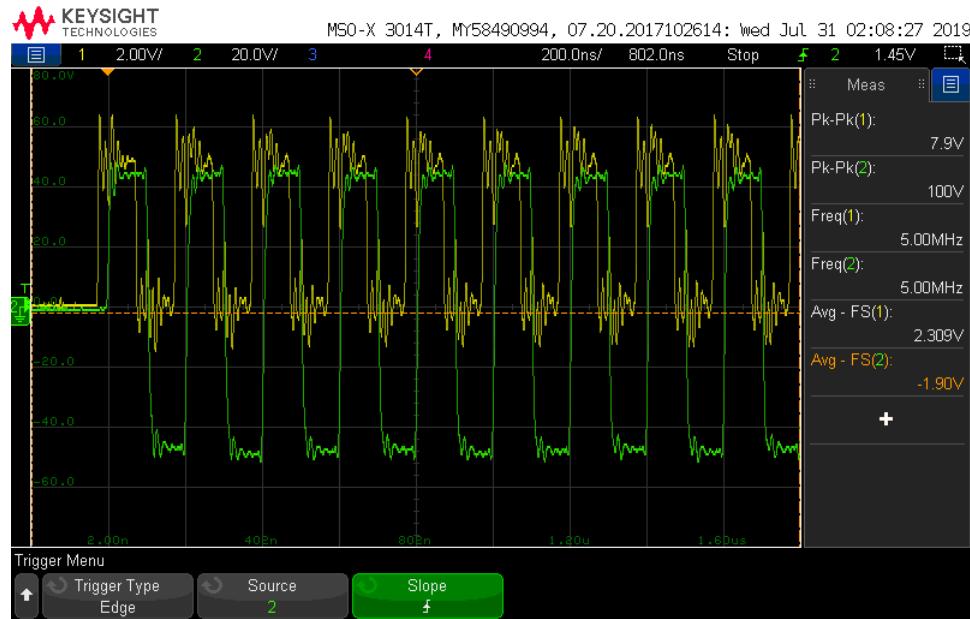


Figure 5.9. DINP and HV out with +/-10 V as high voltage.

The newest update to the testing of the MAX1808 incorporates single pulse mode, which allows a single configurable pulse to be sent from the FPGA. The parameters include frequency, number of pulses, and damping time. For the test shown in Fig. 5.11

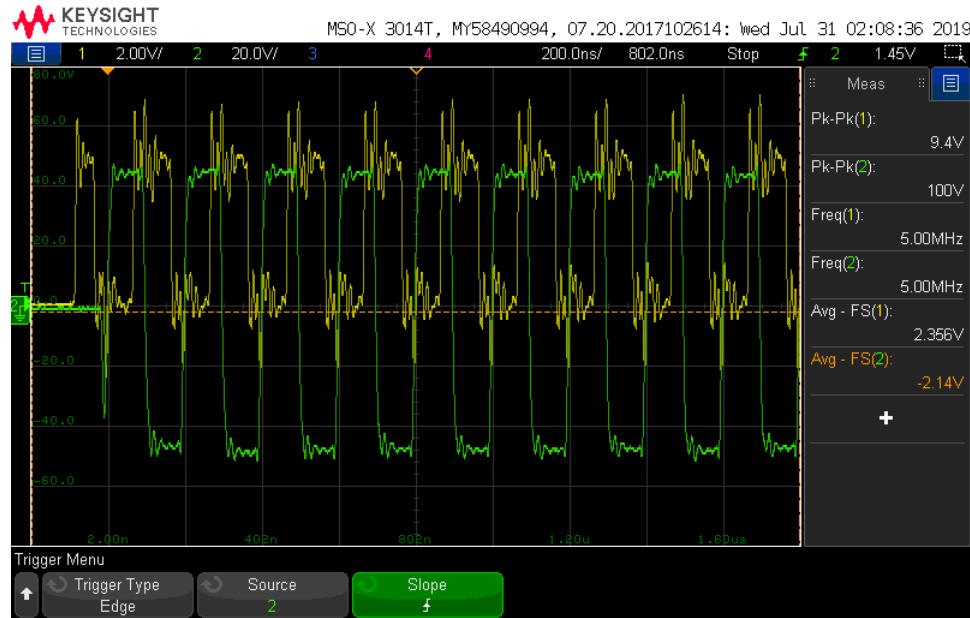


Figure 5.10. DInN and HV out with +/-10 V as high voltage.

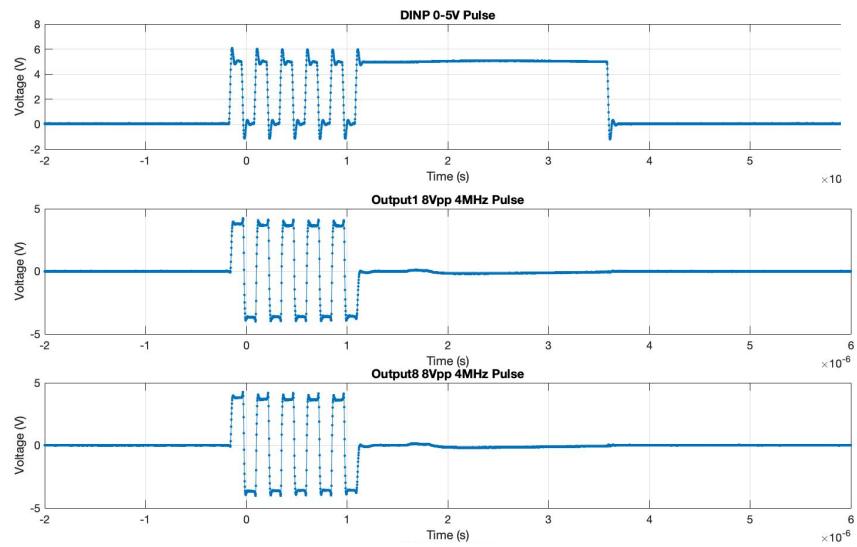


Figure 5.11. Fixed DINP vs. outputs 1 and 8 to show consistency across outputs.

uses 4 MHz, 5 pulse cycles, and 10 cycles for damping. The pulse voltage that is supplied is +/-4 V. All 16 inputs and 8 outputs were checked to ensure all were identical, and for the sake of conciseness, we only show one input and two outputs.

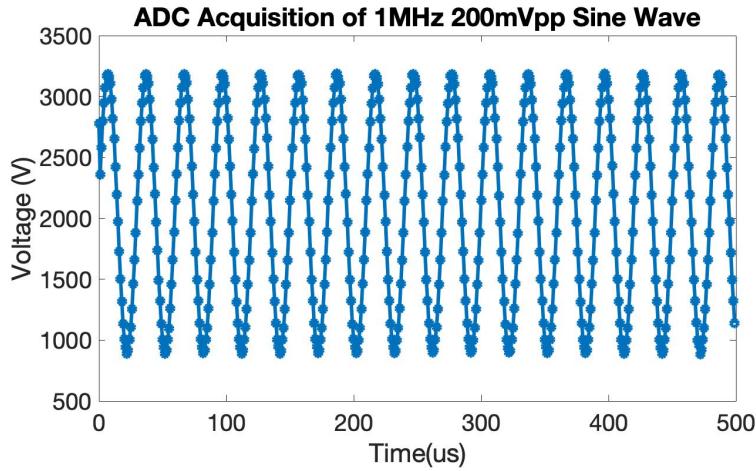


Figure 5.12. ADC acquisition of a generated sine wave.

5.4 AD9276 Verification

As mentioned earlier, there were no changes made to the AD9276 acquisition code. Previously, the ADC was on a development board, so this section is to verify the hardware implementation of the AD9276 on the custom transceiver board. To verify the functionality of the AD9276, we had to verify that we could: communicate with the IC through SPI, output the pre-programmed patterns, and enable analog to digital conversion of a known input and receive the output. Fig. 5.12 shows the successful acquisition of a 1 MHz 200 mV_{PP} sine wave from a signal generator.

5.5 MAX14866 Verification

The MAX14866 ICs are new to the system, so to verify functionality, we had to implement SPI communications. Once this was achieved, we programmed a known pattern and tested the switches ohmically to ensure that the correct switches were open/closed. The next step to verify the MAX14866 was to actually output pulses to the switches and see if we could record the HV pulses from the pulser at the output of the switches. These

tests were successfully completed, although the first time they were conducted, some of the connections in the cables had to be soldered again properly, as they were poorly connected and gave inconsistent results. Once this issue was fixed, the system had no problems interfacing with these switches.

5.6 Battery Life Discussion

In terms of battery life, the discussion has to be discussed a bit more in depth. The system draws about 2.1 W during active mode but only 336 mW during passive mode. At 12 V, this means active mode current consumption reaches about 175 mA and passive mode current consumption is roughly 28 mA. To average this out, pulse and acquisition takes no longer than 10 μ s per pulse, so a maximum of 80 μ s per image. Passive mode is active while not imaging, so active mode will likely be roughly 0.1% of the time that the system is on (assuming a frame rate of 12.5 FPS). When weighing this in, we see that the average current consumption comes out to $I_{AVG} = 175 \text{ mA} \times 0.001 + 30 \text{ mA} \times 0.999 = 30.2 \text{ mA}$, i.e., is dominated by the passive mode. From here we can calculate how long the a few battery packs would last in powering the system. Table 5.2 shows the calculations for battery life and displays the difference between the AA's we use currently and the benefits of converting to Li-ion.

Table 5.2. Battery Comparison

Battery Type	Equation	Battery Life
8x AA	1600 mAh/30.2 mA	53.1 hours
4x Li-ion	3000 mAh/30.2 mA	99.5 hours

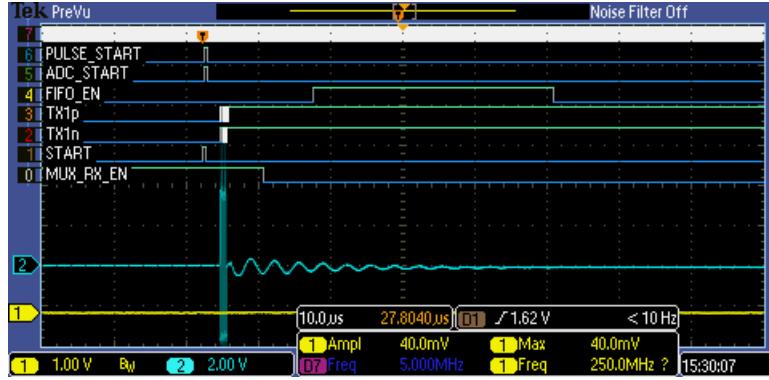


Figure 5.13. Full transmit and receive cycle with control logic and output pulse.

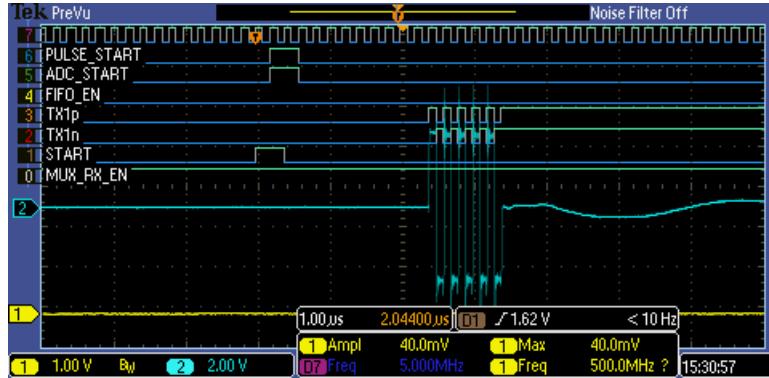


Figure 5.14. Pulse zoomed in to show configurable pulse length and accurate number of pulses produced.

5.7 Comprehensive System Verification

System verification testing started with ensuring that the code was correct and interfacing correctly with the transceiver and multiplexer boards before connecting the probe. Fig. 5.13 shows the system going through a transmit and receive cycle. At this point, the probe was not connected, so there was no data to acquire. Because of this, the ADC acquired data is not useful to display here. Fig. 5.14 shows the output pulses generated from the pulser to show that the FPGA is correctly outputting all control signals and the pulses are generated according to the user inputs.

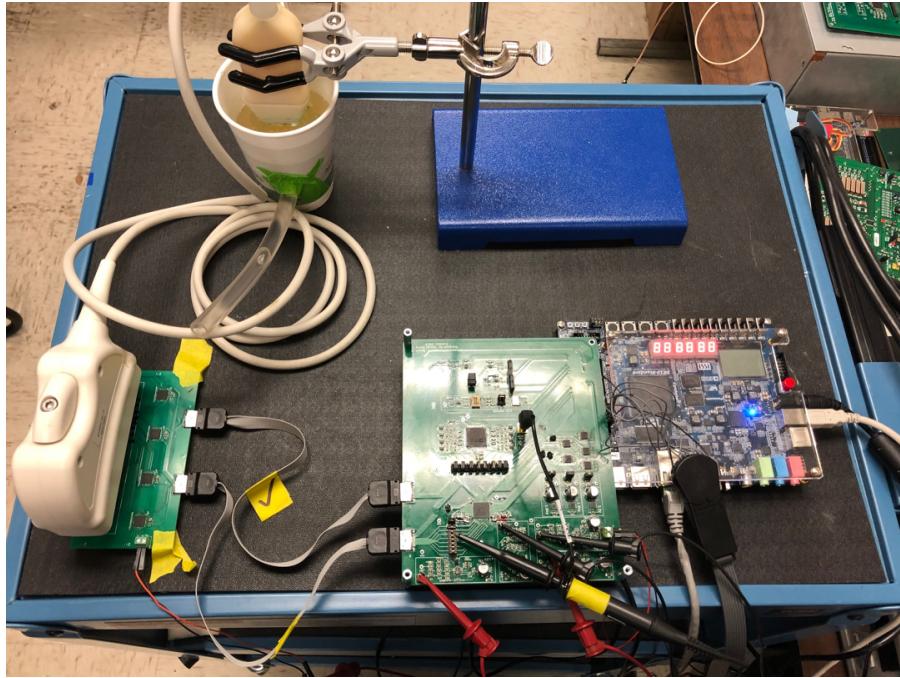


Figure 5.15. Final system test-setup for acquiring echoes.

The next step in verification testing for the system was actually plugging in the probe and trying to capture an echo. Fig. 5.15 shows the echo capture test step. For this testing we used the Blatek probe discussed earlier and a gelatin phantom with a tube running through it. This tube was filled with water in an attempt to replicate imaging an artery in the human body. The results of this testing are shown below in Figs. 5.16 & 5.17. For Fig. 5.16, we received from eight channels with the probe in air and the probe on the phantom in order to subtract out the low-frequency ringing seen in the first two graphs. We discovered that this low frequency noise can be removed by enabling the high-pass filter (HPF) in the AD9276 IC. Fig. 5.16 shows the subtracted data and a clear echo near the bottom right. Fig. 5.17, on the other hand, shows the data from a single element in air, on the phantom, and subtracted to see the received echo individually. Fig. 5.18 shows the high-pass filtered echo data from channel 60 of the transducer.

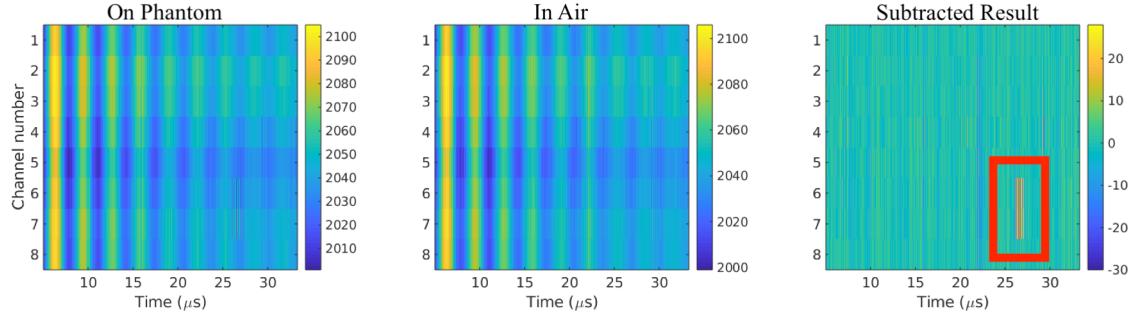


Figure 5.16. 8 element received signal on phantom subtracted from received signal in air to subtract ring-down of probe to reveal returned echoes.

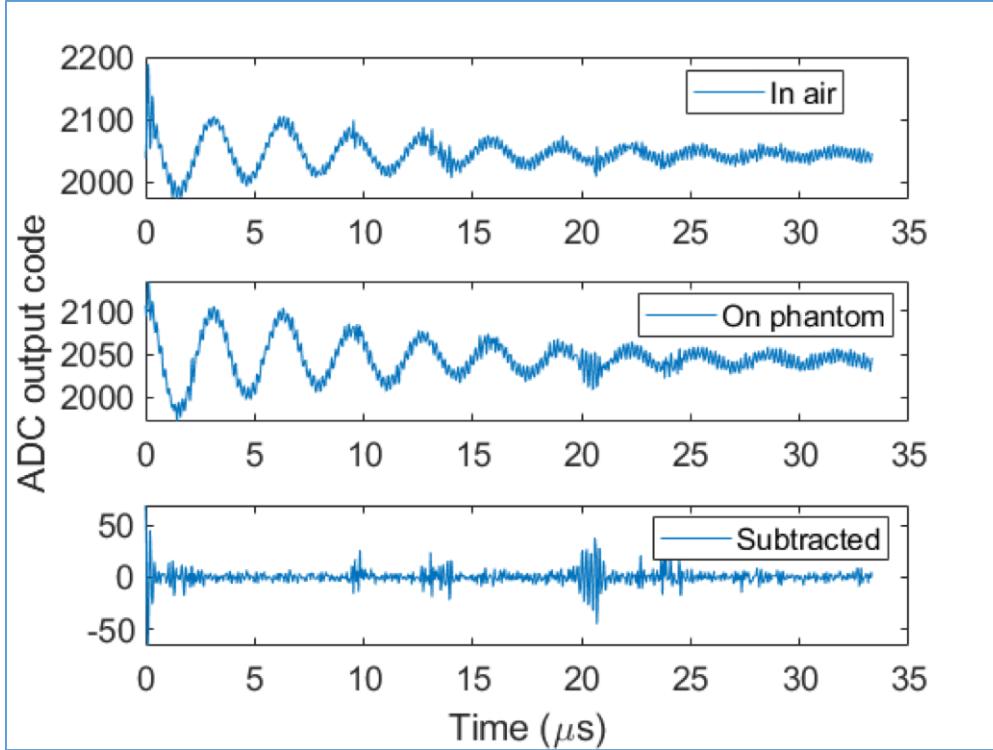


Figure 5.17. Acquisition from a single element on Transducer to ensure echo could be seen.

We were able to generate images in MATLAB using the data collected in the system testing. Fig. 5.19 shows the collected data using approximation with phase shift compensation and fixed focal point. Fig. 5.20 shows the same data ran through a delay and

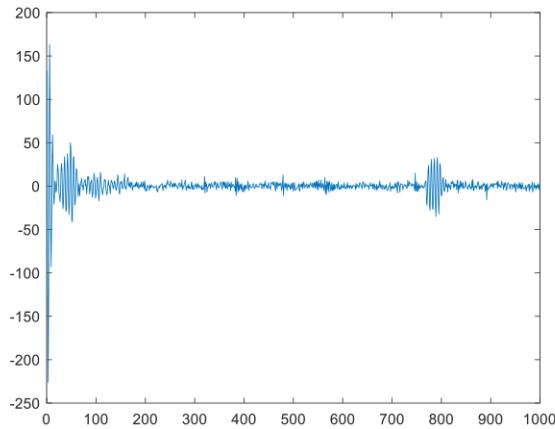


Figure 5.18. A zoom in of a single receive channel to show the receive echo after the HPF.

Pixels 700 to 900

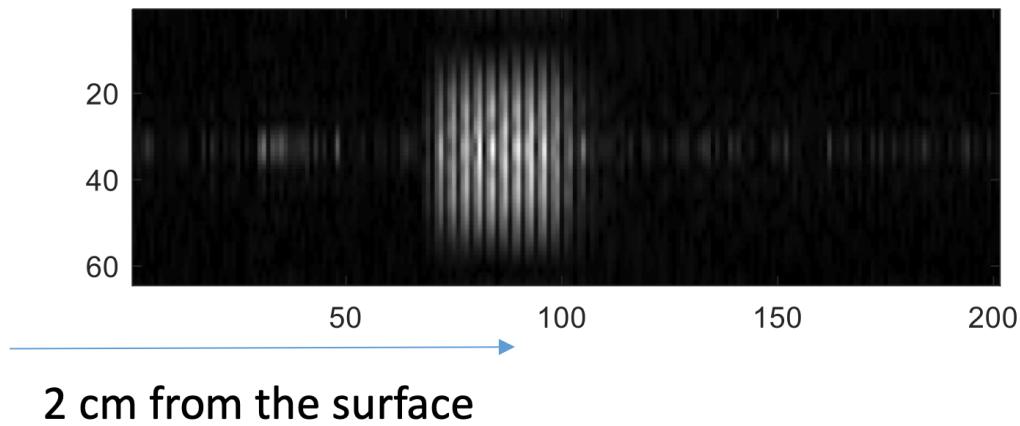


Figure 5.19. Raw data from pixels 700-900 displayed, showing the echo 2 cm from the surface of the phantom.

sum algorithm. Fig. 5.21 shows the data when a 64-point spatial FFT was used instead. These show promising results. The target of these ultrasound tests was a tube about 2 cm below the surface of the phantom, so the results in the images make sense.

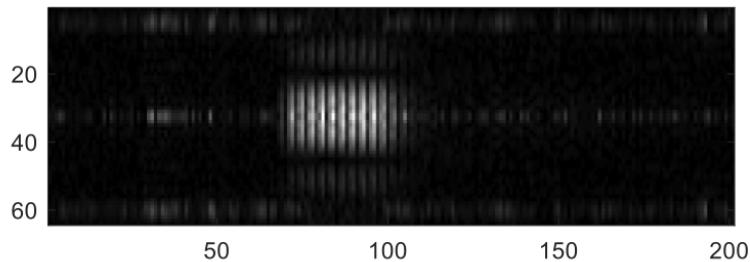


Figure 5.20. Received data for pixels 700-900 ran through a delay and sum algorithm.

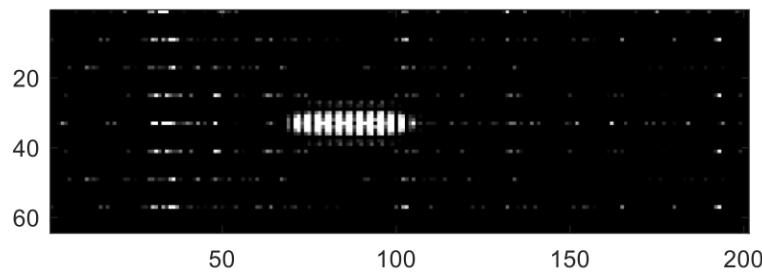


Figure 5.21. 64-point spatial FFT on data for pixels 700-900.

6 Conclusion

In this thesis, we have discussed the design and verification of a configurable low-cost 64 channel ultrasound system. The system is widely versatile, as it is designed to work with configurable back-end software and interchangeable front-end hardware. The total cost of the system, including PCB fabrication, DE-10 board, and all necessary components except the ultrasound probe, comes out to \$871.59. At this price, the system is very affordable for educational, hobbyist, and point-of-care (POC) applications.

Careful simulation, PCB design, Verilog programming, and C programming were necessary to test the individual parts of the system to ensure functionality. Further implementation of the system as a whole was tested and we received promising results. The results show that the system is able to transmit ultrasound pulses and receive ultrasound echo data that can be processed off-board. This system was not verified to function with on-board image processing, but has the capabilities to do so if the software is developed. Aside from the lack of on-board image processing, the system has promise in aiding the development of wearable applications, which are discussed in our related publications^{1,9}.

7 Suggested Future Research

The improvements suggested here are gauged towards making steady progression towards the final goal of an autonomous and portable system.

PCB Layout Improvements:

- A small change that will help with quality of life for testing and working with the transceiver board is changing the 12 V battery input to a regular 2.1 mm power plug. And put the batteries in one battery pack. This will alleviate some of the awkwardness of fumbling with extra wires.
- Another smaller layout fix that would help is reworking the wiring of the ultrasound probe board. This is not entirely necessary, but in order to have better control over adjacent elements, reworking the pin-out to the probe would fix this.
- Add bypass capacitors to HV pulser inputs (100 nF/1 μ F).
- Add current-limiting resistors to pins with direct connection to the FGPA (THP, SYNC, CLK, CLKB).
- R10 should be connected to 1.8 V, currently 3.3 V.
- All low-frequency control signals should be low-pass filtered with capacitors.
- Add test pins for all control pins.

- Remove cascaded voltage sources for generating 3.3 V and 1.8 V from 5 V, and instead draw them individually from 12 V.
- Add high-pass filter to duplexer.
- Add user-friendly test points on Blatek Probe PCB.
- Rewire probe to allow adjacent-channel acquisition if required.

Hardware Improvements:

- Moving away from the DE-10 Standard board would be the next big step in size reduction. Next, implementing something like the MitySOM-5CSx, which is a System-on-Module (SoM) that contains the same Cyclone V SoC that is on the DE-10, but without all the peripherals that the DE-10 has.
 - The MitySOM-5CSx has room for up to 2GB of DDR3 RAM, which would also ensure the goal of local image generation is possible.
- The transceiver can be redesigned to optimize for space. Moving the power supplies to the back of the board would almost cut board size in half. This would also require assembly at the fabrication stage, because hand-soldering would be unfeasible with both sides of the board containing ICs with ground pads.
- Once these miniaturization steps have been accomplished, designing a case for the system would be beneficial. This would increase portability, make the design look more attractive, and also protect the board from physical touch and any electrostatic discharge (ESD) issues.

Software Improvements:

- Using different programming patterns for the solid-state switches would allow for new imaging modalities and open the door to Doppler imaging. This could add an edge to the application that has not been attempted yet.

- On-board image processing is possible and can be applied to this system, but the processing rate will be slow.
- Improving efficiency of the image processing software to improve overall processing time and move towards faster scan times and real-time image generation.
- Adding “Start/Stop” and “Power Save” controls on the GUI in the app would be convenient, instead of having to reprogram registers in the C code.

Appendix A

PCB Schematics and Gerbers

Included in this section are the PCB schematics for the two PCBs designed for the project.

All hardware and software files for this project can be found at
<https://github.com/generalg1969/OpenSourceUltrasound2019>.

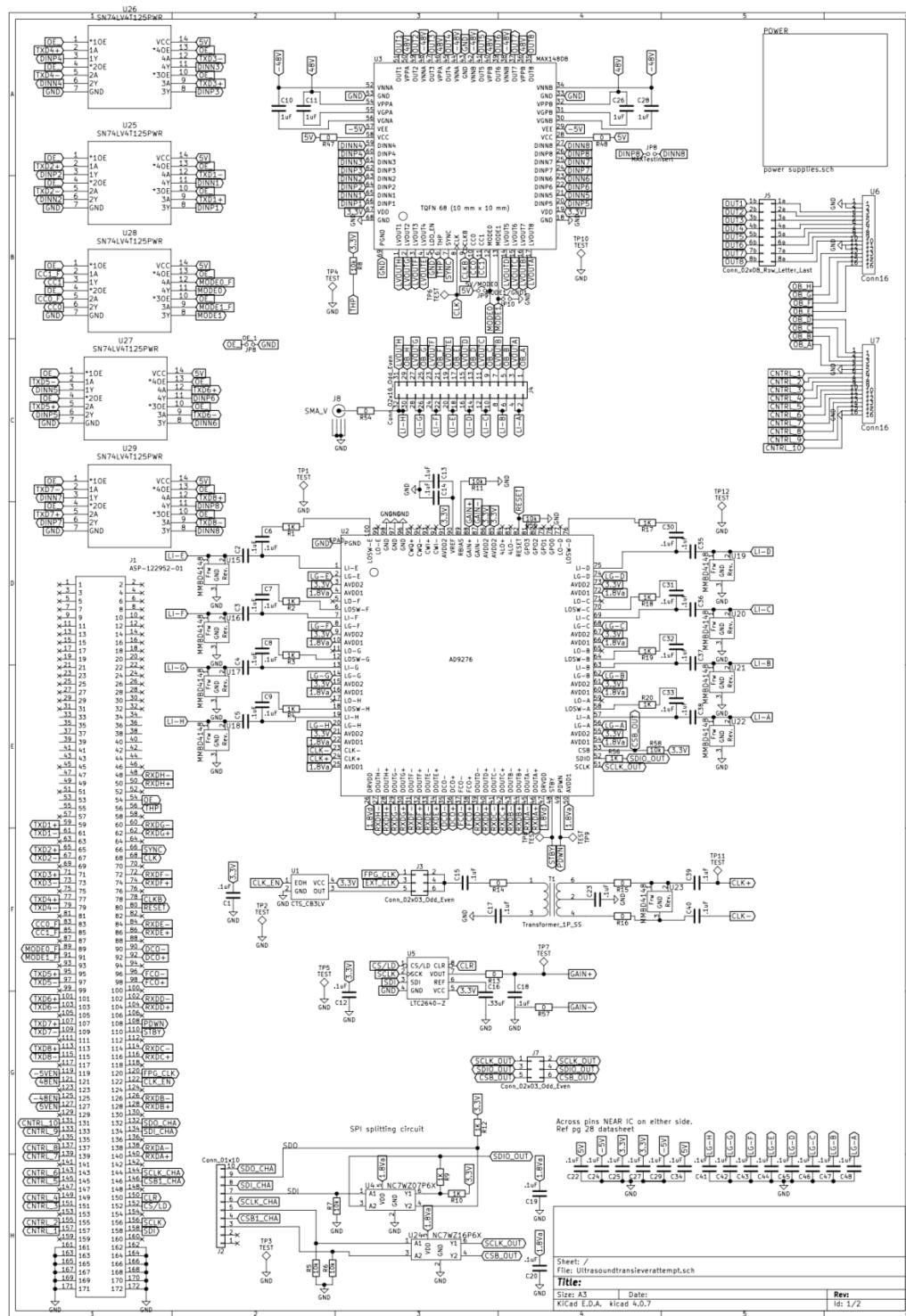
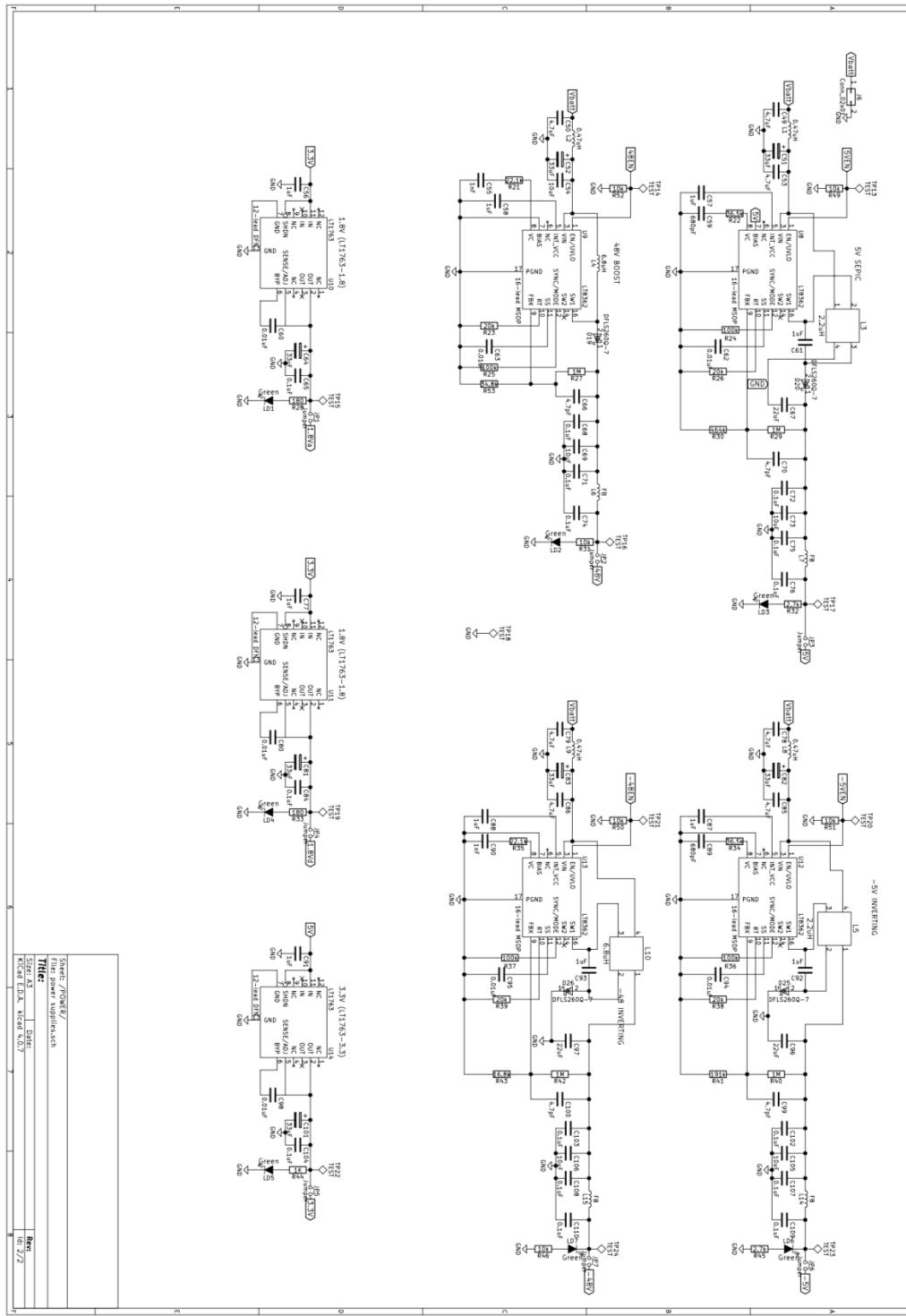


Figure A.1. Custom Transceiver Board Schematic.



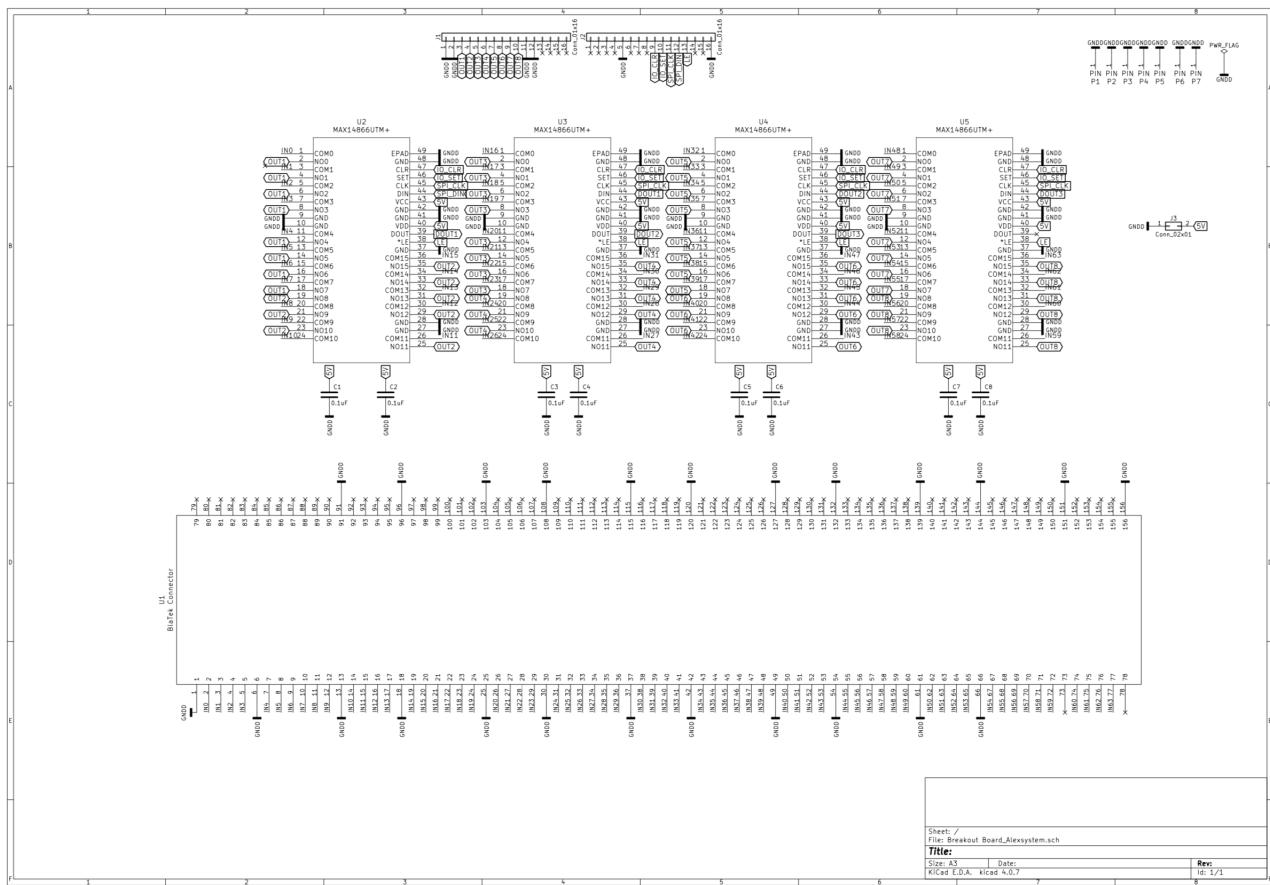


Figure A.3. PCB Schematic of Breakout Board.

Appendix B

Preparation of this document

This document was prepared using pdfL^AT_EX and other open source tools. The (free) programs implemented are as follows:

- L^AT_EX implementation:

MiK_TE_X

<http://www.miktex.org/>

T_EXLive

<https://www.tug.org/texlive/>

MacT_EX

<https://tug.org/mactex/>

- T_EX-oriented editing environments:

Vim Text Editor

<https://www.vim.org/>

- Bibliographical:

BibT_EX

<http://www.bibtex.org/>

Zotero

<https://www.zotero.org/>

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