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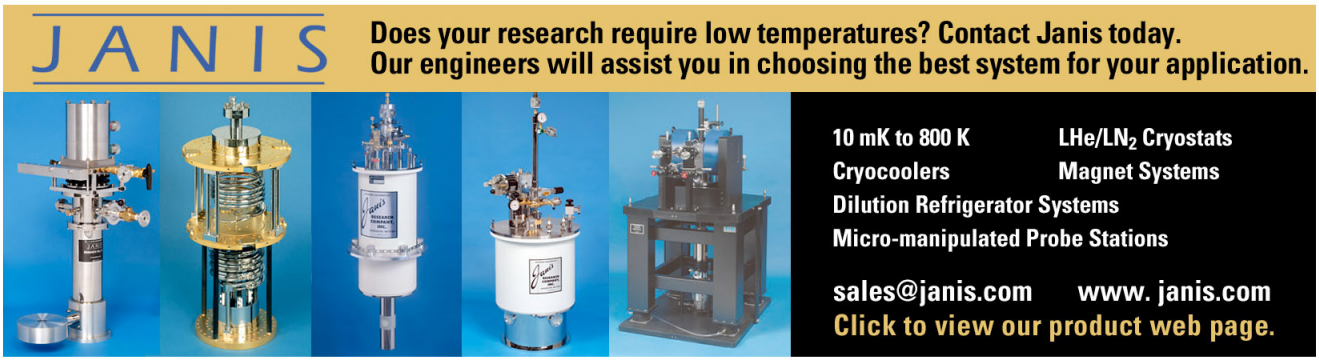


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# A digital receiver module with direct data acquisition for magnetic resonance imaging systems

Weinan Tang, Hongyu Sun, and Weimin Wang[a)]
*Institute of Quantum Electronics, School of Electronic Engineering and Computer Science, Peking University, Beijing, People's Republic of China*

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A digital receiver module for magnetic resonance imaging (MRI) with detailed hardware implementations is presented. The module is based on a direct sampling scheme using the latest mixed-signal circuit design techniques. A single field-programmable gate array chip is employed to perform software-based digital down conversion for radio frequency signals. The modular architecture of the receiver allows multiple acquisition channels to be implemented on a highly integrated printed circuit board. To maintain the phase coherence of the receiver and the exciter in the context of direct sampling, an effective phase synchronization method was proposed to achieve a phase deviation as small as 0.09°. The performance of the described receiver module was verified in the experiments for both low- and high-field (0.5 T and 1.5 T) MRI scanners and was compared to a modern commercial MRI receiver system. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4755089]

## I. INTRODUCTION

Commercially available MRI systems are delivered with exceptional performance and versatility for major clinical markets and research. However, they cannot always satisfy the needs of some emerging and application-specific studies because such rigorously designed instruments require significant costs and engineering efforts. In addition, innovations for these standard systems may be hindered from adopting the latest techniques due to long-term development cycles and quality controls such as American College of Radiology (ACR) accreditation and Food and Drug Administration (FDA) regulations. Therefore, it is feasible for researchers to design home-built magnetic resonance imaging (MRI) systems as well as their components.[1–7]

In an MRI system, a receiver (Rx) is utilized to convert the radio frequency (RF) signal induced in the receive coil into complex baseband data that are suitable for image reconstruction. Many receiver designs of different architectures are possible. Conventional heterodyne receivers mostly use a local oscillator (LO) reference to mix down the RF signal to an intermediate frequency for acquisition.[1,8] However, the image signals and unwanted noise will be introduced into the imaging bandwidth because of analog down-conversion circuits, ultimately reducing the available signal-to-noise ratio (SNR). With advances in wide band high-resolution analog-to-digital converters (ADCs) and digital RF integrated circuits, several new receivers have been designed for direct sampling, a concept generally known as direct digital receiver.[9–12] The direct sampling approach drives the receiver chain much closer to the coil site while it eliminates the need for analog mixers, LO generator, and related filters, therefore achieving improved performance while reducing the system cost, form factor, and design complexity.

In digital receiver systems, the digital down conversion (DDC) is necessary and widely performed using dedicated integrated chips (ICs).[1,2,12–14] These receiver ICs have been extensively utilized, but they are generally short of flexibility and sufficient dynamic range at the low imaging bandwidth.[2] In recent years, field-programmable gate array (FPGA)-based solutions have been proposed.[11,15,16] These designs allow efficient DDC implementation with reconfigurability, scalability, and cost effectiveness. However, even with the off-the-shelf intellectual property (IP) cores, the development of the receivers as reported in the literature still seems complex because it is quite time-consuming to perform functional modeling, iterative simulations, and verifications with hardware description language programming.

In MRI, it is crucial to maintain the phase coherence of exciter and receiver throughout the pulse sequence, especially for multi-slice and fast spin echo (FSE) imaging. One solution—called frequency rewinding[13]—makes it possible to keep the receiver phase locked to the exciter (Tx) phase but it increases the duration of the pulse sequence. Another useful approach is to simultaneously switch the frequency of the receiver to the same value of that of the exciter.[13] However, this method may not be suitable in certain conditions where the Tx/Rx frequencies are inherently different, for example, the system combining all-digital RF excitation and direct reception with undersampling.

Previously we constructed a custom-built receiver prototype that incorporates four sets of 16-bit ADC (AD9446, Analog Devices, Norwood, MA) and Analog Devices digital receiver chip AD6620, as shown in Fig. 1. The module was integrated and used for a novel intraoperative imaging system proposed at the 2011 RSNA.[17] The challenge and success of this first generation inspire us to develop a new digital receiver module that can resolve the issues mentioned before. As shown in Fig. 2, the second-generation architecture is based on a modular mixed-signal circuit that employs a single-chip FPGA to implement multiple reception channels.

a)E-mail: wmwang@ele.pku.edu.cn.

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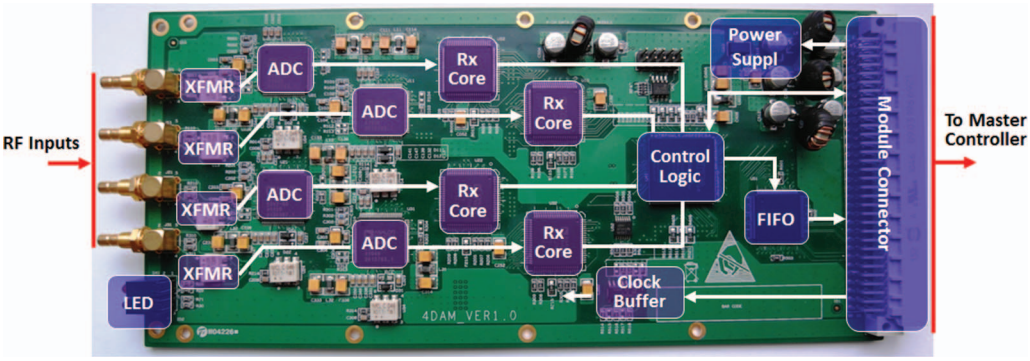


FIG. 1. Photograph of the first-generation digital receiver module prototype with each dedicated Rx core containing a single Rx channel.

The design flow of the DDC function is greatly simplified by leveraging an open development tool—System Generator (Xilinx, San Jose, CA). Moreover, a new phase synchronization method is proposed to maintain consistent k-space data. Finally, the performance of the receiver module was tested, compared to a standard modern receiver, and demonstrated by experimental results that were carried out on both low- and high-field MRI systems.

## II. SYSTEM DESIGN

### A. Hardware architecture

The presented digital receiver module (DRM) along with the RF front-end essentially completes the receiver hardware architecture shown in Fig. 3. The RF signal output from the preamplifier is injected into the front-end module where it is first amplified through a variable gain stage. The total receiver gain is digitally controllable from −32 dB to +48 dB with a resolution of 0.5 dB. Prior to the ADC, an anti-aliasing filter is required to remove frequency components outside the Nyquist zone where the RF signal is located. The unwanted signals or noise that fall outside the bandwidth of the RF signal can be further eliminated in the subsequent digital filtration. For baseband sampling, a low-pass filter is used for selection of the first Nyquist zone whose width is given by half the sampling rate; for undersampling where the band of sampled RF signal lies within the higher order Nyquist zones, a band-pass filter is employed.

Once the signal has been anti-aliasing filtered, it is then passed into the DRM. The DRM essentially contains four independent reception channels on a carrier card. The card directly digitizes inputs using a single quad-channel 16-bit ADC (ADS5263, Texas Instruments, Dallas, TX) that operates at 50 MSPS. Each input is differentially coupled with two cascadable RF transformers (WBC1-1TL, Craft Coil, Cary, IL). The DRM is also capable of accommodating four additional channels using a FPGA Mezzanine Card via a low pin count connector. The network of sampling clock is distributed with low-level jitter (<1 ps) and derived from the system clock of 50 MHz.

The sampled signals from the ADC are converted into four serial data streams over a low-voltage differential signaling interface. The data are then fed into an FPGA chip (XC5VSX50T, Xilinx, San Jose, CA) where a receiver core is implemented to perform digital quadrature demodulation, multi-rate channel filtration, and data buffering. The XC5VSX50T is one of the Xilinx Virtex-5 platforms that target high-performance signal processing with advanced serial connectivity. The chip consists of 8 160 logic slices, 288 DSP48E slices, a maximum of 4752 Kb block RAMs, and 12 RocketIO transceivers with a package size of 35 × 35 $mm^2$.[18] The baseband signals from the selected reception channels are combined to create an in-phase and quadrature (I/Q) interleaved data stream that is finally to be buffered and uploaded.

As depicted in Fig. 4, the DRMs can be integrated into a home-built MRI console (PKSpec, Peking University, Beijing, China) in a distributed manner. The console is designed

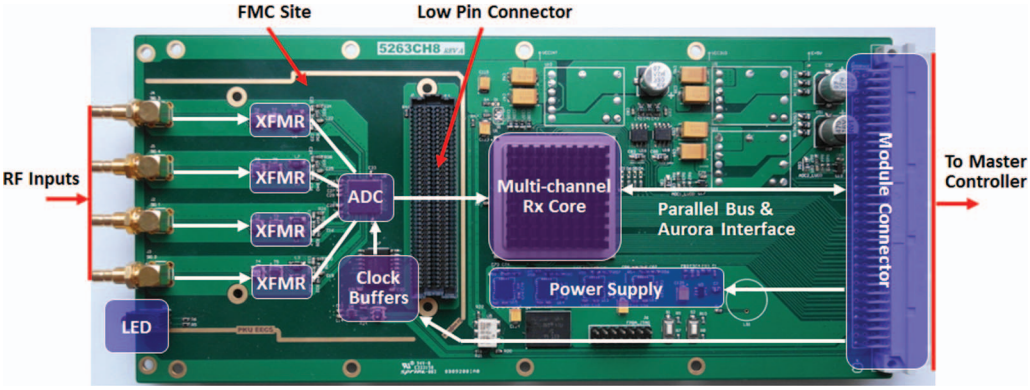


FIG. 2. Photograph of the proposed digital receiver module with multiple Rx channels implemented inside a single FPGA-based Rx core.

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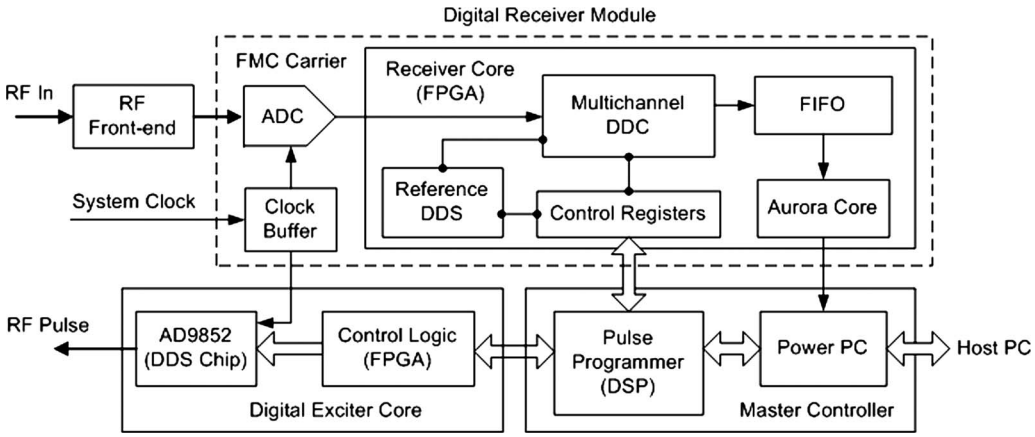


FIG. 3. Block diagram of the proposed receiver hardware incorporated in a self-built digital transceiver.

upon a modular architecture that consists of four major components: master controller, RF exciter, gradient waveform generator, and RF receiver. A master controller communicates with a host PC through the Gigabit Ethernet and coordinates the DRMs over a customized parallel interface. Each DRM supports up to eight reception channels and is capable of streaming acquired data to the master controller via a high-speed serial data link (the Aurora link). When the expected count of channels is beyond a single master controller's data throughput limit, additional controllers (each with up to 12 DRMs) can be employed via the Ethernet.

## B. Receiver core

The receiver core is implemented inside the FPGA chip. It contains a multichannel DDC block and one-lane Aurora interface. The ADC outputs are captured and aligned into 16 bits in the FPGA's deserializers (ISERDESs). The data are then down-mixed with a quadrature direct digital synthesizer (DDS) outputs to generate I/Q data that are, respectively, fed into five stages of the cascaded integrator comb (CIC5) filtering where the incoming samples are decimated by a factor that is programmable from 4 to 8192. The CIC5 filter has a Sinc-like shaping on the output that is then corrected for by a CIC compensation filter (CFIR) with a fixed decimation factor of four. A decimating FIR (DFIR) that provides further level of filtration follows the CFIR. The resultant I/Q data out of the DFIR are then rounded and sent to a channel builder. Over there, the data are combined with samples from other channels before being transferred into an on-chip first-in first-out (FIFO) memory that is capable of storing up to 8 192 complex samples. The DFIR is customizable in decimation rate (up to 1024) and supports for up to 256 sets of filter coefficients with 2–2048 coefficients per set. The DDC internal data paths and the filter coefficients are quantized into 24-bit and 18-bit two's complement data, respectively, in order to achieve maximum dynamic range while maintaining effective usage of the FPGA resources. The acquisition parameters inside the receiver control registers, such as number of samples, receiver frequency/phase, and filter coefficients, can be flexibly reconfigured by the master controller through the parallel interface. The implementation of the DDC can be rather simple and direct by modeling its functions onto various building blocks using free IP cores provided by the Xilinx's System Generator software.

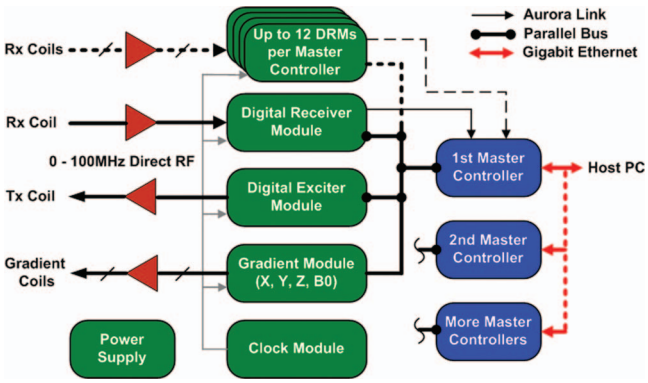


FIG. 4. Block diagram of the console that integrates the proposed DRMs. Up to 12 DRMs are available under control of a single master controller. The number of the controllers can be further increased using distributed Ethernet network.

As an open, lightweight, and customizable protocol provided by Xilinx, the Aurora interface encapsulates the FIFO data, creates a single serial data stream at 500 Mbps, and transmits it to the master controller. The one-lane protocol allows the data to be transferred over a point-to-point link at a high-speed data rate. In addition, multiple lanes can be bonded for higher total bandwidth.

## C. Phase synchronization

In MRI, the maintenance of phase coherence between transverse magnetization and receiver is crucial to achieve correct phase information of the acquired signal for a successful k-space reconstruction. After RF pulse excitation, the initial phase of a free-induction decay signal is given by

$$\phi_0 = \omega_0 t_n + \phi_t - \pi/2, \tag{1}$$

where $\omega_0$ is the center frequency, $\phi_t$ is the Tx phase shift set in the pulse sequence, and $\omega_0 t_n$ is the time-dependent phase with respect to the center frequency. After digital quadrature demodulation, the initial phase of the signal relative to the

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receiver is written as

$$\begin{aligned}\phi_s &= \phi_1 - \phi_0 \\ &= (\omega_0 t_{n+1} + \phi_r + \phi_f) - (\omega_0 t_n + \phi_t - \pi/2) \\ &= \omega_0 \Delta t + \phi_r + \phi_f - \phi_t + \pi/2. \end{aligned} \quad (2)$$

In Eq. (2), $\phi_1$ is the initial Rx phase, $\phi_r$ is the Rx phase shift set in the pulse sequence, $\phi_f$ is the digital filter phase, and $\Delta t$ represents time interval between the RF pulse and the start of every acquisition.

From Eq. (2), $\phi_f$ and $\omega_0 \Delta t$ will introduce phase uncertainty to the acquired signal, leading to incorrect signal averaging and phase encoding during scanning. In our design, $\phi_f$ can be easily kept constant by providing a synchronization signal to reset the filter stage before each readout period, and the time-dependent phases ($\omega_0 t_n$ and $\omega_0 t_{n+1}$) can be combined with the relative phase shifts when setting the initial phases of the Tx/Rx frequency synthesizers. Therefore, the only need is to provide a reference phase ($\omega_0 t$) in real time. Here, we employ an alternative DDS that generates the reference phase data inside the Rx core (shown in Fig. 3). This DDS operates at a 200 MHz clock that is generated from a programmable phase-locked loop driven by the system clock. The reference phase is not only used for the receiver, but also monitored by the master controller which calculates such an initial Tx phase that the Tx/Rx phases become consistent with each other and sends it to the exciter accordingly. Figure 5 depicts the flow chart of the phase synchronization scheme for both the receiver and exciter. The Tx/Rx phase shifts are predefined in the phase lists that are sent to the console with pulse sequence. At the time point ($t = t_n$) just before the RF pulse is generated, the master controller acquires the reference DDS's phase ($\omega_0 t_n$) from the Rx core and calculates the initial Tx phase by adding the acquired phase to the predefined Tx phase shift ($\phi_t$). Then, the calculated phase information is loaded and updated inside the Tx DDS (AD9852, Analog Device, Norwood, MA)—the frequency source that was previously reported by our group.[19] When the time point ($t = t_{n+1}$) is reached, the initial Rx phase that contains the sum of the reference phase ($\omega_0 t_{n+1}$) and a predefined Rx phase shift ($\phi_r$) is directly calculated in the Rx core and then sent to the Rx quadrature DDS. The phase accumulators of Tx/Rx DDSs must be cleared prior to being updated with the new initial phase values so that both the synthesizers can always start from the known and steady phase conditions given by

$$\begin{cases} \varphi_0 = \omega_0 t_n + \phi_t \\ \varphi_1 = \omega_0 t_{n+1} + \phi_r \end{cases}, \quad (3)$$

where $\varphi_0$ is the initial phase set to the exciter and $\varphi_1$ is the initial phase set to the receiver.

With reference to the system clock, the latency for the phase synchronization process is 23 clock cycles throughout the exciter path and 12 clock cycles throughout the receiver path. Both the delays are fixed and can be calibrated during the pulse sequence. The resolutions of the Tx/Rx synthesizers and that of the reference DDS are required to be exactly matched. In this case, they are all implemented using a 48-bit phase accumulator and a 14-bit phase offset register.

## III. EXPERIMENTAL RESULTS

Initial performance tests of the presented DRM were operated on the PKSpec console with a four-channel RF receive configuration. To verify the phase coherence of the exciter and receiver, we first developed a loop-back procedure with a similar functionality described in the study of Ruipeng *et al.*[13] In this case, the data to be demodulated in the receiver module were a Sinc pulse shape. The procedure was continuously repeated for 256 times to test if the phase of the acquired data remained stable. As depicted in Fig. 6, the phase fluctuation was within 0.09°, which is 0.025% of the full phase variation range. Then, we incorporated the console into a commercial 0.5 T MRI system (i_open, Wandong Medical, Beijing, China). By using a standard spin echo (SE) sequence, multiple echoes were captured with zero phase-encoding gradients. As shown in Fig. 7, the initial phase of the each echo at every acquisition was measured. The maximum phase

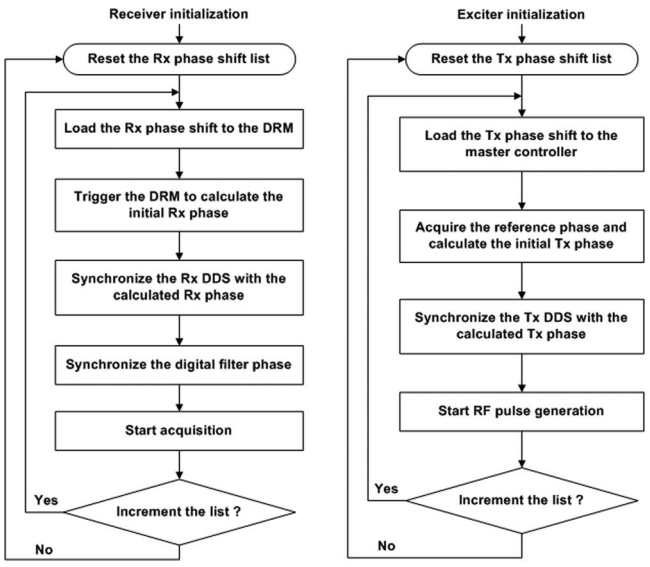


FIG. 5. Flow chart of the phase synchronization method for both the receiver and exciter.

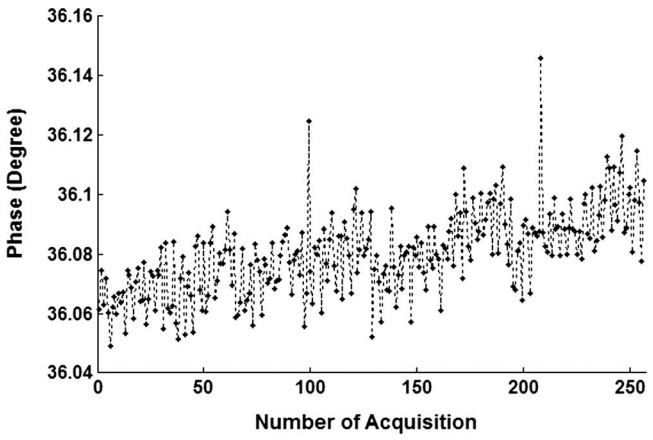


FIG. 6. Plot of the phase variation acquired by the repeated loop-back test procedures. The dots represent the phase values of the Sinc pulse's peak captured every one second.

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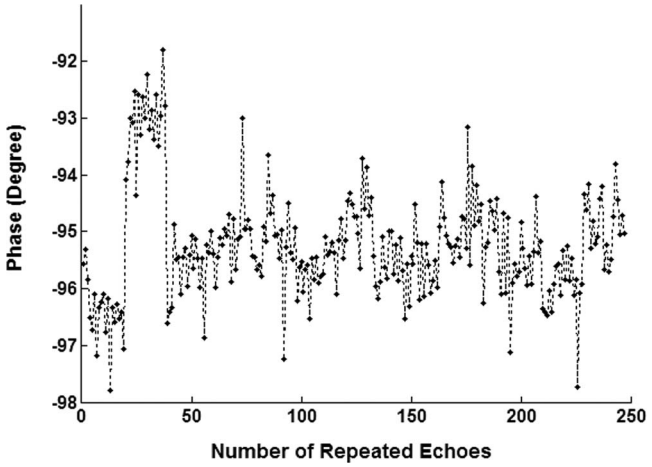


FIG. 7. Plot of the phase variation acquired using repeated standard SE sequences. A total of 247 echoes were captured at the center line of the k-space. The dots represent initial phase values of the each echo. The phase variation mainly results from the magnetic field stability.

deviation among the repeated scans was less than 6° and it was mainly caused by the static field stability of our system (typically about 10 ppm per hour for the 0.5 T permanent magnet). From Fig. 8, we can see that the resultant phase deviation did not degrade the image quality so much and there were no clearly obvious artifacts in the images obtained from a multi-slice two-dimensional (2D) FSE experiment.

The DRM was subsequently tested in comparison to the first-generation module equipped with the dedicated receiver chips—the AD6620s—that are commonly used in the MRI

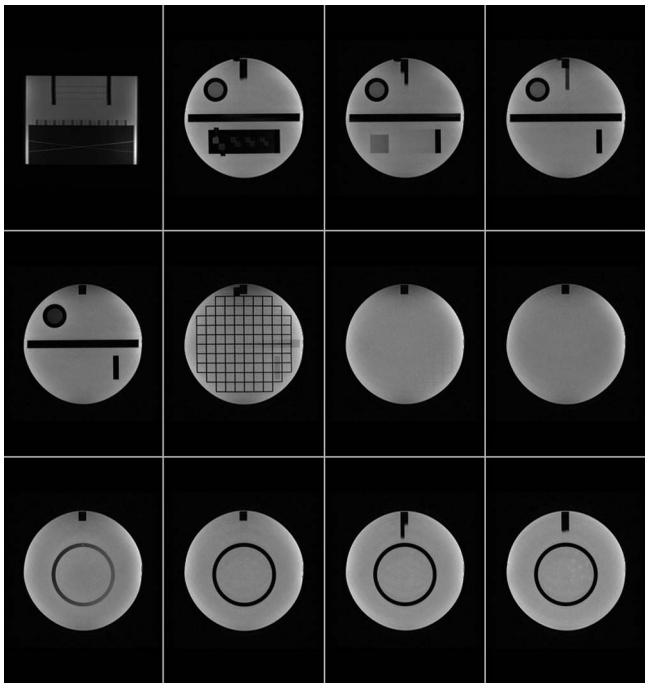

FIG. 8. Multi-slice T2-weighted 2D FSE images of a standard phantom (J5298, J. M. Specialty Parts, San Diego, CA) with a localizer image shown in the upper left. Imaging parameters: TR/TE/FA = 3000 ms/115 ms/90°; image matrix (MAT) = 256 × 256; field of view (FOV) = 250 × 250 mm; thickness (THK) = 5 mm; number of excitation (NEX) = 4; RF frequency (SF) = 21.4 MHz.

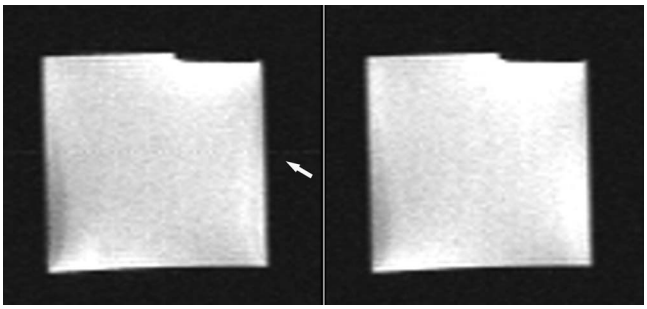

FIG. 9. Axial cross section of a square water phantom selected from the LSDWI images (TR/TE/FA = 150 ms/128 ms/90°, MAT = 128 × 82, FOV = 199 × 250 mm, THK = 7 mm, NEX = 2, SF = 21.4 MHz). Left-hand images were acquired using an AD6620 receiver and a dc artifact is induced from the intrinsic truncation effects of the chipset; right-hand images were acquired using the DRM where the dc bias is eliminated with minimized quantization error. Both images were displayed at the same window and level.

receiver designs.[1,2,12,13] It is clear from Fig. 9 that, in a phantom imaging comparison experiment using the line scan diffusion weighted imaging (LSDWI) sequence, a dc artifact (indicated by the white arrow) was introduced from the AD6620 receiver, but it was not incurred with the second-generation module.

The DRM can be easily adapted to a 1.5 T custom-built scanner with the PKSpec console by just modifying the anti-aliasing filters at the RF front-end and a few sequence parameters (e.g., center frequency and receiver gain). The anti-aliasing filters that were used in the experiments have the specifications detailed in Table I. Here, the low-pass and band-pass filters were employed for the 0.5 T and 1.5 T MRI systems, respectively.

The basic 1.5 T system configuration included a superconducting magnet (Oxford Instruments, Oxfordshire, UK), a three-channel gradient amplifier (GA-300, Performance Control, Montgomeryville, PA), a RF power amplifier (THF18, Toshiba Teli, Japan), and a set of in-house RF coils. Main characteristics of the DRM were measured at a center frequency of 63.89 MHz (1.5 T). The RF frequency range was from dc to 100 MHz and the imaging bandwidth was from 10 kHz to 1 MHz. The maximum ADC input level provided a signal-to-noise and distortion ratio of 70.9 dBc. The spur-free dynamic range was measured at 80.2 dBc and the channel-to-channel crosstalk was below 98.75 dBF with a 63.89 MHz tone at −1dBF on an adjacent channel and with no inputs on the other channels. Typically, at a baseband of 400 kHz, the receiver module achieved a dynamic range of 93.2 dB (∼16.5 bits).

TABLE I. The specifications of the anti-aliasing filters used in 0.5 T and 1.5 T MRI experiments.

| Filter type | Passband (MHz) (loss < 1 dB) | Passband (MHz) (loss = 3 dB) | Stopband (MHz) (loss > 50 dB) |
|---|---|---|---|
| Low-pass | dc − 22 | 24.5 | >45 |
| Band-pass | 63.89 ± 500 kHz | 63.89 ± 2 MHz | <50 and >78 |

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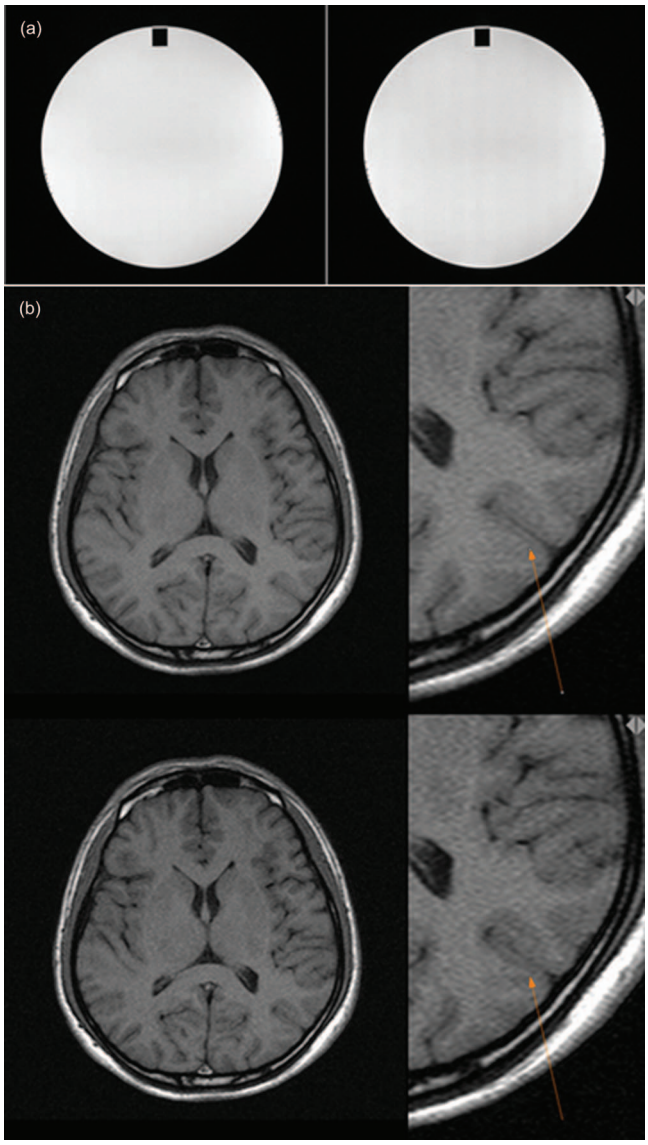


FIG. 10. (a) Two spin echo images of a standard phantom (J5298) acquired with a commercial receiver of a DRX2 console (left-hand image), and with the proposed receiver module (right-hand image). Imaging parameters: TR/TE/FA = 460 ms/16 ms/90°; MAT = 256 × 192; FOV = 250 × 250 mm; THK = 5 mm; NEX = 2; SF = 63.89 MHz. (b) Axial cross section of a normal volunteer's brain selected from T1-weighted images (TR/TE/FA = 560 ms/13 ms/90°, MAT = 320 × 202, FOV = 220 × 220 mm, THK = 5 mm, NEX = 2, SF = 63.89 MHz), acquired with the DRX2 (lower images), and with the proposed DRM (upper images). Right-hand images = enlarged view (×4). All images were displayed at the same window and level.

Two multi-slice SE acquisitions were operated on a commercial imaging receiver system (DRX2, Oxford Instruments, Oxfordshire, UK) and the proposed DRM. Figure 10(a) shows the phantom images acquired from both the receivers. The resultant SNR comparison between both the cases resulted in values of 161 for the DRX2 receiver and 176 for the DRM, respectively, using a single Rx channel. The SNR was calculated as the mean signal in the center of the phantom divided by the average standard deviation of noise from the background regions. Figure 10(b) shows the axial T1-weighted images of a normal volunteer's brain. In comparison, the enlarged view (×4) shows that the image reconstructed from the DRM even displayed a finer anatomical structure (indicated by the yellow arrow). The superior image resulted from an increased dynamic range due to the reduced background noise level. Finally, a three-dimensional (3D) time-of-flight (TOF) vascular imaging experiment was performed to further demonstrate the feasibility of the DRM. The result was processed using the maximum intensity projection (MIP) method and the image is shown in Fig. 11.

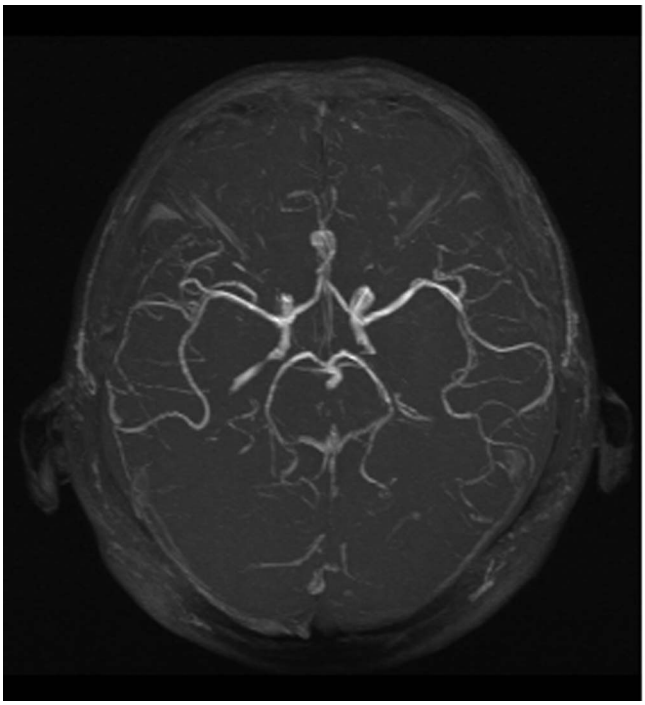

FIG. 11. The MR vascular image acquired from 3D TOF sequence with MIP post-processing. Imaging parameters: TR/TE/FA = 35 ms/10.6 ms/30°; MAT = 256 × 192; FOV = 200 × 200 mm; THK = 1 mm; NEX = 1; SF = 63.89 MHz.

## IV. DISCUSSION AND CONCLUSION

The digital receiver module investigated in this paper is a scalable and reconfigurable acquisition platform for MR imaging based on the latest FPGA technology and high-performance mixed-signal techniques. By implementing the desired digital work inside a single chip FPGA, we constructed an eight-channel prototype with highly integrated circuits on a 220 mm × 110 mm printed circuit board (PCB). The analog input bandwidth for the receiver module is 700 MHz and the maximum sampling rate provided by the ADC device is 100 MHz. When the ADC is operated at 50 MHz, the RF carrier signal (21.4 MHz) for the experiments at 0.5 T is acquired using baseband sampling (i.e., the center frequency lies in the first Nyquist zone) and that (63.89 MHz) for 1.5 T is acquired using undersampling (i.e., the center frequency lies in the third Nyquist zone). Given the maximum sampling rate and the sufficient image quality, the maximum RF input frequency is estimated to be 135 MHz. So, based on our current proposed hardware, direct data acquisition is feasible for high-field applications up to 3 T in terms of hardware simplicity, cost-effectiveness, and less distortion compared to

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analog down-mixing scheme. With the eight-channel configuration per module and without the RF front-ends, the total cost per channel is ~$250.

The receiver module is managed from the master controller via two independent interfaces. The parallel interface provides for triggering and synchronization signals and updates the registers of acquisition parameters. The Aurora interface, according to its specification,[20] is capable of uploading the baseband data at high speeds of 100 Mbps to 3.75 Gbps. Here, we set the data transfer rate at 500 Mbps. This transfer speed helps in retrieving data from the receiver FIFO in a short period, e.g., the transmission from eight channels with 512 complex samples per channel can be completed in less than 300 $\mu$s. Transfer speeds higher than 500 Mbps may cause signal integrity problems due to a data rate bottleneck of the backplane connector. In addition, the latency for the data transmission through the Aurora interface is low and fixed at only 300 ns.

In multi-slice imaging, phase stability is a key factor so that the k-space data remain consistent. Unlike frequency rewinding and fast frequency switching techniques, the suggested phase coherence maintenance method is completely independent of the frequency relationship between the exciter and receiver so that the frequencies generated by the Tx/Rx DDSs can be different. This is quite useful when the undersampling scheme is employed along with the direct transmission and no specific design of the exciter or receiver is required in the application.

Oversampling by a factor of 4 (followed by digital filtering) corresponds to one bit of improvement in the dynamic range. As a result, the DDC internal data path uses a 24-bit word size in case of inefficient dynamic range at lower imaging bandwidths. The gain stepping technique[13,21] might be employed in the future to further increase the dynamic range in the high-field and high-resolution 3D imaging.

In this paper, the proposed digital receiver module's performance has been demonstrated for both the low- and high-field systems. We believed that this compact module is not only available for a specific console, but also suitable for a variety of MR imaging applications and systems due to its customized interface, and it is expected to be used in the novel MR research such as intraoperative and interventional imaging applications.

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