Learn to Code, Code to Learn
CODING ACADEMY

NUS National University of Singapore
School of Computing

Floorplans &
Arithmetic Expressions

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(20-24 Dec 2021, Mon-Fri)

Outline of the Camp:

- Day 1: Arrays
- Day 2: Stacks and Queues
- Day 3: Sets and MultiSets
- Day 4: Recursion
- Day 5: Sorting (and Searching?)

What we will emphasize

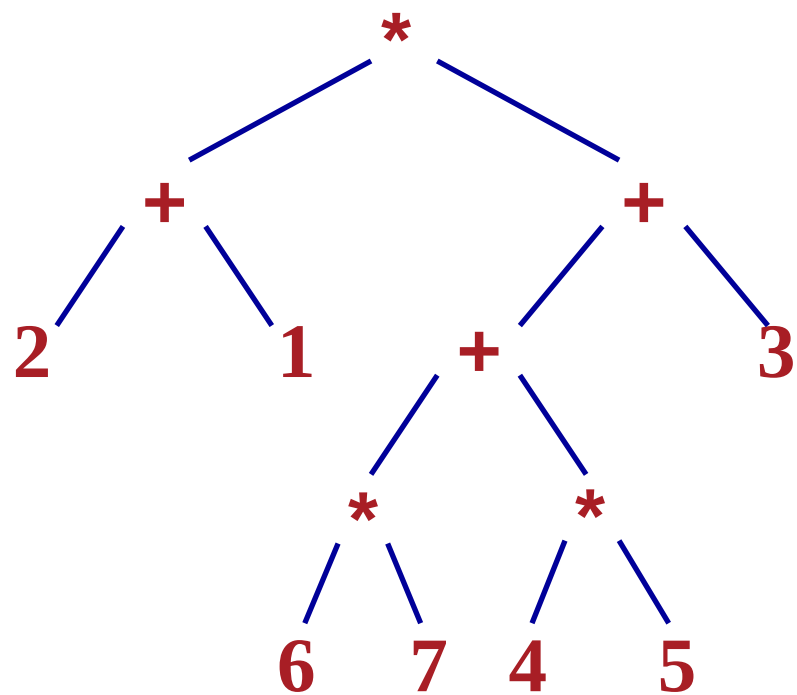
- **Problem Solving**
  - **with Algorithmic thinking**
  - **and Data Structures**
- **Emphasis on Efficiency**
  - **Complexity of an algorithm**
  - **Difference between slow, fast, and very fast**
  - **Why it is important**
- **PSPP Problem Solving Process…**

Exercise 5

Arithmetic Expression

10 + (2*8) – 3)

Expression Tree



10 2 8 * + 3 –

Polish Expression

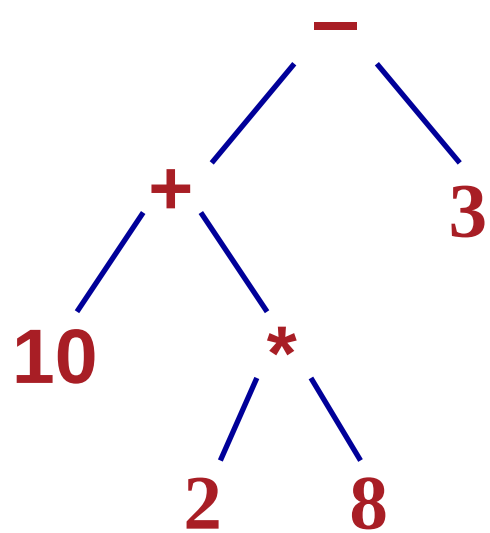
(postorder traversal of expr tree)

Exercise 5

Arithmetic Expression

10 + (2*8) – 3)

Expression Tree



10 2 8 * + 3 –

Polish Expression

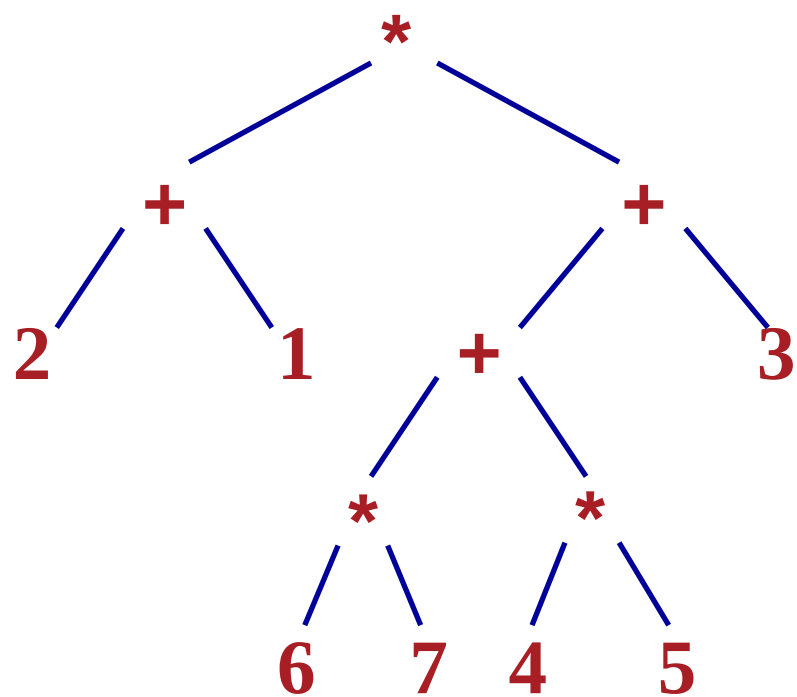
(postorder traversal of expr tree)

Another expression trees

Arithmetic Expression

(2+1) * ((6*7) + (4*5)) + 3)

Expression Tree



21+67*45*+3+*

Polish Expression

(postorder traversal of slicing tree)

Unexpected use of Expression Trees

"A Plan" vs "A Solution"

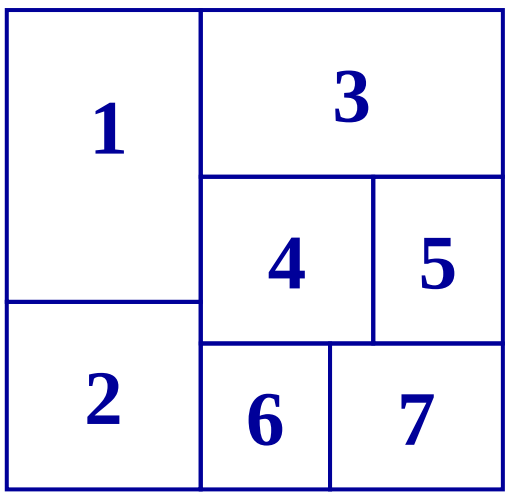
- **Plan: rough idea of solution. only main big steps.**

- **Solution: everything is all worked out.**

Slicing Floorplan

Idea by D. F. Wong
(Slide by Evangeline Young, CUHK)

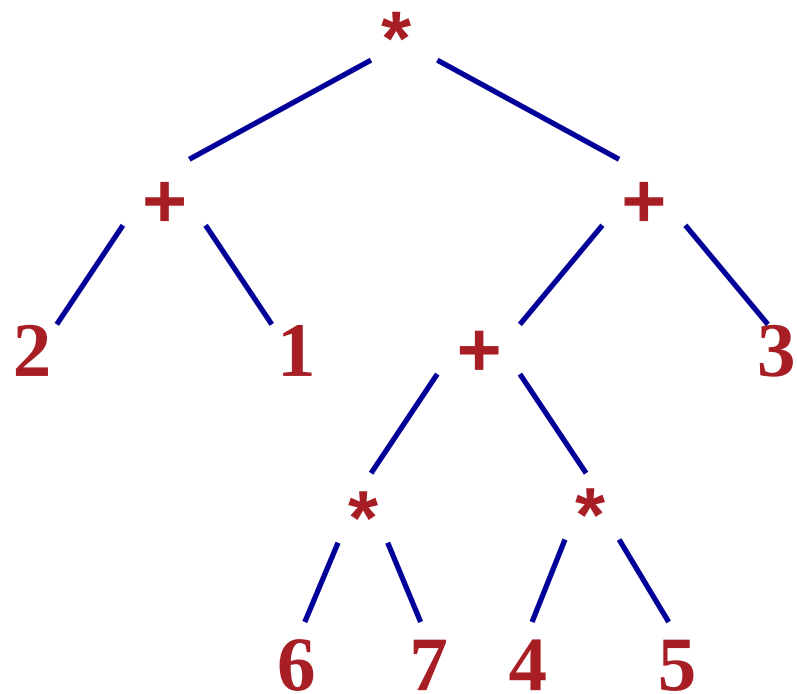
Slicing Floorplan



21+67*45*+3+*

Polish Expression
(postorder traversal of slicing tree)

Slicing Tree



This came from…

"A New Algorithm for Floorplan Design", D.F. Wong and C.L. Liu, Design Automation Conference, pp.101-107, 1986.

A NEW ALGORITHM FOR FLOORPLAN DESIGN.[1]

D. F. Wong and C. L. Liu

Department of Computer Science
University of Illinois at Urbana–Champaign
1304 W. Springfield, Urbana, IL 61801

Abstract

We present in this paper a new algorithm for floorplan design using the method of simulated annealing. The major contributions of the paper are: 1. A new representation of floorplans (normalized Polish expressions) which enables us to carry out the neighborhood search effectively. 2. A simultaneous minimization of area and total interconnection length in the final solution. Experimental results indicate that the algorithm performs well in many test problems.

which provides information on the wiring density between each pair of modules.

A *feasible solution* of the floorplan design problem consists of an enveloping rectangle R subdivided by horizontal and vertical line segments into n nonoverlapping rectangles labeled 1,2,...,n. The aspect ratio of R is between p and q, and for each i, rectangle i (with dimensions (x_i,y_i)) is large enough to accommodate module i. (*i.e.* $x_i \geq w_i$ and $y_i \geq h_i$ where w_i and h_i satisfy the above three conditions.)

Floorplan and connections…

(C. L. Liu)
MIT > UIUC >
Tsinghua (TW)

H.W. Leong,
UIUC > NUS

D. F. Wong,
UT-A > UIUC
> CUHK

Evangeline Young
CUHK

FUN Activity:
Find out who all these people are.

Thank you!

If you want to contact me,
Email, FB at leonghw@comp.nus.edu.sg
or Google "Leong Hon Wai"