EE203 – Electrical Circuits Laboratory

Experiment 2 Laboratory Report

Time-Varying Signals

Group Members:

Name: Korkut Emre Arslantürk **Number: 250206039**

Submission Date: 17/11/2020

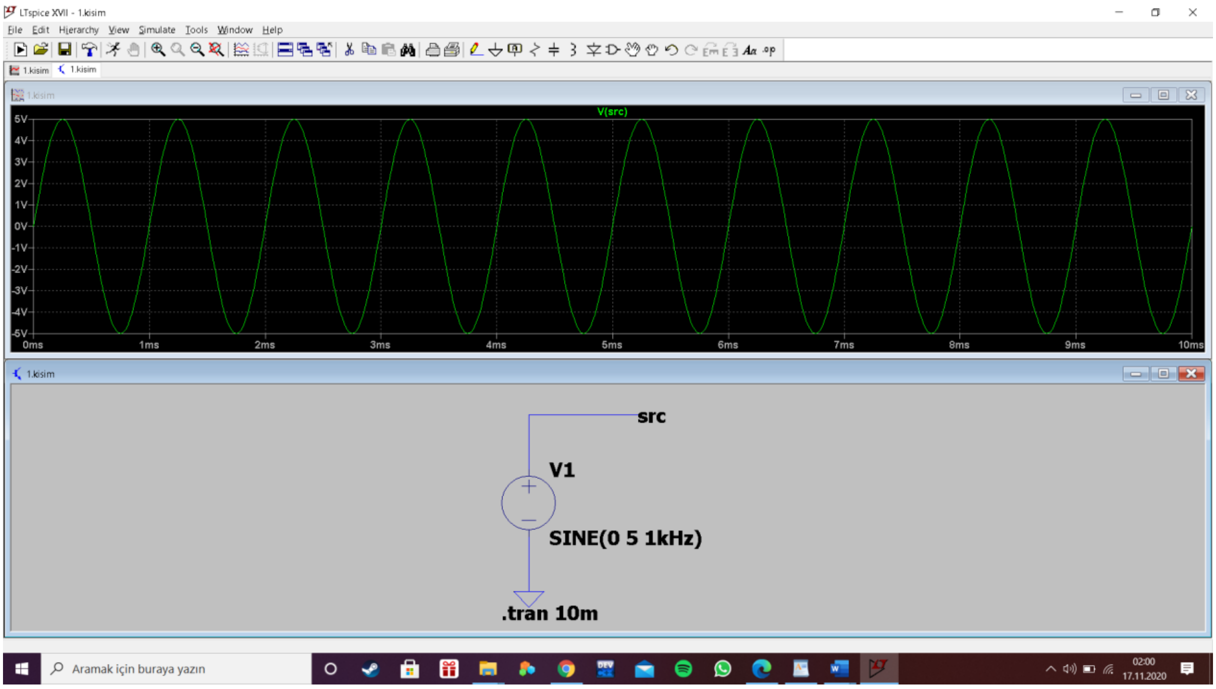
Preliminary Work

1. Read the procedure given for this experiment, and make sure that you have the required knowledge about the laboratory equipment to perform the specified steps in case you need to make the measurements with real components and devices. Refer to EELab_GuideBeginner.pdf to refresh your memory. Read the section titled Grounding of Test Equipment, regarding monitoring of differential voltages with an oscilloscope.

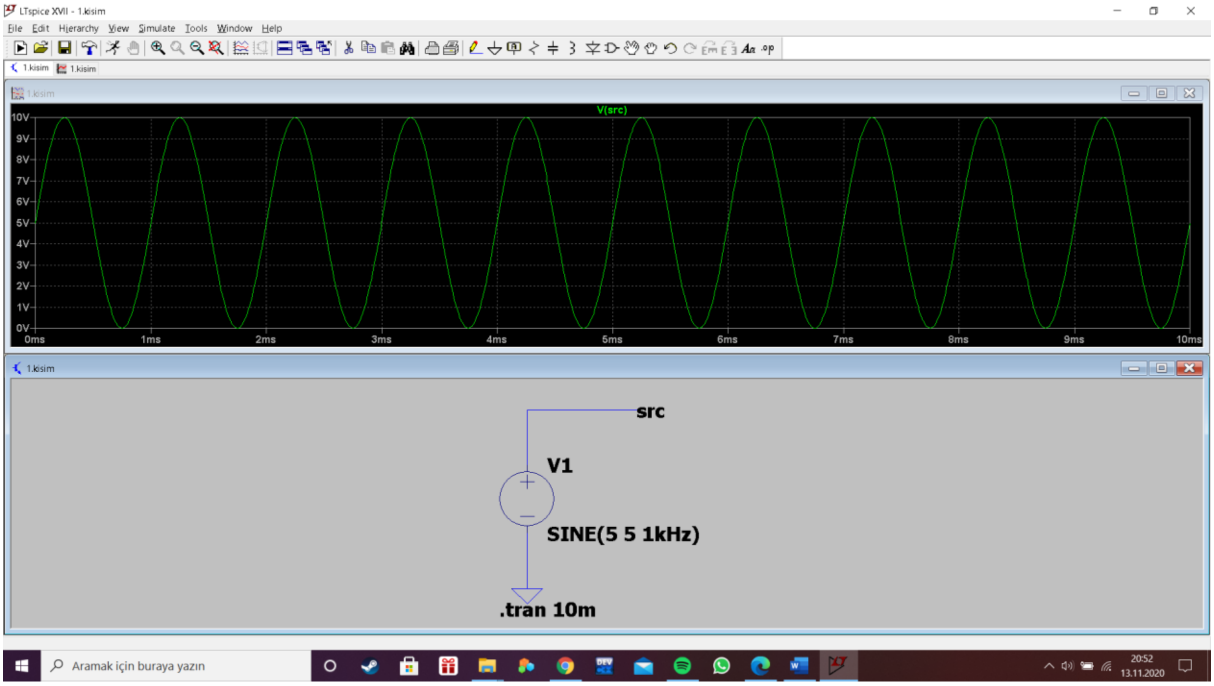
2 Open a new schematic file in LTspice and place a voltage source with a net label at its positive output as shown below.

Set the Vsrc parameters to obtain the following waveforms. Verify the voltage output by displaying the voltage at the src node after running a simulation.

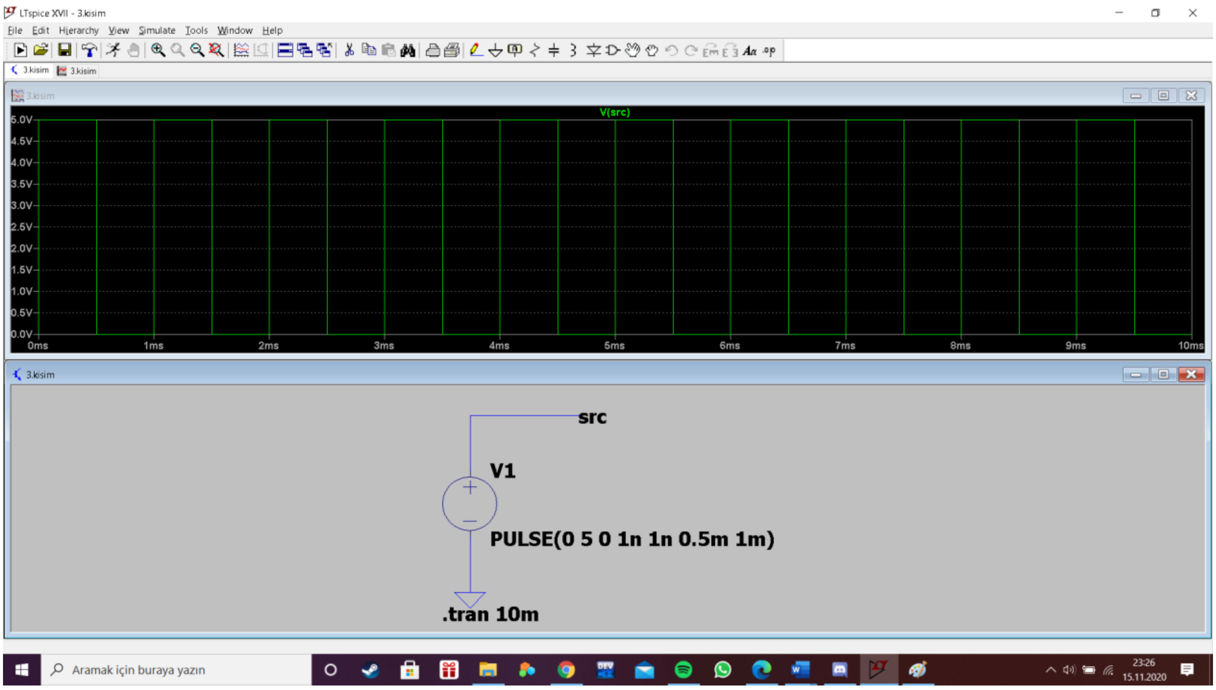
a) 1 kHz sinusoidal signal with 10 Vp-p amplitude and 0 V DC offset



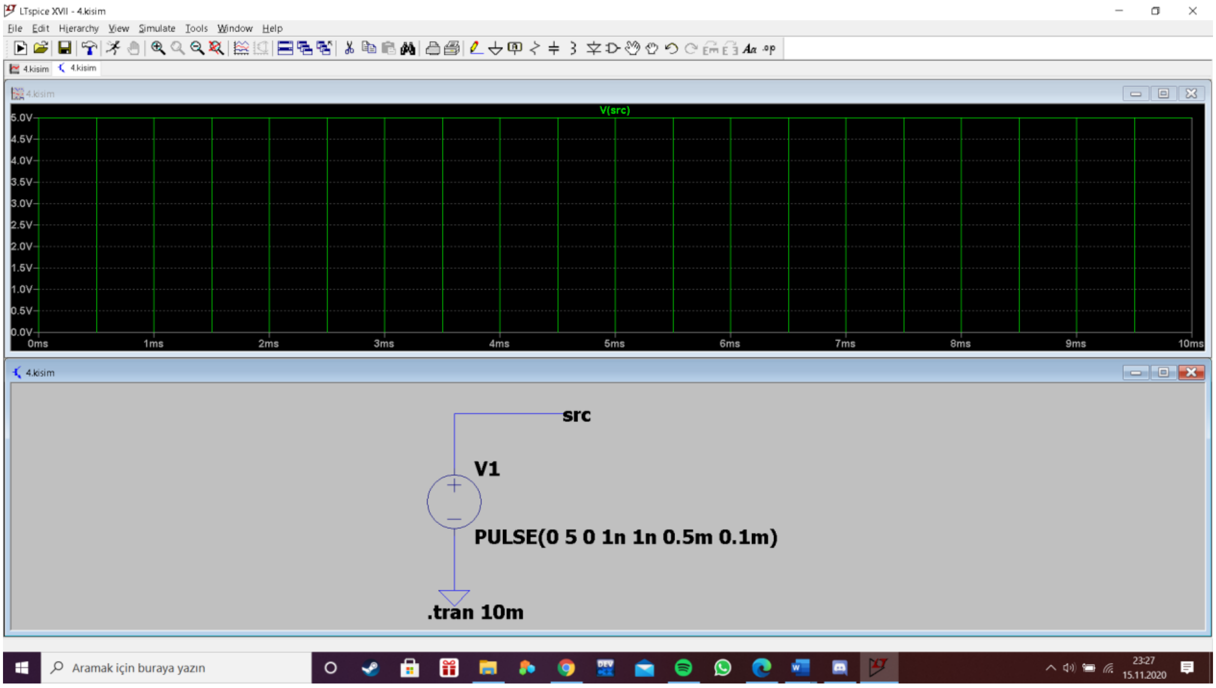
b) 1 kHz sinusoidal signal with 10 Vp-p amplitude and 5 V DC offset



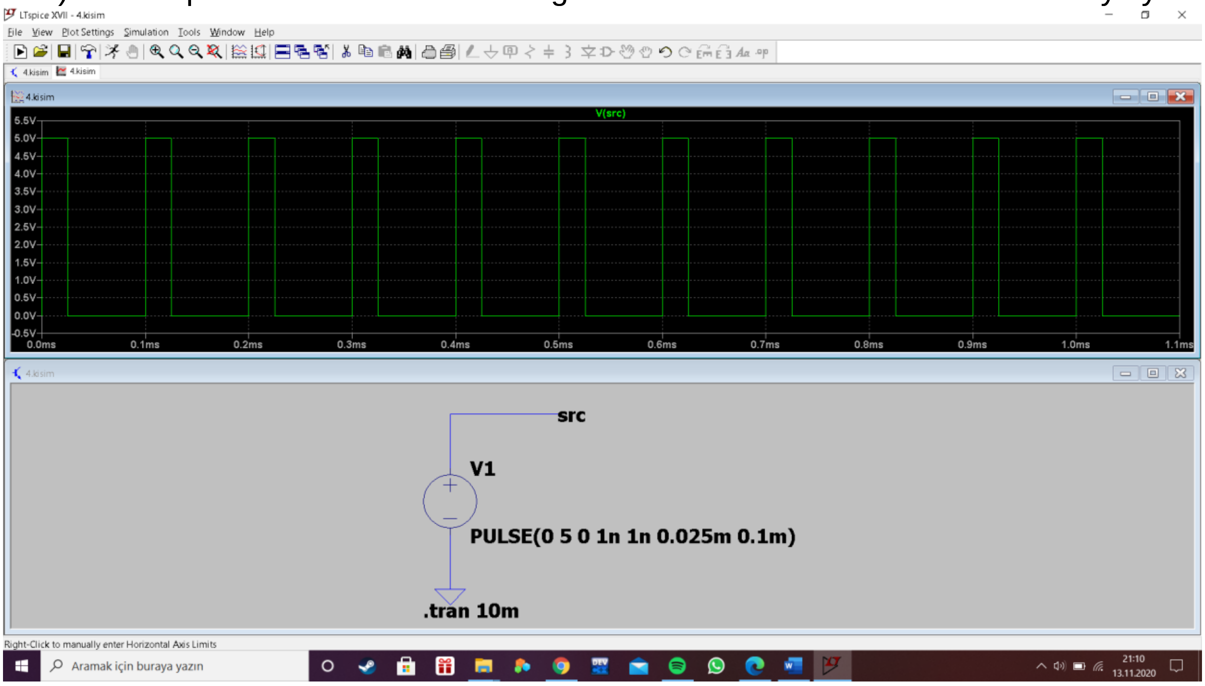
c) 1 kHz pulse waveform that changes between 0 V and 5 V with 50% duty cycle



d) 10 kHz pulse waveform that changes between 0 V and 5 V with 50% duty cycle

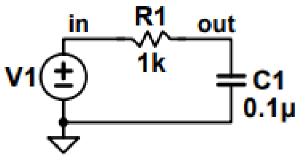


e) 10 kHz pulse waveform that changes between 0 V and 5 V with 25% duty cycle



Results

1.1 Build the circuit shown below on LTspice. Enter the C1 capacitor value as 0.1u (with the letter "u") or 100n. The C1 capacitor is necessary just to obtain different waveforms from a single voltage source. You will not make any calculations with C1

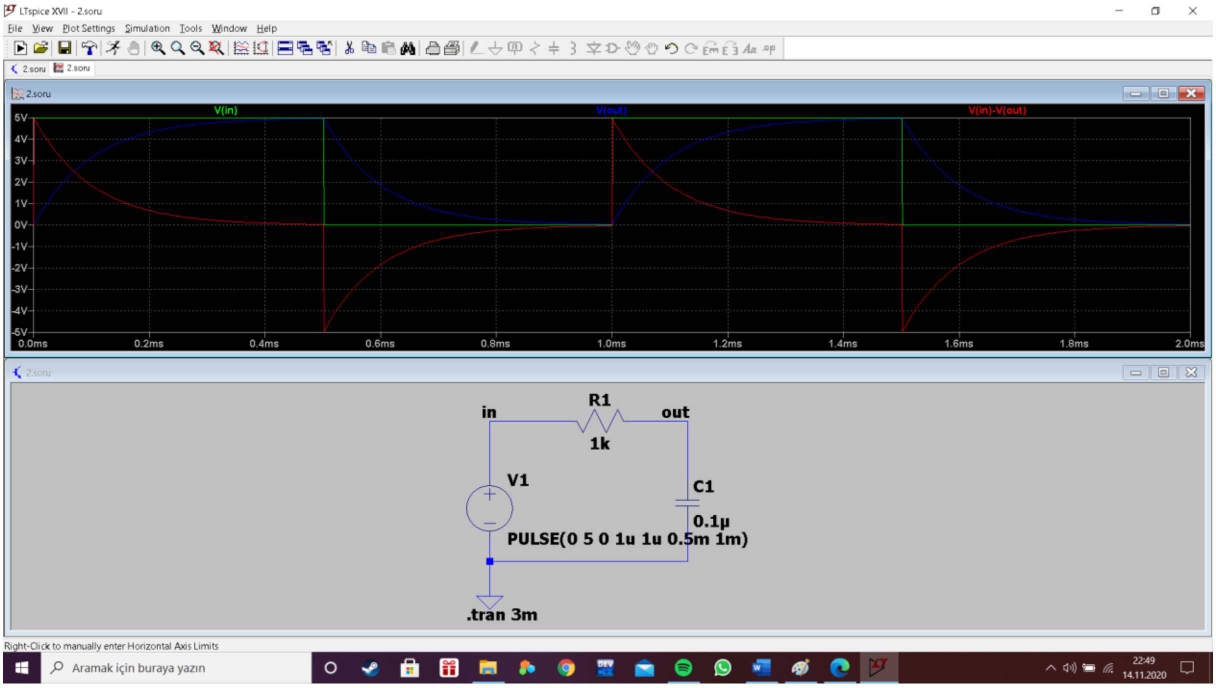


1.2 Set the V1 signal to **5 V sin(2π 1000 t)**. Right-click on the V1 voltage source, click on the **Advanced** button and select the **SINE** option to obtain a **1 kHz** sinusoidal signal with 0 V offset and 5 V peak amplitude. The component value of V1 should appear as "**SINE(0 5 1k)**" on the schematic. Place the net labels "**in**" and "**out**" as shown in the figure.

1.3 Enter the SPICE directive "**.tran 10m**" to set the simulation time to **10 ms**. Run the simulation with the V1 frequency and **R1** settings listed in the following table. Measure the peak-to-peak amplitude of $\mathbf{V_{out}}$ and its time delay relative to $\mathbf{V_{in}}$, and calculate $\mathbf{V_{out}}$ phase.

V1 Frequency (kHz)	**R1(kΩ)**	**V_{out} amplitude ($V_{p\text{-}p}$)**	**V_{out} delay(ms)**	**V_{out} phase** (degree)
1.0	**1.0**	8.44V	0.092ms	33.12
1.0	**3.3**	4.33V	0.184ms	66.24
1.0	**10.0**	1.57V	0.231ms	83.16
3.3	**1.0**	3.95V	0.055ms	65.35
3.3	**3.3**	1.42V	0.068ms	80.79
3.3	**10.0**	0.47V	0.075ms	89.11
10.0	**1.0**	1.44V	0.023ms	82.8
10.0	**3.3**	0.44V	0.0241ms	86.76
10.0	**10.0**	0.15V	0.0257ms	92.52

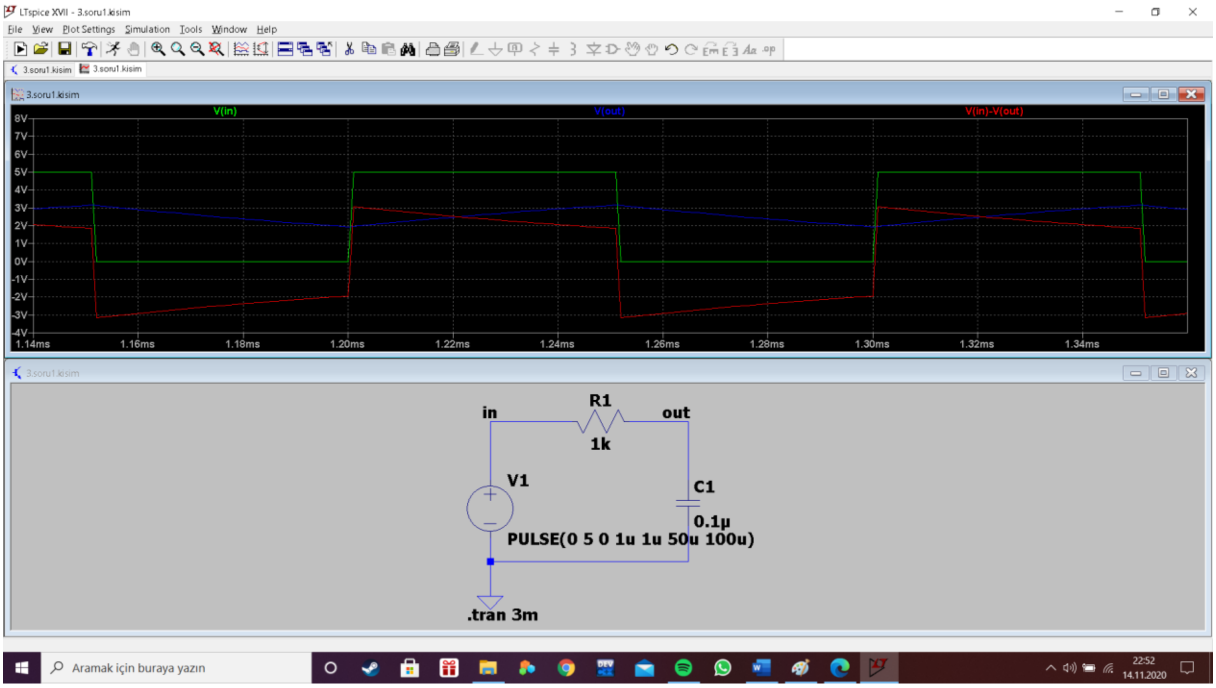
2.1 Change the **V1** source to obtain a **1 kHz** pulse waveform. Right-click on the **V1** voltage source, select the **PULSE** option, and enter the following parameters: Vinitial = **0**, Von = **5**, Tdelay = **0**, Trise = **1u**, Tfall = **1u**, Ton = **0.5m**, Tperiod = **1m**



2.2 Measure the three voltages displayed on the waveform window at the time instants specified in the following table.

Time of measurement	**V_{in}(V)**	**V_{out}(V)**	**V_{in}(V)- V_{out}(V)**
right after **V_{in}** rising edge	5V	58mV	4.941V
middle of **V_{in}** ON **(5V)** cycle	5V	4.59V	409mV
right before vin falling edge	5V	4.96V	0.4V
right after **V_{in}** falling edge	0V	4.94V	-4.94V
middle of **V_{in}** OFF (0V) cycle	0V	414.50mV	-414.50mV
right before **V_{in}** rising edge	0V	33.96mV	-33.96mV

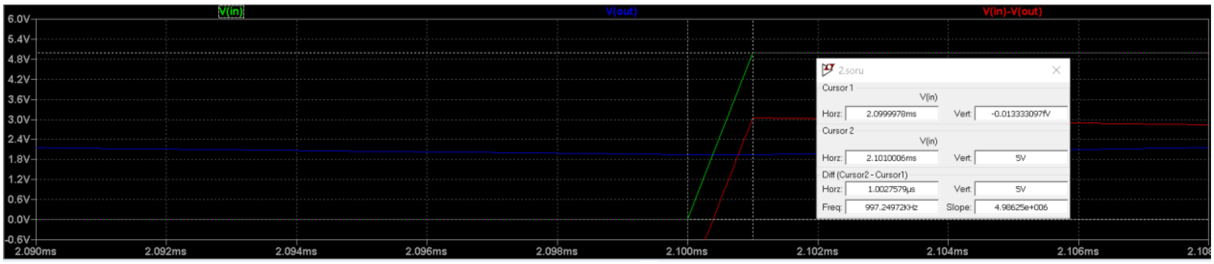
2.3 Repeat part **2.2** after changing pulse frequency to **10 kHz** (set the V1 source parameters: Ton = **50u**, Tperiod = **100u**).



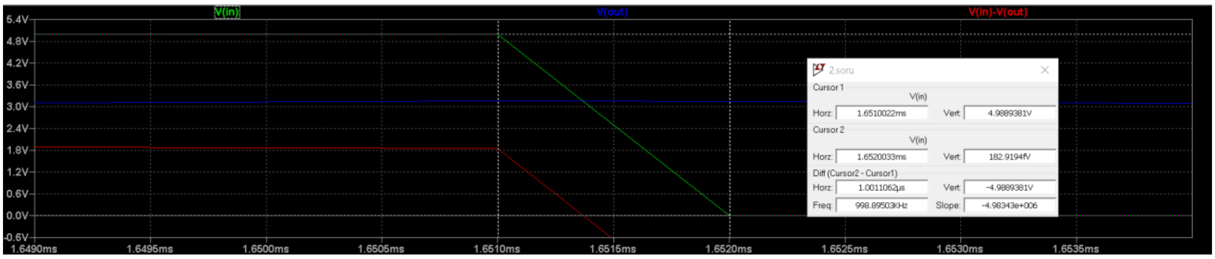
Measure the three voltages displayed on the waveform window at the time instants specified in the following table.

Time of measurement	**V_{in}(V)**	**V_{out}(V)**	**V_{in}(V)- V_{out}(V)**
right after V_{in} rising edge	5V	1.95V	3.05V
middle of V_{in} ON **(5V)** cycle	5V	2.625V	2.375V
right before vin falling edge	5V	3.15V	1.85V
right after V_{in} falling edge	0V	3.144V	-3.144V
middle of V_{in} OFF (0V) cycle	0V	2.475V	-2.475V
right before V_{in} rising edge	0V	1.94V	-1.94V

3.1 Zoom into the rising edge of the $\mathbf{V_{in}}$ waveform repeatedly until you can clearly identify the linear ramp from **0 V** to **5 V**. Measure the rise time from **0 V** to **5 V** and verify the **Trise** setting of the voltage source. Similarly, zoom into the falling edge of the $\mathbf{V_{in}}$ waveform and mesure the fall time.

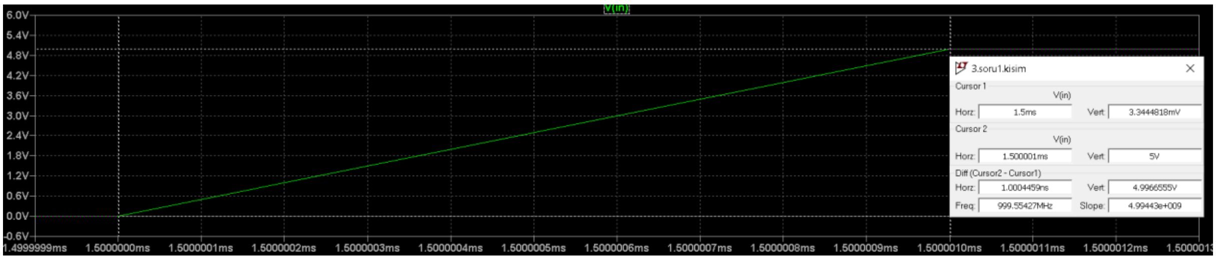


$\mathbf{T_{rise}}$ =1.002µ **s**

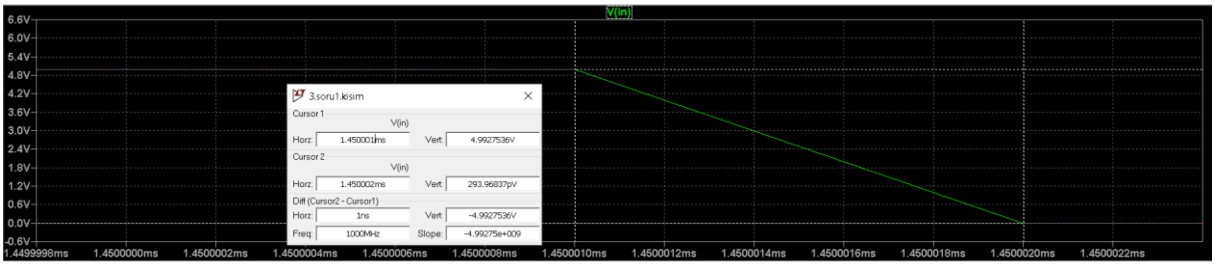


$\mathbf{T_{fall}}$ = 1.001µ **s**

3.2 Right-click on the value text "**PULSE(0 5 0 1u 1u 50u 100u)**" of V1 source on the schematic and enter a new value given by "**PULSE(0 5 0 1n 1n 50u 100u)**". Run simulation and repeat the rise time and fall time measurements on the vin waveform.



$\mathbf{T_{rise}}$ =1.00ns



$\mathbf{T_{fall}}$ = 1.00ns

Conclusion

In this experiment, In preliminary work, we place a voltage source and we set it first to get 1 kHz sinusoidal signal with 10 Vp-p amplitude and 0 V DC offset then we change 5V DC offset. Then we set as 1 kHz pulse waveform that changes between 0 V and 5 V with 50% duty cycle. After that we changed frequency 1kHz to 10kHz and finally we changed duty cyclye to 25%. In first part, we built a circuit using voltage source, 1kΩ resistor and 0.1μ capacitor. Then, we setted the V_1 signal to 5Vsin(2π 1000t). After that we calculated the V_{out} amplitude(V_{p-p}),V_{out} delay and V_{out} phase values by changing the frequency (1.0kHz-3.3kHz-10.0kHz) and resistance values(1kΩ-3.3 kΩ-10kΩ), step by step. In second part, we built same circuit with before part but we change voltage source to obtain a 1 kHz pulse waveform. We entered following parameters $V_{initial}$ = 0, V_{on} = 5, T_{delay} = 0, T_{rise} = 1u, T_{fall} = 1u, T_{on} = 0.5m, T_{period} = 1m. After that, we display V_{in}, V_{out} and V_{in}-V_{out} and we measured V_{in}, V_{out} and V_{in}-V_{out} on right after v_{in} rising edge, middle of v_{in} ON (5V) cycle, right before v_{in} falling edge, right after v_{in} falling edge, middle of v_{in} OFF (0V) cycle, right before v_{in} rising edge using cursor. In next step, we changed frequency 1kHz to 10kHz, T_{on} = 50u, T_{period} = 100u and we repeated same display and measurement. In third part, first we measured the rise time from 0V to 5V and and verified the T_{rise} setting of the voltage source and then we repeated same calculation for falling time. Then, we change to values from “PULSE(0 5 0 1u 1u 50u 100u)" to "PULSE(0 5 0 1n 1n 50u 100u)" and we repeated the rise time and fall time measurements on the V_{in} waveform.

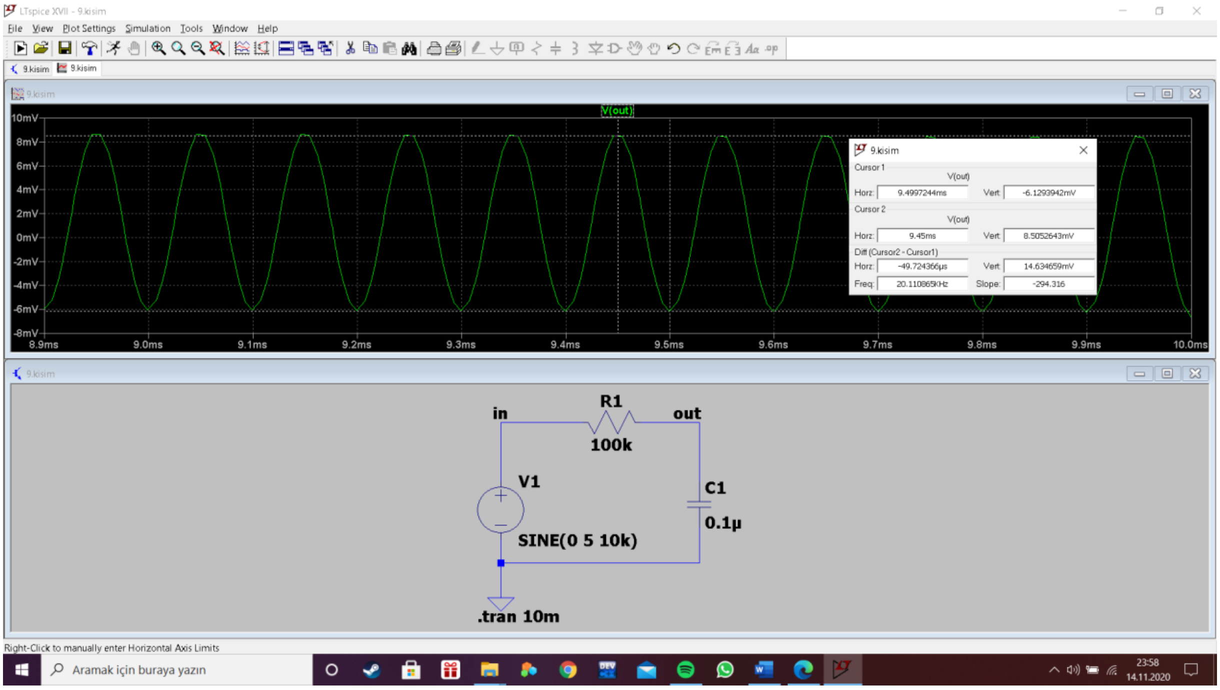
To sum up in this experiment, we learnt parameters that describe time-varying signals, what is the peak amplitude(V_{peak}), peak-to-peak amplitude(V_{p-p}), period, delay time and phase. We learnt how we calculate them. Then we learnt pulse waveform parameters, what is the T_{on} and T_{off} , we learnt how we calculate duty cycle using them. We learnt what is the falling edge and rising edge and how we measure T_{rise} and T_{fall}. We become familiar with measurement of time-varying signal parameters.

Answers

Q1. Describe the variations in v_{out} amplitude and phase as a function of R1 when the v_{in} frequency is 10 kHz in step-2 of the experiment. Predict the v_{out} amplitude and phase that will be obtained at 10 kHz when R1 is 100 kΩ.
We can get estimate value for this equation:

$$Vout = \frac{1.44}{\mathrm{R1}}$$

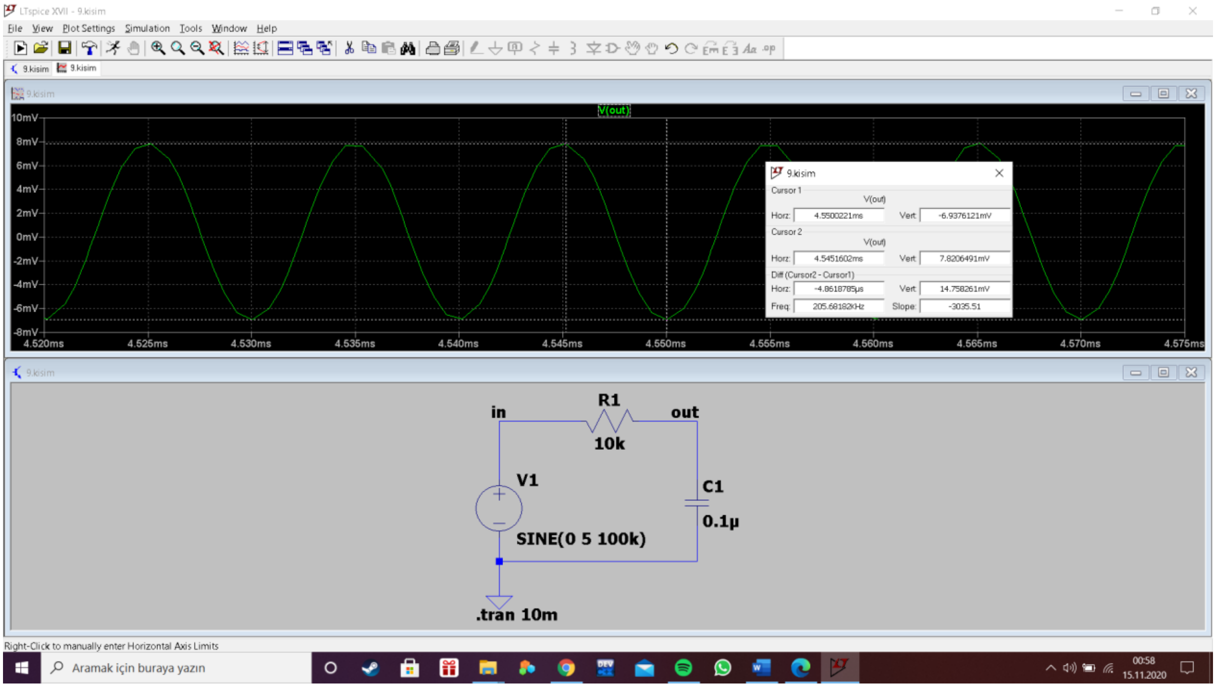
And using this equation for R1 is 100 kΩ,
our expected v_{out} amplitude(**$V_{p\text{-}p}$**)=1.44/100=0.0144V



Our calculated v_{out} amplitude=0.01463V and
our expected v_{out} amplitude=0.0144V so our percentage error is just 1.6.

About phase, we can see at frequency constant, when resistor increasing phase increasing but when resistor increasing rate increase, phase increasing rate decreasing(because of that we can say it will be logarithmic function according to resistance value). Thus, for for R1 is 100 KΩ, we can expect phase increasing but not so much so it will be bigger than 92.52 and when we calculate we see phase is 93.62 so our expectation is true.

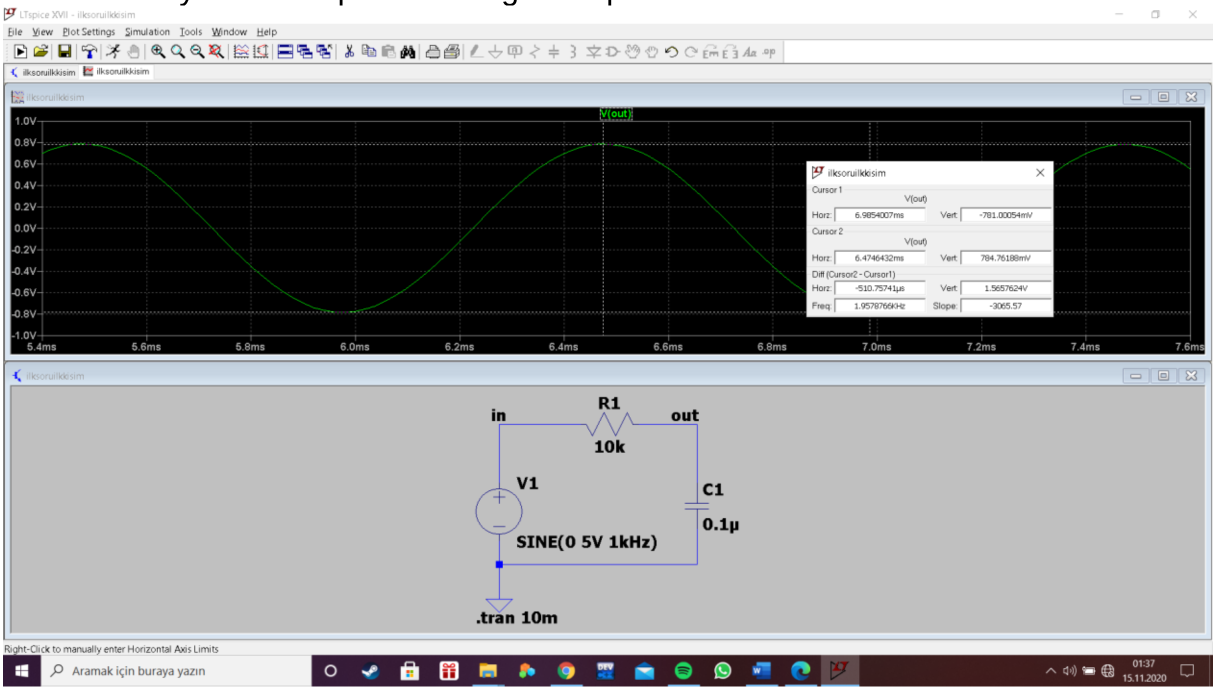
Q2. Describe the variations in vout amplitude and phase as a function of vin frequency when R1 is 10 kΩ in step-2 of the experiment. Predict the vout amplitude and phase that will be obtained at 100 kHz when R1 is 10 kΩ.
We can say, V_{out} amplitude($\mathbf{V_{p\text{-}p}}$)= 1.57/V_{in} frequency so our expected $V_{out\ at}$ 100 kHz is 0.0157V.



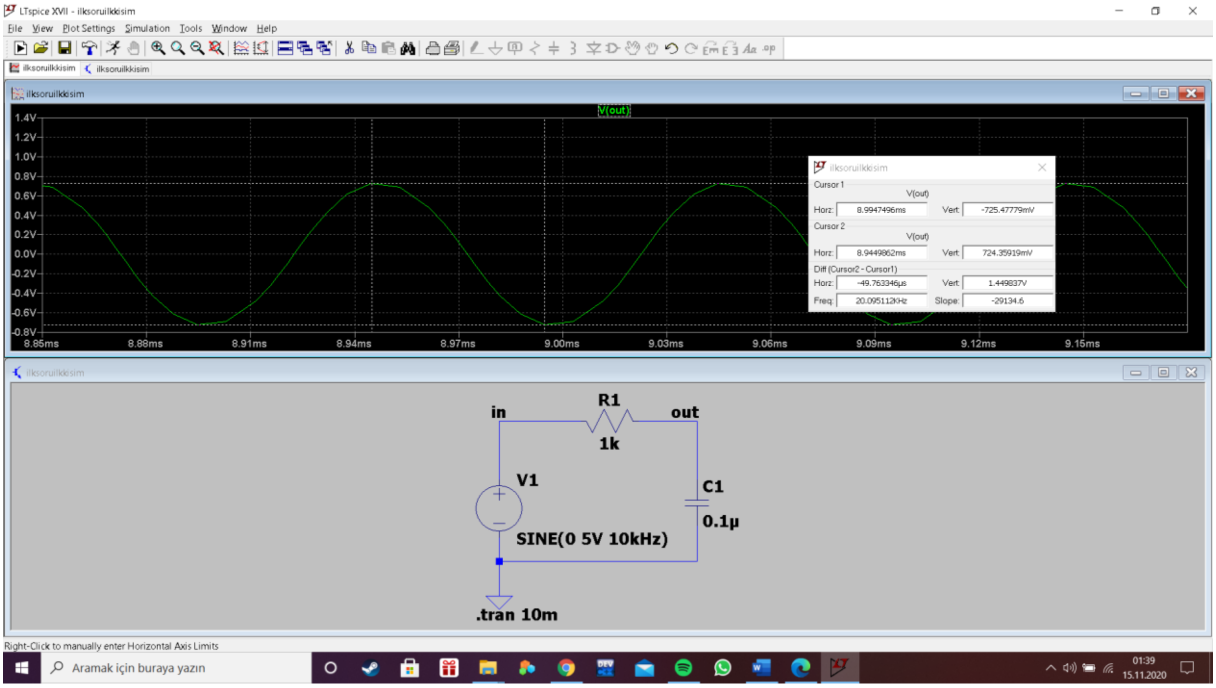
Our calculated V_{out} amplitude=0.0146V and
our expected V_{out} amplitude=0.015V so our percentage error is just 2.6.

About phase, we can see at resistance constant, when frequeny increasing phase increasing but when frequeny increasing rate increase, phase increasing rate decreasing(because of that we can say it will be logarithmic function according to frequeny value). Thus, for for frequeny is 100 kHz, we can expect phase increasing but not so much so it will be bigger than 92.52 and when we calculate we see phase is 93.64 so our expectation is true.

Q3. Compare the **V_{out}** amplitude and phase obtained in step-2 of the experiment for the couple of settings given below.
setting 1: V_{in} frequency = **1 kHz**, **R1 = 10 kΩ**
setting 2: V_{in} frequency = **10 kHz, R1 = 1 kΩ**
Are there any other couple of settings that produced similar results?



setting 1: V_{in} frequency = **1 kHz**, **R1 = 10 kΩ,** V_{out} amplitude(**$V_{p\text{-}p}$**)=1.56V



setting 2: V_{in} frequency = **10 kHz, R1 = 1 kΩ** , V_{out} amplitude(**$V_{p\text{-}p}$**)=1.45V

For example if we use **V_{in}** frequency = **100 Hz, R1 = 100 kΩ** , our V_{out} amplitude(**$V_{p\text{-}p}$**) will be 1.75V or **V_{in}** frequency = **100k Hz, R1 = 100Ω** , our V_{out} amplitude(**$V_{p\text{-}p}$**) will be 1.44V. We can see when we multiply a constant one of them, if we divided by other of them with same constant we will calculate close results.

Q4. Verify that the voltage measurements recorded in step 2.2 and 2.3 are in accordance with the Kirchhoff's Voltage Law. Explain any discrepancies.

Time of measurement	**V_{in}(V)**	**V_{out}(V)**	**V_{in}(V)- V_{out}(V)**
right after **V_{in}** rising edge	5V	58mV	4.941V
middle of **V_{in}** ON **(5V)** cycle	5V	4.59V	409mV
right before vin falling edge	5V	4.96V	0.4V
right after **V_{in}** falling edge	0V	4.94V	-4.94V
middle of **V_{in}** OFF (0V) cycle	0V	414.50mV	-414.50mV
right before **V_{in}** rising edge	0V	33.96mV	-33.96mV

Table 2.2

Time of measurement	**V_{in}(V)**	**V_{out}(V)**	**V_{in}(V)- V_{out}(V)**
right after **V_{in}** rising edge	5V	1.95V	3.05V
middle of **V_{in}** ON **(5V)** cycle	5V	2.625V	2.375V
right before vin falling edge	5V	3.15V	1.85V
right after **V_{in}** falling edge	0V	3.144V	-3.144V
middle of **V_{in}** OFF (0V) cycle	0V	2.475V	-2.475V
right before **V_{in}** rising edge	0V	1.94V	-1.94V

Table 2.3

Kirchhoff's Voltage Law states that for a closed loop series path the algebraic sum of all the voltages around any closed loop in a circuit is equal to zero. When we look at at the circuit, we saw 3 voltage: V_{in},$V_{out}V_r$. V_r is equal to V_{in}-V_{out} and because of ..To verify rule, this equation must be true V_{in}= V_{in}-$V_{out.}$+V_{out} and when we look at the table we can see this condition is true, some of rows we can see %0.01 error this is about decimal rounding while doing calculation.

Q5. In a practical laboratory environment, V1 voltage source will be a signal generator. What happens if you try to monitor the voltage across R_1 by using a single oscilloscope probe as shown below? Why?

If we do that, we will measure Voltage on resistor on the other words, we will measure V_{in}-V_{out} .When we measure normally, we touch voltage source with one part of probe and we touch ground with other part of probe and we know ground is 0V but in this situation it will have voltage value.