

國立清華大學 電機工程系
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SOC Design Laboratory

Lab #4-2



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Block diagram

1.1 Datapath

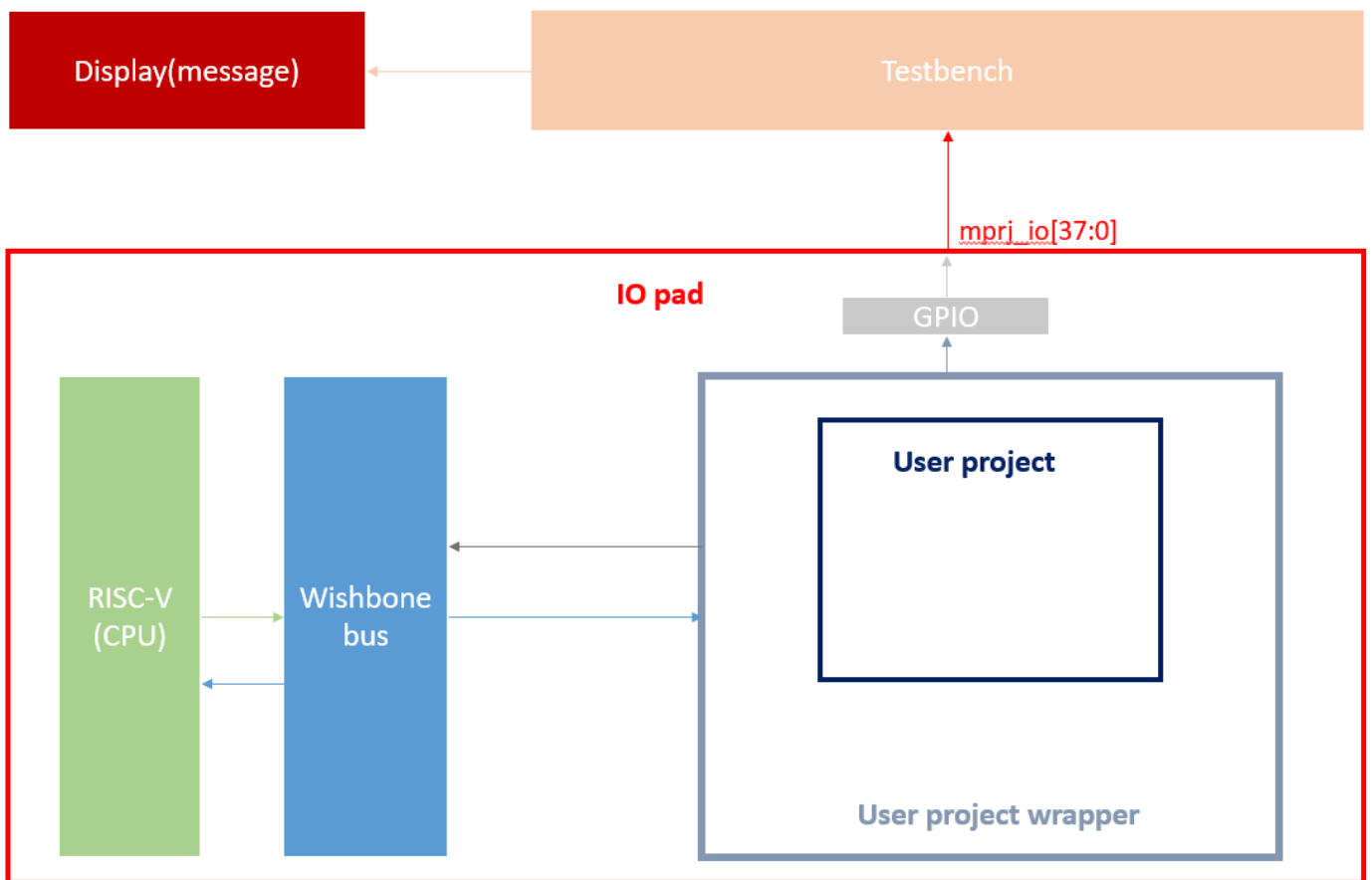


Fig 1. Datapath diagram

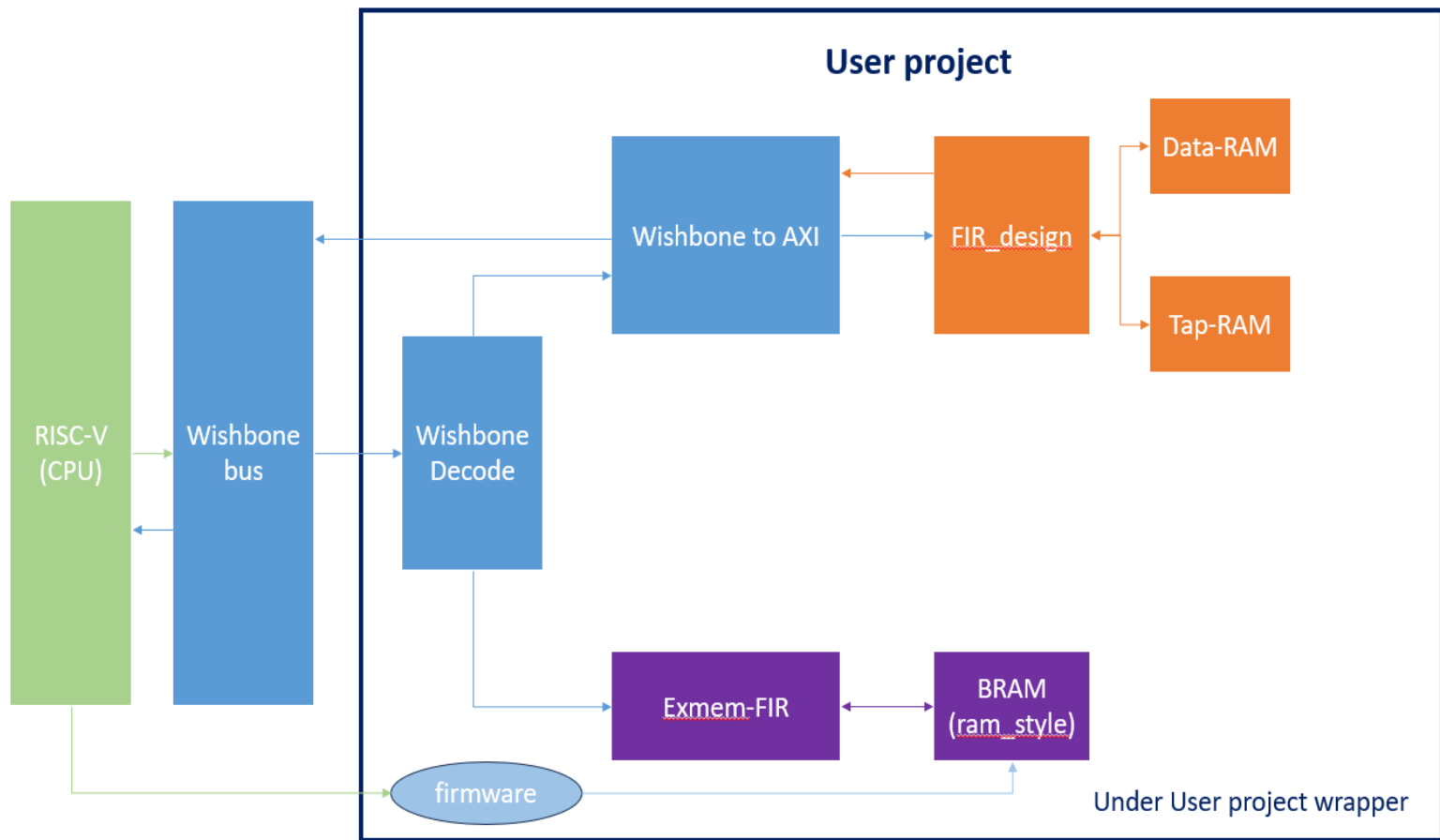


Fig 2. User project block of Datapath diagram

1.2 Controls-path

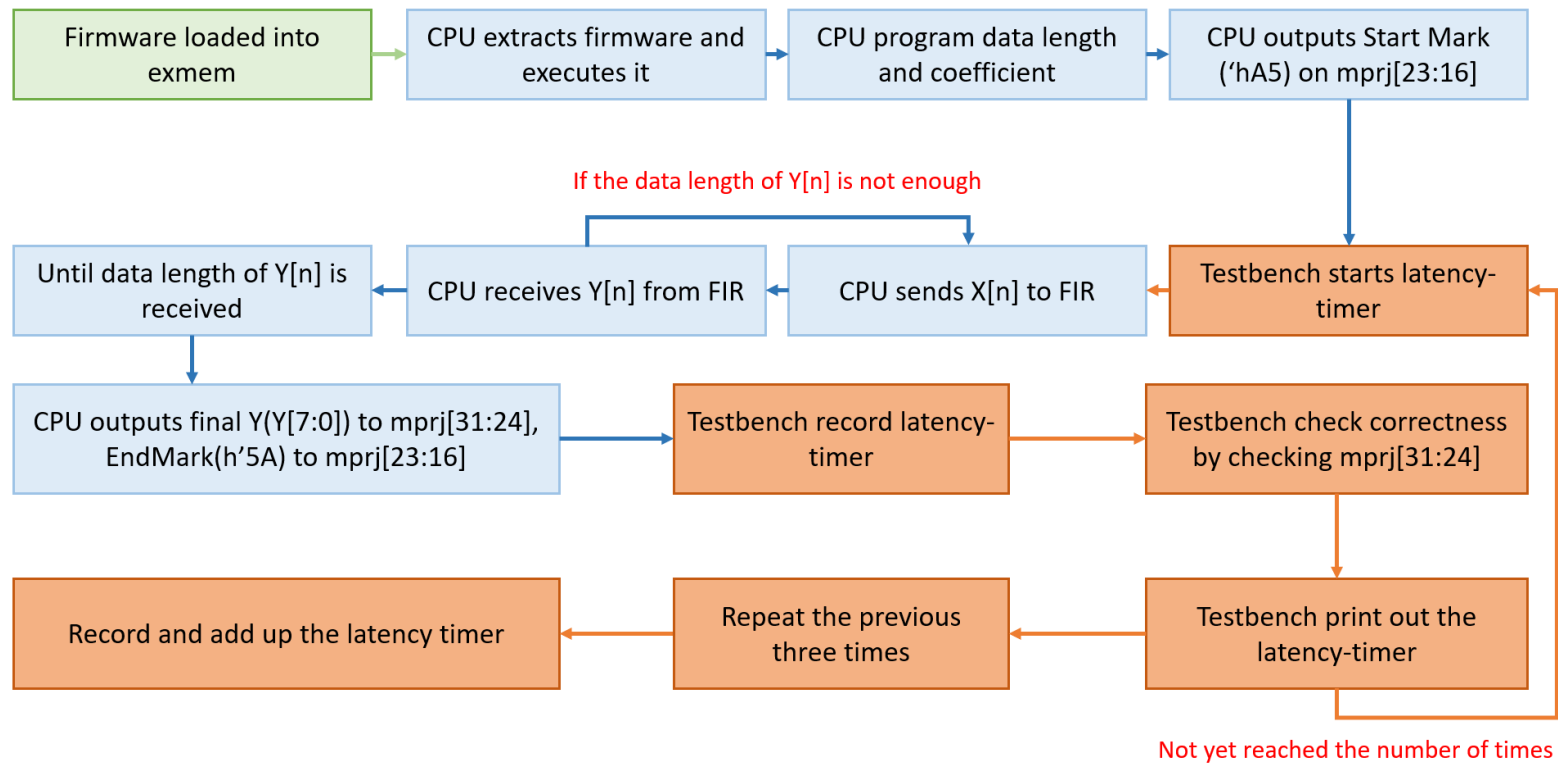


Fig 3. Control-path diagram

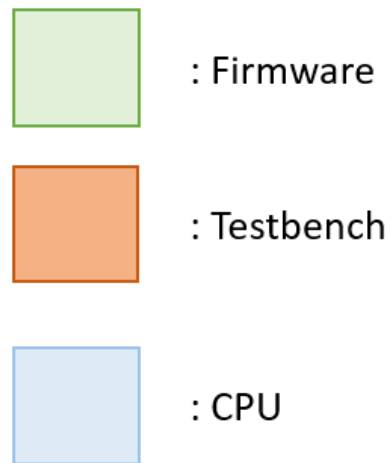


Fig 4. Block representation of Control-path diagram

Description:

First, load the firmware code into BRAM and execute it. Then the CPU will execute the program coefficient and data length according to the firmware code. After the program is completed, mprj[23:16] will output a start mark ('hA5) to notify Testbench to start latency-timer, then the CPU sends $X[n]$ to FIR calculation, and receives $Y[n]$ after calculation. The CPU will then repeatedly send $X[n]$ and receiving $Y[n]$ until data length of $Y[n]$ is

received. when finish, the CPU write final $Y[7:0]$ output to $mprj[31:24]$, and write EndMark('h5A) to $mprj[23:16]$, then record the latency timer, Testbench check correctness by checking $mprj[31:24]$, and print out the latency-timer, and finally repeat three times(The CPU output the start Mark('hA5) on $mprj[23:16]$, sends $x[n]$ to FIR, receives $Y[n]$ from FIR and until the data length of $Y[n]$ is received and write the final $Y[n]$ to $mprj[31:24]$ and output the EndMark('h5A) to $mprj[23:16]$, then check correctness to $mprj[31:24]$), and finally record and add up the latency-timer.

Interface protocol

firmware

```
for(int i=0; i<3; i++){  
    reg_mprj_data1 = 0x00A50000;  
    int* tmp = fir();  
    reg_mprj_data1 = ((*tmp & 0xFF) << 24 | (0x5A << 16));  
}
```

Testbench

```
initial begin  
    // analysis timer  
    // 1 time  
    wait(checkbits[7:0] == 8'hA5);  
    $display("1st: MPRJ-Logic WB started, time at ", $realtime, " ns");  
    wait(checkbits[7:0] == 8'h5A);  
    $display("1st: Mega-Project WB (RTL) passed, time at ", $realtime, " ns");  
    // 2 time  
    wait(checkbits[7:0] == 8'hA5);  
    $display("2nd: MPRJ-Logic WB started, time at ", $realtime, " ns");  
    wait(checkbits[7:0] == 8'h5A);  
    $display("2nd: Mega-Project WB (RTL) passed, time at ", $realtime, " ns");  
    // 3 time  
    wait(checkbits[7:0] == 8'hA5);  
    $display("3rd: MPRJ-Logic WB started, time at ", $realtime, " ns");  
    wait(checkbits[7:0] == 8'h5A);  
    $display("3rd: Mega-Project WB (RTL) passed, time at ", $realtime, " ns");  
    #10000;  
    $finish;  
end
```

Fig 5. Interface between firmware and Testbench

firmware

```
reg_mprj_coeff_0 = 1;
reg_mprj_coeff_1 = -10;
reg_mprj_coeff_2 = -9;
reg_mprj_coeff_3 = 23;
reg_mprj_coeff_4 = 56;
reg_mprj_coeff_5 = 63;
reg_mprj_coeff_6 = 56;
reg_mprj_coeff_7 = 23;
reg_mprj_coeff_8 = -9;
reg_mprj_coeff_9 = -10;
reg_mprj_coeff_10 = 0;
```

```
reg_mprj_control = 1;
```

```
reg_mprj_x = i+1;
```

```
outputsignal[i] = reg_mprj_y;
```

Firmware define mmio

```
#define reg_mprj_control (*(volatile uint32_t*)0x30000000)
#define reg_mprj_datlen (*(volatile uint32_t*)0x30000010)
#define reg_mprj_coeff_0 (*(volatile uint32_t*)0x30000040)
#define reg_mprj_coeff_1 (*(volatile uint32_t*)0x30000044)
#define reg_mprj_coeff_2 (*(volatile uint32_t*)0x30000048)
#define reg_mprj_coeff_3 (*(volatile uint32_t*)0x3000004C)
#define reg_mprj_coeff_4 (*(volatile uint32_t*)0x30000050)
#define reg_mprj_coeff_5 (*(volatile uint32_t*)0x30000054)
#define reg_mprj_coeff_6 (*(volatile uint32_t*)0x30000058)
#define reg_mprj_coeff_7 (*(volatile uint32_t*)0x3000005C)
#define reg_mprj_coeff_8 (*(volatile uint32_t*)0x30000060)
#define reg_mprj_coeff_9 (*(volatile uint32_t*)0x30000064)
#define reg_mprj_coeff_10 (*(volatile uint32_t*)0x30000068)
#define reg_mprj_x (*(volatile uint32_t*)0x30000080)
#define reg_mprj_y (*(volatile uint32_t*)0x30000084)
```

User_project

```
// wb_axi
wb_axi wb_axi(
    .wb_clk_i(wb_clk_i),
    .wb_rst_i(wb_rst_i),
    .wbs_cyc_i(wbs_cyc_i_wbaxi),
    .wbs_stb_i(wbs_stb_i),
    .wbs_we_i(wbs_we_i),
    .wbs_sel_i(wbs_sel_i),
    .wbs_adr_i(wbs_adr_i),
    .wbs_dat_i(wbs_dat_i),
    .wbs_ack_o(wbs_ack_o_wbaxi),
    .wbs_dat_o(wbs_dat_o_wbaxi)
);
```

Fig 6. Interface between firmware and User_project

Waveform

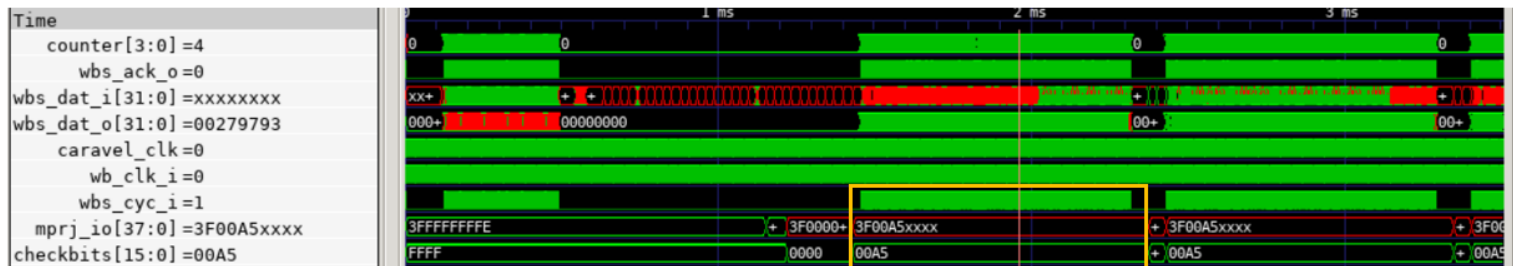


Fig 7. CPU interaction with Wishbone and mprj_io

Description:

From the yellow box in Fig 7, you can see that when the CPU sends a request to the user project through wishbone, the wbs_cyc_i will be pulled to 1, and then wb_decode in the user project will determine whether wbs_cyc_i is to be given to exmem or FIR, and then the hardware that receives the signal will start executing the behavior. Before executing the behavior, the CPU will

first outputs a start mark('hA5) on mprj[23:16] to tell testbench to perform, so you can see the Start mark ('hA5) output by mprj[23:16] from Fig 7, and then the check bit is used by testbench to check whether the mprj output is correct.



Questions

What is the FIR engine theoretical throughput?

Description:

It takes 11 cycles to complete a FIR operation, and a total of 64 data are continuously sent to the FIR operation, so it is $11 \times 1 + 63 = 74$ cycles.

Throughput = $\frac{1}{74}$

What is latency for firmware to feed data?

```
1st: MPRJ-Logic WB started, time at 1429912.500 ns
1st: Mega-Project WB (RTL) passed, time at 2373012.500 ns
2nd: MPRJ-Logic WB started, time at 2430912.500 ns
2nd: Mega-Project WB (RTL) passed, time at 3347512.500 ns
3rd: MPRJ-Logic WB started, time at 3405412.500 ns
3rd: Mega-Project WB (RTL) passed, time at 4322012.500 ns
```

Fig 8. Show message in display

Description:

$$\text{Latency} = 2373012.500 - 1429912.500 = 943100(\text{ns})$$

\therefore 1ns per cycle, so it is 943100 cycles.

What techniques used to improve the throughput?

- Does bram12 give better performance? In what way?

Description:

Yes, we can put data in one more location to reduce the number of reads and writes, but it will increase the area.

- Can you suggest other method to improve the performance?

Description:

Use circuit techniques such as unfolding, pipelines to increase throughput and performance.

GitHub

https://github.com/ken01235/SOC_Design/tree/master/course-lab_4-2%20report

