SOC lab3

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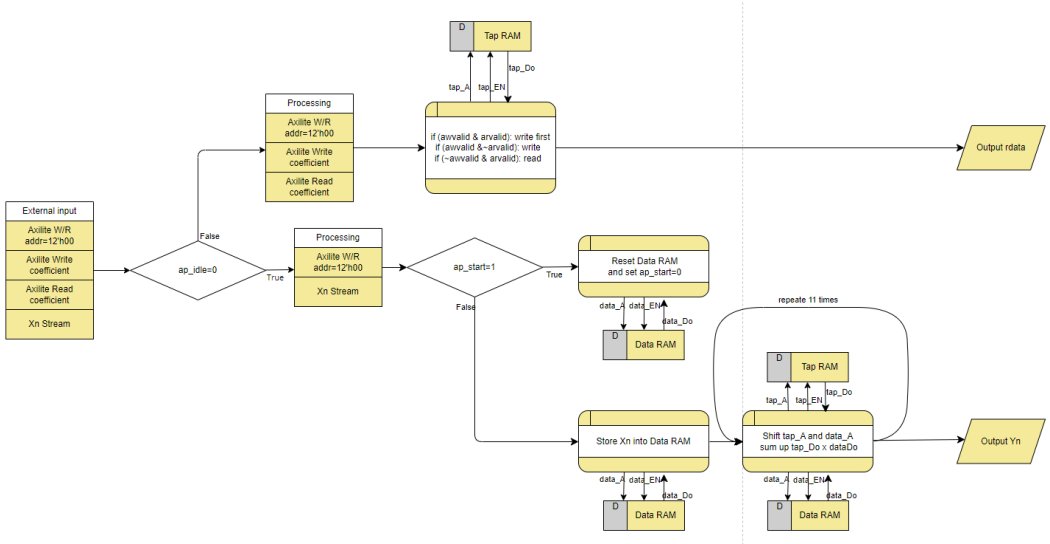
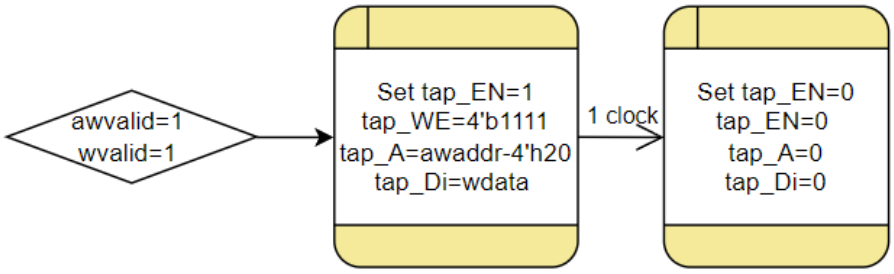
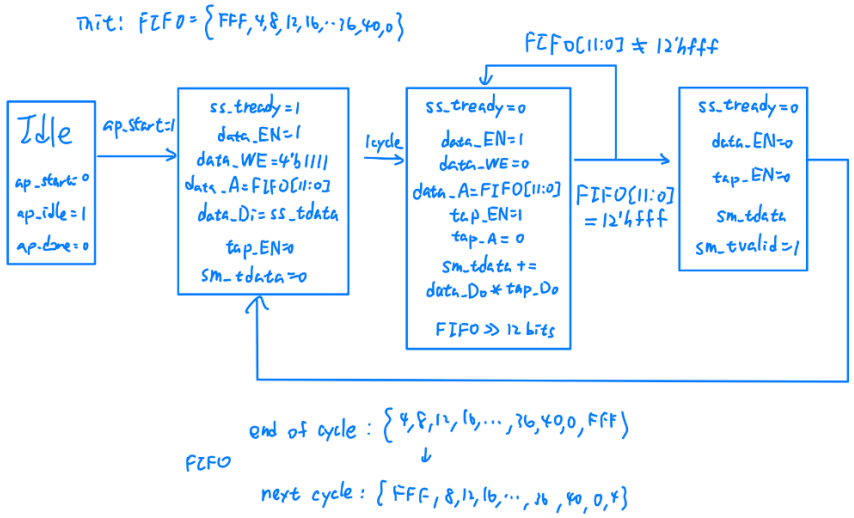
1. Block Diagram



2. Describe operation
   - ShiftRAM: can only be write before ap_start turn on.



   - TapRAM: can only be write after ap_start turn on. And there is a FIFO to store the address of DataRAM.



   - ap_done is generated when ss_tlast = 1 & sm_tvalid = 1

3. Simulation report

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Time resolution is 1 ps
------------Start simulation-----------
----Start the data input(AXI-Stream)----
----Start the coefficient input(AXI-lite)----
 Check Coefficient ...
OK: exp =           0, rdata =           0
OK: exp =         -10, rdata =         -10
OK: exp =          -9, rdata =          -9
OK: exp =          23, rdata =          23
OK: exp =          56, rdata =          56
OK: exp =          63, rdata =          63
OK: exp =          56, rdata =          56
OK: exp =          23, rdata =          23
OK: exp =          -9, rdata =          -9
OK: exp =         -10, rdata =         -10
OK: exp =           0, rdata =           0
 Tape programming done ...
 Start FIR
----End the coefficient input(AXI-lite)----
[PASS] [Pattern          0] Golden answer:           0, Your answer:           0
[PASS] [Pattern          1] Golden answer:         -10, Your answer:         -10
[PASS] [Pattern          2] Golden answer:         -29, Your answer:         -29
[PASS] [Pattern          3] Golden answer:         -25, Your answer:         -25
[PASS] [Pattern          4] Golden answer:          35, Your answer:          35
[PASS] [Pattern          5] Golden answer:         158, Your answer:         158
[PASS] [Pattern          6] Golden answer:         337, Your answer:         337
[PASS] [Pattern          7] Golden answer:         539, Your answer:         539
[PASS] [Pattern          8] Golden answer:         732, Your answer:         732
[PASS] [Pattern          9] Golden answer:         915, Your answer:         915
[PASS] [Pattern         10] Golden answer:        1098, Your answer:        1098
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[PASS] [Pattern        580] Golden answer:       -4392, Your answer:       -4392
[PASS] [Pattern        581] Golden answer:       -4209, Your answer:       -4209
[PASS] [Pattern        582] Golden answer:       -4026, Your answer:       -4026
[PASS] [Pattern        583] Golden answer:       -3843, Your answer:       -3843
[PASS] [Pattern        584] Golden answer:       -3660, Your answer:       -3660
[PASS] [Pattern        585] Golden answer:       -3477, Your answer:       -3477
[PASS] [Pattern        586] Golden answer:       -3294, Your answer:       -3294
[PASS] [Pattern        587] Golden answer:       -3111, Your answer:       -3111
[PASS] [Pattern        588] Golden answer:       -2928, Your answer:       -2928
[PASS] [Pattern        589] Golden answer:       -2745, Your answer:       -2745
[PASS] [Pattern        590] Golden answer:       -2562, Your answer:       -2562
[PASS] [Pattern        591] Golden answer:       -2379, Your answer:       -2379
[PASS] [Pattern        592] Golden answer:       -2196, Your answer:       -2196
[PASS] [Pattern        593] Golden answer:       -2013, Your answer:       -2013
[PASS] [Pattern        594] Golden answer:       -1830, Your answer:       -1830
[PASS] [Pattern        595] Golden answer:       -1647, Your answer:       -1647
[PASS] [Pattern        596] Golden answer:       -1464, Your answer:       -1464
[PASS] [Pattern        597] Golden answer:       -1281, Your answer:       -1281
OK: exp =           0, rdata =           0
[PASS] [Pattern        598] Golden answer:       -1098, Your answer:       -1098
------End the data input(AXI-Stream)------
```

4. Resource usage: including FF, LUT, BRAM

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	246	0	0	53200	0.46
LUT as Logic	237	0	0	53200	0.45
LUT as Memory	9	0	0	17400	0.05
LUT as Distributed RAM	0	0			
LUT as Shift Register	9	0			
Slice Registers	232	0	0	106400	0.22
Register as Flip Flop	232	0	0	106400	0.22
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

3. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	3	0	0	220	1.36
DSP48E1 only	3				

5. Timing Report

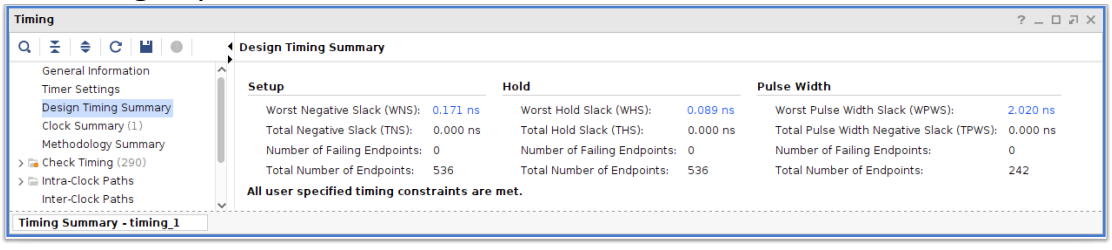

Fig. Design Timing Summary as clock cycle time 6ns

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             0.171ns  (required time - arrival time)
  Source:                 genblk1.FIFO_reg[8]/C
                            (rising edge-triggered cell FDSE clocked by axis_clk  {rise@0.000ns fall@3.000ns period=6.000ns})
  Destination:            genblk1.tap_A_reg[0]/R
                            (rising edge-triggered cell FDRE clocked by axis_clk  {rise@0.000ns fall@3.000ns period=6.000ns})
  Path Group:             axis_clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            6.000ns  (axis_clk rise@6.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        5.092ns  (logic 1.145ns (22.486%)  route 3.947ns (77.514%))
  Logic Levels:           4  (LUT4=1 LUT6=3)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 8.128 - 6.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
```

Fig. Max Delay Paths

6. Simulation Waveform

- # of clock cycles from ap_start to ap_done:
  ap_start: 1.085ps; ap_done: 79.085ps; clock cycle: 6ns
  →13000 clock cycles

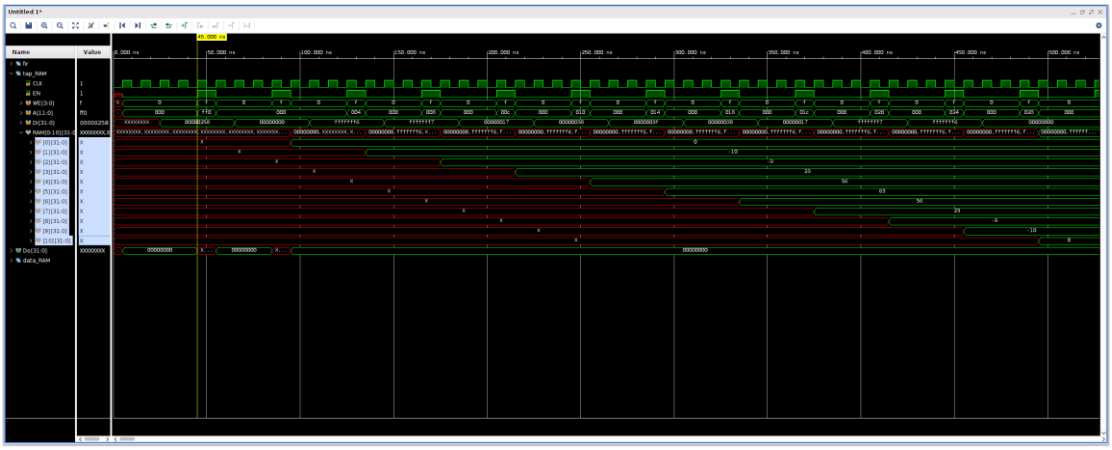

Fig. TapRAM write

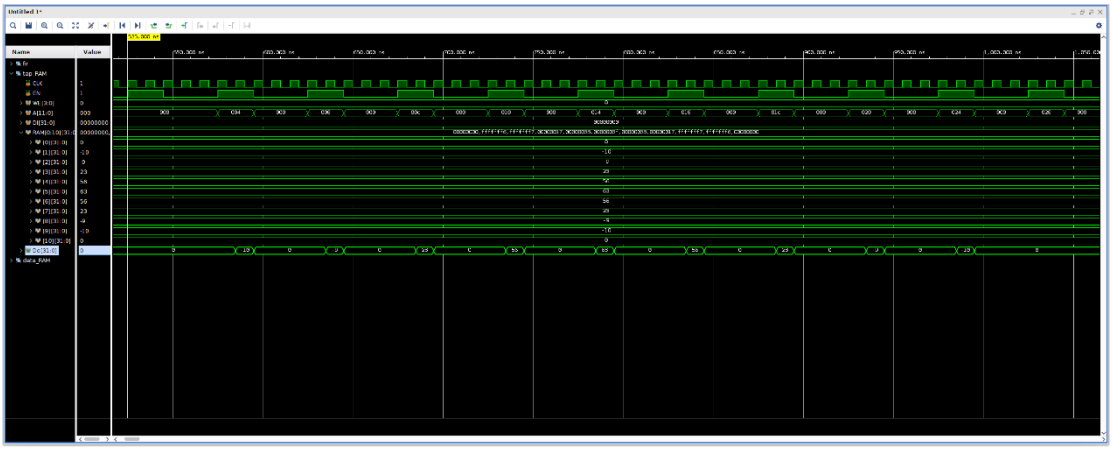

Fig. TapRAM Read

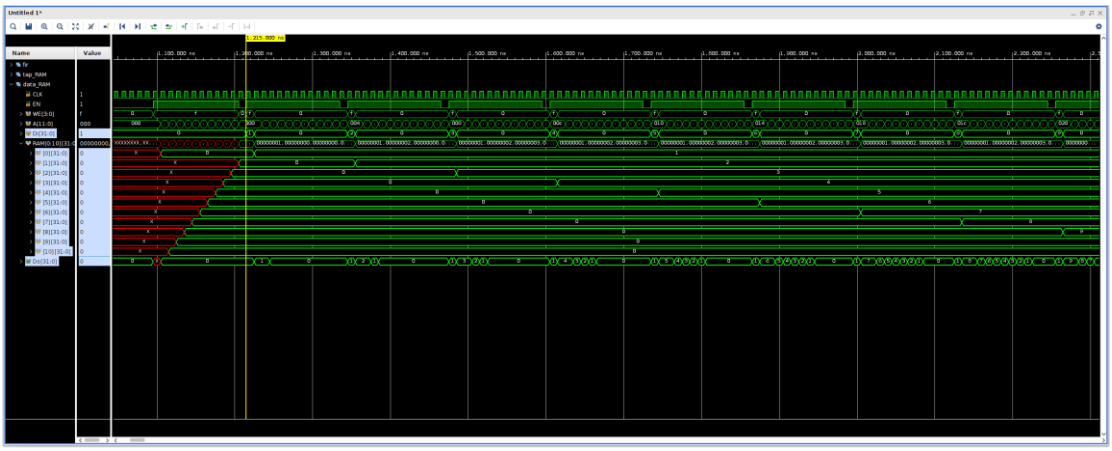

Fig. dataRAM write and read

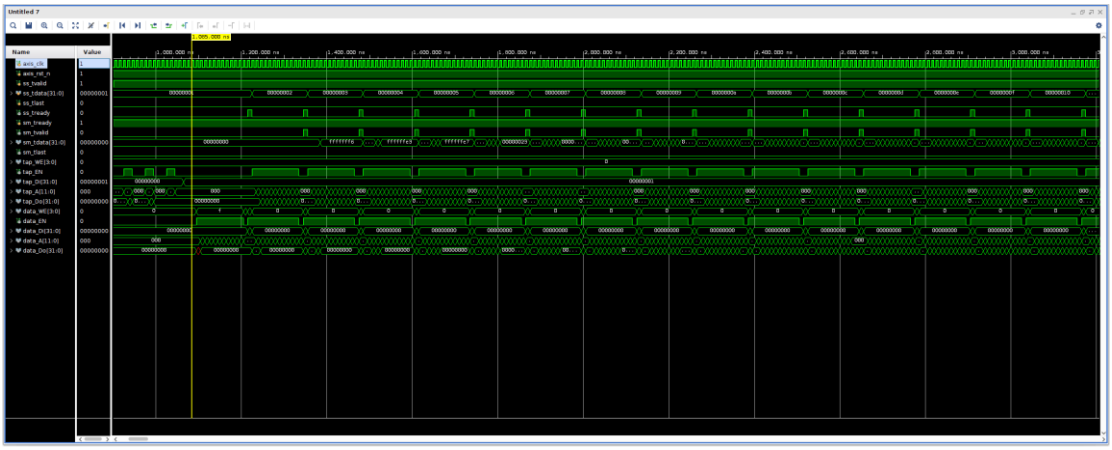

Fig. X_n Stream and Y_n Stream

7. GitHub Link
   https://github.com/ken01235/SOC_Design/tree/master/lab-fir%20report