SOC Design Lab01

112061611 陳伯丞

1.

Lab1 要將 c 語言的程式轉換成 RTL code，再合成到 FPGA 板上執行，所以第一步驟要先確認初始的 c program 的正確性。

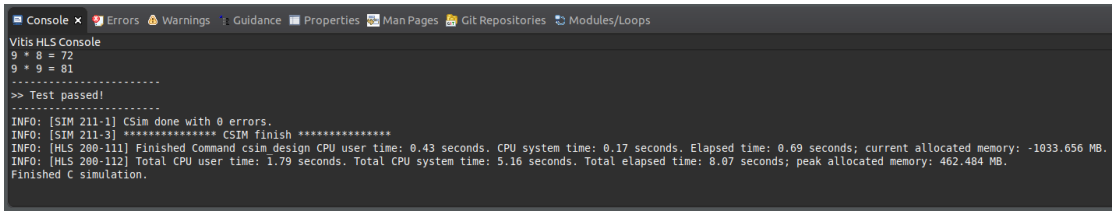

Figure1. C simulation

其次，要將 c program 轉換成 RTL code，並且確認 RTL code 的正確性。

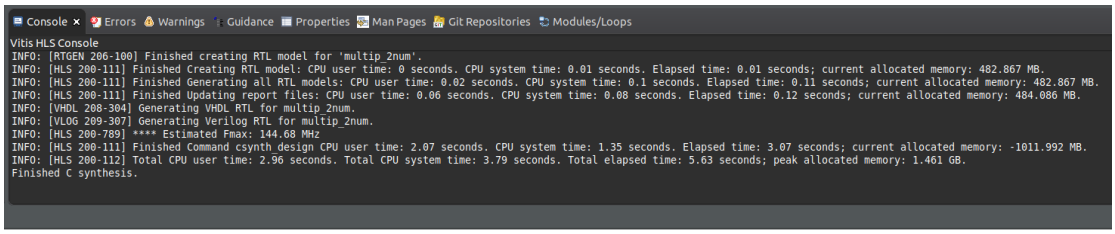

Figure2. C Synthesis

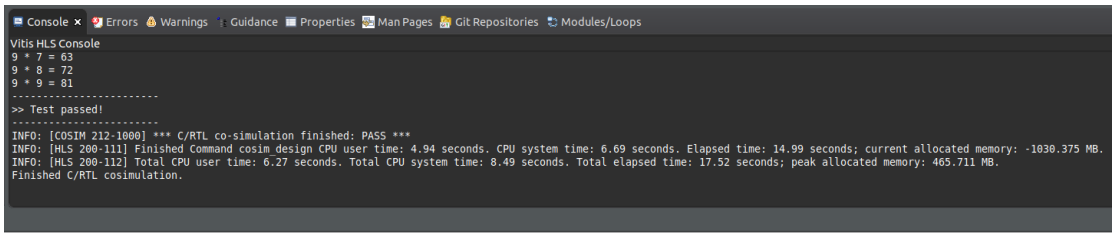

Figure3. RTL Cosimulation

接著將 RTL code 匯出至 Vivado。

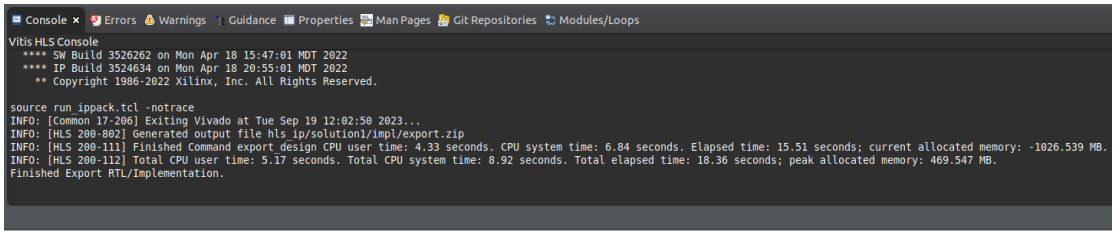

Figure4. Export RTL

在 Vivado 中將先前得到的 RTL code 與 processor 等區塊相接，並且輸出 FPGA 能夠執行的 bit 檔。

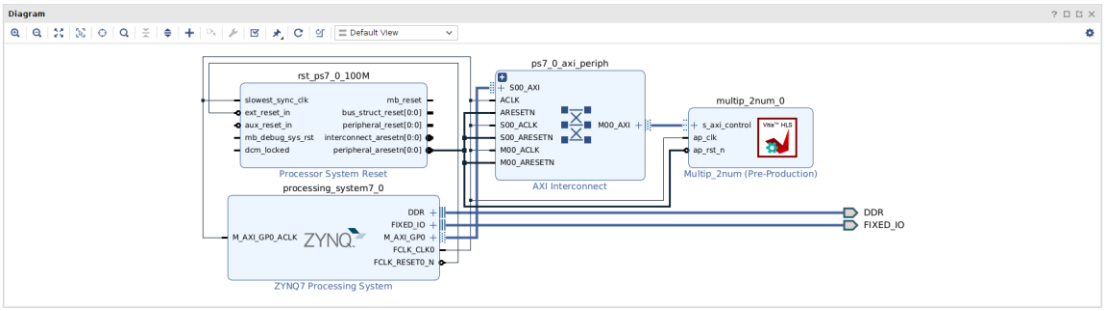

Figure5. Block Diagram

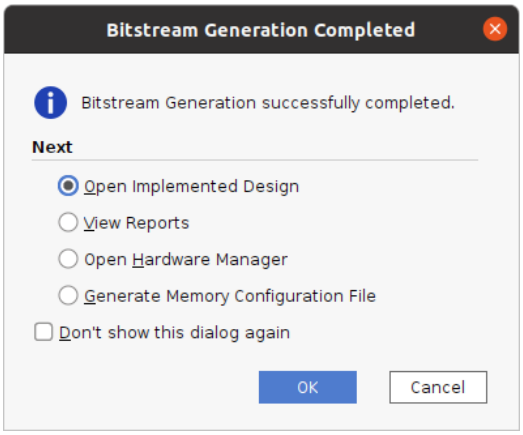

Figure6. Bitstream Generation

最後在 onlineFPGA 上執行，確認執行結果正確。

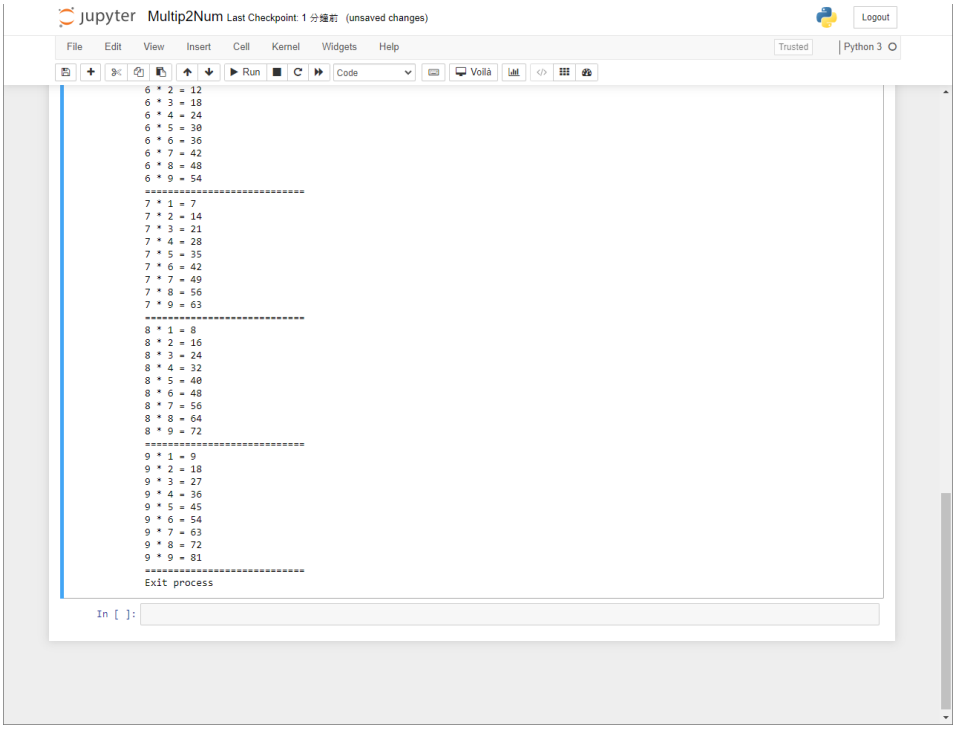

Figure7. OnlineFPGA

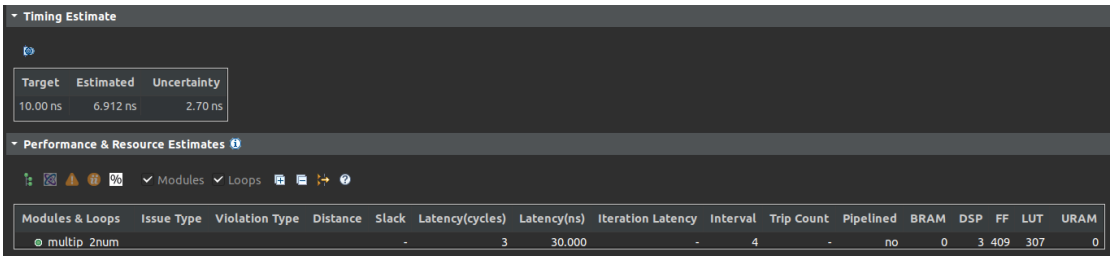

Figure8. Performance

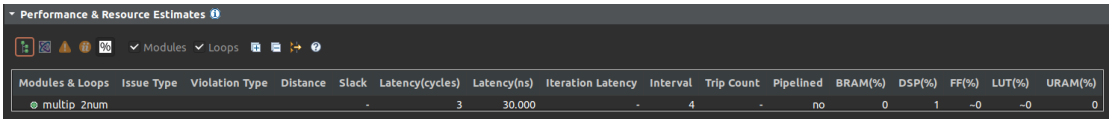

Figure9. Utiliztion

Figure10. Co-simulation Script

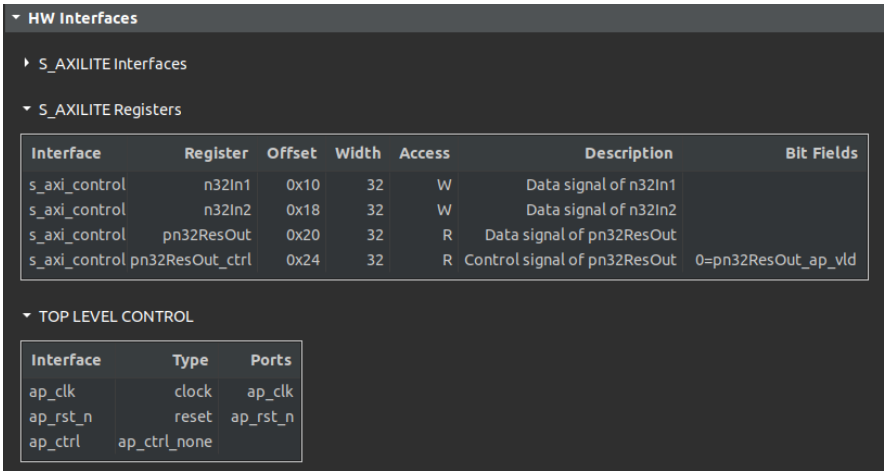

Figure11. Interfaces

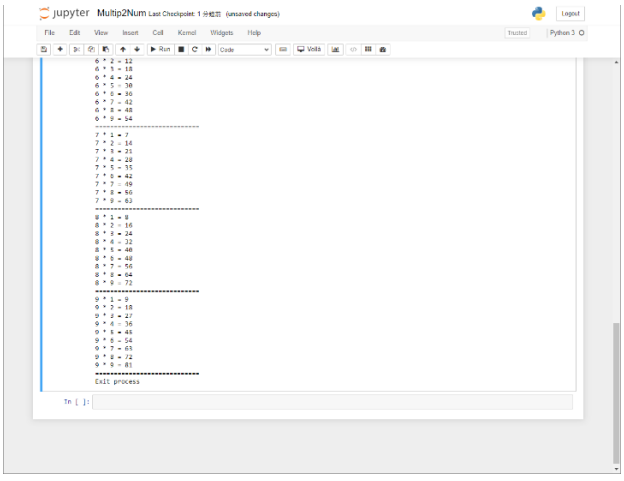

Figure12. Jupyter