Bridge of Life Education

SoC Design

2023-Fall Lecture Outline

Jiin Lai

First Semester – SoC Design

Lecture Schedule

1	**7-Sep**	**Intro**	Course plan / From Gate to HLS
2	**14-Sep**	**HLS**	PYNQ-Lab2 Software Hardware Codesign / HLS Introduction / Kernel IO / Structure Design
3	**21-Sep**	**Verilog**	Verilog and Logic Design
4	**28-Sep**	**-**	No Class
5	**5-Oct**	**Caravel**	Caravel SoC System Introduction
6	**12-Oct**	**Processor**	Computer & Microprocessor Architecture - RISC-V
7	**19-Oct**	**Peripheral**	SoC Peripherals - UART, SPI, I2C, GPIO, UserProject IO, DMA
8	**26-Oct**	**Bus**	SOC Interconnect (Wishbone, AXI, Switch, DMA)
9	**2-Nov**	**Memory**	SOC Memory - Cache/DDR
10	**9-Nov**	**Present**	Caravel SOC Lab Presentation - Lab#4-1, Lab#4-2, Lab#5
11	**16-Nov**		Midterm
12	**23-Nov**	**FW**	Embedded Programming (ISA, Interrupt, Debugging)
13	**30-Nov**	**EDA**	Static Timing Analysis
14	**7-Dec**	**Present**	Caravel SOC Lab Presentation - Lab#A-D, Final Project Proposal
15	**14-Dec**	**EDA**	Synthesis and Optimization
16	**21-Dec**	**EDA**	Verification & Simulation
17	**28-Dec**		Final Project Presentation

Introduction to HLS & SOC

- Course plan
- Lecture plan
- Lab plan
- From Verilog to HLS

HLS

- HLS Introduction (hls-introduction)
- PYNQ / Lab2 Software/Hardware Codesign (pynq-lab2)
- Kernel IO (kernel-io)
- HLS Structure Design (structure-design)

Level of Proficiency in Verilog Design

1. Code matches simulation result (Test-bench + RTL)
2. Pre-synthesis (RTL) matches Post-synthesis (Gate-level)

3. Design Quality (PPA – Power/Performance/Area)
4. System/Application Level Optimization

Verilog Design

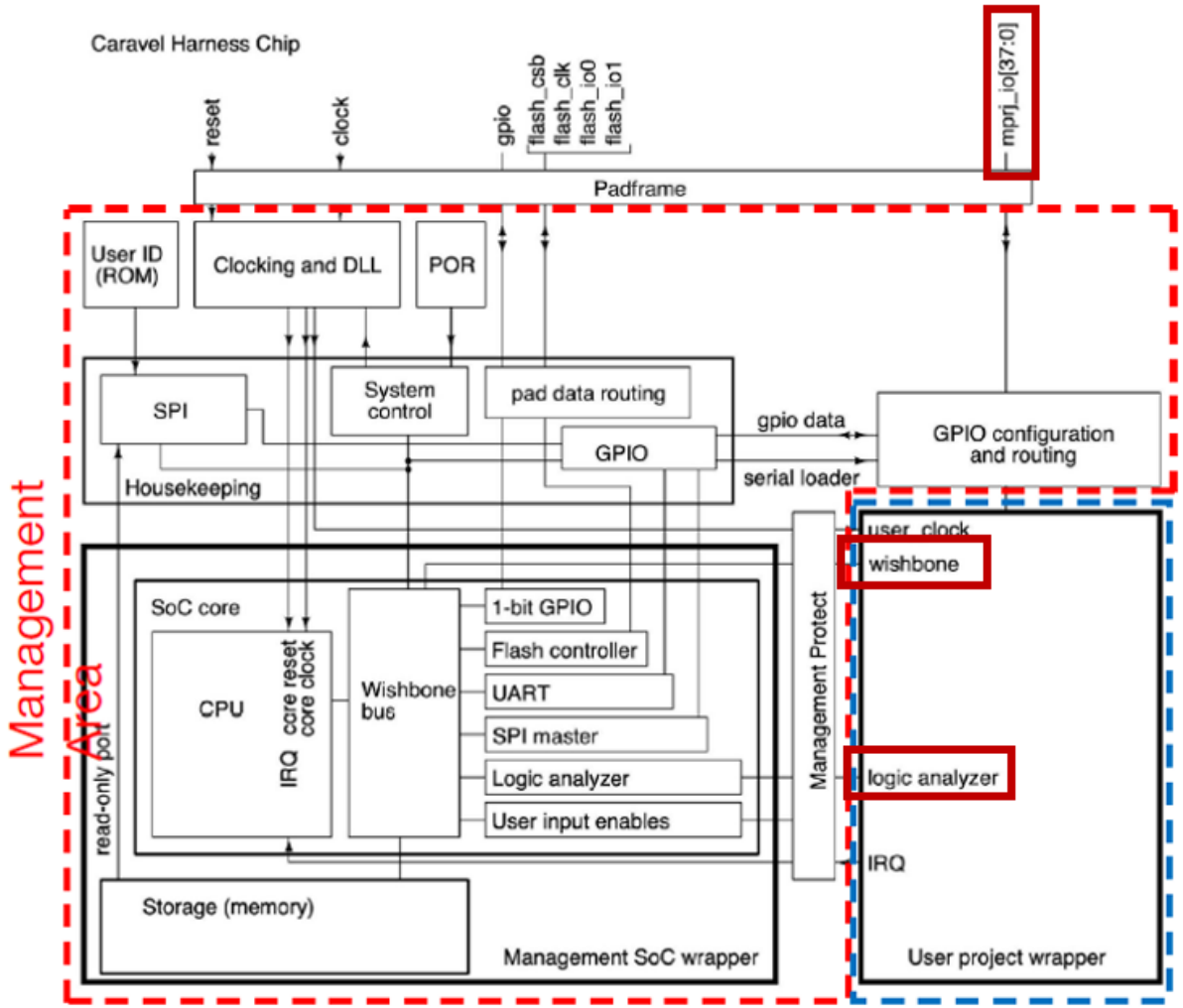
- Combinational / Sequential Circuit (verilog-design)
- FSM Design (verilog-fsm)
- Delay (verilog-delay)
- Critical Concept (verilog-critical-concepts)
  - Scheduling (blocking/nonblocking)
  - Simulation mismatch
  - RTL – Synthesis mismatch
- Design with SRAM (verilog-sram)

Advanced

- Reset (verilog-reset)
  - Synchronous / Asynchronous Reset
- Clock balance, switching, multiple clock (verilog-clock)
- Testbench
- Asynchronous FIFO

Caravel SOC System From Programming Perspective

- System Block Diagram (modules)
- Processor VexRISCV functions & its interface
- Reset / POR
- Management Protect Area – power control
- Clocking / DLL, configuration SPI register
- Housekeeping SPI registers
- GPIO
- SPI
- IRQ
- Memory-mapped IO address
- SRAM – Management area/Storage area
- Bus - Wishbone
- Peripherals – Counter/Timer/UART
- User project design (counter) Interface
- Testbench
- Firmware code



Microprocessor Architecture – RISCV-V

- RISCV ISA
- RISCV Architecture & Design
- Operating System & Processor Support

SOC Peripheral

- Timer/Interrupt/DMA
- GPIO
- Serial Interface – UART, SPI, I2C

SOC Interconnect

- Wishbone
- AXI
- Interconnect (Switch)
- DMA

SOC Memory

- Memory Hierarchy
- Memory Technology
- Cache
- SDRAM
- Memory Application

Embedded Programming

- Tool chains
- Interrupt
- Debugging
- Bit Banging – Software emulated Interface

Static Timing Analysis

- *Basic CMOS Structure and Logic Gate*
- *STA Concepts*
- *Delay Calculation*
- *STA Environment*
- *Timing Check*

Advanced

- *Standard Cell Library*
- *Interconnect Parasitics*
- *Crosstalk and Noise*
- *Interface Analysis*
- *Robust Verification*

Synthesis

- Synthesis on IC Design Flow
- Design Specification
- Coding Style – Simulation and Synthesis Mismatch
- Synthesis Flow
- Describe Design Environment
- Define Design Constrains
- Synthesis & Optimization Techniques
- Compile Strategy

Verification & Simulation

- Verification v.s. Validation v.s. Testing
- Stimulus Generation (Driving)
- Checking

Advanced:

- Coverage
- Formal (Advanced)
- Assertion (Advanced)