SOC Design Lab01

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Lab1要將c語言的程式轉換成RTL code，再合成到FPGA板上執行，所以第一步驟要先確認初始的c program的正確性。

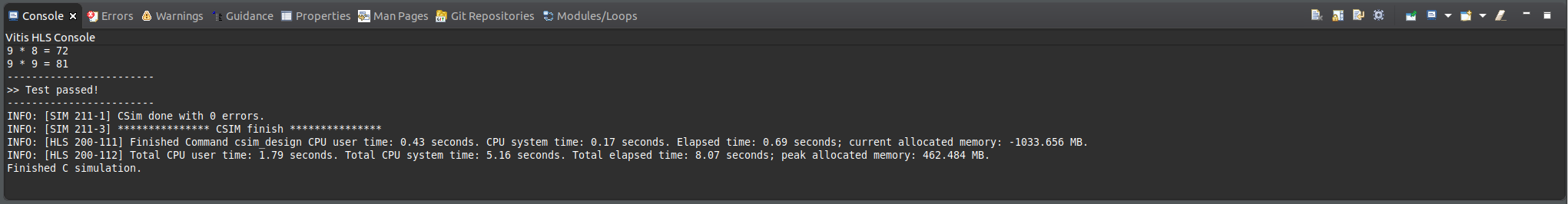


Figure1. C simulation

其次，要將c program轉換成RTL code，並且確認RTL code的正確性。

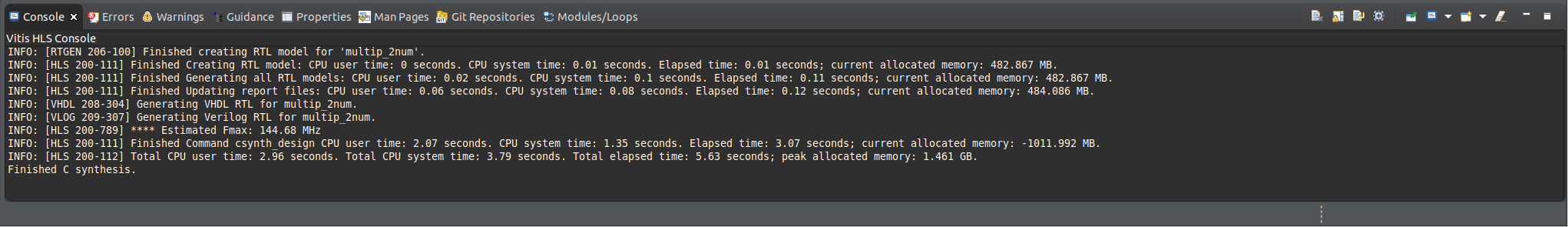


Figure2. C Synthesis

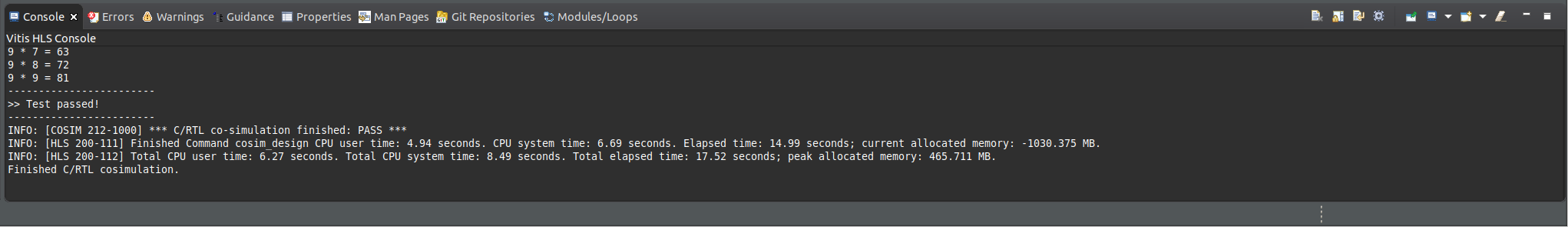


Figure3. RTL Cosimulation

接著將RTL code匯出至Vivado。

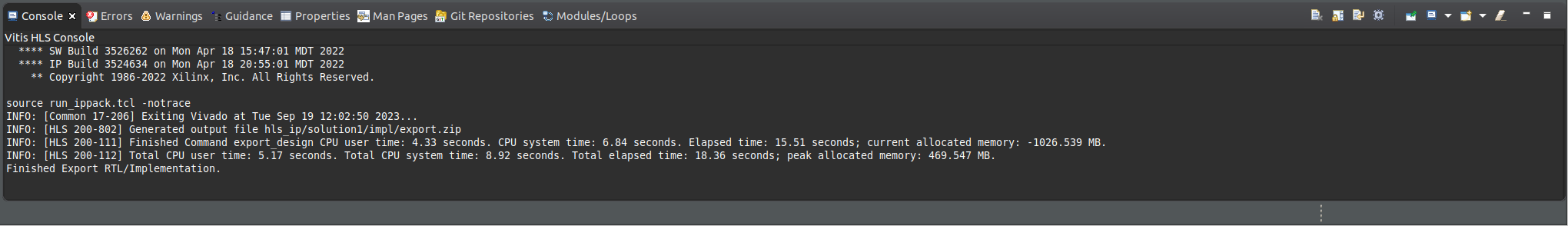


Figure4. Export RTL

在Vivado中將先前得到的RTL code與processor等區塊相接，並且輸出FPGA能夠執行的bit檔。

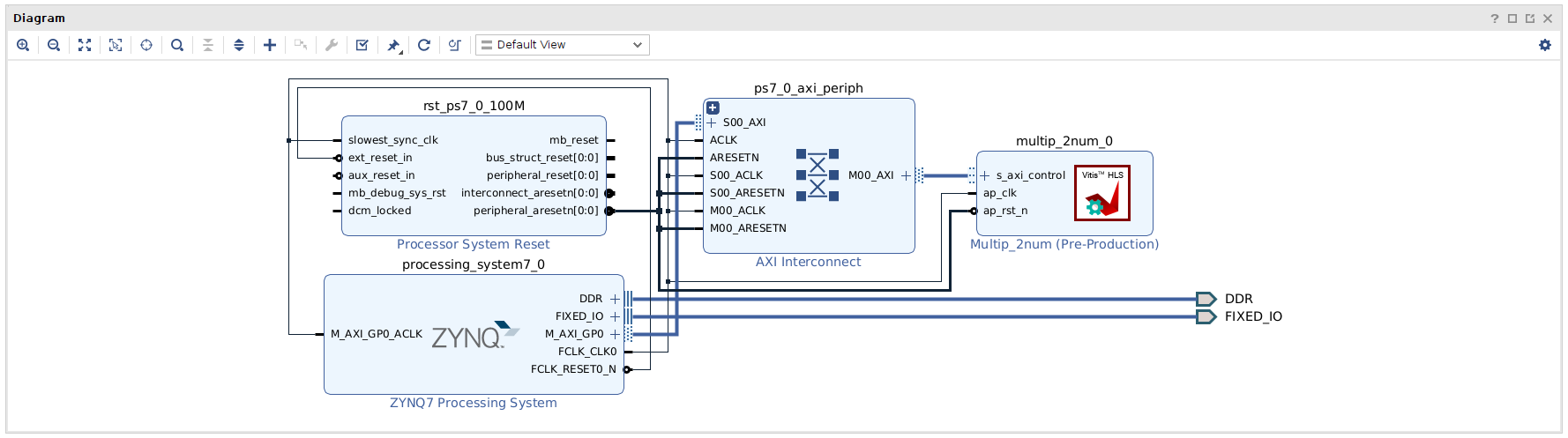


Figure5. Block Diagram

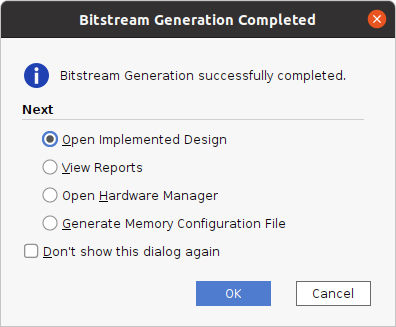


Figure6. Bitstream Generation

最後在onlineFPGA上執行，確認執行結果正確。

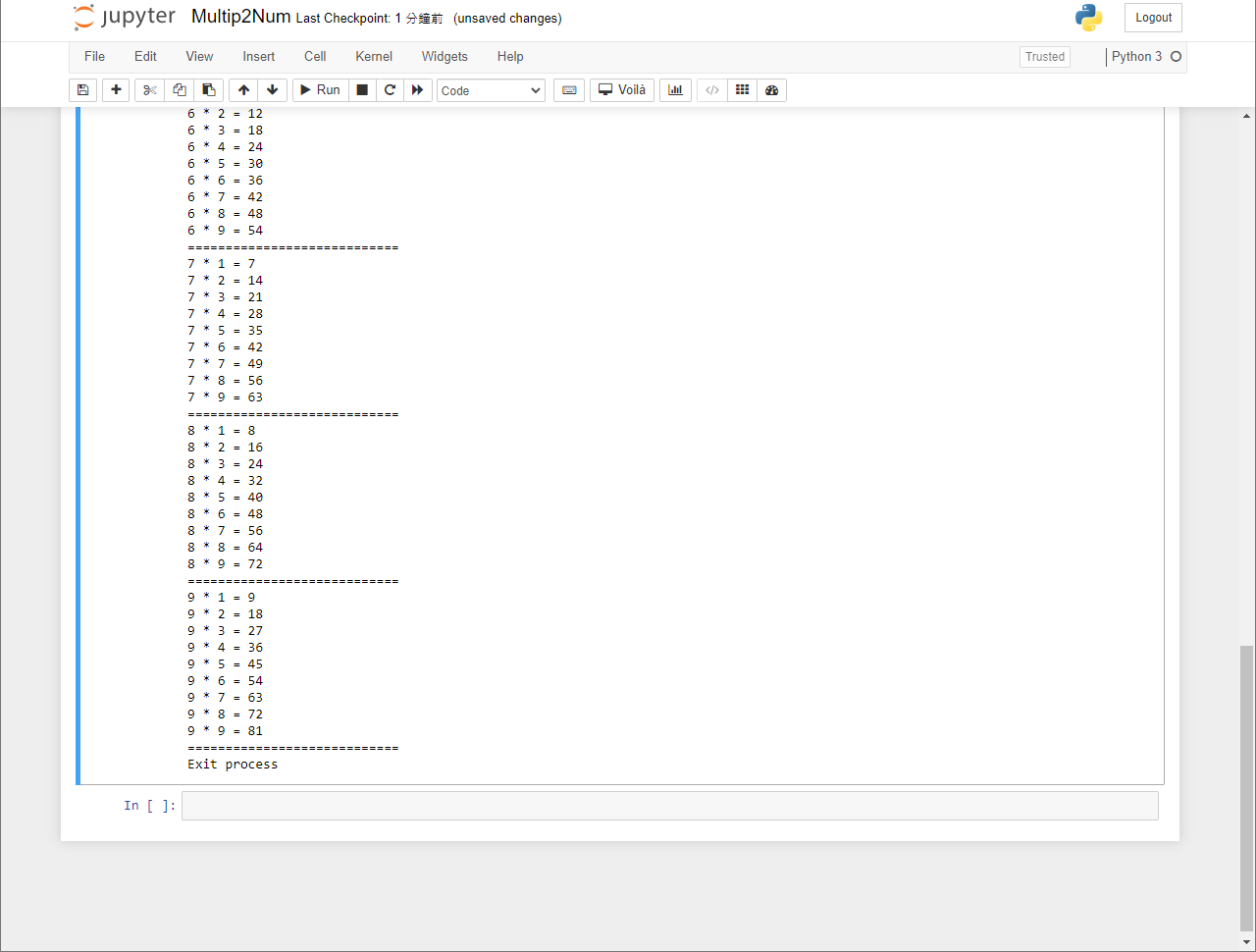


Figure7. OnlineFPGA

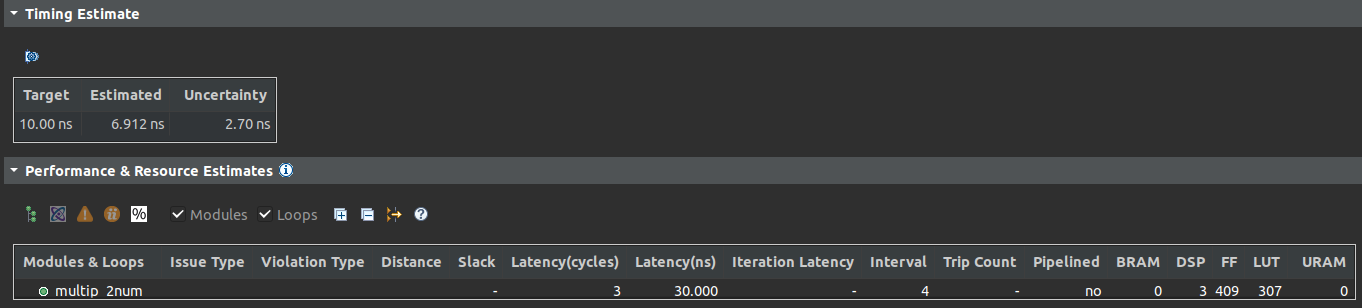


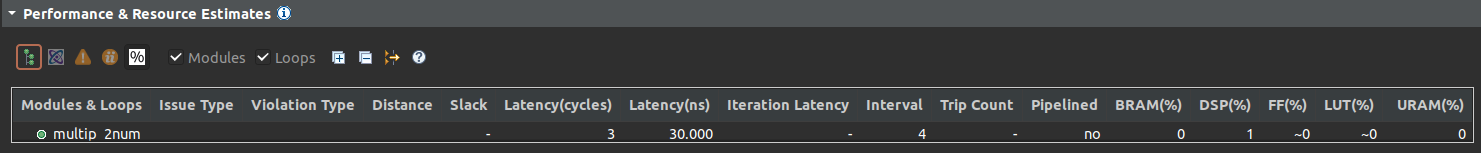
Figure8. Performance

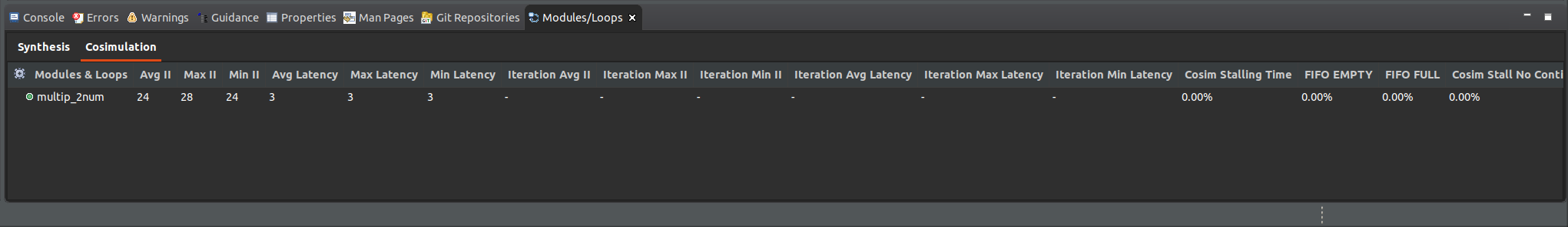
Figure9. Utiliztion

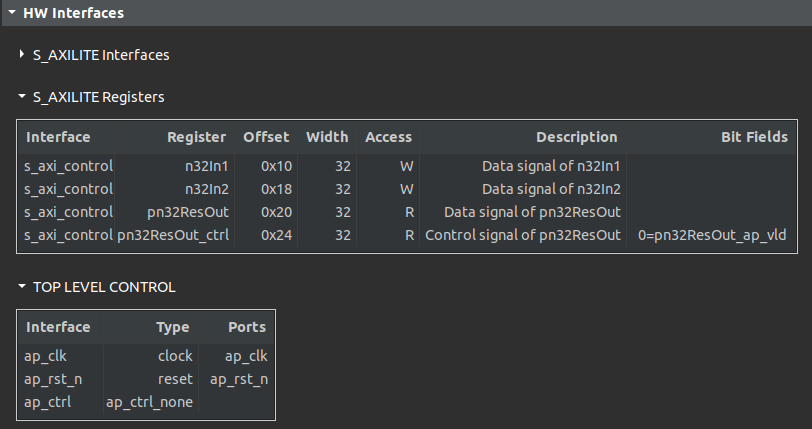
Figure10. Co-simulation Script

Figure11. Interfaces

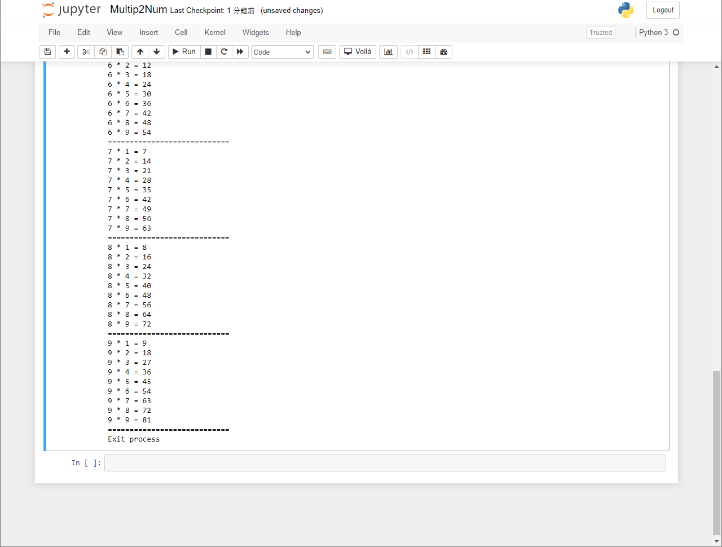


Figure12. Jupyter