**SOC Design Laboratory**

**Lab5** **- Caravel SoC FPGA Integration**

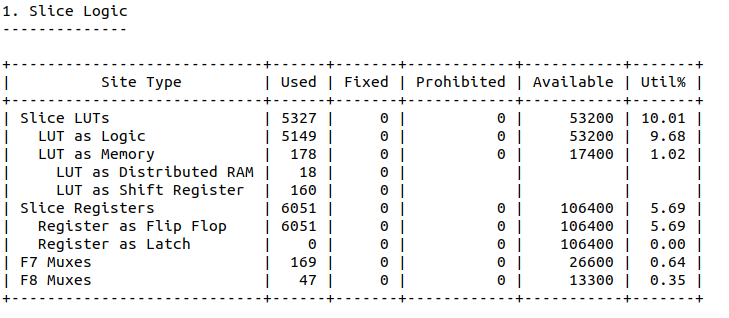
112061611 陳伯丞

112061524 葉又菘

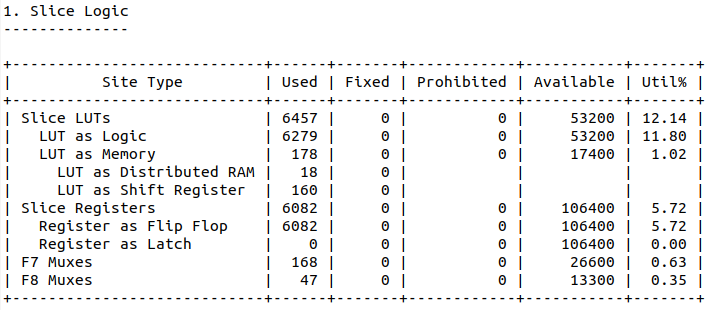
110063553 張傑閔

1. **Block Diagram**
2. **FPGA utilization**

Counter utilization:

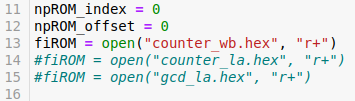


GCD utilization:



1. **IP Functions**
2. **FPGA Running result**

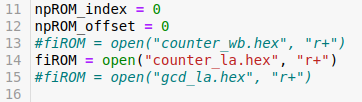
In the first run, select file.

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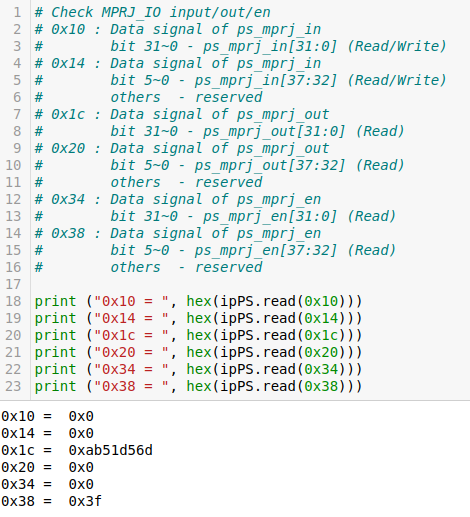
And the result is the following, the value at address 0x1c is 0xab61.



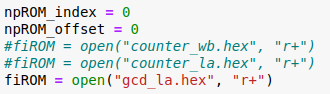
In the second run, we select the file.



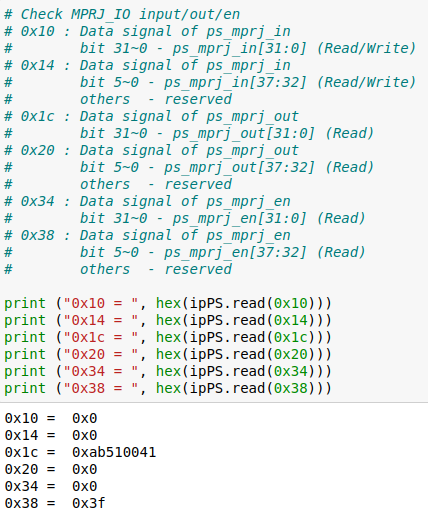
The value at address 0x1c is 0xab51.



Last, select the file.



The value at address 0x1c is 0xab51.



1. **caravel\_fpga.ipynb**