**Lab6 Workload optimized SOC – baseline**

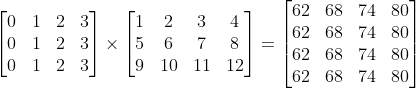
Group 6: 112061611 陳伯丞

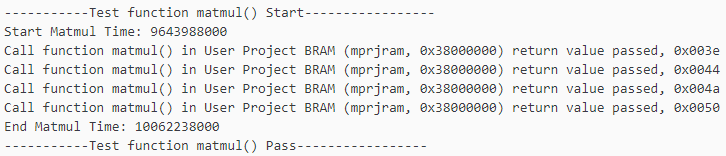
112061524 葉又菘

110063553 張傑閔

1. **How do you verify your answer from notebook**

* Matrix Multiplication:

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計算結果正確，答案以16進位顯示。

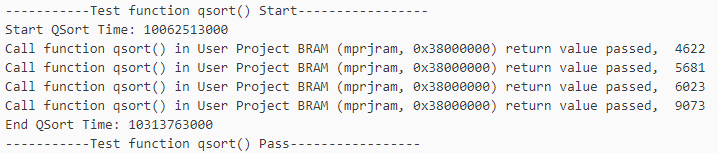
Calculation time in testbench:

* Quick Sort

Golden pattern:

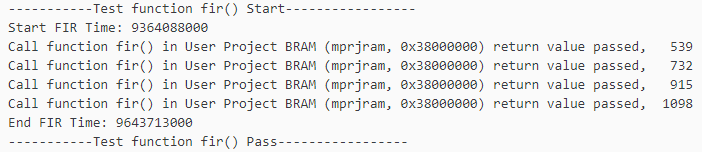


Testbench中我們只確認後4個答案。



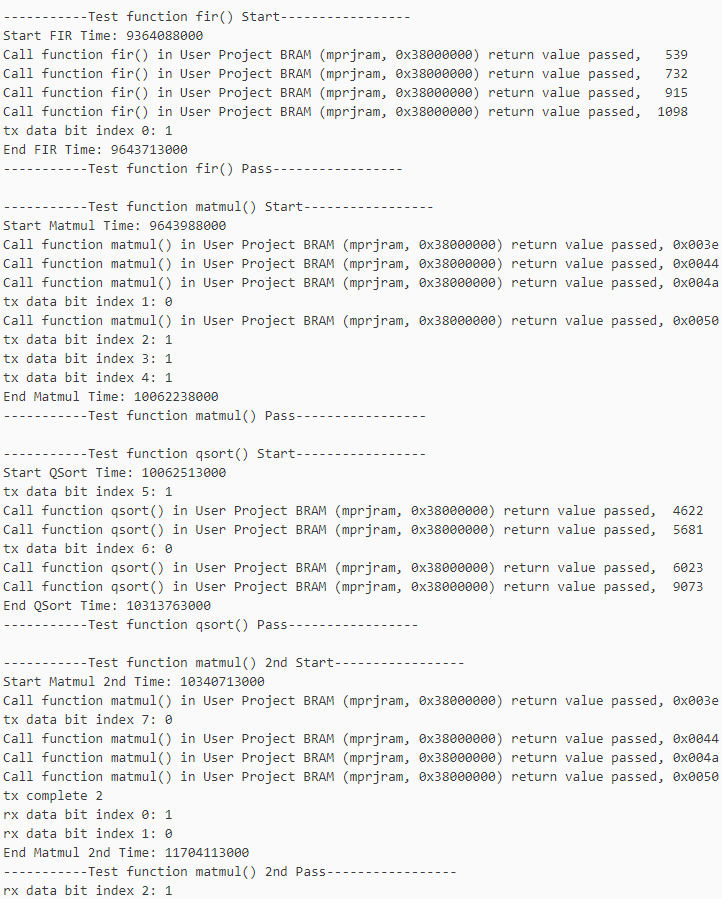
Calculation time in testbench:

* FIR

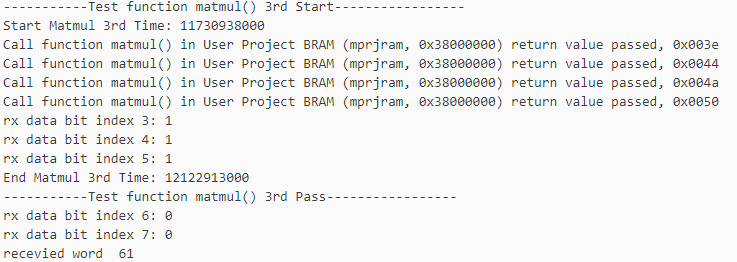


Calculation time in testbench:

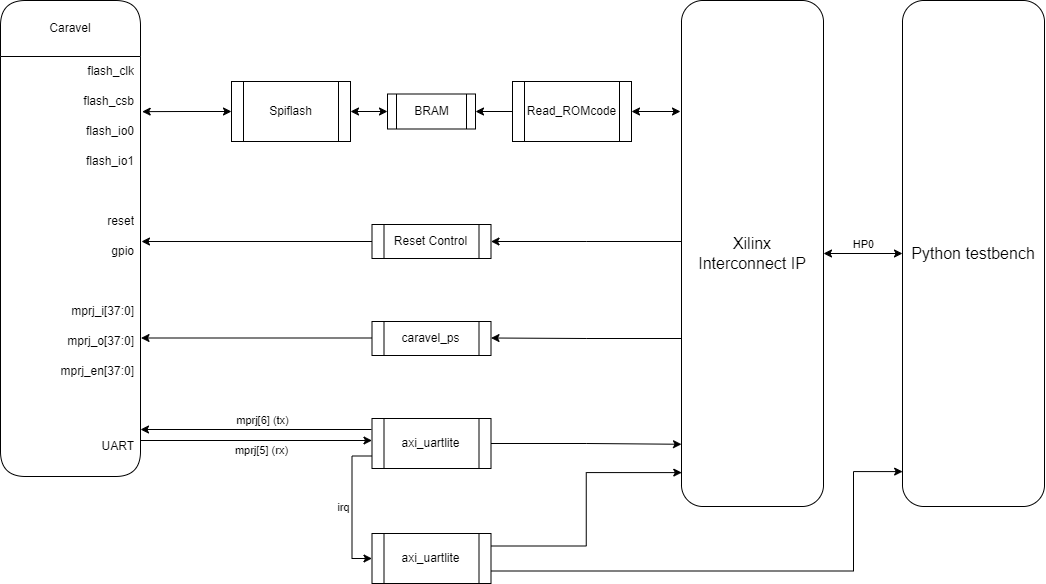
* Integrate the above tasks and UART



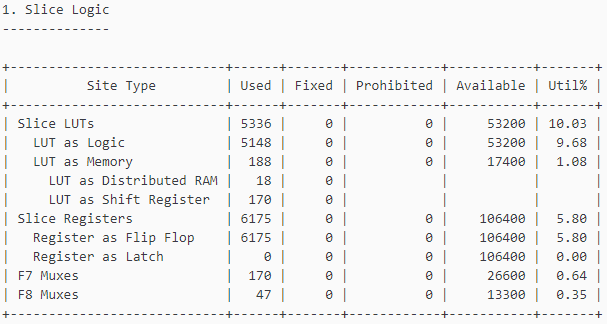
UART interrupts tasks

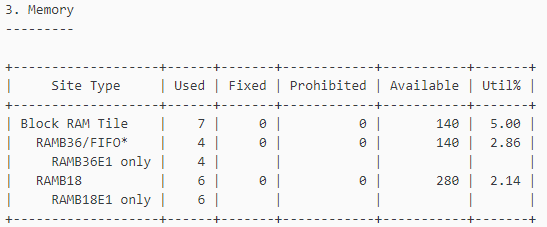


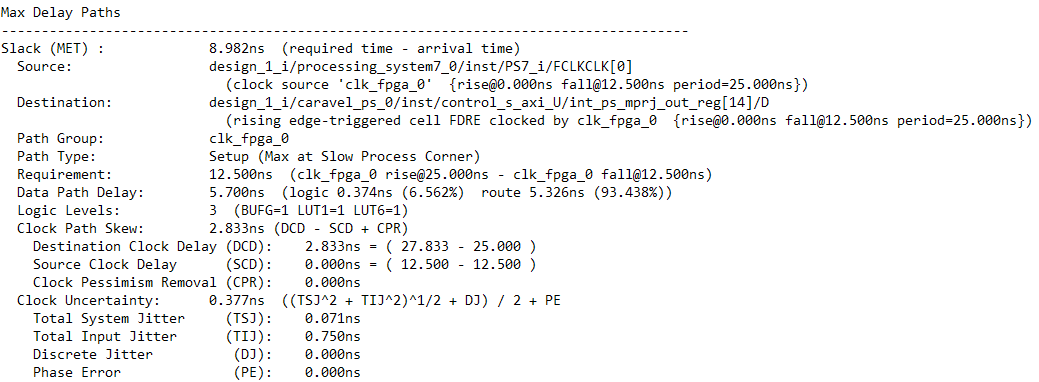
1. **Block design**

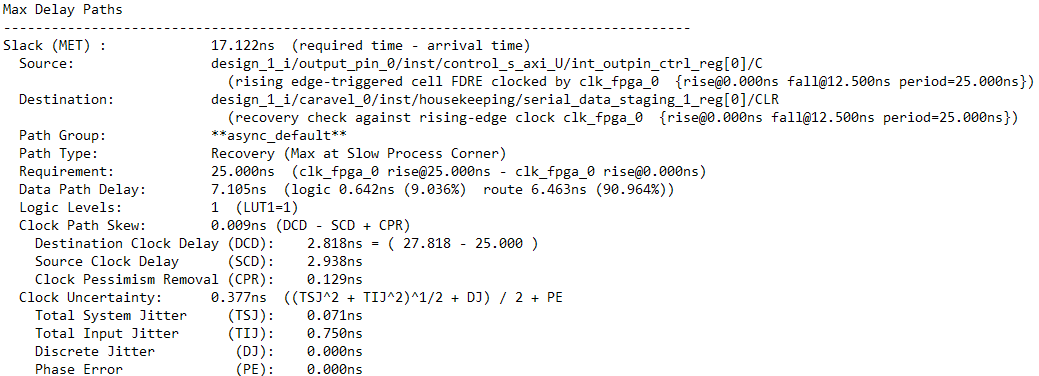


1. **Timing report/ resource report after synthesis**









1. **Latency for a character loop back using UART**
2. **Suggestion for improving latency or UART loop back**
3. **GitHub link**