**Lab6 Workload optimized SOC – baseline**

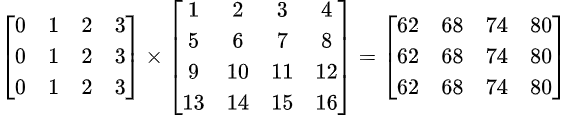
Group 6: 112061611 陳伯丞

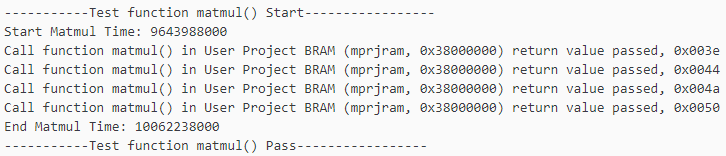
112061524 葉又菘

110063553 張傑閔

1. **How do you verify your answer from notebook**

* Matrix Multiplication:

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計算結果正確，答案以16進位顯示。

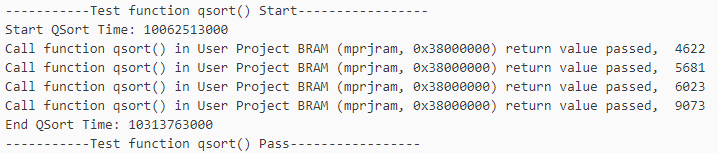
Calculation time in testbench:

* Quick Sort

Golden pattern:

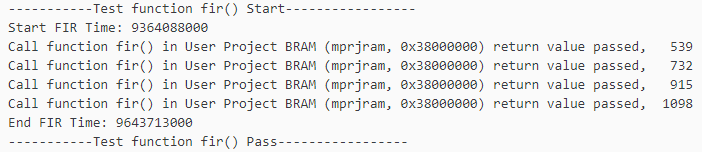


共有10個答案，testbench中我們只顯示後4個。



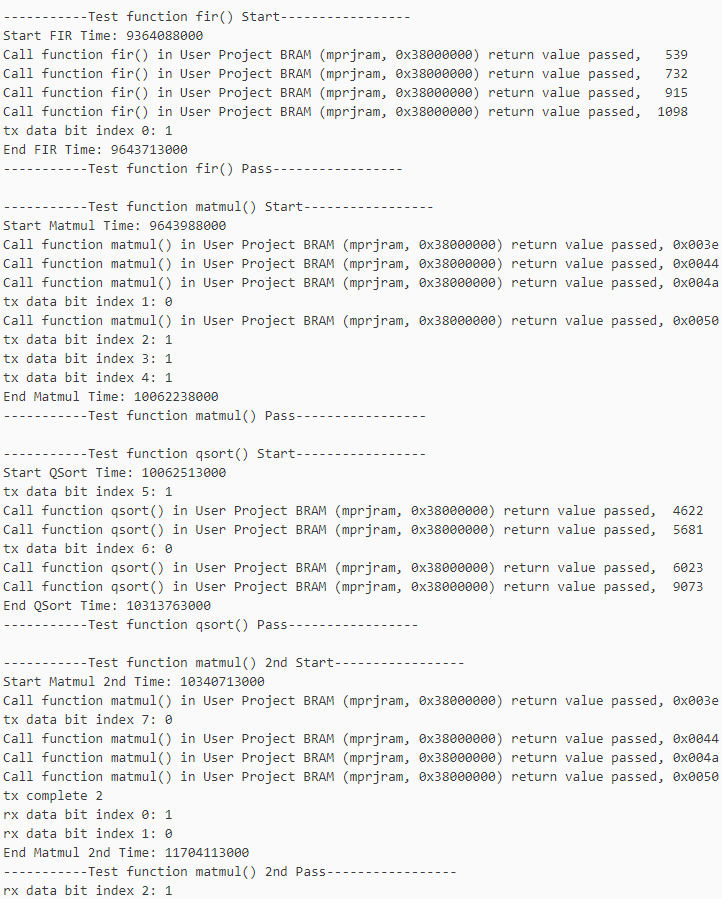
Calculation time in testbench:

* FIR

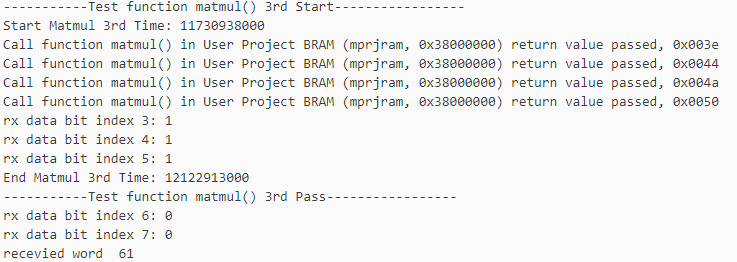


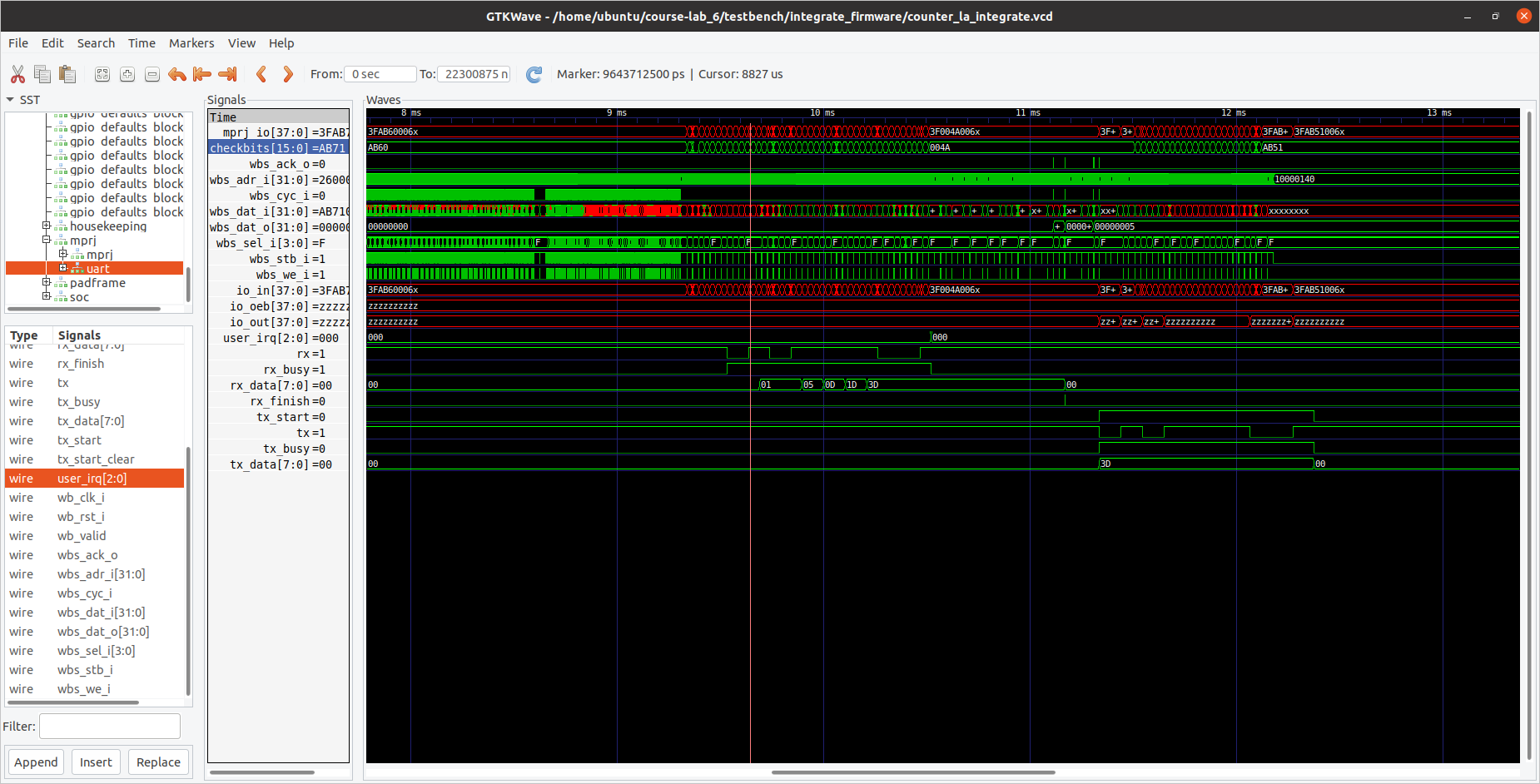
Calculation time in testbench:

* Integrate the above tasks and UART



UART interrupts tasks





SOC Transmitting

SOC Receiving

MM

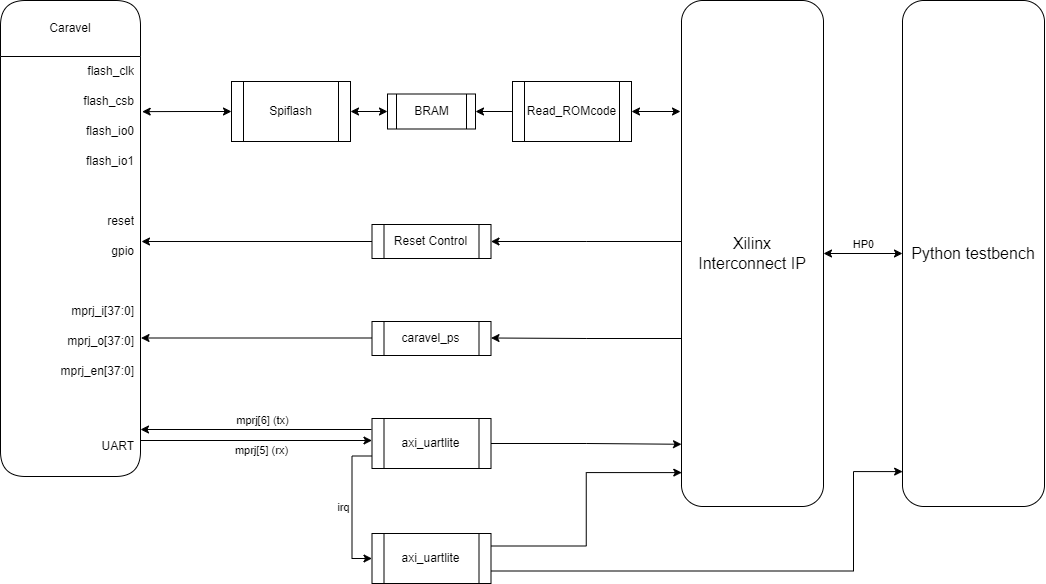
MM

QS

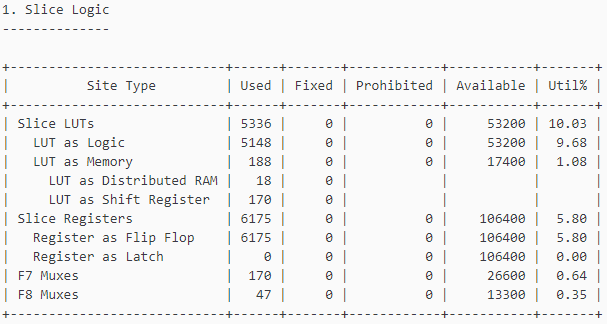
MM

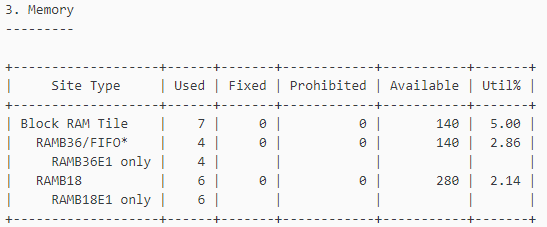
FIR

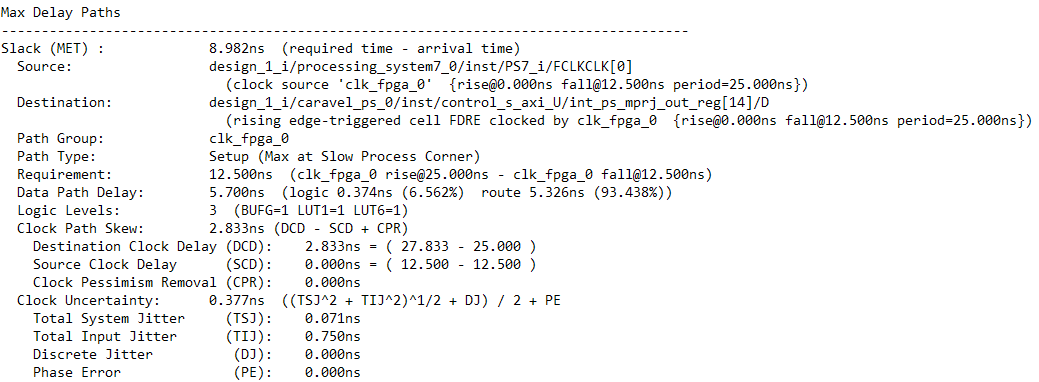
1. **Block design**

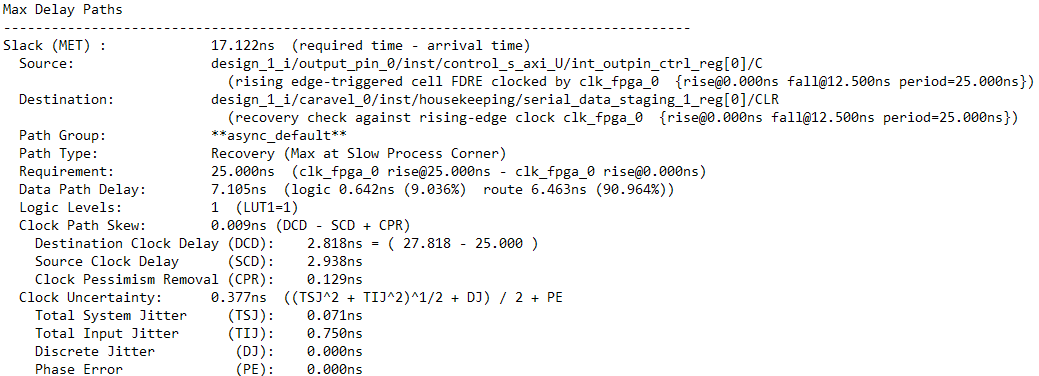


1. **Timing report/ resource report after synthesis**

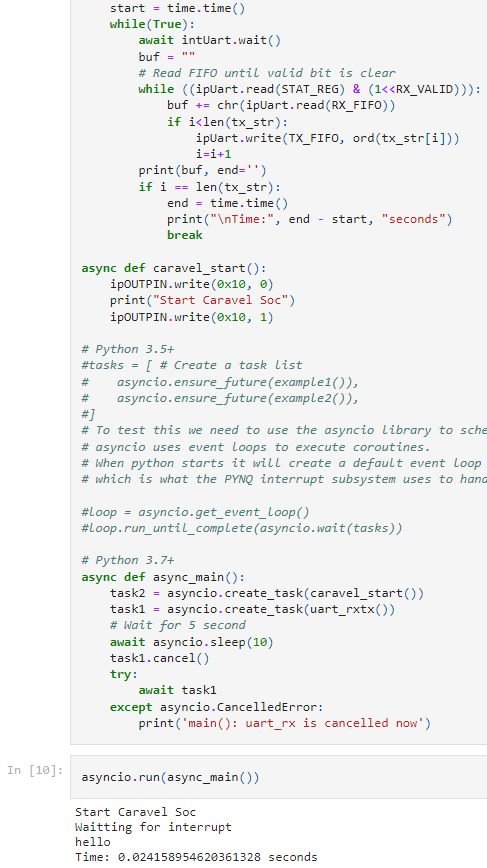
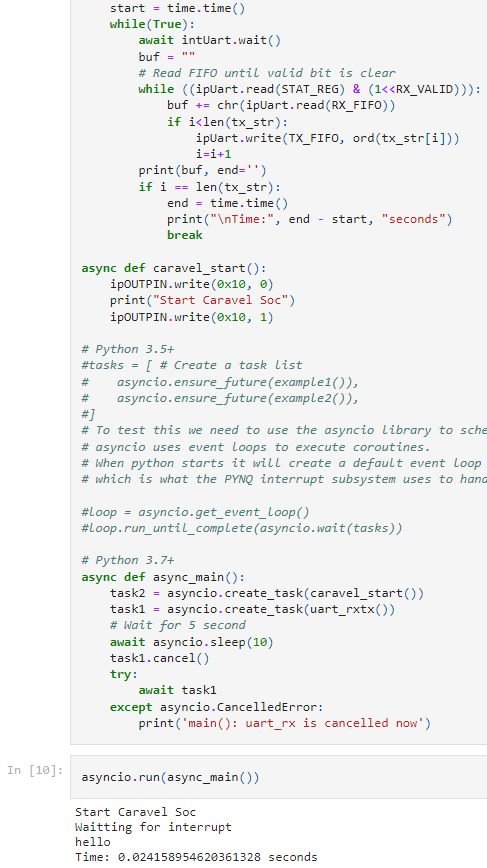




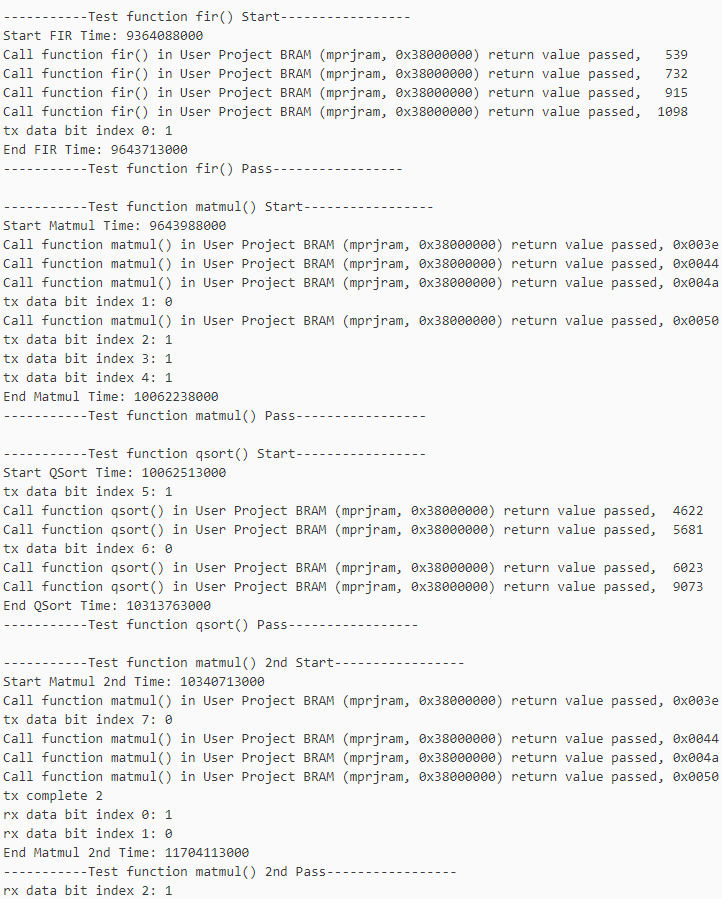




1. **Latency for a character loop back using UART**

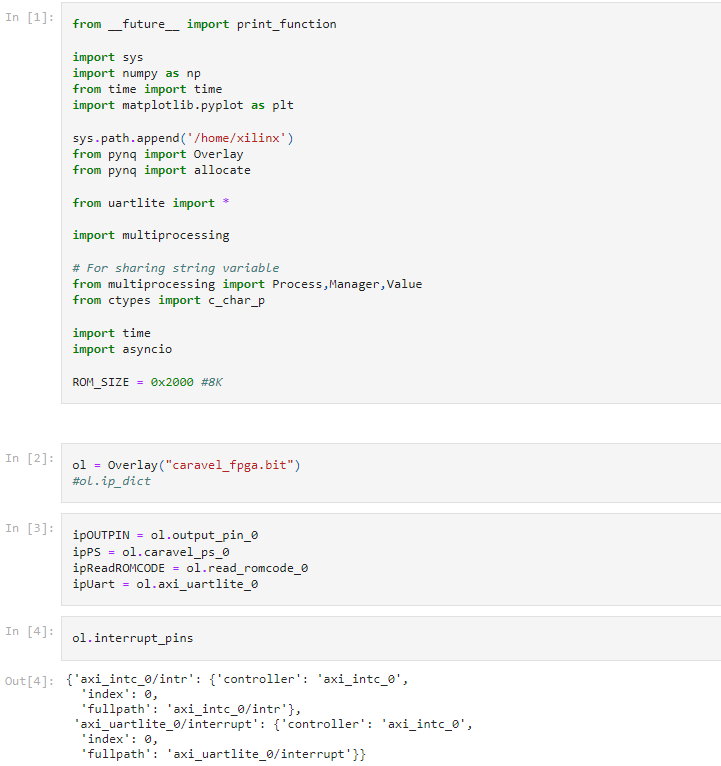


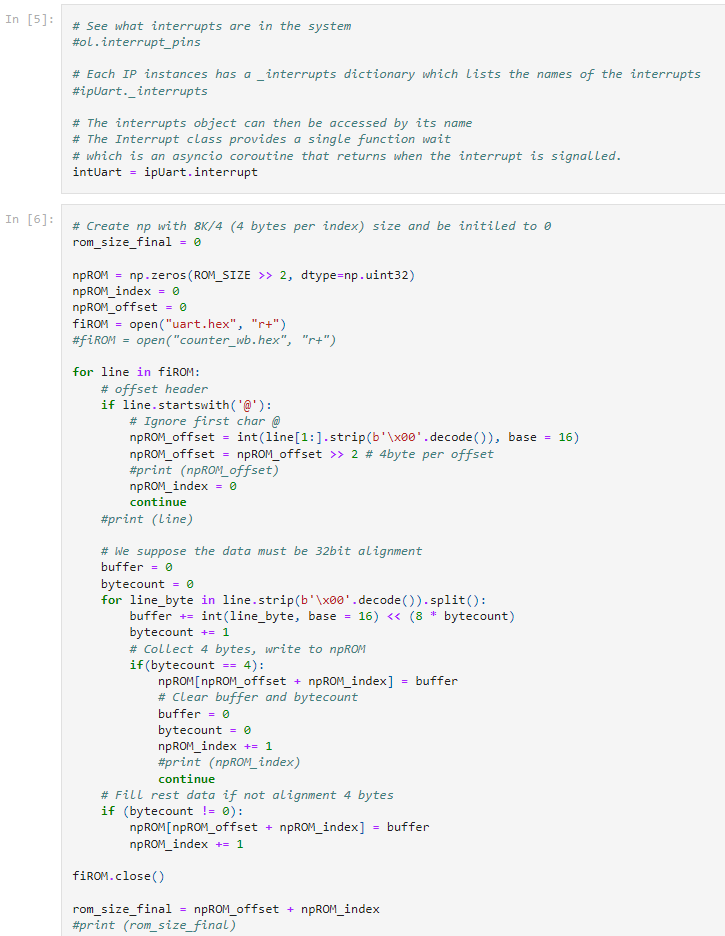
1. **Suggestion for improving latency or UART loop back**

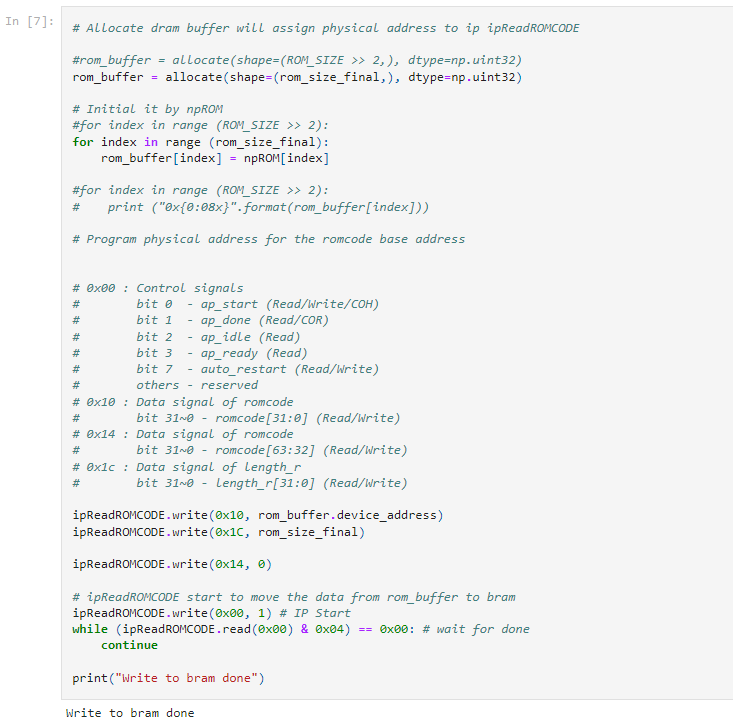


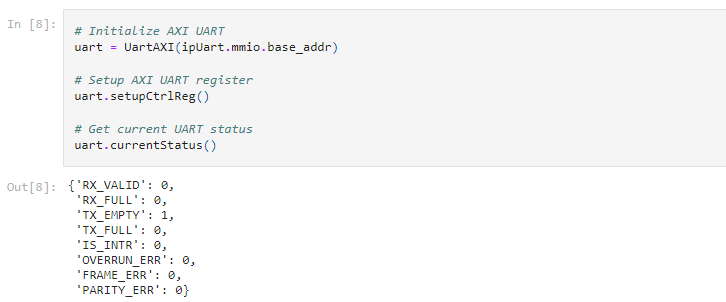
Testbench的結果中我們可以明顯看到每次interrupt之間間隔相當久，所以可以使用FIFO增加一次傳輸的資料數量來達到增加throughput的效果。

1. **FPGA Result (UART)**

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1. **GitHub link**

<https://github.com/yousungyeh/course-lab_6>