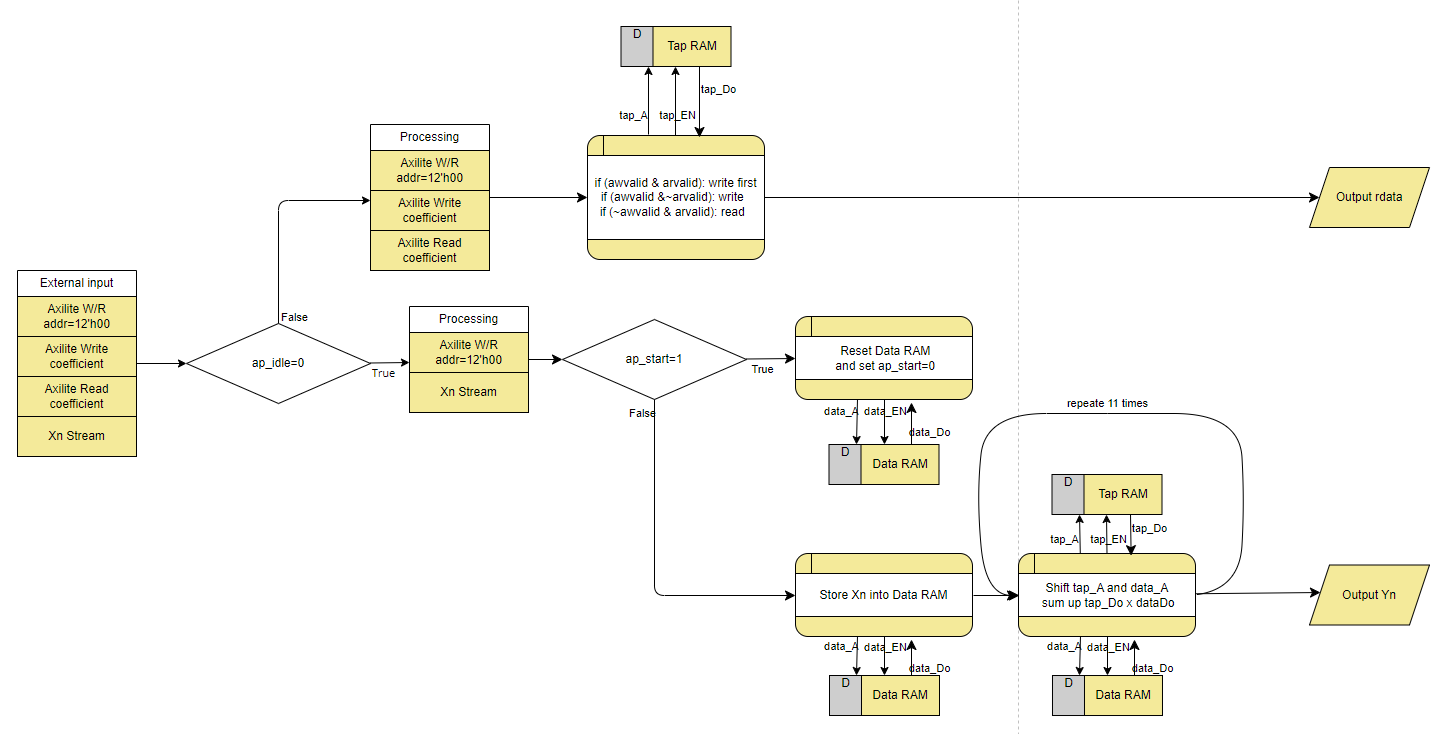
SOC lab3

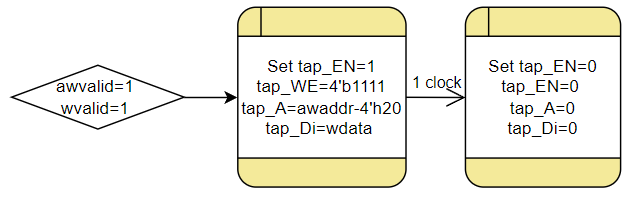
112061611 陳伯丞

1. Block Diagram

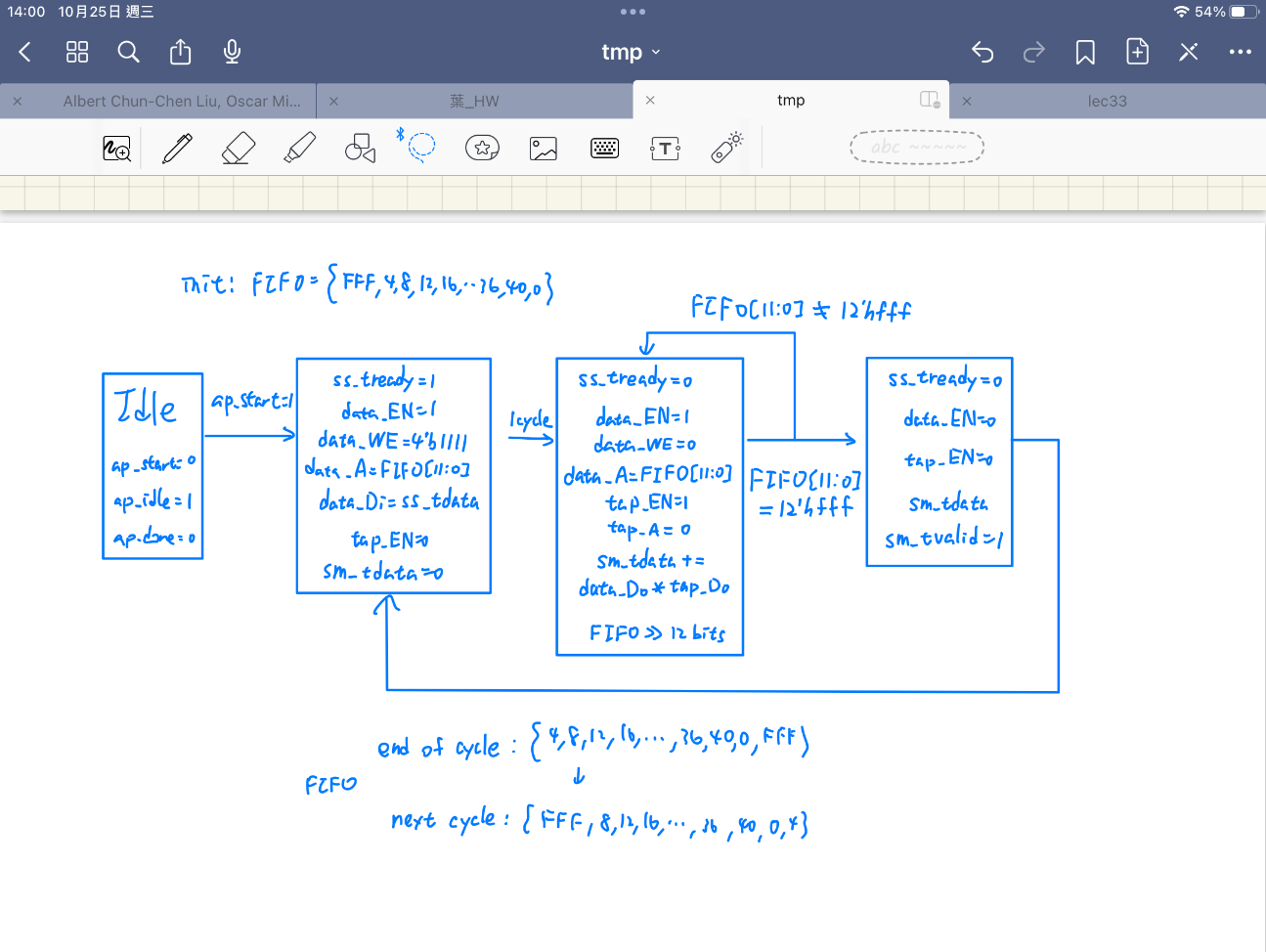


1. Describe operation

* : can only be write before turn on.

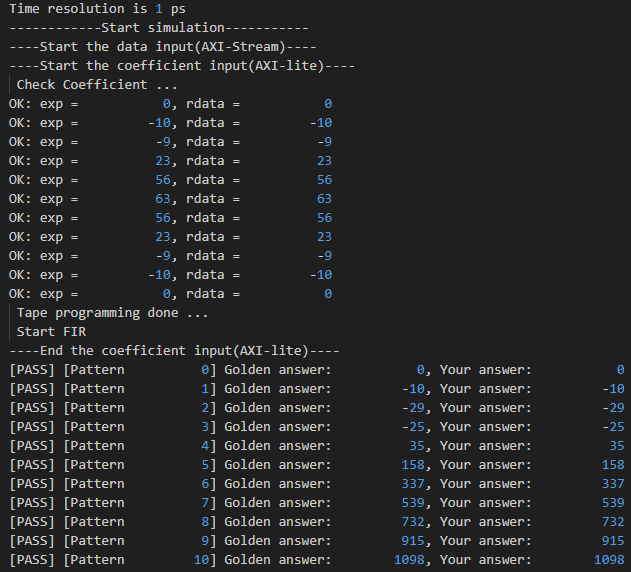


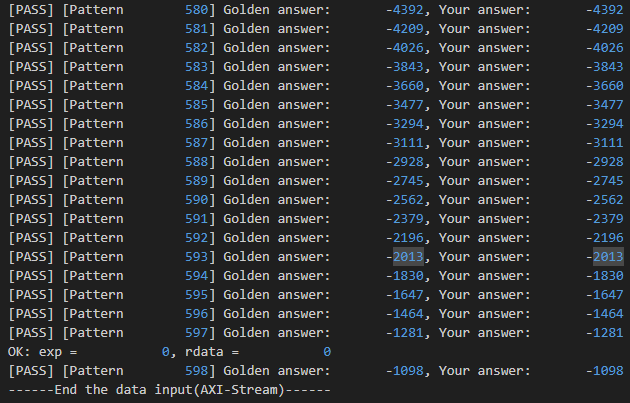
* : can only be write after turn on. And there is a FIFO to store the address of .



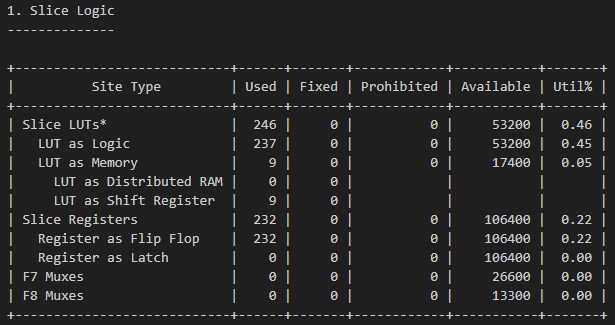
* is generated when

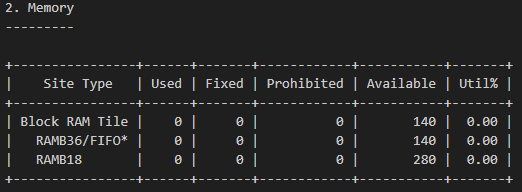
1. Simulation report

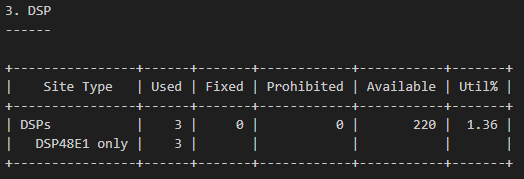




1. Resource usage: including FF, LUT, BRAM







1. Timing Report

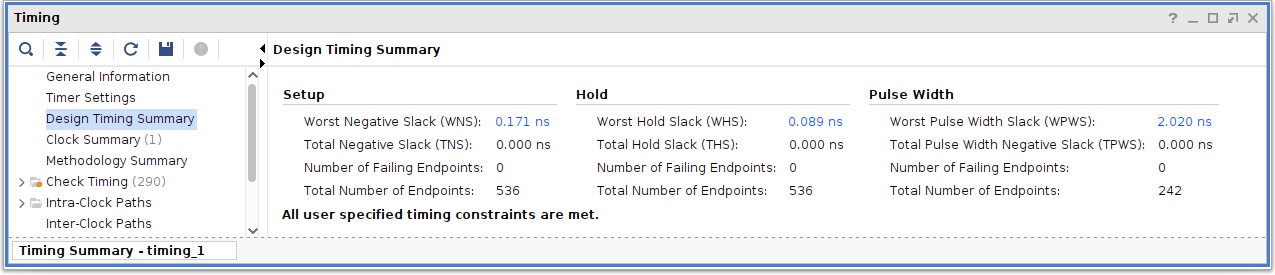


Fig. Design Timing Summary as clock cycle time 6ns

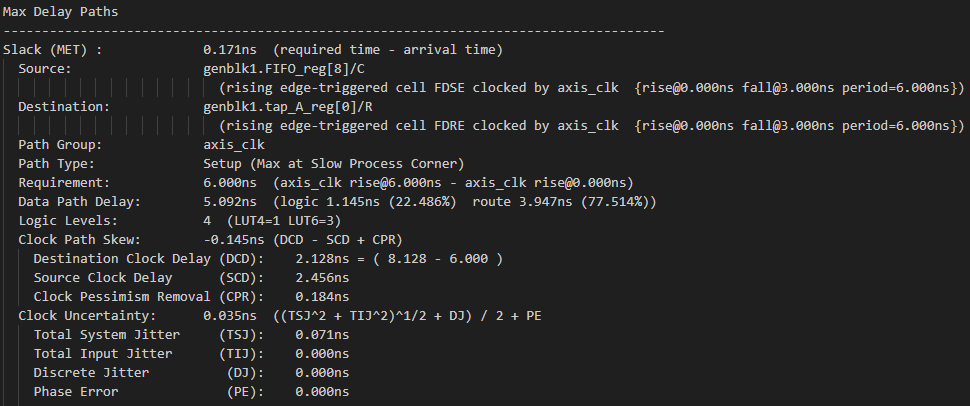


Fig. Max Delay Paths

1. Simulation Waveform

* # of clock cycles from ap\_start to ap\_done:

: 1.085ps; : 79.085ps; clock cycle: 6ns

13000 clock cycles

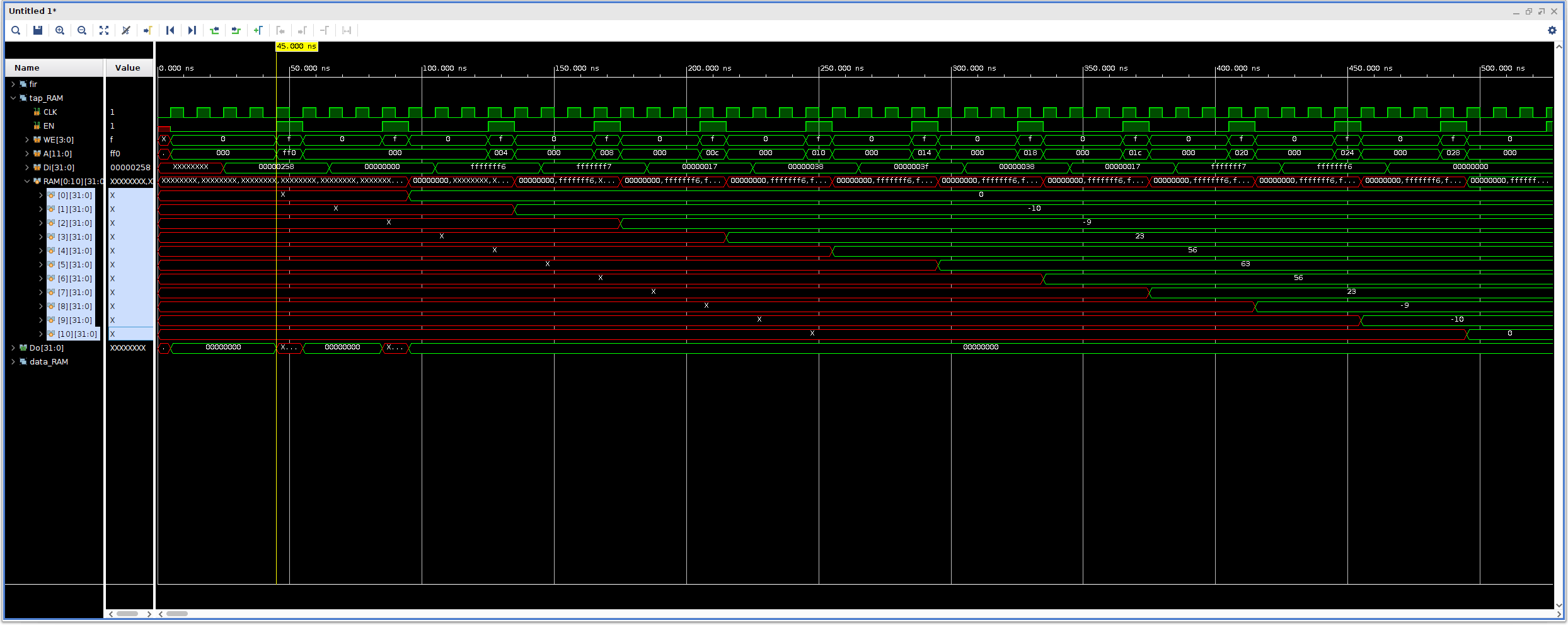


Fig. write

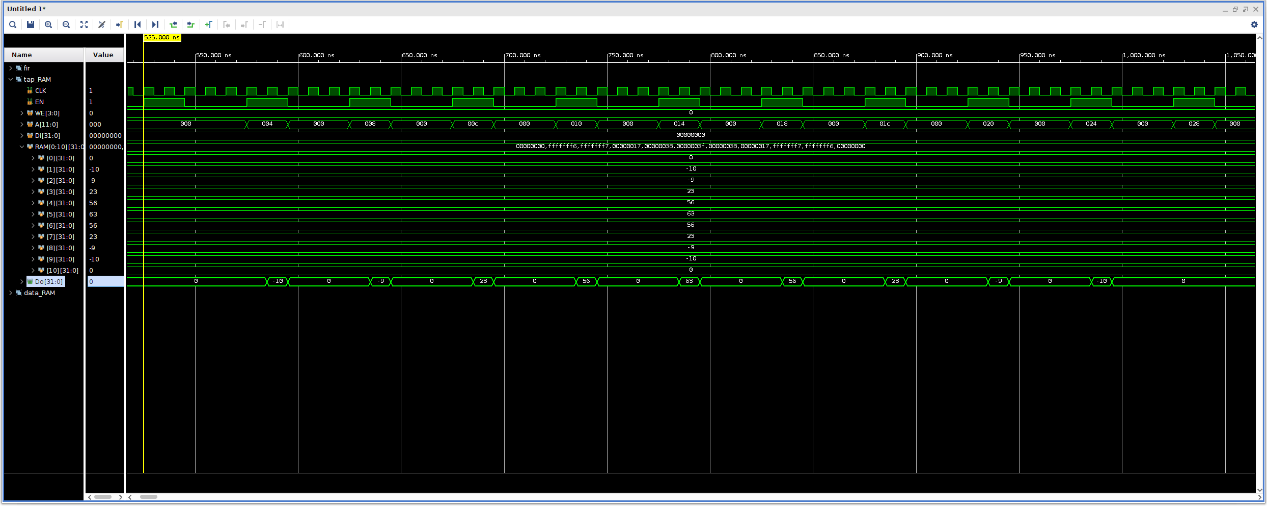


Fig. Read

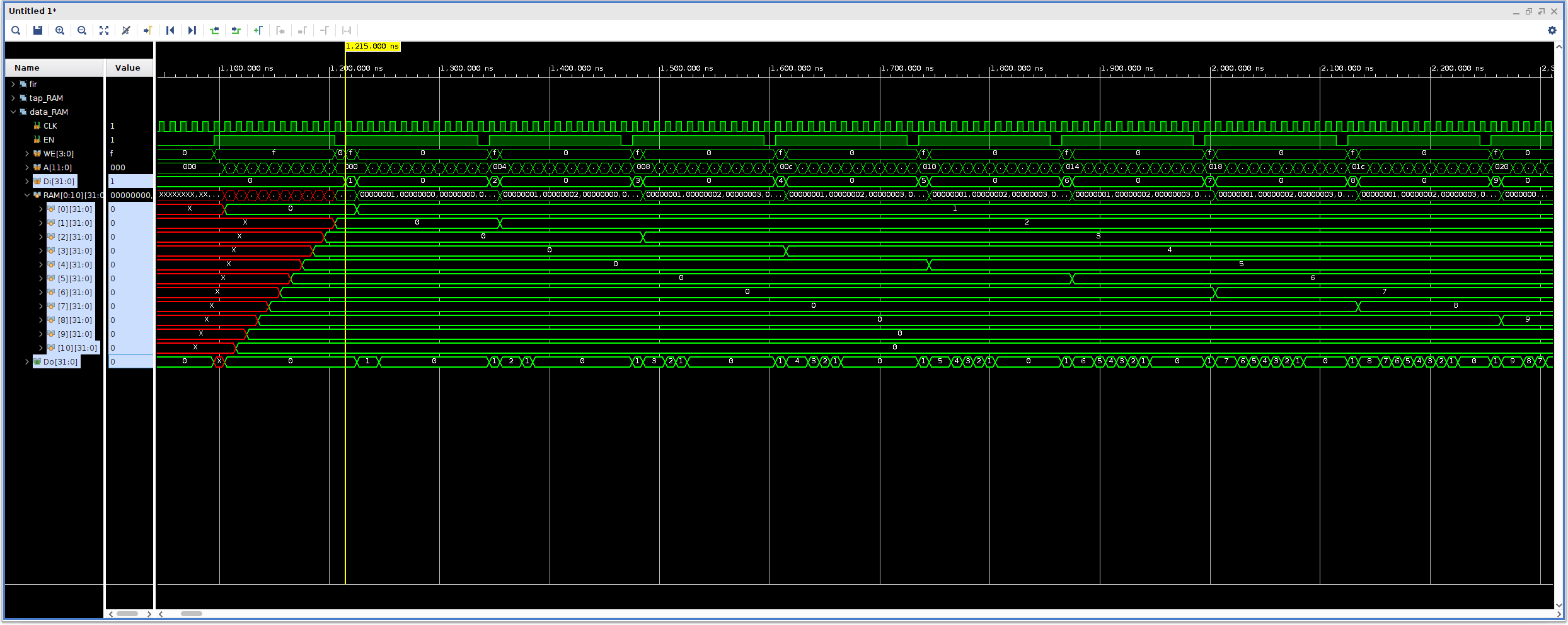


Fig. write and read

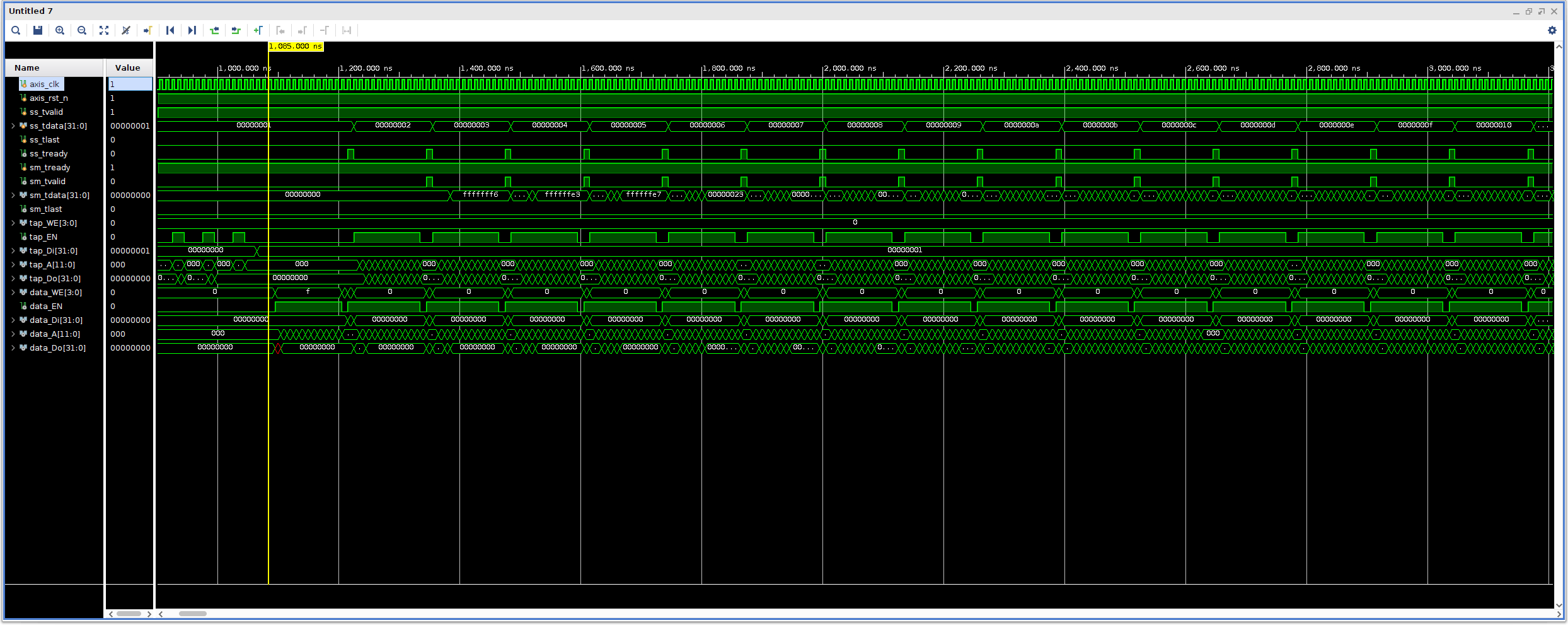


Fig. Stream andStream

1. GitHub Link

<https://github.com/ken01235/SOC_Design/tree/master/lab-fir%20report>