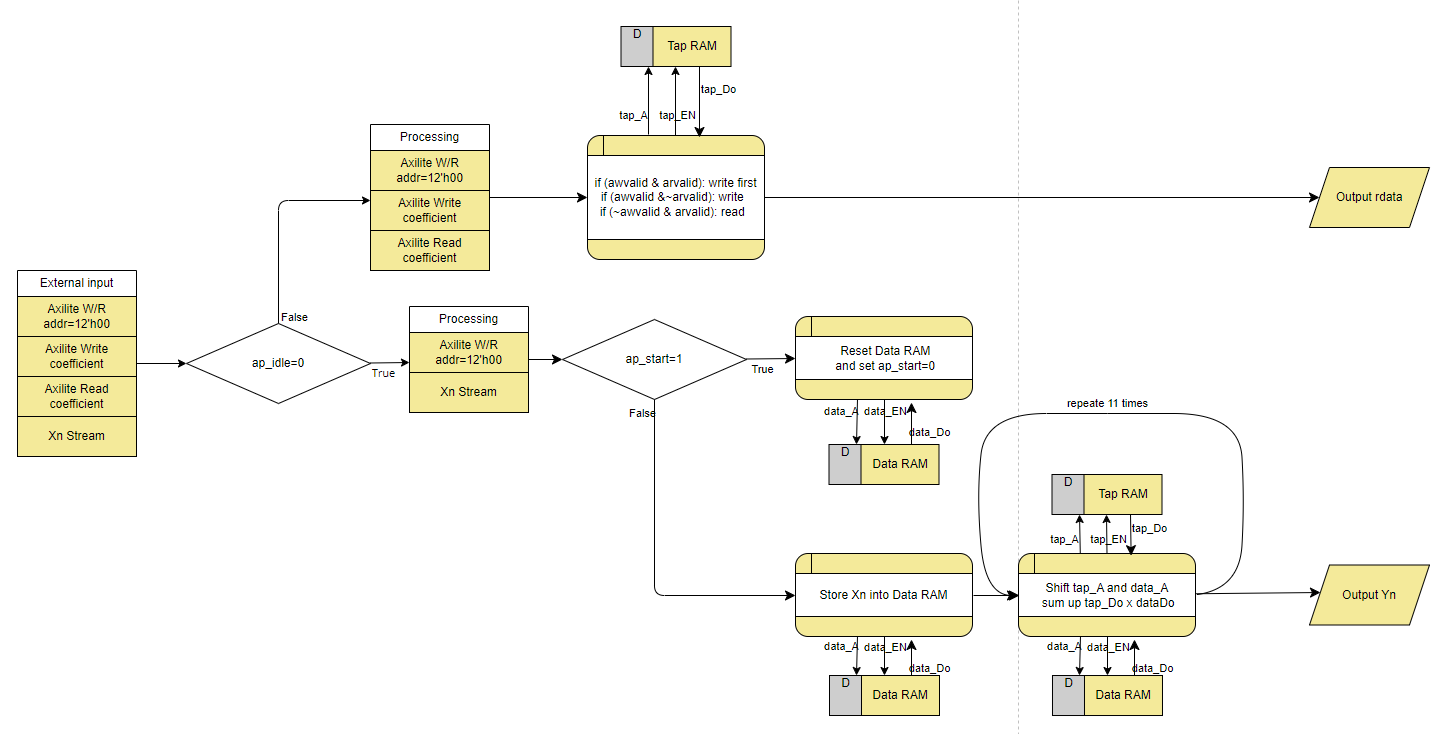
SOC lab3

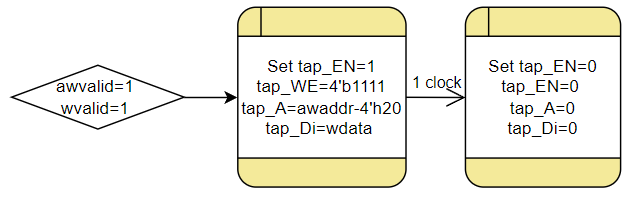
112061611 陳伯丞

1. Block Diagram

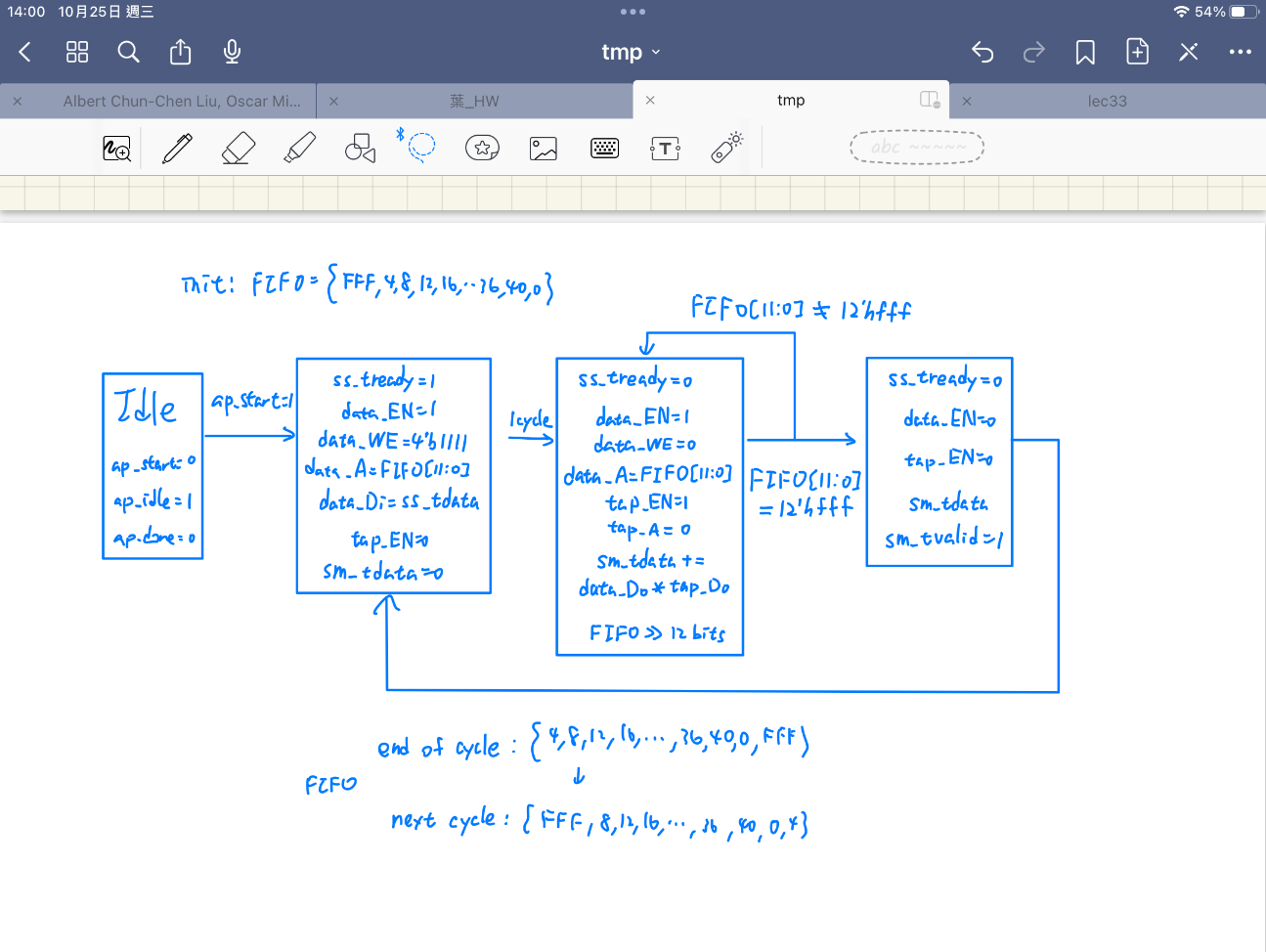


1. Describe operation

* : can only be write before turn on.

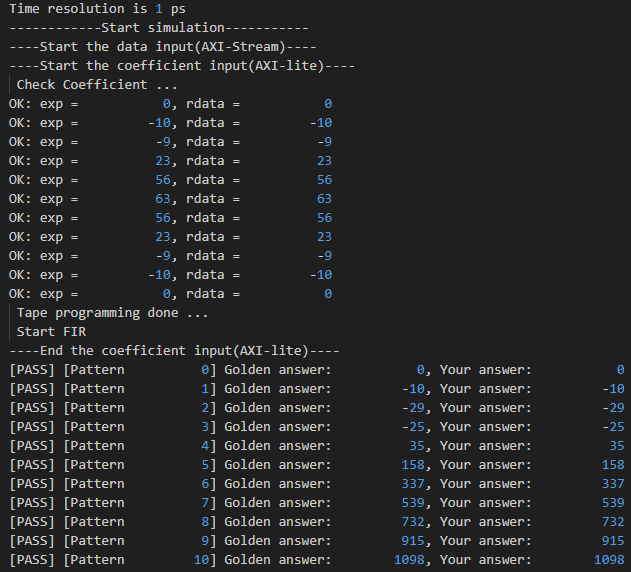


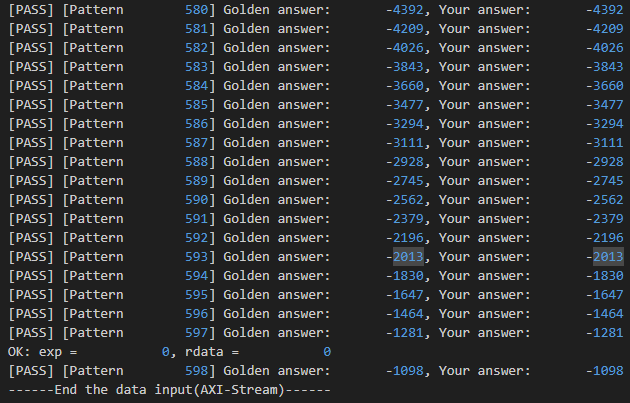
* : can only be write after turn on. And there is a FIFO to store the address of .



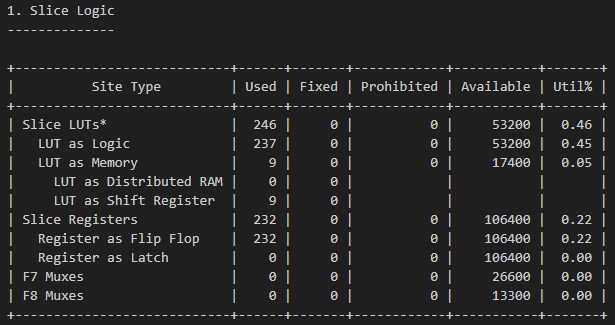
* is generated when

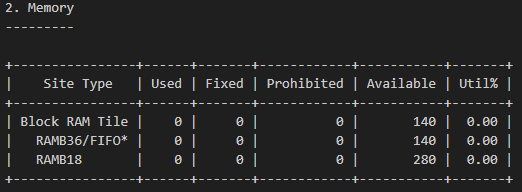
1. Simulation report

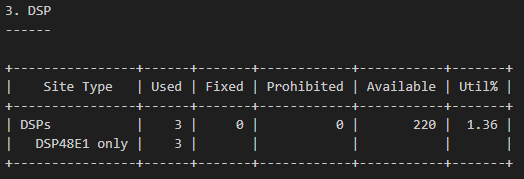




1. Resource usage: including FF, LUT, BRAM







1. Timing Report

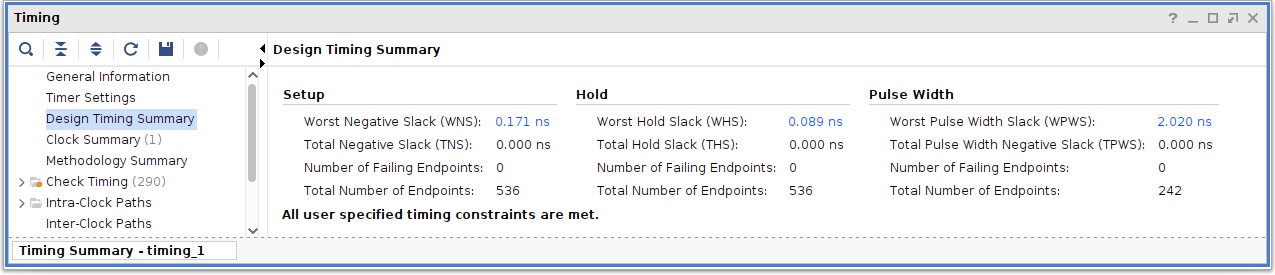


Fig. Design Timing Summary as clock cycle time 6ns

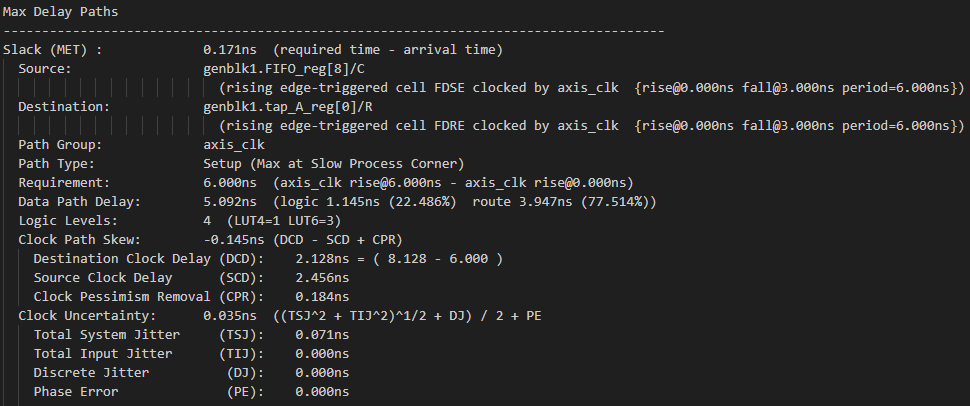


Fig. Max Delay Paths

1. Simulation Waveform, show

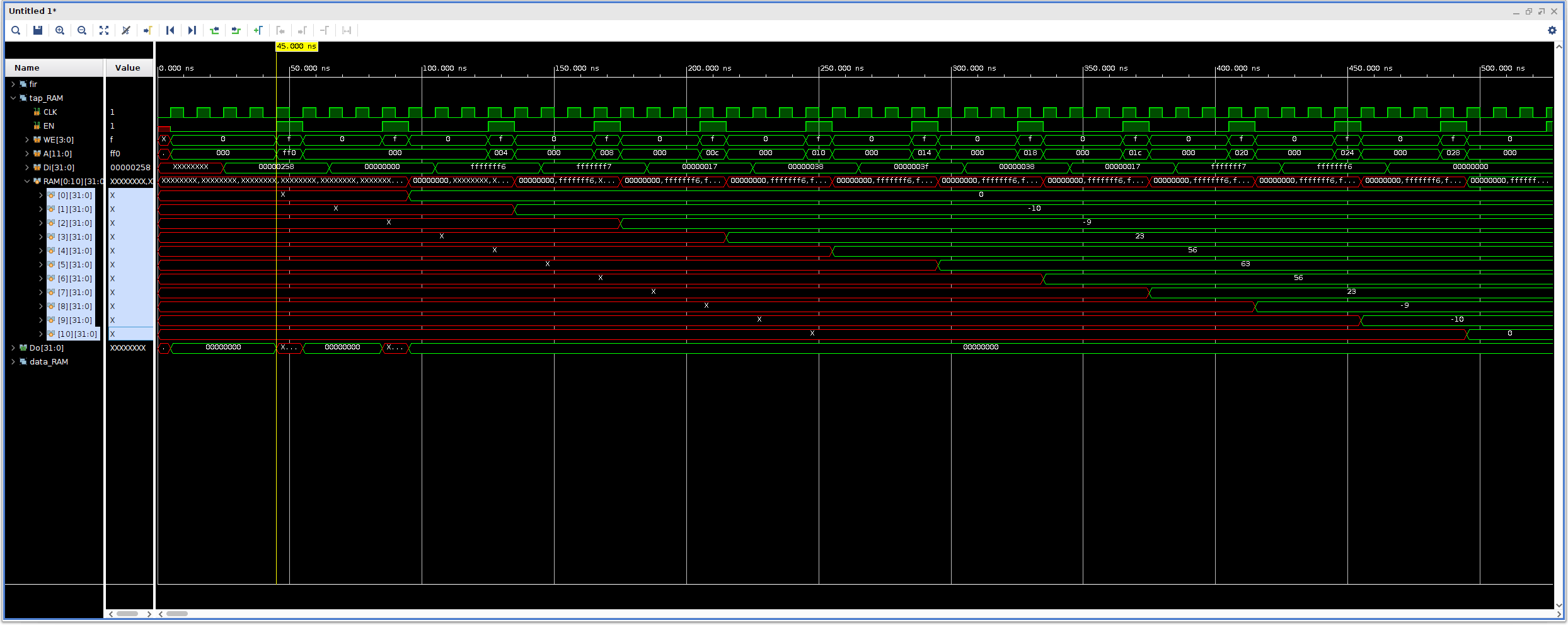


Fig. write

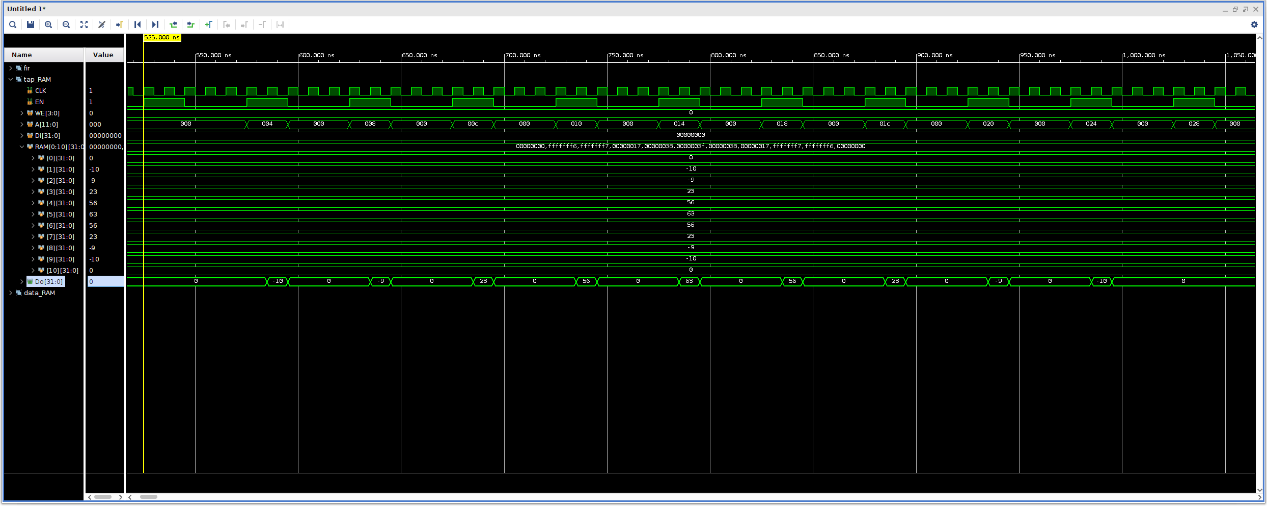


Fig. Read

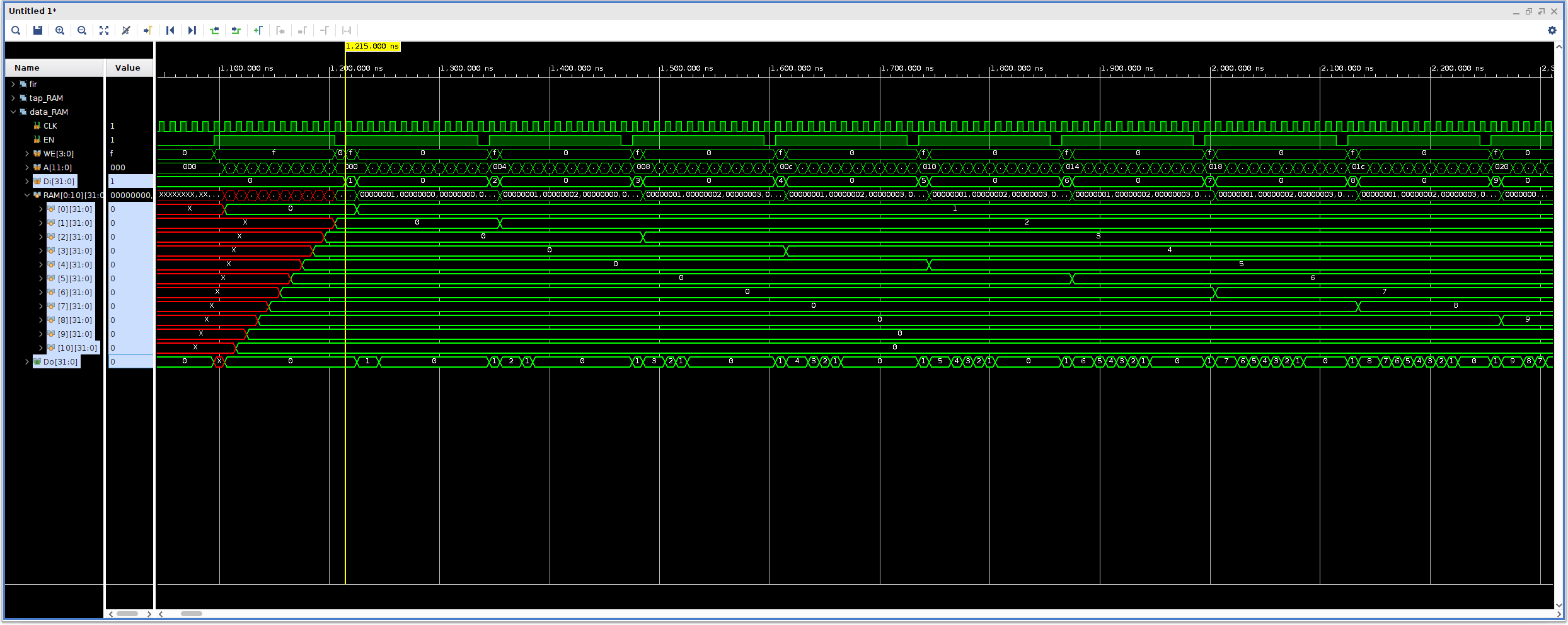


Fig. write and read

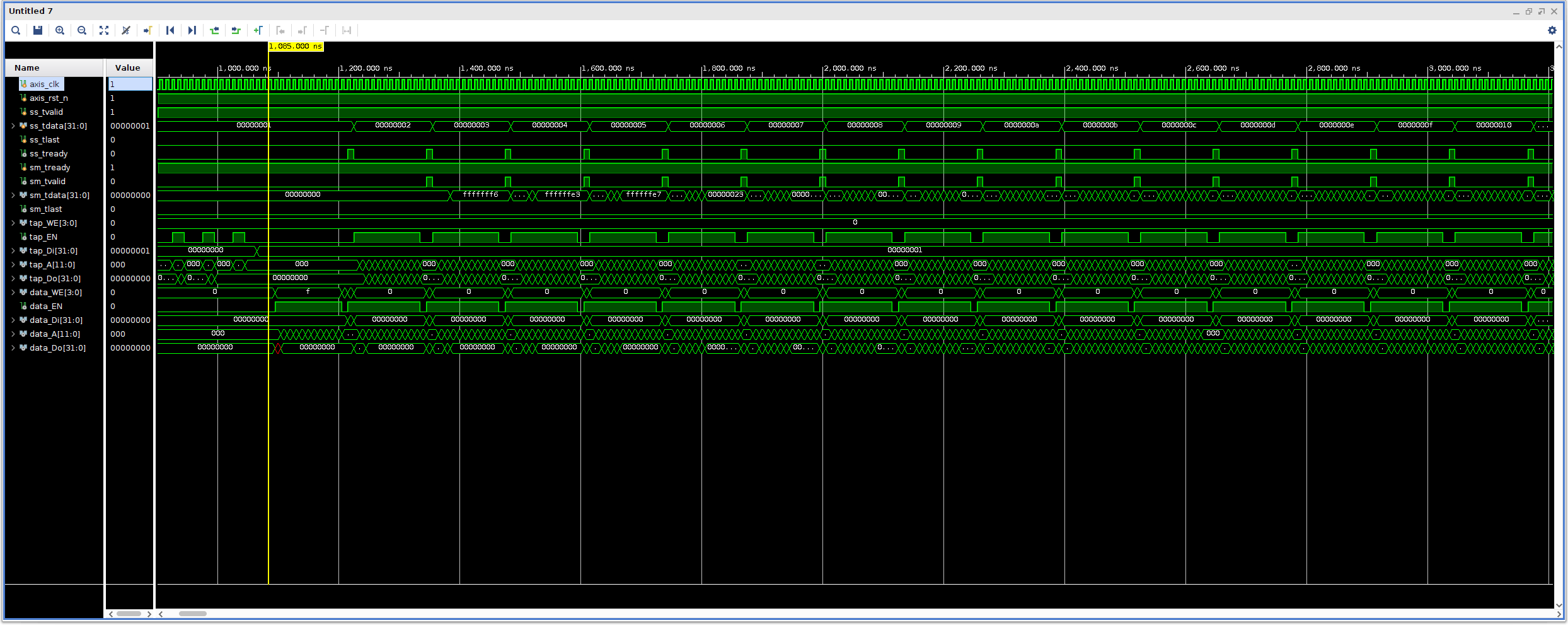


Fig. Stream andStream

1. GitHub Link