

# **SPI slave with single port RAM**

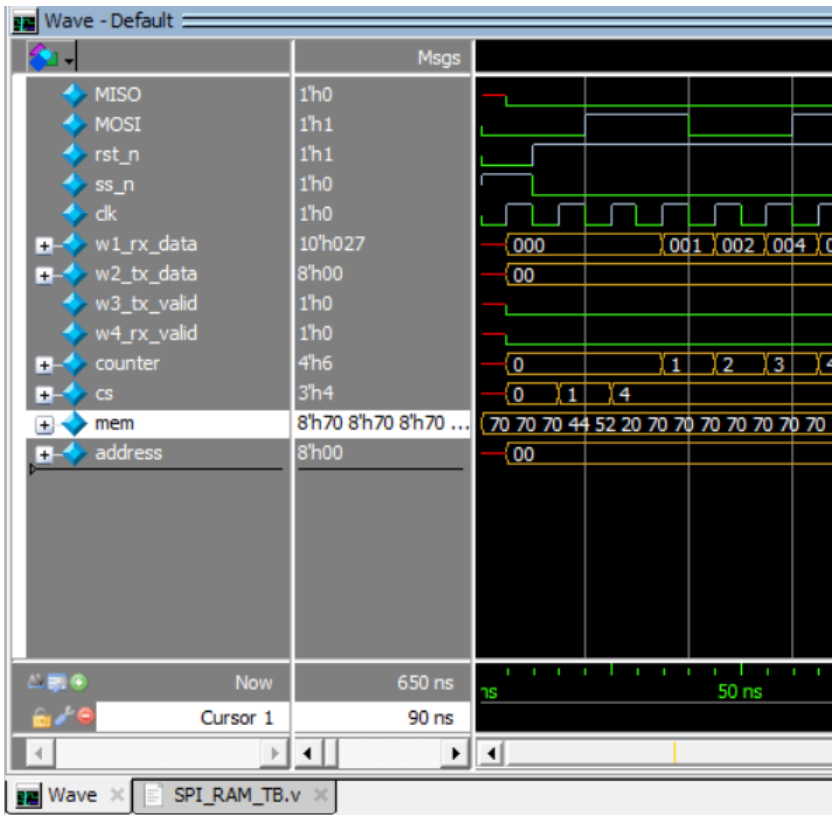
**Teammates:**

**Abdulrahman Mohammad  
Abdelrahman Ahmed Sayed**

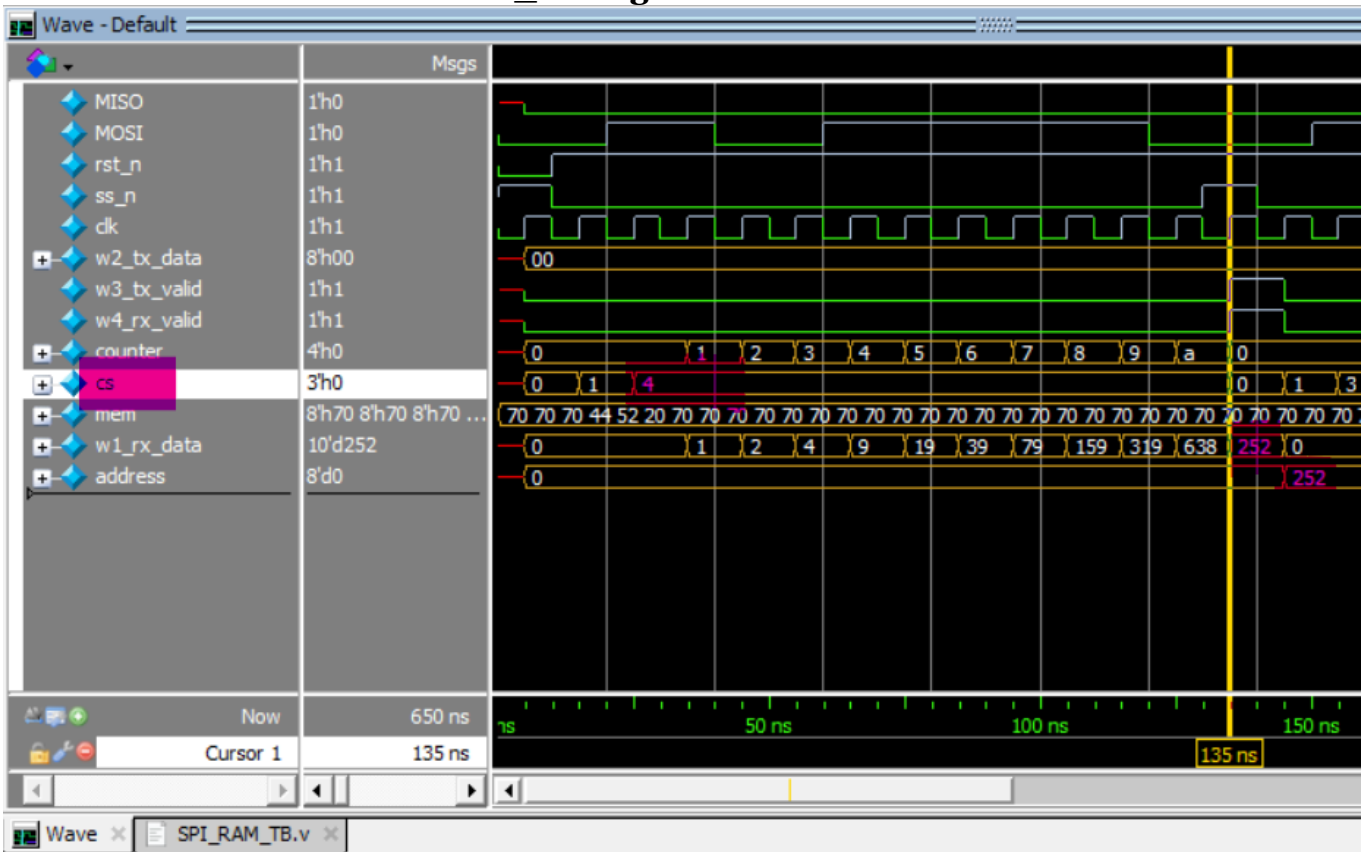
**Under Supervision of:  
Eng. Kareem Waseem**

# Snippets from the waveforms captured from QuestaSim

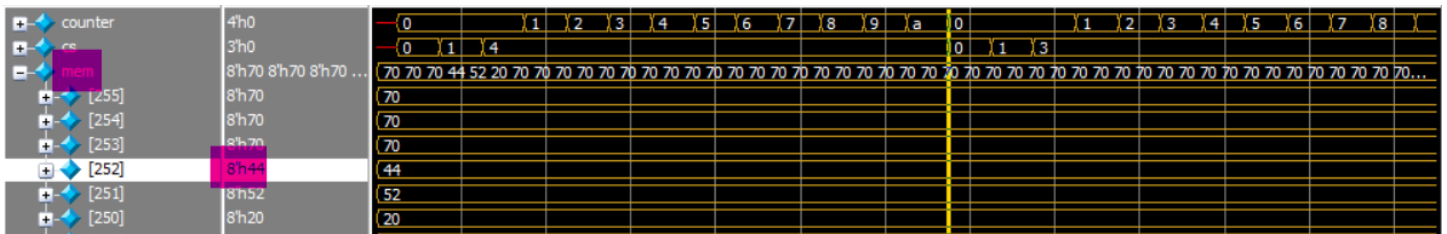
## 1\_testing synchronous reset



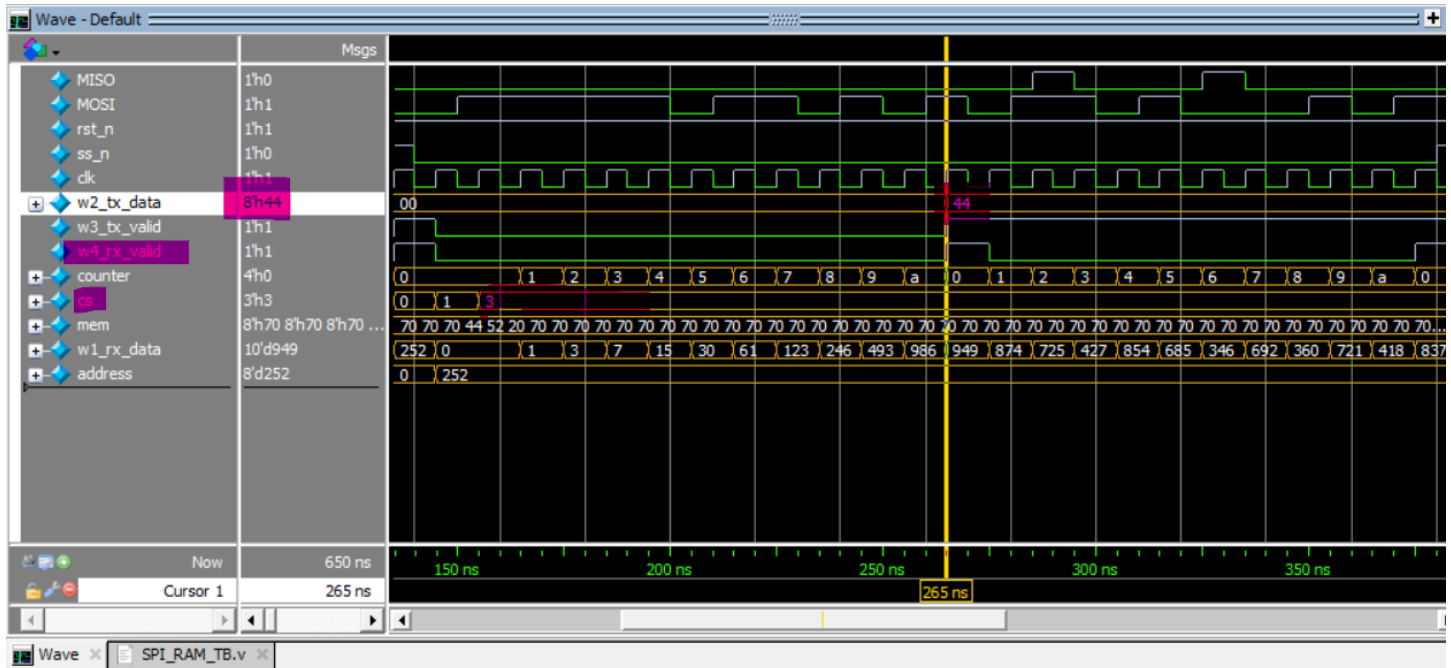
## 2\_testing read address



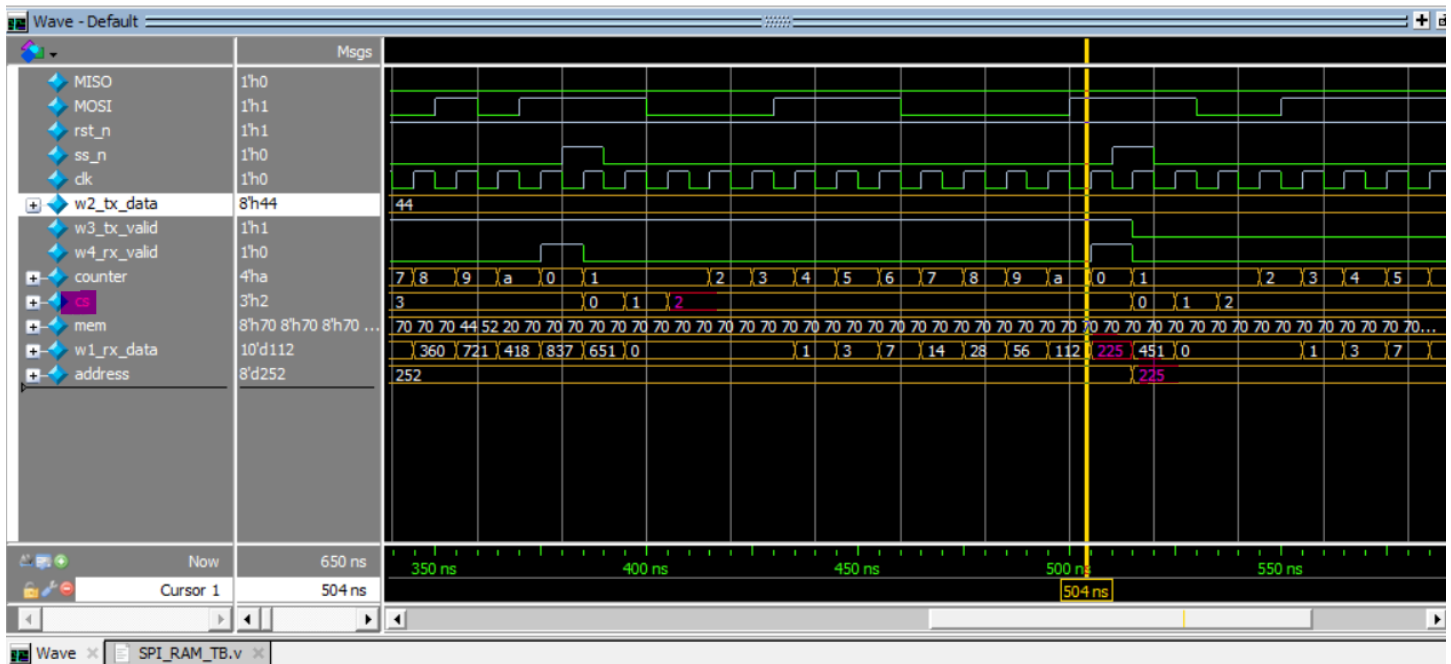
### 3\_what was in the address



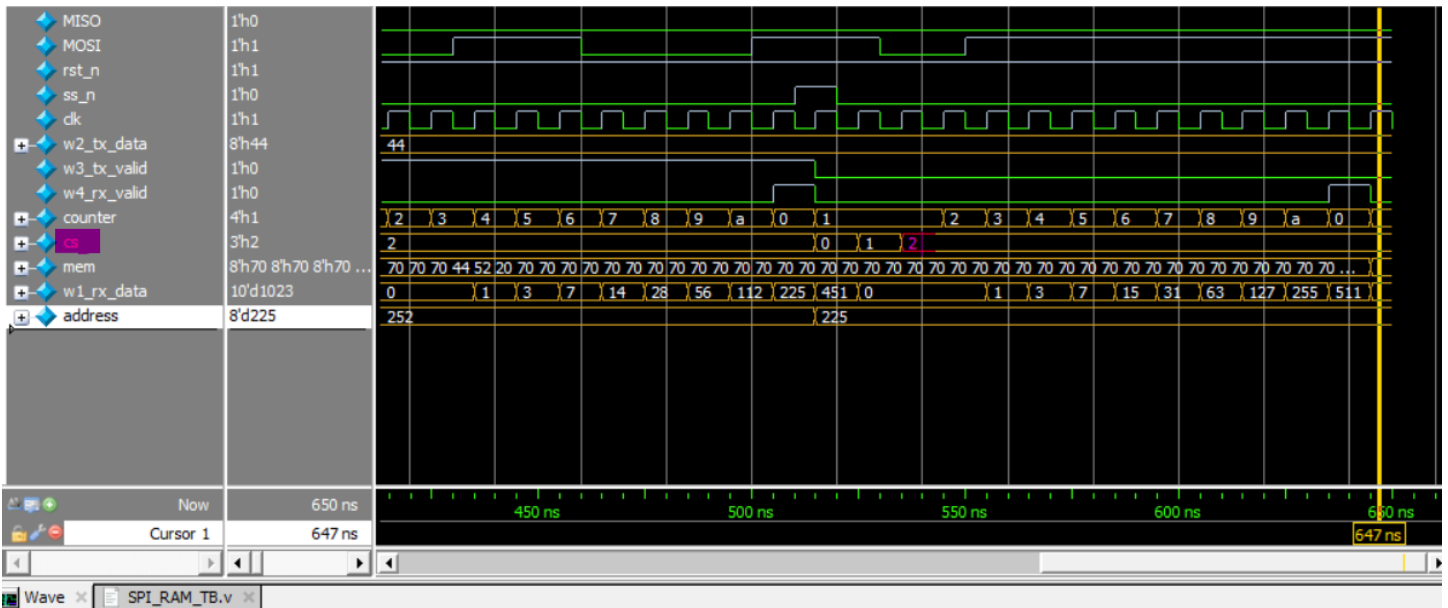
#### 4\_testing read data



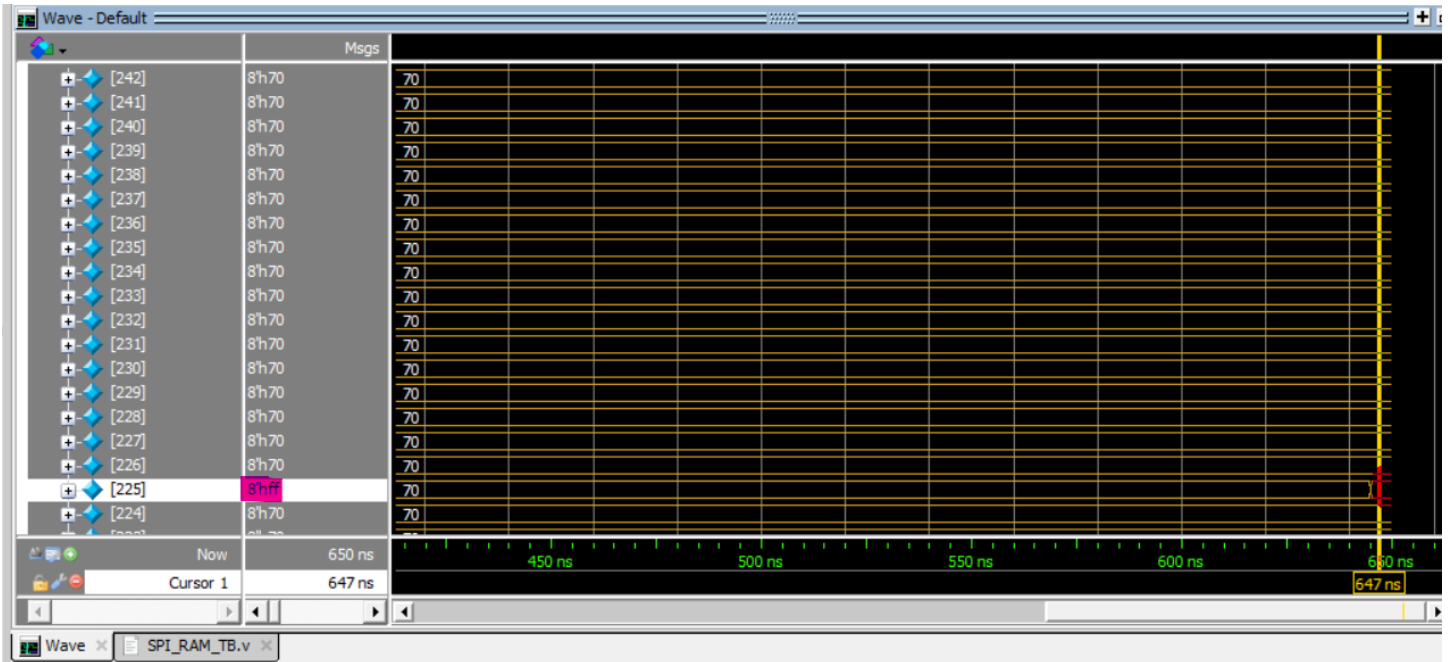
## 5\_test write address



## 6\_testing write data



**7\_what we wrote in TB is written in the address we determined**



## Questa Lint

Questa Lint 2021.1 (...QFT\_2021.1/QFT/V2021.1/win64/bin/lint.db)

File Edit View Source Window Help

Design

Search: Type Sear... Exact

Instance Module

SPI\_w\_RAM (2) SPI\_w\_RAM

```
10 wire[0:0]w1_rx_data;
11 wire[7:0]w2_tx_data;
12 wire w3_tx_valid , w4_rx_valid;
13
14 //connecting modules
15
16 SPI_slave S1(
17     .tx_data(w2_tx_data),
18     .ss_n(ss_n),
19     .rst_n(rst_n),
20     .clk(clk),
21     .tx_valid(w3_tx_valid),
22     .MOSI(MOSI),
23     .rx_data(w1_rx_data),
24     .rx_valid(w4_rx_valid),
25     .MISO(MISO)
26 );
27
28 RAM #(
29     .MEM_DEPTH(MEM_DEPTH),
30     .ADDR_SIZE(ADDR_SIZE)
31 )R1(
32     .din(w1_rx_data),
33     .clk(clk),
34     .rst_n(rst_n),
35     .rx_valid(w4_rx_valid),
36     .dout(w2_tx_data),
37     .tx_valid(w3_tx_valid)
38 );
39
40 endmodule
```

Inst: S1

Lint Summary

(Type Search Text (Press Enter))

Name	Count
Open(uninspected, pending, bug)	5 (6)
Info	5 (6)

Flow Navigator Design

Lint Checks

Filter: Type here

Waived Fixed Pending Uninspected Bug Verified Total : 5 Selected : 0

Severity	Status	Check	Alias	Message	Module	Category
Warning	Warning	parameter_name_duplicate		Same parameter name is used in more than one module. Parameter MEM_DEPTH, Total count 2, First module: Module RAM, File C:/Users/ABDOU/Desktop/Que...	RAM	Nomenclature Style
Warning	Warning	parameter_name_duplicate		Same parameter name is used in more than one module. Parameter ADDR_SIZE, Total count 2, First module: Module RAM, File C:/Users/ABDOU/Desktop/Que...	RAM	Nomenclature Style
Warning	Warning	multi_ports_in_single_line		Multiple ports are declared in one line. Module SPI_slave, File C:/Users/ABDOU/Desktop/Questa-20250315T193333Z-001/Questa/SPI_slave.v, Line 3.	SPI_slave	Rtl Design Style
Warning	Warning	multi_ports_in_single_line		Multiple ports are declared in one line. Module SPI_w_RAM, File C:/Users/ABDOU/Desktop/Questa-20250315T193333Z-001/Questa/SPI_w_RAM.v, Line 7.	SPI_w_RAM	Rtl Design Style
Warning	Warning	multi_ports_in_single_line		Multiple ports are declared in one line. Module RAM, File C:/Users/ABDOU/Desktop/Questa-20250315T193333Z-001/Questa/memory.v, Line 7.	RAM	Rtl Design Style

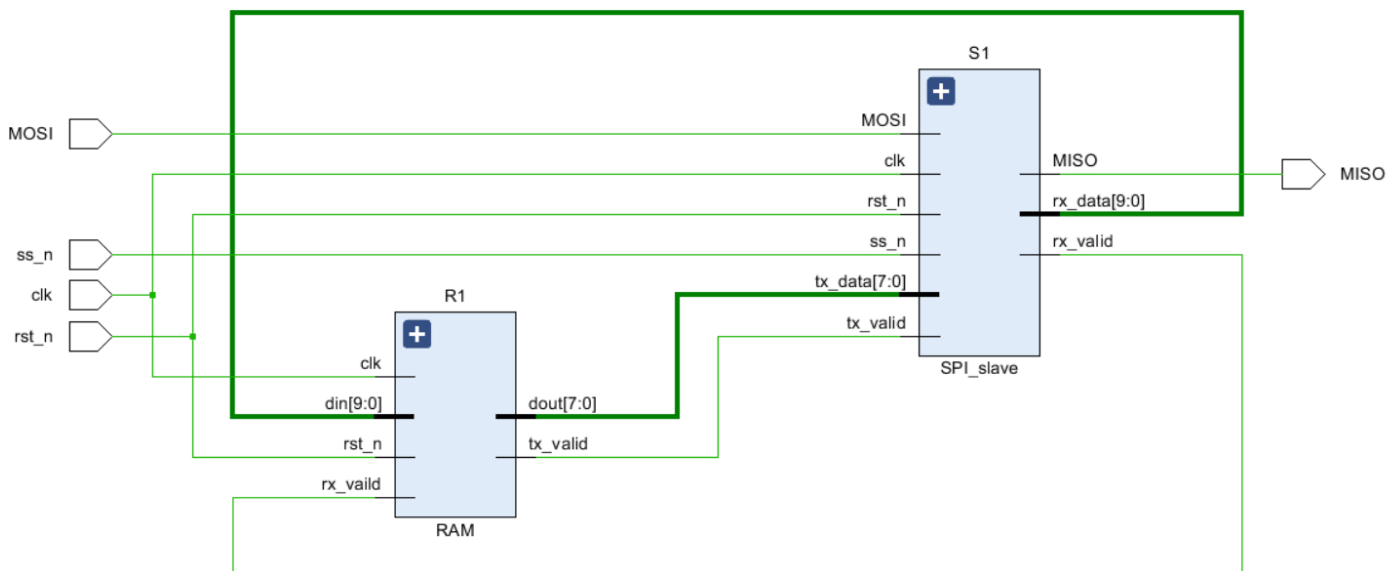
Transcript Message Viewer Lint Checks Design Metrics Design Information Status History Lint Dashboard

C:/Users/ABDOU/Desktop/Questa-20250315T193333Z-001/Questa/SPI\_w\_RAM.v [SPI\_w\_RAM]

## VIVADO

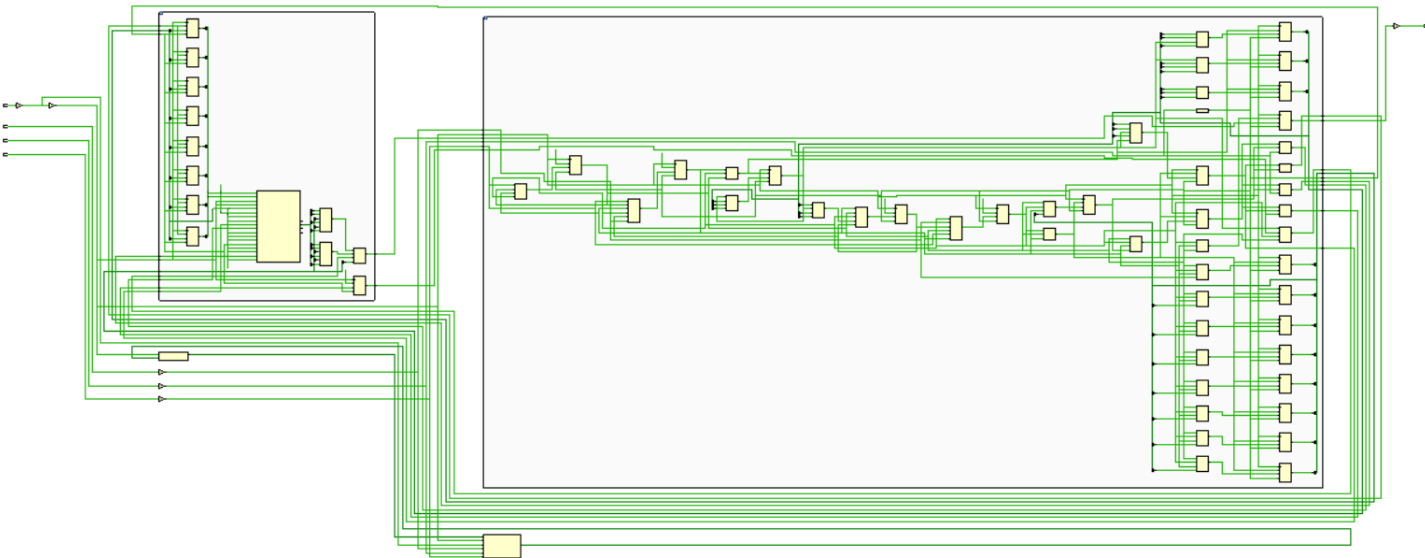
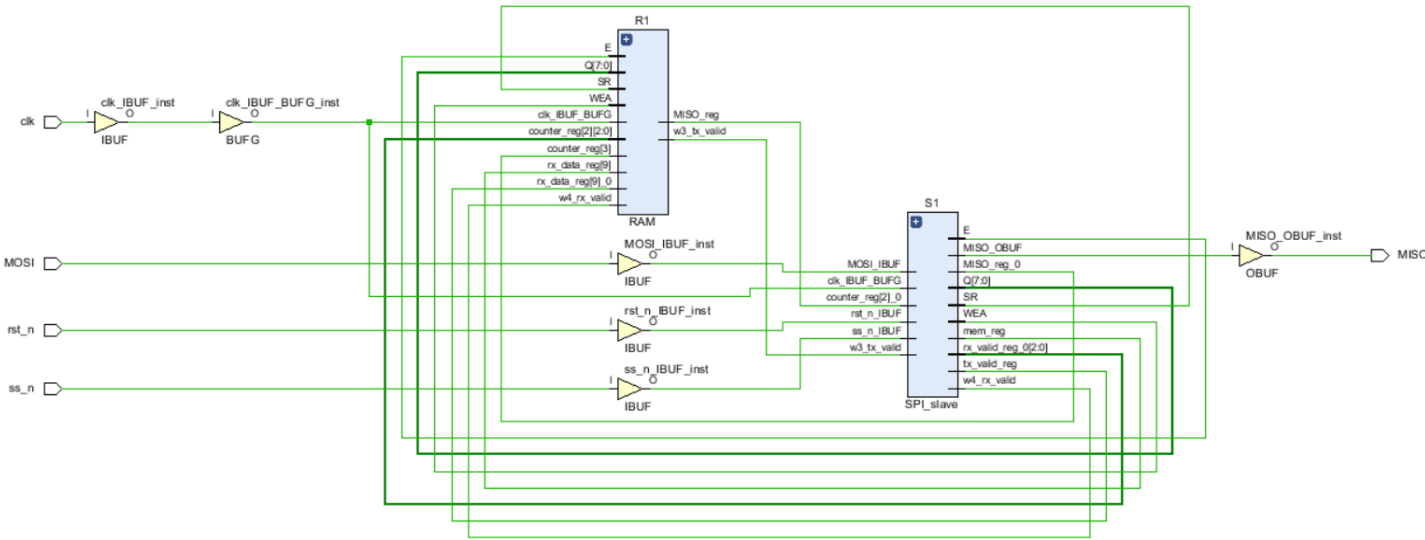
(\* fsm\_encoding = "gray" \*)

### Schematic elaboration





Schematic Synthesis

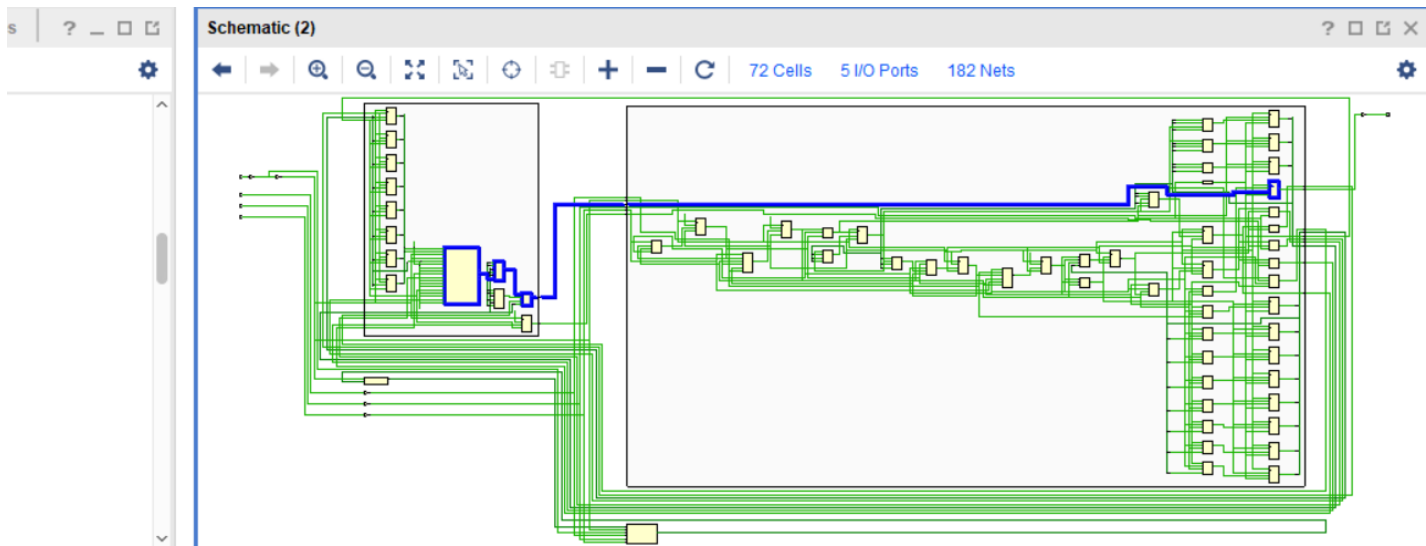


Encoding from report

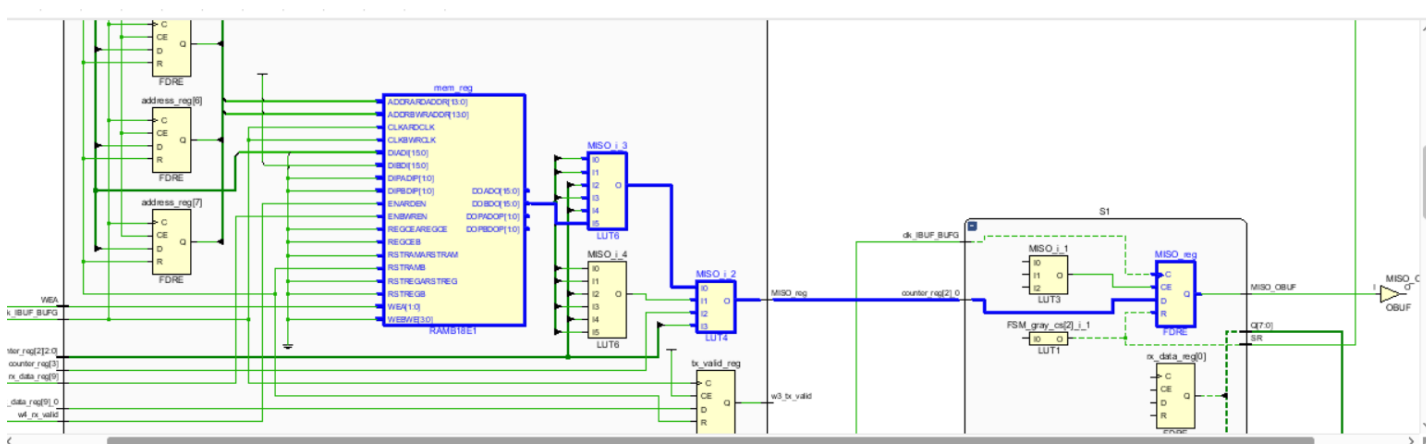
State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	011	010
READ_ADD	010	100
READ_DATA	111	011

Timing report

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.445 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	5.445	2	3	1	R1/mem_reg/CLKBWRLCK	S1/MISO_reg/D	4.404	2.702	1.702	10.0



General Information	Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Timer Settings	Path 1	5.445	2	3	1	R1/mem_reg/CLKBWRCLK	S1MISO_reg/D	4.404	2.702	1.702	
Design Timing Summary	Path 2	6.978	1	2	3	S1/rx_data_reg[9]/C	R1/mem_reg/WEA[0]	2.310	0.751	1.559	

## Implementation

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPI_w_RAM	28	29	9	28	17	0.5	5	1
I R1 (RAM)	3	9	3	3	0	0.5	0	0
I S1 (SPI_slave)	25	20	9	25	16	0	0	0

### Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.578 ns	Worst Hold Slack (WHS): 0.055 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 81	Total Number of Endpoints: 81	Total Number of Endpoints: 32

All user specified timing constraints are met.

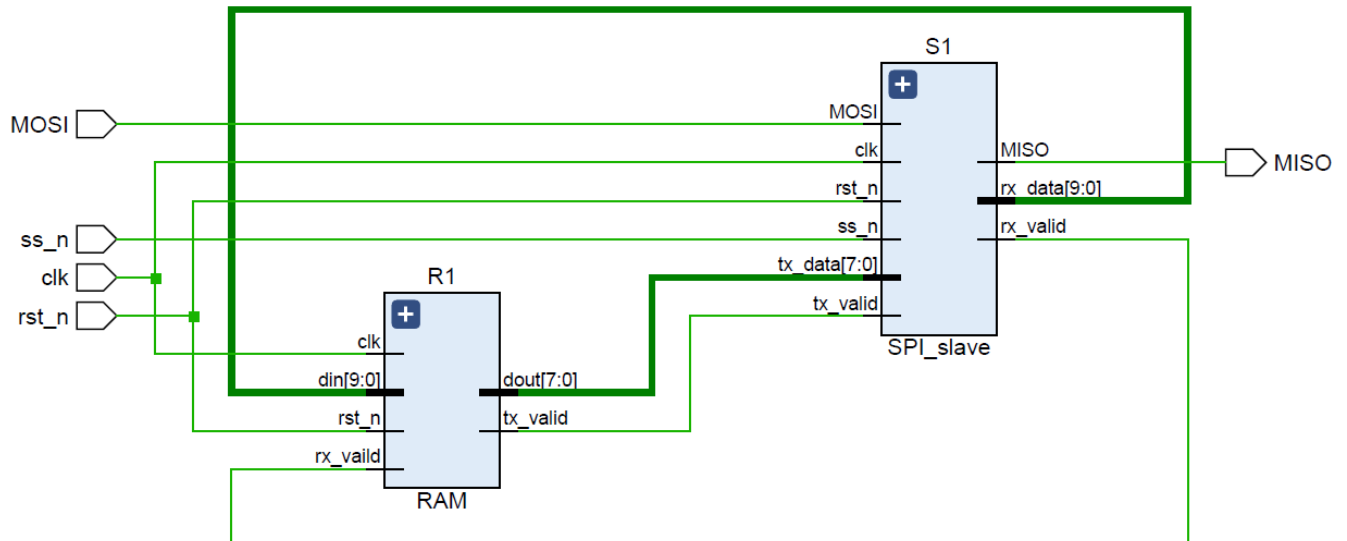
**Device:**

PRINTED DESIGN - xc7a35ticpg236-1L (active)

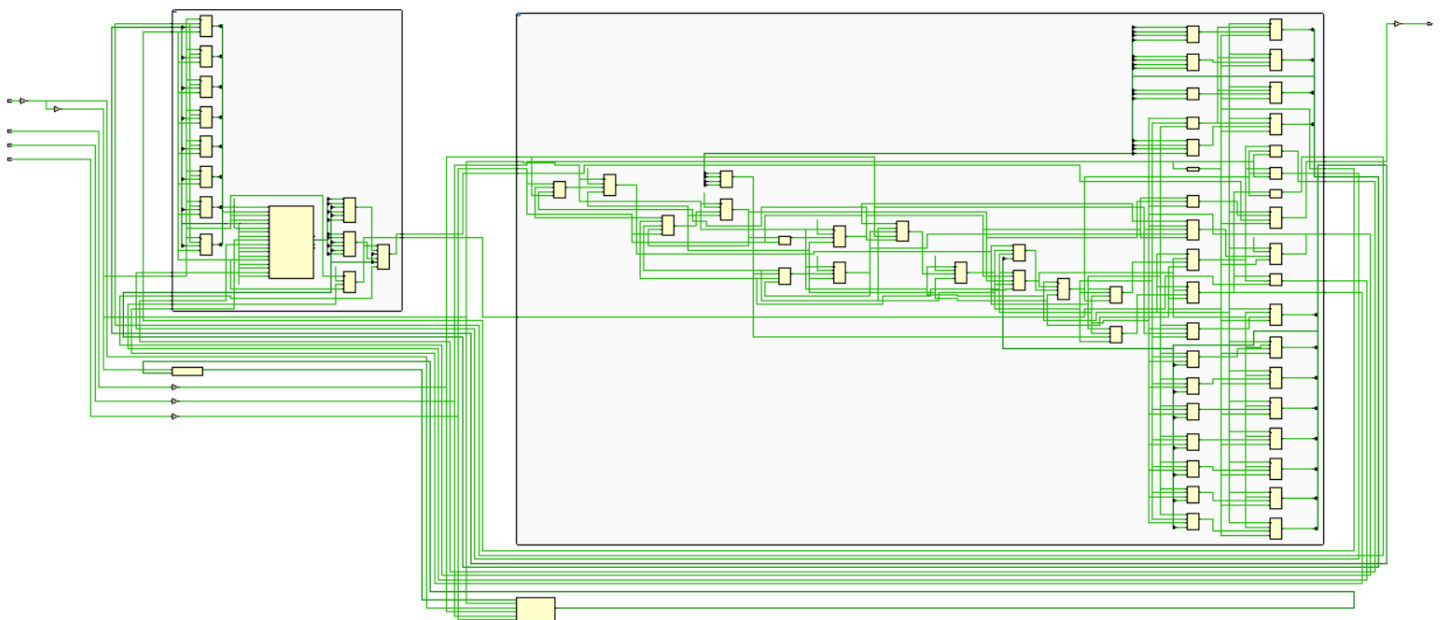


(\* fsm\_encoding = "one\_hot" \*)

## Elaborator



## Schematic Synthesis:



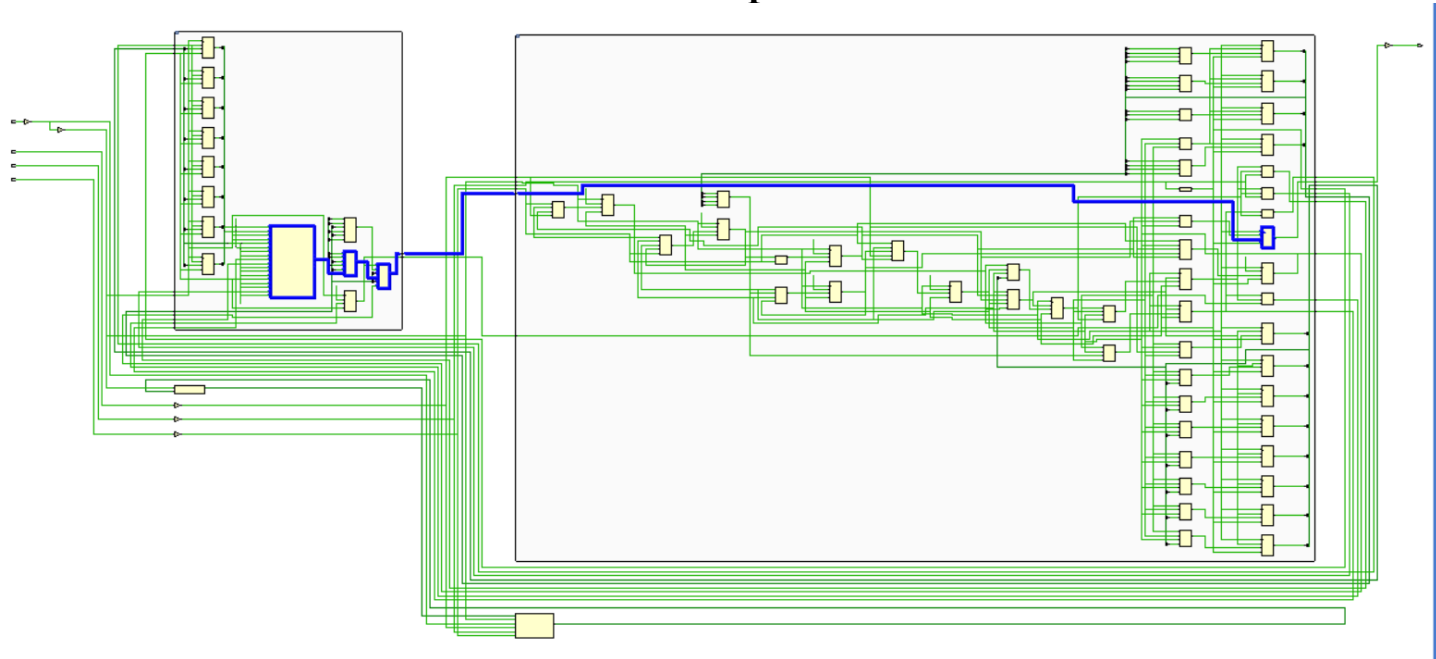
## Encoding Report:

State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
WRITE	00100	010
READ_ADD	01000	100
READ_DATA	10000	011

Timing report:

Design Timing Summary		
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.898 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns

Critical path



Implementation:

Reports

Design Runs

Power

Methodology

Timing

Utilization

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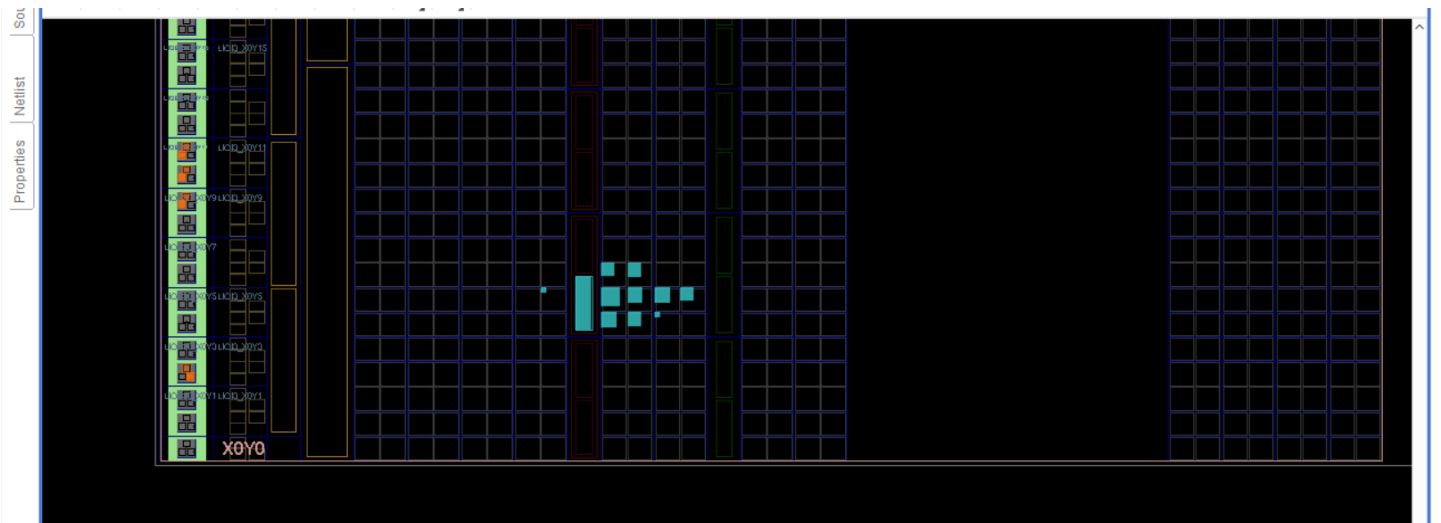
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Hierarchy

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPI_w_RAM		30	31	10	30	20	0.5	5	1
R1 (RAM)		3	9	4	3	0	0.5	0	0
S1 (SPI_slave)		27	22	9	27	19	0	0	0

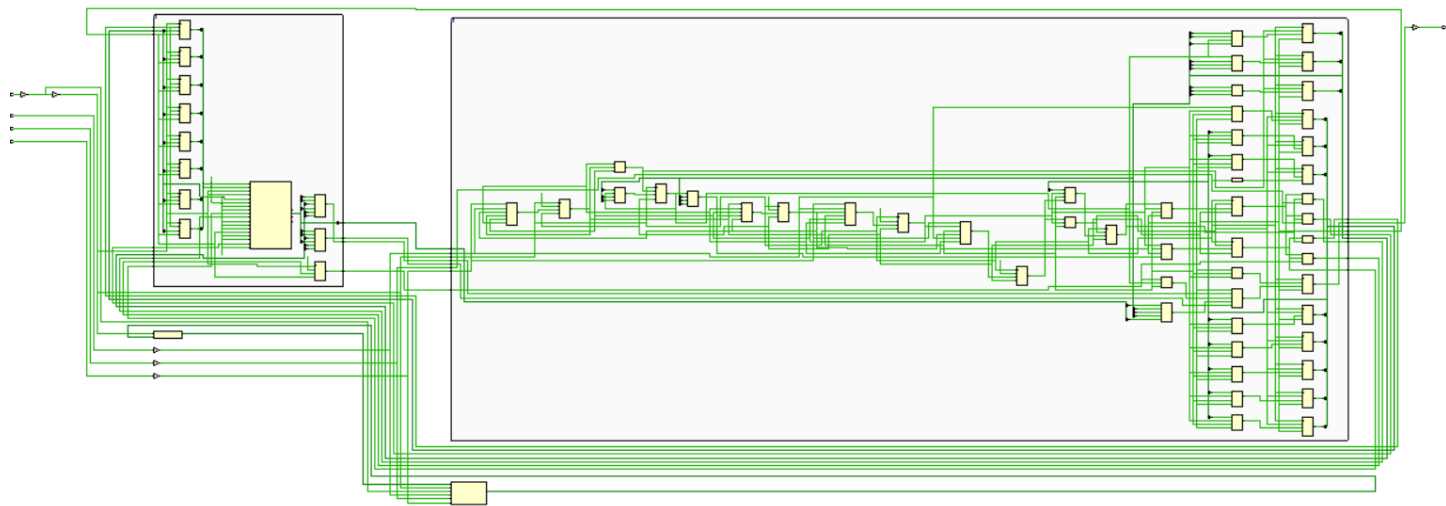
Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.414 ns	Worst Hold Slack (WHS): 0.047 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns



(\* fsm\_encoding = "sequential" \*)

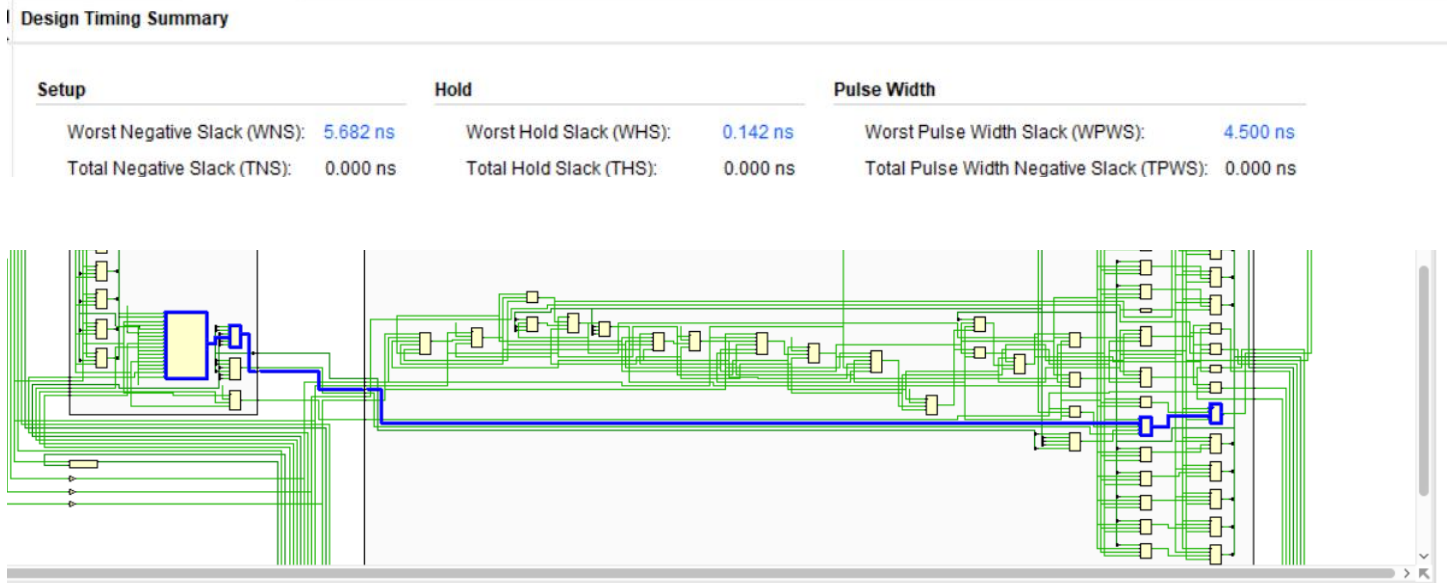
Synthesis Schema:



Encoding report

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	010	010
READ_ADD	011	100
READ_DATA	100	011

Timing report:

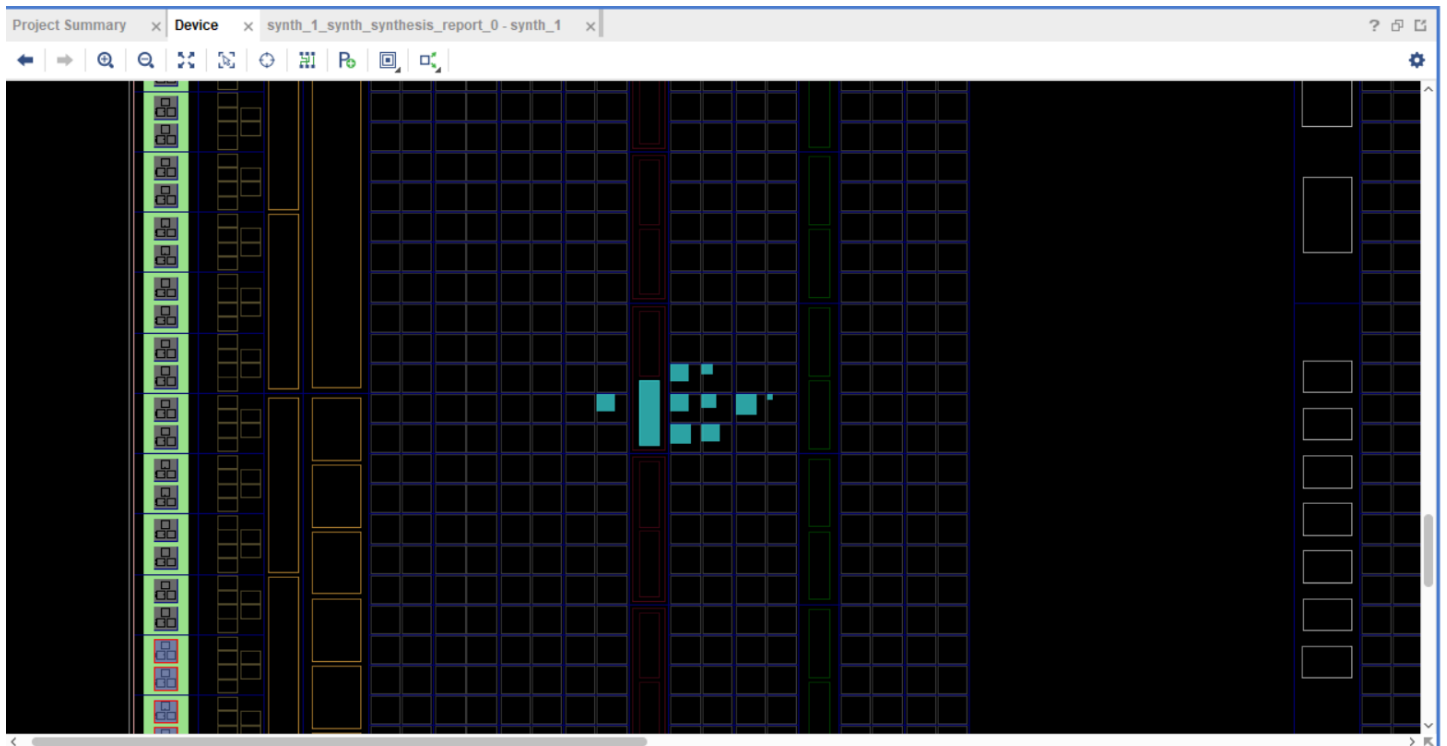


File	Messages	Log	Reports	Design Runs	Timing	x	?	_	□	⌵
Intra-Clock Paths - sys_clk_pin - Setup										
General Information										
Design Settings										
Design Timing Summary										
Clock Summary (1)										
Clock Timing (4)										
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	5.682	2	3	1	R1/mem_reg/CLKBWRCLK	S1/MISO_reg/D	4.167	2.702	1.465	
Path 2	6.978	1	2	3	S1/rx_data_reg[9]/C	R1/mem_reg/WEA[0]	2.310	0.751	1.559	
Path 3	6.978	1	2	3	S1/rx_data_reg[9]/C	R1/mem_reg/WEA[1]	2.310	0.751	1.559	
Path 4	7.067	1	2	3	S1/rx_data_reg[9]/C	R1/mem_reg/ENBWREN	2.310	0.751	1.559	

Implementation

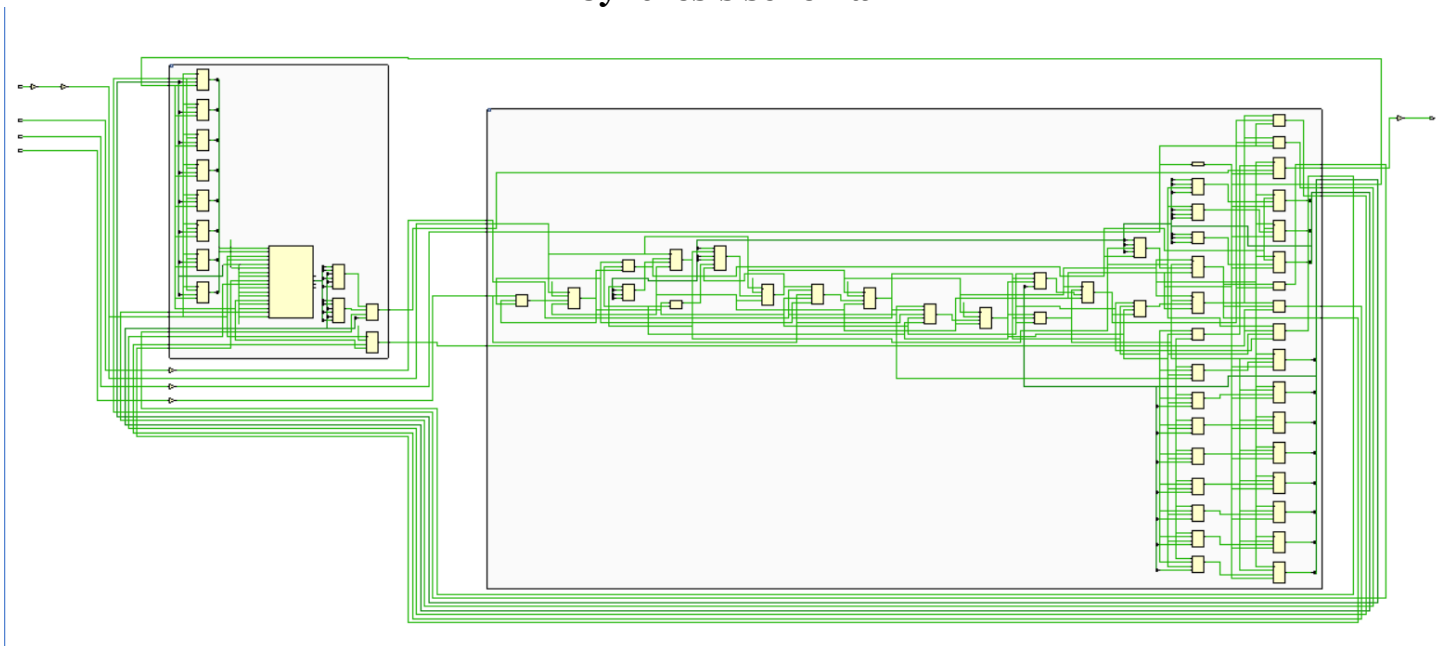
Reports	Design Runs	Power	Methodology	Timing	Utilization	x	?	_	□	⌵
Hierarchy										
Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)		
SPI_w_RAM	29	29	9	29	19	0.5	5	1		
R1 (RAM)	2	9	3	2	0	0.5	0	0		
S1 (SPI_slave)	27	20	8	27	19	0	0	0		

Reports	Design Runs	Power	Methodology	Timing	x	Utilization				
Design Timing Summary										
Setup			Hold			Pulse Width				
Worst Negative Slack (WNS): 5.503 ns			Worst Hold Slack (WHS): 0.044 ns			Worst Pulse Width Slack (WPWS): 4.500 ns				
Total Negative Slack (TNS): 0.000 ns			Total Hold Slack (THS): 0.000 ns			Total Pulse Width Negative Slack (TPWS): 0.000 ns				
Number of Failing Endpoints: 0			Number of Failing Endpoints: 0			Number of Failing Endpoints: 0				



(\* fsm\_encoding = "johnson" \*)

### Synthesis schema





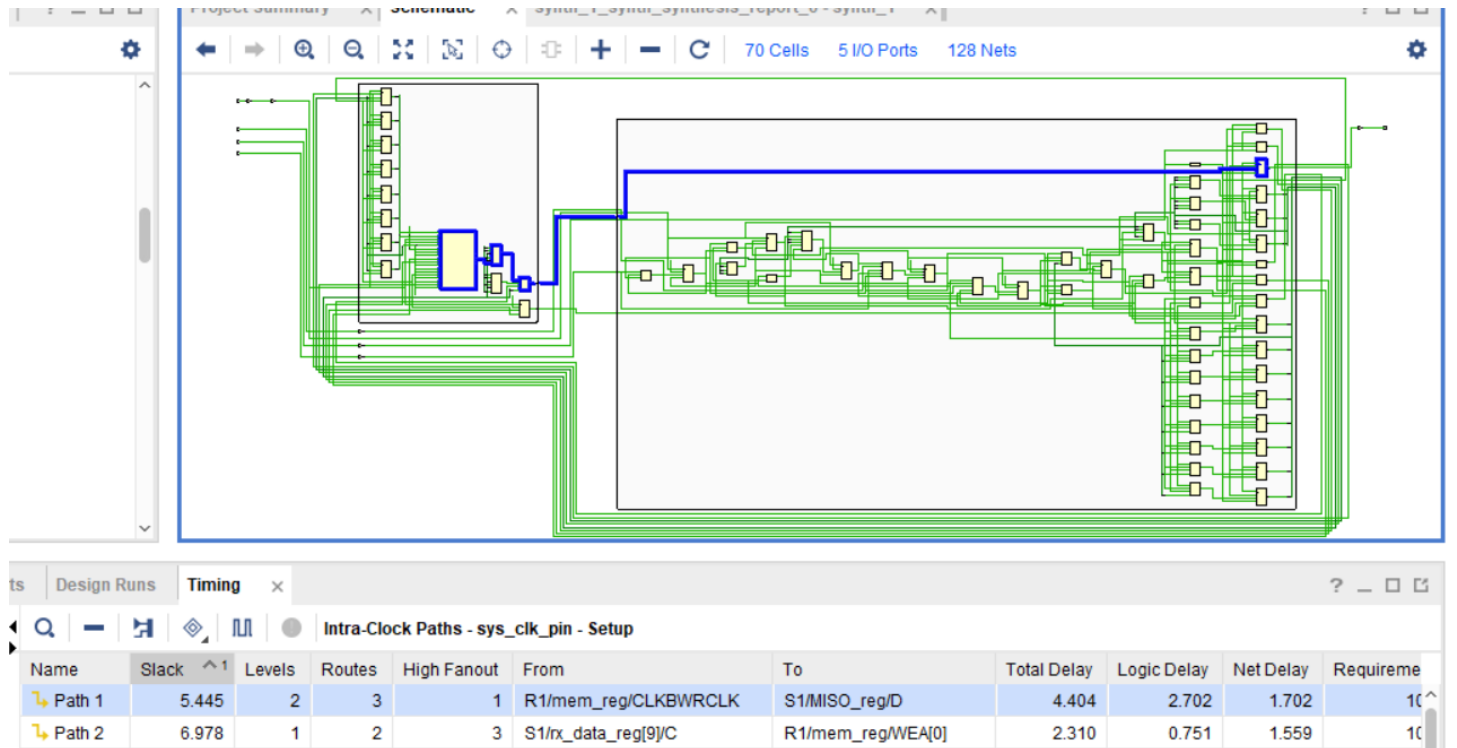
## Encoding Report:

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	100	001
WRITE	110	010
READ_ADD	111	100
READ_DATA	011	011

## Timing report

### Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.445 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns



## Implementation

Reports

Design Runs

Power

Methodology

Timing

Utilization

X

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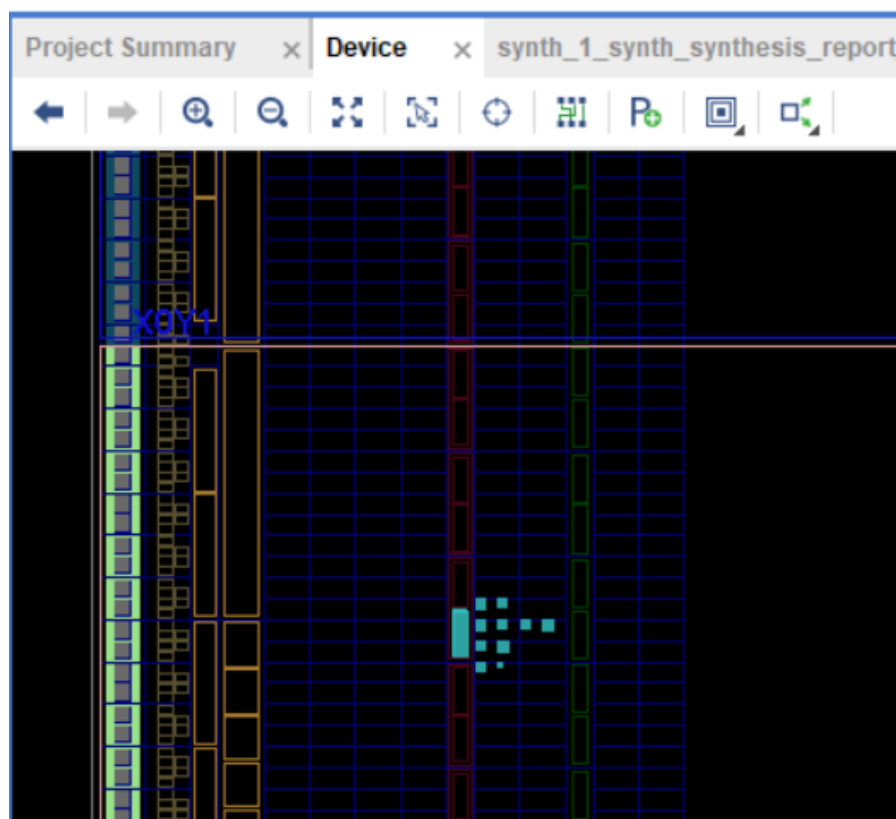
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Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPI_w_RAM	29	29	10	29	18	0.5	5	1
I R1 (RAM)	3	9	4	3	0	0.5	0	0
I S1 (SPI_slave)	26	20	9	26	17	0	0	0

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.635 ns	Worst Hold Slack (WHS): 0.044 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns



write\_bitstream Complete ✓

