CY8C201xx Register Reference Guide

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Contents

1. Register Map and Reference

This chapter is a reference for all the CapSense Express™ registers in address order. The most detailed descriptions of the CapSense Express registers are in the Register Definitions section of each chapter.

1.1 Maneuvering Around the Registers

For ease-of-use, this chapter has been formatted so that there is one register per page, although some registers use two pages. On each page, from top to bottom, there are four sections:

1. Register name and address (from lowest to highest).
2. Register table showing the bit organization, with reserved bits grayed out.
3. Written description of register specifics or links to additional register information.
4. Detailed register bit descriptions.

Use the register tables, in addition to the detailed register bit descriptions, to determine which bits are reserved. Reserved bits are grayed table cells and are not described in the bit description section. Reserved bits must always be written with a value of '0'.

1.2 Register Conventions

This table lists the register conventions that are specific to this chapter.

Table 1-1. Register Conventions

Convention	Example	Description
'x' in a register name	PRTxIE	Multiple instances/address ranges of the same register
R	R : 00	Read register or bit(s)
W	W : 00	Write register or bit(s)
WP	WPR: 00	Write register with passcode
O	RO : 00	Only a read/write register or bit(s).
L	RL : 00	Logical register or bit(s)
C	RC : 00	Clearable register or bit(s)
00	RW : 00	FD value is 0x00 or 00h
FD		Factory default value of the register
Empty, grayed-out table cell		Reserved bit or group of bits, unless otherwise stated

Table 1-2. Register Map User Space

Name	Addr (0,Hex)	Access	Page	Name	Addr (0,Hex)	Access	Page	Name	Addr (0,Hex)	Access	Page	Name	Addr (0,Hex)	Access	Page
INPUT_PORT0	00	R	7	OPR1_PRT0_12	40	RW	26	SLEEP_SA_CTR	80	RW	50		C0		
INPUT_PORT1	01	R	7	OPR1_PRT1_12	41	RW	27	CS_READ_BUTTON	81	RW	51		C1		
STATUS_PORT0	02	R	8	OPR2_PRT0_12	42	RW	28	CS_READ_BL	82	R	52		C2		
STATUS_PORT1	03	R	8	OPR2_PRT1_12	43	RW	29		83		52		C3		
OUTPUT_PORT0	04	W	9	OP_SEL_13	44	RW	24	CS_READ_DIFF	84	R	53		C4		
OUTPUT_PORT1	05	W	9	OPR1_PRT0_13	45	RW	26		85		53		C5		
CS_ENABLE0	06	RW	10	OPR1_PRT1_13	46	RW	27	CS_READ_RAW	86	R	54		C6		
CS_ENABLE1	07	RW	10	OPR2_PRT0_13	47	RW	29		87		54		C7		
GPIO_ENABLE0	08	RW	11	OPR2_PRT1_13	48	RW	29	CS_READ_STATUS	88	R	55		C8		
GPIO_ENABLE1	09	RW	11	OP_SEL_14	49	RW	24		89		55		C9		
INVERSION_MASK0	0A	RW	12	OPR1_PRT0_14	4A	RW	26	CS_READ_CEN_POS	8A	R	56		CA		
INVERSION_MASK1	0B	RW	12	OPR1_PRT1_14	4B	RW	27		8B		56		CB		
INT_MASK0	0C	RW	13	OPR2_PRT0_14	4C	RW	28	CS_READ_CEN_PEAK	8C	R	57		CC		
INT_MASK1	0D	RW	13	OPR2_PRT1_14	4D	RW	29		8D		57		CD		
STATUS_HOLD_MSK0	0E	RW	14	CS_NOISE_TH	4E	RW	30		8E				CE		
STATUS_HOLD_MSK1	0F	RW	14	CS_BL_UPD_TH	4F	RW	31		8F				CF		
DM_PULL_UP0	10	RW	16	CS_SETL_TIME	50	RW	32		90				D0		
DM_STRONG0	11	RW	17	CS_OTH_SET	51	RW	33		91				D1		
DM_HIGHZ0	12	RW	18	CS_HYSTERISIS	52	RW	34		92				D2		
DM_OD_LOW0	13	RW	19	CS_DEBOUNCE	53	RW	35		93				D3		
DM_PULL_UP1	14	RW	16	CS_NEG_NOISE_TH	54	RW	36		94				D4		
DM_STRONG1	15	RW	17	CS_LOW_BL_RST	55	RW	37		95				D5		
DM_HIGHZ1	16	RW	18	CS_FILTERING	56	RW	38		96				D6		
DM_OD_LOW1	17	RW	26	CS_SCAN_POS_00	57	RW	39		97				D7		
PWM_ENABLE0	18	RW	20	CS_SCAN_POS_01	58	RW	39		98				D8		
PWM_ENABLE1	19	RW	20	CS_SCAN_POS_02	59	RW	39		99				D9		
PWM_MODE_DC	1A	RW	21	CS_SCAN_POS_03	5A	RW	39		9A				DA		
PWM_DELAY	1B	RW	23	CS_SCAN_POS_04	5B	RW	39		9B				DB		
OP_SEL_00	1C	RW	24	CS_SCAN_POS_10	5C	RW	39		9C				DC		
OPR1_PRT0_00	1D	RW	26	CS_SCAN_POS_11	5D	RW	39		9D				DD		
OPR1_PRT1_00	1E	RW	27	CS_SCAN_POS_12	5E	RW	39		9E				DE		
OPR2_PRT0_00	1F	RW	28	CS_SCAN_POS_13	5F	RW	39		9F				DF		
OPR2_PRT1_00	20	RW	29	CS_SCAN_POS_14	60	RW	39	COMMAND_REG	A0	W	58		E0		
OP_SEL_01	21	RW	24	CS_FINGER_TH_00	61	RW	40		A1				E1		
OPR1_PRT0_01	22	RW	26	CS_FINGER_TH_01	62	RW	40		A2				E2		
OPR1_PRT1_01	23	RW	27	CS_FINGER_TH_02	63	RW	40		A3				E3		
OPR2_PRT0_01	24	RW	28	CS_FINGER_TH_03	64	RW	40		A4				E4		
OPR2_PRT1_01	25	RW	29	CS_FINGER_TH_04	65	RW	40		A5				E5		
OP_SEL_02	26	RW	24	CS_FINGER_TH_10	66	RW	40		A6				E6		
OPR1_PRT0_02	27	RW	26	CS_FINGER_TH_11	67	RW	40		A7				E7		
OPR1_PRT1_02	28	RW	27	CS_FINGER_TH_12	68	RW	40		A8				E8		
OPR2_PRT0_02	29	RW	28	CS_FINGER_TH_13	69	RW	40		A9				E9		
OPR2_PRT1_02	2A	RW	29	CS_FINGER_TH_14	6A	RW	40		AA				EA		
OP_SEL_03	2B	RW	24	CS_IDAC_00	6B	RW	41		AB				EB		
OPR1_PRT0_03	2C	RW	26	CS_IDAC_01	6C	RW	41		AC				EC		
OPR1_PRT1_03	2D	RW	27	CS_IDAC_02	6D	RW	41		AD				ED		
OPR2_PRT0_03	2E	RW	28	CS_IDAC_03	6E	RW	41		AE				EE		
OPR2_PRT1_03	2F	RW	29	CS_IDAC_04	6F	RW	41		AF				EF		
OP_SEL_04	30	RW	24	CS_IDAC_10	70	RW	41		B0				F0		
OPR1_PRT0_04	31	RW	27	CS_IDAC_11	71	RW	41		B1				F1		
OPR1_PRT1_04	32	RW	27	CS_IDAC_12	72	RW	41		B2				F2		
OPR2_PRT0_04	33	RW	28	CS_IDAC_13	73	RW	41		B3				F3		
OPR2_PRT1_04	34	RW	29	CS_IDAC_14	74	RW	41		B4				F4		
OP_SEL_10	35	RW	24	CS_SLID_CONFIG	75	RW	42		B5				F5		
OPR1_PRT0_10	36	RW	26		76				B6				F6		
OPR1_PRT1_10	37	RW	27	CS_SLID_MULM	77	RW	43		B7				F7		
OPR2_PRT0_10	38	RW	28	CS_SLID_MULL	78	RW	43		B8				F8		
OPR2_PRT1_10	39	RW	29	I2C_DEV_LOCK	79	RW	44		B9				F9		
OP_SEL_11	3A	RW	24	DEVICE_ID	7A	R	45		BA				FA		
OPR1_PRT0_11	3B	RW	26	DEVICE_STATUS	7B	R			BB				FB		
OPR1_PRT1_11	3C	RW	27	I2C_ADDR_DM	7C	RW	47		BC				FC		
OPR2_PRT0_11	3D	RW	28		7D				BD				FD		
OPR2_PRT1_11	3E	RW	29	SLEEP_PIN	7E	RW	48		BE				FE		
OP_SEL_12	3F	RW	24	SLEEP_CTRL	7F	RW	49		BF				FF		

Gray fields are reserved. # Access is bit specific.

1.3 GPIO Status Registers

1.3.1 INPUT_PORTx

Input Port 0/1 Registers

Individual Register Names and Addresses:

INPUT_PORT0 : 00h INPUT_PORT1 : 01h

	7	6	5	4	3	2	1	0
Access : FD				R : 00				
Bit Name				GP[4:0]				

The Input Port registers represent the actual logical levels on the pins and are used for I/O port reading operations. For CapSense® pins, they represent the status of the sensor, ON (1) or OFF (0).

The Inversion registers (0Ah-0Bh) change the state of reads from these ports.

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of '0'.

Bit	Name	Description
4:0	**GP[4:0]**	For GPIOs, these bits represent the read value from port. For CapSense pins: 0 Sensor OFF. 1 Sensor ON.

1.3.2 STATUS_PORTx

Status Since Last Read Port 0/1 Registers

Individual Register Names and Addresses:

STATUS_PORT0 : 02h STATUS_PORT1 : 03h

	7	6	5	4	3	2	1	0
Access : FD				R : 00				
Bit Name				GP[4:0]				

These registers hold the port bit status in the corresponding line since the last read of the register. The status latch direction can be set in registers 0Eh-0Fh. Bits in the STATUS_PORTx registers are reset to the opposite of registers 0Eh-0Fh after a read of or write to registers 0Eh-0Fh.

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
4:0	**GP[4:0]**	Status of the port pins since last read of the register.

1.3.3 OUTPUT_PORTx

Output Port 0/1 Registers

Individual Register Names and Addresses:

OUTPUT_PORT0 : 04h OUTPUT_PORT1 : 05h

	7	6	5	4	3	2	1	0
Access : FD				W : 00				
Bit Name				GP[4:0]				

These registers are used to write data to GPIO ports. By default, both ports are in high Z mode. Pins defined as CapSense inputs or as output of combinational logic (see registers 1Ch-4Dh) cannot be set using this register.

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of '0'.

Bit	Name	Description
4:0	**GP[4:0]**	A bit set in this register sets the logic level of the output (depending on the drive mode selected as per Table 1-3, "Drive Mode Registers," on page 16). 0 0 logic level. 1 1 logic level.

1.4 GPIO Setting Registers

1.4.1 CS_ENABLEx

Select CapSense Input Port 0/1 Registers

Individual Register Names and Addresses:

CS_ENABLE0 : 06h CS_ENABLE1 : 07h

	7	6	5	4	3	2	1	0
Access : FD				RW : 00				
Bit Name				GP[4:0]				

These registers select which pins of the two ports are to be used as CapSense inputs. If a pin is selected as CapSense input, its configuration in registers 0Ch -0Dh (Interrupt Masks) and 10h-17h (Drive Modes) is ignored.

It is mandatory that you set these registers before finger threshold and IDAC setting (registers 61h to 6Ah and 6Bh to 74h) registers are set.

A pin enabled for CapSense cannot be enabled for GPIO. If a pin needs to be changed from CapSense to GPIO, it first has to be disabled from CapSense and then enabled to GPIO.

Further CapSense pin parameters are configurable in subsequent registers.

These registers have read only access in "Normal Operation Mode" and read/write access in "Setup Operation Mode" (also see the COMMAND_REG register on page 58).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
4:0	**GP[4:0]**	These bits are used for selecting the pins of two ports to be used as CapSense inputs. 0 Disable CapSense input. 1 Enable CapSense input.

1.4.2 GPIO_ENABLEx

Select Enabled GPIO Port 0/1 Registers

Individual Register Names and Addresses:

GPIO_ENABLE0 : 08h GPIO_ENABLE1 : 09h

	7	6	5	4	3	2	1	0
Access : FD				RW : 00				
Bit Name				GP[4:0]				

These registers are used to select which pins of each port are enabled as GPIO.

Pins not enabled are tri-stated.

A pin enabled for GPIO cannot be enabled for CapSense. If a pin needs to be changed from GPIO to CapSense, it first has to be disabled from GPIO and then enabled to CapSense.

These registers have read only access in "Normal Operation Mode" and read/write access in "Setup Operation Mode" (also see the COMMAND_REG register on page 58).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
4:0	**GP[4:0]**	These bits are used for selecting the pins of each port enabled as GPIO. 0 Disable GPIO. 1 Enable GPIO.

1.4.3 INVERSION_MASKx

Inversion Port 0/1 Registers

Individual Register Names and Addresses:

INVERSION_MASK0 : 0Ah INVERSION_MASK1 : 0Bh

	7	6	5	4	3	2	1	0
Access : FD				RW : 00				
Bit Name				GP[4:0]				

These registers invert the logic of the input ports and also of the “Status since last read” registers. Each ‘1’ written to this register inverts the logic of the corresponding bit in the Input/Status register of the related port. This register is also used to invert the inputs and outputs for the logic operations of the I/O and CapSense pins (see registers 1Ch, 4Eh).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
4:0	**GP[4:0]**	These bits invert the logic of the input ports and status since last read registers. 0 No inversion. 1 Inversion.

1.4.4 INT_MASKx

Interrupt Mask Port 0/1 Registers

Individual Register Names and Addresses:

INT_MASK0 : 0Ch INT_MASK1 : 0Dh

	7	6	5	4	3	2	1	0
Access : FD				RW : 00				
Bit Name				GP[4:0]				

The INT_MASKx registers are used to set which GPIO (not CapSense pins) can generate internal hardware interrupts on 0-1 and 1-0 transitions. Its main purpose is to enable wakeup from sleep upon GPIO changes. If a pin is to be configured for an interrupt, it should be enabled as a GPIO using the GPIO_ENABLEx Register, and the corresponding mask bit in this INT_MASKx register should be written with a value '1'.

In addition, if a pin is configured as a sleep control pin using the SLEEP_PIN register, the corresponding bit in the INT_MASK is automatically enabled.

These registers have read only access in "Normal Operation Mode" and read/write access in "Setup Operation Mode" (also see the COMMAND_REG register on page 58).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description	
4:0	**GP[4:0]**	0	GPIO disabled to generate internal hardware interrupts on 0-1 and 1-0 transitions.
		1	GPIO enabled to generate internal hardware interrupts on 0-1 and 1-0 transitions.

1.4.5 STATUS_HOLD_MSKx

Port Status Hold Mask Port 0/1 Registers

Individual Register Names and Addresses:

STATUS_HOLD_MSK0 : 0Eh STATUS_HOLD_MSK1 : 0Fh

	7	6	5	4	3	2	1	0
Access : FD				RW : 03/1F[1]				
Bit Name				GP[4:0]				

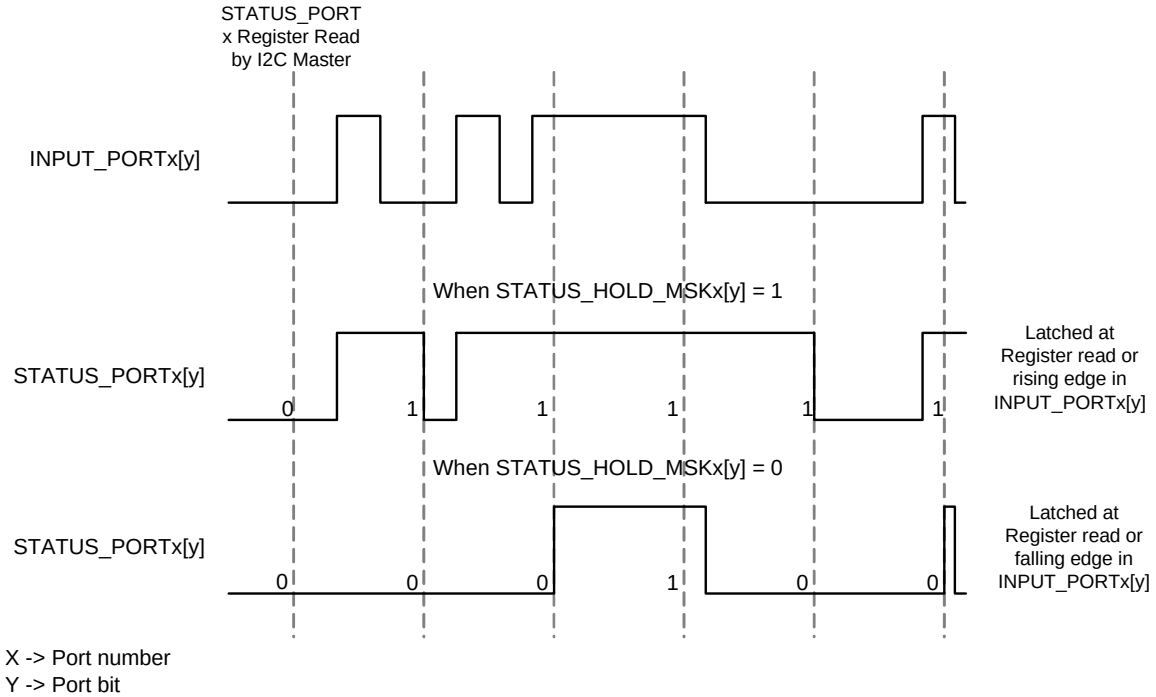
1. 03 is for CY8C20142 part only

These registers are used to define the value to be held (0 or 1) in registers 02h-03h until the next read. They set the latch direction of registers 02h-03h. This register can be written with a value of 1 only if the corresponding pin is enabled either as a GPIO or as a CapSense button. Else, this register will always return 0.

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of '0'.

Bit	Name	Description
4:0	**GP[4:0]**	These bits are used to set the latch direction of registers 02h-03h.

Figure 1-1. Latch Direction of STATUS_PORTx Register



1.5 Drive Mode Registers

Each port's data pin can be set separately to one of four available drive modes. To perform this configuration, the four drive mode registers are used. Each '1' written to this register changes the corresponding line drive mode. Registers 10h through 17h have last-register priority meaning that the bit set to high in which the last register was written will overwrite those that came before. Reading these registers reflects the actual setting, not what was originally written.

The register settings for bits assigned to CapSense inputs are ignored. Table 1-3 summarizes the drive mode register settings.

Table 1-3. Drive Mode Registers

Register	Pin State	Description
10h/14h	Resistive Pull Up	Resistive High, Strong Low (Default)
11h/15h	Strong Drive	Strong High, Strong Low
12h/16h	High Impedance	High Z - Analog
13h/17h	Open Drain Low	Strong Low, High Z High

Note To enable a GPIO pin for digital input, set it to drive mode open drain low or resistive pull up with its corresponding output registers 04h-05h set to '1'. The high impedance drive mode is used only for analog input (e.g., CapSense) and disconnects the pin from the internal digital bus.

1.5.1 DM_PULL_UPx

Pull Up Port 0/1 Registers

Individual Register Names and Addresses:

DM_PULL_UP0 : 10h DM_PULL_UP1 : 14h

	7	6	5	4	3	2	1	0
Access : FD				RW : 00				
Bit Name				GP[4:0]				

These registers have read only access in "Normal Operation Mode" and read/write access in "Setup Operation Mode" (also see the COMMAND_REG register on page 58).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of '0'.

Bit	Name	Description
4:0	**GP[4:0]**	These bits are used to set the pull up drive mode for the port pins. 0 1 Enables pull up drive mode.

1.5.2 DM_STRONGx

Strong Port 0/1 Registers

Individual Register Names and Addresses:

DM_STRONG0 : 11h DM_STRONG1 : 15h

	7	6	5	4	3	2	1	0
Access : FD				RW : 00				
Bit Name				GP[4:0]				

These registers have read only access in "Normal Operation Mode" and read/write access in "Setup Operation Mode" (also see the COMMAND_REG register on page 58).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
4:0	**GP[4:0]**	These bits are used to set the strong mode for the port pins. 0 1 Enables strong drive mode.

1.5.3 DM_HIGHZx

High Z Port 0/1 Registers

Individual Register Names and Addresses:

DM_HIGHZ0 : 12h DM_HIGHZ1 : 16h

	7	6	5	4	3	2	1	0
Access : FD				RW : 00				
Bit Name				GP[4:0]				

These registers have read only access in "Normal Operation Mode" and read/write access in "Setup Operation Mode" (also see the COMMAND_REG register on page 58).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
4:0	**GP[4:0]**	These bits are used to set the high Z mode for the port pins. 0 1 Enables high Z drive mode.

1.5.4 DM_OD_LOWx

Open Drain Low Port 0/1 Registers

Individual Register Names and Addresses:

DM_OD_LOW0 : 13h DM_OD_LOW1 : 17h

	7	6	5	4	3	2	1	0
Access : FD				RW : 00				
Bit Name				GP[4:0]				

These registers have read only access in "Normal Operation Mode" and read/write access in "Setup Operation Mode" (also see the COMMAND_REG register on page 58).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
4:0	**GP[4:0]**	These bits are used to set the open drain low mode for the port pins. 0 1 Enables open drain low drive mode.

1.6 PWM Output Registers

1.6.1 PWM_ENABLEx

PWM Enable 0/1 Registers

Individual Register Names and Addresses:

PWM_ENABLE0 : 18h PWM_ENABLE1 : 19h

	7	6	5	4	3	2	1	0
Access : FD				RW : 00				
Bit Name				GP[4:0]				

These registers are used to select which GPIO pins are enabled for PWM output. Only pins that have been enabled for GPIO can be enabled for PWM output. These GPIO pins must be previously enabled by writing to the GPIO_ENABLEx register on page 11. For pins enabled as PWM, their output is set to 0, 1, or the PWM signal, depending on the PWM configuration (PWM_MODE_DC register on page 21) and the output settings.

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
4:0	**GP[4:0]**	These bits are used to select which GPIO pins are enabled for PWM output. 0 Disable PWM output. 1 Enable PWM output.

1.6.2 PWM_MODE_DC

PWM Mode and Duty Cycle Configuration Register

Individual Register Names and Addresses:

PWM_MODE_DC : 1Ah

	7	6	5	4	3	2	1	0
Access : FD	RW : 00		RW : 00	RW : 00	RW : 00			
Bit Name	Mode[1:0]		0/1 Link	Apply Delay	Duty Cycle[3:0]			

This register controls PWM mode output and duty cycle.

Bit	Name	Description
7:6	**Mode[1:0]**	Used to select the PWM mode of operation. 00 **Normal mode**. PWM output is activated and released the same time as the source event (e.g., a button press). 01 **Single Flash mode**. PWM output is activated by one transition event (a button press or release) and released automatically after the delay (PWM_DELAY register on page 23) has elapsed (20 ms to 5s). In case the reverse transition event occurs before the delay has elapsed, the PWM output is released at the same time. 10 **Delayed Transition mode**. PWM output is activated by one transition event (e.g., a button press or release) and released after the reverse transition event and the delay (PWM_DELAY register on page 23) has elapsed (20 ms to 5s). 11 **Toggle Flip-Flop mode**. PWM output is activated and released alternately only at one of the two transition events (e.g., a button press or release).
5	**0/1 Link**	Used to select the link between 0/1 logic state of the pin and the PWM/logic level of the output. 0 Pin state 0 = output level 0 (0% duty cycle). Pin state 1 = output PWM signal (selected duty cycle). 1 Pin state 0 = output PWM signal (selected duty cycle). Pin state 1 = output level 1 (100% duty cycle).
4	**Apply Delay**	Used to select whether to apply the delay value (for Flash and Delayed Transition modes) to the PWM output ‘0’ or the logic level output ‘1’. This bit has no effect on Normal and Toggle Flip-Flop modes.
3:0	**Duty Cycle[3:0]**	Used to select among 15 duty cycles (duty cycle is defined as the “high” time write to the full PWM signal period). See the following table:

(continued on next page)

1.6.2 PWM_MODE_DC *(continued)*

Bit 3	Bit 2	Bit 1	Bit 0	HEX	DC%
0	0	0	0	0x0	Reserved
0	0	0	1	0x1	2.5
0	0	1	0	0x2	5
0	0	1	1	0x3	10
0	1	0	0	0x4	15
0	1	0	1	0x5	22.5
0	1	1	0	0x6	30
0	1	1	1	0x7	45
1	0	0	0	0x8	55
1	0	0	1	0x9	70
1	0	1	0	0xA	77.5
1	0	1	1	0xB	85
1	1	0	0	0xC	90
1	1	0	1	0xD	95
1	1	1	0	0xE	97.5
1	1	1	1	0xF	99.5

1.6.3 PWM_DELAY

PWM Delay Register

Individual Register Names and Addresses:

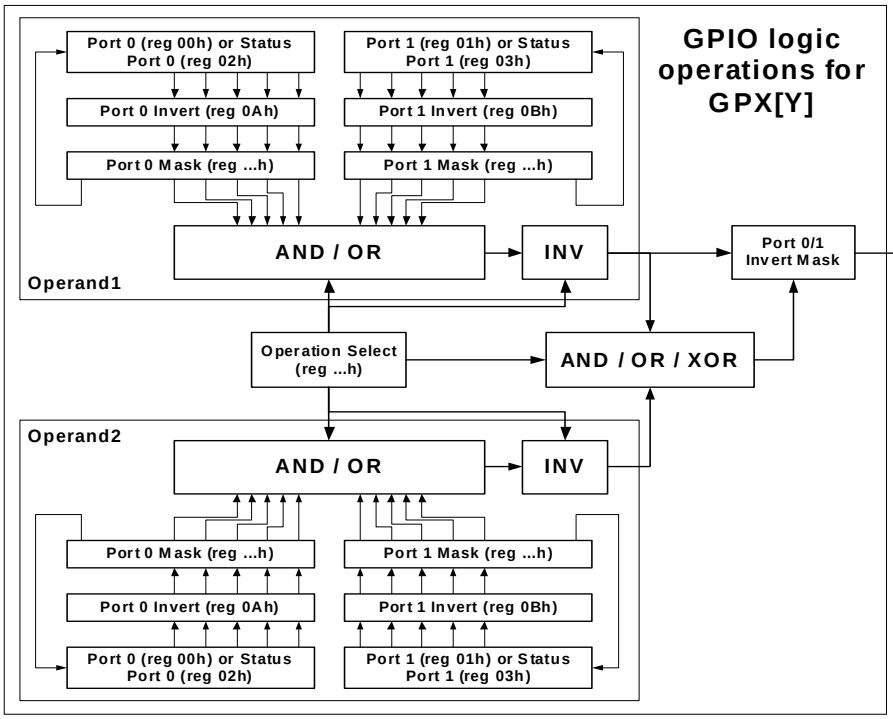
PWM_DELAY : 1Bh

	7	6	5	4	3	2	1	0
Access : FD	RW : 00							
Bit Name	Delay[7:0]							

This register sets the delay value for Normal mode (‘01’) and Single Flash mode (‘10’) in increments of approximately 20 ms. The minimum value is 0, and the maximum value is 0xFE (~5s). The value 0xFF indicates an indefinite delay.

Bit	Name	Description
7:0	**Delay[7:0]**	Sets the delay value for Normal mode (‘01’) and Single Flash mode (‘10’) in increments of approximately 20 ms.

1.7 Output Control Setting Registers



Registers Summary

GPIO	Operation select	Op1 Port0 Mask	Op1 Port1 Mask	Op2 Port0 Mask	Op2 Port1 Mask
0[0]	1Ch	1Dh	1Eh	1Fh	20h
0[1]	21h	22h	23h	24h	25h
0[2]	26h	27h	28h	29h	2Ah
0[3]	2Bh	2Ch	2Dh	2Eh	2Fh
0[4]	30h	31h	32h	33h	34h
1[0]	35h	36h	37h	38h	39h
1[1]	3Ah	3Bh	3Ch	3Dh	3Eh
1[2]	3Fh	40h	41h	42h	43h
1[3]	44h	45h	46h	47h	48h
1[4]	49h	4Ah	4Bh	4Ch	4Dh

1.7.1 OP_SEL_xx

Operation Select Registers

Individual Register Names and Addresses:

OP_SEL_00 : 1Ch OP_SEL_01 : 21h OP_SEL_02 : 26h OP_SEL_03 : 2Bh
OP_SEL_04 : 30h OP_SEL_10 : 35h OP_SEL_11 : 3Ah OP_SEL_12 : 3Fh
OP_SEL_13 : 44h OP_SEL_14 : 49h

	7	6	5	4	3	2	1	0
Access : FD	RW : 00	RW : 00	RW : 00	RW : 00	RW : 00	RW : 00	RW : 00	RW : 00
Bit Name	Oper	N_Op	Comb[1:0]		InvOp2	Op2	InvOp1	Op1

These registers are used to select the operation to be performed on a combination of buttons and/or GPIOs.

The number of pins configurable as this type of output depends on the number of pins used as CapSense inputs and GPIOs. Only the pins enabled as GPIOs in registers 08h and 09h are configured with this set of registers. Configuration for pins already defined as CapSense Input are ignored.

1.7.1 OP_SEL_xx *(continued)*

Operations are performed using the selected input bits (registers 00h-01h) or Port Status Since Last Read bits (registers 02h-03h) from the two ports, inverted according to the Inversion Mask (registers 0Ah-0Bh), ORed or ANDed together, outputting the result (optionally inverted) on the selected output pin.

Having two operands to select allows maximum flexibility for various conditions able to trigger the status of an output pin. If further complexity is needed, the master device can always read the input registers and set the output registers directly.

Bit	Name	Description
7	**Oper**	This bit enables or disables the operation on the selected output. To enable the operation with the operands defined in the next registers, set the bit to '1'. The bits used for the operations depend on the content of the Op1/2 Port0/1 Mask registers, input (registers 00h-01h), and Port Status Since Last Read (registers 02h-03h). Op1/2 Port0/1 Mask registers define a mask to select which pins should be used for the operation, and also have one bit to select whether to use bits from the Input or Port Status register. The output is always inverted according to the Inversion Mask (registers 0Ah-0Bh).
6	**N_Op**	This bit determines whether the operation uses one or two operands. A value of '0' uses only Operand 1 and the result of the operation is the calculated Operand 1 (optionally inverted). A value of '1' will uses both operands, and the result of the operation is Operand 1 AND/OR/XOR (depending on bits 4-5) Operand 2.
5:4	**Comb[1:0]**	These two bits select which operator should be used to combine Operand 1 and Operand 2 according to the table below.
3	**InvOp2**	Setting this bit to '1' enables the Operand 2 inversion.
2	**OP2**	This bit selects which operator should be used to compute Operand 2. A value of '0' calculates the OR of the bits selected with the Op2 Port0/1 Mask registers. A value of '1' calculates the AND of the bits.
1	**InvOp1**	Setting this bit to '1' enables the Operand 1 inversion.
0	**Op1**	This bit selects which operator should be used to compute Operand 1. A value of '0' calculates the OR of the bits selected with the Op1 Port0/1 Mask registers. A value of '1' calculates the AND of the bits.

Comb[1:0]	Operation
00	Reserved
01	Operand 1 OR Operand 2
10	Operand 1 AND Operand 2
11	Operand 1 XOR Operand 2

1.7.2 OPR1_PRT0_xx

Op1 Port 0 Registers

Individual Register Names and Addresses:

OPR1_PRT0_00 : 1Dh OPR1_PRT0_01 : 22h OPR1_PRT0_02 : 27h OPR1_PRT0_03 2Ch
OPR1_PRT0_04 : 31h OPR1_PRT0_10 : 36h OPR1_PRT0_11 : 3Bh OPR1_PRT0_12 40h
OPR1_PRT0_13 : 45h OPR1_PRT0_14 : 4Ah

	7	6	5	4	3	2	1	0
Access : FD	RW : 00			RW : 00				
Bit Name	Status			GP[4:0]				

These registers select pins from Port 0 for Operand 1. Enables selection of registers 00h, 02h.

If the “Status” bit is set to ‘1‘, the inputs are taken from the Port Status Since Last Read registers (02h-03h) instead of the Input registers (00h-01h).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
7	**Status**	0 1 Inputs are taken from the Port Status Since Last Read registers (02h-03h) instead of Input registers.
4:0	**GP[4:0]**	These bits identify the bitmask for Port 0 (pins to be used for Operand 1).

1.7.3 OPR1_PRT1_xx

Op1 Port 1 Registers

Individual Register Names and Addresses:

OPR1_PRT1_00 : 1Eh	OPR1_PRT1_01 : 23h	OPR1_PRT1_02 : 28h	OPR1_PRT1_03 2Dh
OPR1_PRT1_04 : 32h	OPR1_PRT1_10 : 37h	OPR1_PRT1_11 : 3Ch	OPR1_PRT1_12 41h
OPR1_PRT1_13 : 46h	OPR1_PRT1_14 : 4Bh		

	7	6	5	4	3	2	1	0
Access : FD	RW : 00			RW : 00				
Bit Name	Status			GP[4:0]				

These registers are used to select pins from Port 1 for Operand 1. Enables selection of registers 01h, 03h.

If the “Status” bit is set to ‘1‘, the inputs are taken from the Port Status Since Last Read registers (02h-03h) instead of the input registers (00h-01h).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
7	**Status**	0 1 Inputs are taken from the Port Status Since Last Read registers (02h-03h) instead of Input registers.
4:0	**GP[4:0]**	These bits identify the bitmask for Port 1 (pins to be used for Operand 1).

1.7.4 OPR2_PRT0_xx

Op2 Port 0 Registers

Individual Register Names and Addresses:

OPR2_PRT0_00	: 1Fh	OPR2_PRT0_01	: 24h	OPR2_PRT0_02	: 29h	OPR2_PRT0_03	2Eh
OPR2_PRT0_04	: 33h	OPR2_PRT0_10	: 38h	OPR2_PRT0_11	: 3Dh	OPR2_PRT0_12	42h
OPR2_PRT0_13	: 47h	OPR2_PRT0_14	: 4Ch				

	7	6	5	4	3	2	1	0
Access : FD	RW : 00			RW : 00				
Bit Name	Status			GP[4:0]				

These registers are used to select pins from Port 0 for Operand 2. Enables selection of registers 00h, 02h.

If the “Status” bit is set to ’1’, the inputs are taken from the Port Status Since Last Read registers (02h-03h) instead of the Input registers (00h-01h).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
7	**Status**	0 1 Inputs are taken from the Port Status Since Last Read registers (02h-03h) instead of Input registers.
4:0	**GP[4:0]**	These bits identify the bitmask for Port 0 (pins to be used for Operand 2).

1.7.5 OPR2_PRT1_xx

Op2 Port 1 Registers

Individual Register Names and Addresses:

OPR2_PRT1_00 : 20h	OPR2_PRT1_01 : 25h	OPR2_PRT1_02 : 2Ah	OPR2_PRT1_03 2Fh
OPR2_PRT1_04 : 34h	OPR2_PRT1_10 : 39h	OPR2_PRT1_11 : 3Eh	OPR2_PRT1_12 43h
OPR2_PRT1_13 : 48h	OPR2_PRT1_14 : 4Dh		

	7	6	5	4	3	2	1	0
Access : FD	RW : 00			RW : 00				
Bit Name	Status			GP[4:0]				

These registers select pins from Port 1 for Operand 2. Enables selection of registers 01h, 03h.

If the “Status” bit is set to ’1’, the inputs are taken from the Port Status Since Last Read registers (02h-03h) instead of the Input registers (00h-01h).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
7	**Status**	0 1 Inputs are taken from the Port Status Since Last Read registers (02h-03h) instead of Input registers.
4:0	**GP[4:0]**	These bits identify the bitmask for Port 1 (pins to be used for Operand 2).

1.8 CapSense Global Parameter Registers

1.8.1 CS_NOISE_TH

Noise Threshold Register

Individual Register Names and Addresses:

CS_NOISE_TH : 4Eh

	7	6	5	4	3	2	1	0
Access : FD	RW : 28							
Bit Name	Bits[7:0]							

This register sets the noise threshold value. For individual sensors, the noise threshold parameter sets the count value above which the baseline is not updated. For slider sensors, it sets the count value below which the results are not counted in the calculation of the centroid.

The range is 3 to 255.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits are used to set the noise threshold value.

1.8.2 CS_BL_UPD_TH

Baseline Update Threshold Register

Individual Register Names and Addresses:

CS_BL_UPD_TH : 4Fh

	7	6	5	4	3	2	1	0
Access : FD	RW : 64							
Bit Name	Bits[7:0]							

When the new raw count value is above the current baseline and the difference is below the noise threshold, the difference between the current baseline and the raw count is accumulated into a “bucket.” When the bucket fills, the baseline increments and the bucket is emptied. This parameter sets the threshold that the bucket must reach for the baseline to increment.

The range is 0 to 255.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits set the threshold that the bucket must reach for baseline to increment.

1.8.3 CS_SETL_TIME

Setting Time Register

Individual Register Names and Addresses:

CS_SETL_TIME : 50h

	7	6	5	4	3	2	1	0
Access : FD	RW : A0							
Bit Name	Bits[7:0]							

The settling time parameter controls the duration of the capacitance-to-voltage conversion phase. The parameter setting controls a software delay that allows the voltage on the integrating capacitor to stabilize. Possible values are 2 to 255.

This register has read only access in "Normal Operation Mode" and read/write access in "Setup Operation Mode" (also see the COMMAND_REG register on page 58).

It is mandatory that you set this register before finger threshold and IDAC setting (registers 61h to 6Ah and 6Bh to 74h) registers are set.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits are used to set the settling time value.

1.8.4 CS_OTH_SET

External Capacitor, Sensors Auto-Reset, Clock Select Register

Individual Register Names and Addresses:

CS_OTH_SET : 51h

	7	6	5	4	3	2	1	0
Access : FD		RW : 00			RW : 00		RW : 00	
Bit Name		Clk[1:0]			Sns R		Ext C	

External Capacitor, Sensors Auto-Reset, Clock Select.

This register has read only access in "Normal Operation Mode" and read/write access in "Setup Operation Mode" (also see the COMMAND_REG register on page 58).

It is mandatory that you set this register before finger threshold and IDAC setting (registers 61h to 6Ah and 6Bh to 74h) registers are set.

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit **Name** **Description**

6:5 **Clk[1:0]**

These bits set the Clock Select parameter. This parameter selects the CapSense module frequency of operation, and can be used to increase the amount of effective resistance of the sensor, to compensate for high capacitance values.

Clk[1:0]	Frequency of Operation
00	IMO
01	IMO/2
10	IMO/4
11	IMO/8

3 **Sns R**

This bit sets the Sensors Auto-Reset parameter. This parameter determines whether the baseline is updated at all times or only when the signal difference is below the noise threshold. When set to ‘1’ (enabled), the baseline is updated constantly. This setting limits the maximum time duration of the sensor, but it prevents the sensors from permanently turning on when the raw count suddenly rises without anything touching the sensor. This sudden rise can be caused by a large power supply voltage fluctuation, a high-energy RF noise source, or a very quick temperature change. When the parameter is set to ‘0’ (disabled), the baseline is updated only when raw count and baseline difference is below the noise threshold parameter. This parameter may be enabled unless there is a demand to keep the sensors in the on state for a long time.

1 **Ext C**

This bit chooses whether to connect an external integrating capacitor or to use the internal capacitor.
0 Internal capacitor.
1 External capacitor.

1.8.5 CS_HYSTERISIS

Hysteresis Register

Individual Register Names and Addresses:

CS_HYSTERISIS : 52h

	7	6	5	4	3	2	1	0
Access : FD	RW : 0A							
Bit Name	Bits[7:0]							

The Hysteresis parameter adds to or subtracts from the finger threshold depending on whether the sensor is currently active or inactive. If the sensor is off, the difference count must overcome the finger threshold plus hysteresis. If the sensor is on, the difference count must go below the finger threshold minus hysteresis. It is used to add debouncing and “stickiness” to the finger detection algorithm.

Possible values are 0 to 255. However, the setting must be lower than the finger threshold parameter setting.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits are used to set the hysteresis value.

1.8.6 CS_DEBOUNCE

Debounce Register

Individual Register Names and Addresses:

CS_DEBOUNCE : 53h

	7	6	5	4	3	2	1	0
Access : FD	RW : 03							
Bit Name	Bits[7:0]							

The Debounce parameter adds a debounce counter to the sensor active transition. In order for the sensor to transition from inactive to active, the difference count value must stay above the finger threshold plus hysteresis for the number of samples specified.

Possible values are 1 to 255. A setting of ‘1’ provides no debouncing.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits are used to set the debounce value.

1.8.7 CS_NEG_NOISE_TH

Negative Noise Threshold Register

Individual Register Names and Addresses:

CS_NEG_NOISE_TH : 54h

	7	6	5	4	3	2	1	0
Access : FD	RW : 14							
Bit Name	Bits[7:0]							

This parameter adds a negative difference count threshold. If the current raw count is below the baseline and the difference between them is greater than this threshold, the baseline is not updated. However, if the current raw count stays in the low state (difference greater than the threshold) for the number of samples specified by the Low Baseline Reset parameter, the baseline is reset.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits are used to set the negative noise threshold value.

1.8.8 CS_LOW_BL_RST

Low Baseline Reset Register

Individual Register Names and Addresses:

CS_LOW_BL_RST : 55h

	7	6	5	4	3	2	1	0
Access : FD	RW : 14							
Bit Name	Bits[7:0]							

This parameter works together with the Negative Noise Threshold parameter. If the sample count values are below the baseline minus the negative noise threshold for the specified number of samples, the baseline is set to the new raw count value. It essentially counts the number of abnormally low samples required to reset the baseline. It is generally used to correct the false baseline initializations that may occur if the finger is already on the sensor when device is being powered (baseline may be initialized at higher value than what it should be). With this parameter the first touch which occurs before or during the power up will be ignored and successive touches will be detected.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits are used to set the low baseline reset value.

1.8.9 CS_FILTERING

CapSense Filtering Register

Individual Register Names and Addresses:

CS_FILTERING : 56h

	7	6	5	4	3	2	1	0
Access : FD	RW : 20		RW : 20	RW : 20			RW : 20	
Bit Name	RstBL		I2C DTS	Avg_En			AvgSamples[1:0]	

This register controls CapSense filtering operation.

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of '0'.

Bit	Name	Description
7	**RstBL**	This bit set to '1' forces an immediate baseline initialization for all sensors. It auto-resets to '0' once the baseline initialization completes. This can help recovery from "button stuck" events. 0 Auto-resets once the baseline initialization completes. 1 Forces an immediate baseline initialization for all sensors.
5	**I2C DTS**	This bit set to '1' enables the I2C "Drop the Sample" filter. I2C communication that occurs while a scan is in progress invalidates the resulting sample. 0 1 Enables the I2C "Drop the Sample" filter (factory default).
4	**Avg_En**	0 1 Enables the averaging filter.
1:0	**AvgSamples[1:0]**	These bits are used to select the number of CapSense samples to average:

Bit 1	Bit 0	HEX	Samples to Average
0	0	0x0	2
0	1	0x1	4
1	0	0x2	6
1	1	0x3	8

1.9 CapSense Sensor Parameter Registers

These registers are used to adjust sensor specific parameters.

1.9.1 CS_SCAN_POS_xx

Scan Position Registers

Individual Register Names and Addresses:

CS_SCAN_POS_00	: 57h	CS_SCAN_POS_01	: 58h	CS_SCAN_POS_02	: 59h	CS_SCAN_POS_03	: 5Ah
CS_SCAN_POS_04	: 5Bh	CS_SCAN_POS_10	: 5Ch	CS_SCAN_POS_11	: 5Dh	CS_SCAN_POS_12	: 5Eh
CS_SCAN_POS_13	: 5Fh	CS_SCAN_POS_14	: 60h				

	7	6	5	4	3	2	1	0
Access : FD					RW : FF			
Bit Name					Bits[3:0]			

This register is used to set the position of the sensors in the switch table for proper scanning sequence because the CapSense sensors are scanned in sequence.

It is mandatory that you set these registers after setting the 06h, 07h, 50h, and 51h registers.

This is mainly needed for slider functionality. The position (0-9, as CapSense Express supports a maximum of 10 sensors) of each sensor connected to a specific pin can be set in the table using this register. Sensors are added to or removed from the switch table when writing to registers 06h-07h, so only sensors already in the table can be repositioned. When the user requires positioning a sensor in place of another, the two positions are swapped.

Users must take into consideration the following table to understand starting positions of sensors for buttons and sliders.

CapSense Express Configuration	Starting Position for Buttons Sensors	Starting Position for Slider Sensors
Buttons Only (1-10)	0	NA
5 Buttons + 1 Slider	5	0
1 Slider	NA	0
1 Slider with 10 Sensors	NA	0

Upon selection of a CapSense sensor in registers 06h-07h, the scan position value for all the sensors is overwritten with the value reloaded from Flash. Reading from these registers returns the actual sensor position in the sensor table or 0xFF if the selected pin is not enabled as a sensor.

Enable all the needed sensors before setting the scan position values.

These registers have read only access in "Normal Operation Mode" and read/write access in "Setup Operation Mode" (also see the COMMAND_REG register on page 58).

In the register table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
3:0	**Bits[3:0]**	These bits are used to set the position of sensors in the switch table for proper scanning sequence.

1.9.2 CS_FINGER_TH_xx

Finger Threshold Registers

Individual Register Names and Addresses:

CS_FINGER_TH_00 : 61h CS_FINGER_TH_01 : 62h CS_FINGER_TH_02 : 63h CS_FINGER_TH_03 : 64h
CS_FINGER_TH_04 : 65h CS_FINGER_TH_10 : 66h CS_FINGER_TH_11 : 67h CS_FINGER_TH_12 : 68h
CS_FINGER_TH_13 : 69h CS_FINGER_TH_14 : 6Ah

	7	6	5	4	3	2	1	0
Access : FD	RW : 64							
Bit Name	Bits[7:0]							

This register sets the finger threshold for the selected sensor (range is 3 to 255).

It is mandatory that you set these registers after setting the 06h, 07h, 50h, and 51h registers.

Upon selection of a CapSense sensor in registers 06h-07h, the finger threshold value for all the sensors is overwritten with the value reloaded from Flash. It is recommended to enable all the needed sensors before setting the finger threshold values.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits are used to set the finger threshold values.

1.9.3 CS_IDAC_xx

IDAC Setting Registers

Individual Register Names and Addresses:

CS_IDAC_00	: 6Bh	CS_IDAC_01	: 6Ch	CS_IDAC_02	: 6Dh	CS_IDAC_03	: 6Eh
CS_IDAC_04	: 6Fh	CS_IDAC_10	: 70h	CS_IDAC_11	: 71h	CS_IDAC_12	: 72h
CS_IDAC_13	: 73h	CS_IDAC_14	: 74h				

	7	6	5	4	3	2	1	0
Access : FD	RW : 0A							
Bit Name	Bits[7:0]							

The IDAC current controls the slope of the single slope ADC charging ramp. This register is used to tune the current for the selected sensor.

Possible values are 1 to 255.

It is mandatory that you these registers after setting the 06h, 07h, 50h, and 51h registers.

Upon selection of a CapSense sensor in registers 06h-07h, the IDAC setting value for all the sensors is overwritten with the value reloaded from Flash. If the value in Flash is less than 1, it is set to a default value of 10.

Enable all the needed sensors before setting the IDAC setting values.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits are used to set the IDAC values.

1.10 CapSense Slider Setting Registers

1.10.1 CS_SLID_CONFIG

Slider Configuration Register

Individual Register Names and Addresses:

CS_SLID_CONFIG : 75h

	7	6	5	4	3	2	1	0
Access : FD							RW : 00	RW : 00
Bit Name							5/10	En

This register is used to enable the slider (set En bit to ‘1’), and configure it as 5 or 10-element slider (5 or 10 sensors – set “5/10” bit to ‘1’ for 10-element slider).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
1	**5/10**	Configures the slider as 5 or 10 element. If set to ‘1’, it configures the slider as 10 element.
0	**En**	Used to enable the slider (when set to ‘1’).

1.10.2 CS_SLID_MULx

Slider Resolution MSB/LSB Registers

Individual Register Names and Addresses:

CS_SLID_MULM : 77h CS_SLID_MULL : 78h

	7	6	5	4	3	2	1	0
Access : FD	RW : 00							
Bit Name	Bits[7:0]							

These two registers define the resolution for the slider.

The table represents the fixed-point multiplier that the slider's calculated centroid is multiplied by to achieve the resolution desired. The multiplier is two bytes containing the following bit definitions:

Resolution Multiplier MSB, 77h (Whole Number)							
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
*128	*64	*32	*16	*8	*4	*2	*1
Resolution Multiplier LSB, 78h (Number Fractional Part)							
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
*1/2	*1/4	*1/8	*1/16	*1/32	*1/64	*1/128	*1/256

The formula for the resolution is:

Resolution = (SensorsInSlider - 1) * Multiplier

For example, if you had a 5 sensor slider and you wanted a resolution of 50, the multiplier would need to be 12.5. Therefore the fixed-point value would be:

MSB = 0Ch; LSB = 80h as 8+4+1/2 = 12.5.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits are used to determine the fixed-point multiplier that the slider's calculated centroid is multiplied by to get the required resolution.

1.11 Device Setting Registers

1.11.1 I2C_DEV_LOCK

I2C Lock Register

Individual Register Names and Addresses:

I2C_DEV_LOCK : 79h

	7	6	5	4	3	2	1	0
Access : FD								WPR : 01
Bit Name								I2CDL

The LSB of the register is: I2C Device Address Lock.

The device I2C address can be modified by writing to register 7Ch. Before being able to modify this register, the LSB in register 79h must be unlocked. The changed value of register 7Ch does not take effect until the LSB in register 79h is locked.

To lock/unlock the I2CDL bit, the following three bytes must be written to register 79h:

- unlock I2CDL: 3Ch A5h 69h
- lock I2CDL: 96h 5Ah C3h

Reading from register 79h informs the user of the current lock state: ‘1’ signifies locked.

This mechanism gives a high level of protection against “accidental” changes of register 7Ch and actual effectiveness of its value.

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
0	**I2CDL**	I2C Device Address Lock.

1.11.2 DEVICE_ID

Device ID Register

Individual Register Names and Addresses:

DEVICE_ID : 7Ah

	7	6	5	4	3	2	1	0
Access : FD	RO : 42/ 40/ 60/ 80/ 10/ A0[1]							
Bit Name	PN[7:0]							

1. This value is equal to last two digits of the device part number.

Reading from this register returns the Device ID. It is the LSB of the two-byte Device ID/Status register (with 7Bh). This register contains the encoded last two digits of the part number. These correspond to ‘XX” in CY8C201XX.

Bit	Name	Description
7:0	**PN[7:0]**	These bits represent the part number (Device ID).

Part Number (201xx)	Description
20110	10 Configurable I/Os
20180	8 Configurable I/Os
20160	6 Configurable I/Os
20140	4 Configurable I/Os
201A0	10 Configurable I/Os with Slider
20142	4 Configurable I/Os

1.11.3 DEVICE_STATUS

Status Register

Individual Register Names and Addresses:

DEVICE_STATUS : 7Bh

	7	6	5	4	3	2	1	0
Access : FD	RO : 0		RO : 0	RO : 0	RO : 0	RO : 0	RO : 0	RO : 0
Bit Name	VCC[1:0]		WDRS	POR	No Write	SLD	CS	GPIO

Reading from this register returns the Device Status. It is the MSB of the two-byte Device ID/Status register (with 7Ah).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of '0'.

Bit	Name	Description
7:6	**VCC[1:0]**	VCC range is automatically detected and the bits are set according to the following table:

VCC Bits[7:6]	Voltage
00	5
01	3.3
10	2.7
11	Reserved

5	**WDRS**	When set to '1', this bit indicates that a Watchdog Timer Reset occurred.
4	**POR**	When set to '1', this bit indicates that at power up, the Factory Default configuration is loaded. When set to '0', it indicates that at power up, the User Default configuration is loaded.
3	**No Write**	When set to '1', this bit indicates that the supply voltage applied to the device is too low for a write to nonvolatile memory operation, and no write is performed. This bit should be checked before any Store or Write POR command.
2	**SLD**	When set to '1', this bit indicates that the device has both CapSense buttons and slider enabled. When set to '0', it indicates that only CapSense buttons are enabled. This bit is valid only if Bit[1] = 1.
1	**CS**	When set to '1', this bit indicates that the CapSense functionality is enabled. When set to '0', it indicates that the CapSense functionality is disabled.
0	**GPIO**	When set to '1', this bit indicates that the GPIO functionality is enabled. When set to '0', it indicates that the GPIO functionality is disabled.

1.11.4 I2C_ADDR_DM

Device I2C Address and I2C Pin Drive Mode Register

Individual Register Names and Addresses:

I2C_ADDR_DM : 7Ch

	7	6	5	4	3	2	1	0
Access : FD	RW : 0	RW : 00						
Bit Name	I2CDM	Bits[6:0]						

To be able to write to this register, register 79h must first be unlocked. The value written to register 7Ch is applied only after locking register 79h again.

Reading this register returns the uncommitted value, which may or may not be the same as the current address, depending on the lock status.

Bit	Name	Description
7	**I2CDM**	Used to set the I2C pins to drive mode. 0 Resistive pull up to minimize external components. 1 Open drain low to accommodate the device in an already existing I2C 'environment' with pull up resistors.
6:0	**Bits[6:0]**	Used to set the device I2C address.

1.11.5 SLEEP_PIN

Sleep Control Pin Register

Individual Register Names and Addresses:

SLEEP_PIN : 7Eh

	7	6	5	4	3	2	1	0
Access : FD	RW : 0			RW : 00				
Bit Name	Port			GPX[4:0]				

This register is used to select which pin is used to control safe I2C communication in cases in which the sleep mode is enabled.

In CapSense Express, I2C communication while the device has sleep mode enabled needs a control pin to guarantee reliability of I2C data transfers. To avoid this condition, one pin must be set as a “control” pin for proper I2C communication. The master can pull the selected pin LOW before starting an I2C communication and hold it until the communication is completed. While the pin is pulled LOW, the device will never enter into sleep mode.

The pin must have been previously enabled for GPIO operation (GPIO_ENABLEx).

Care should be taken in properly setting the drive mode for this pin. Typically, it is a digital input drive mode (resistive pull up and open drain low) to let the host device control the status of the pin.

This register has read only access in "Normal Operation Mode" and read/write access in "Setup Operation Mode" (also see the COMMAND_REG register on page 58).

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
7	**Port**	This bit identifies the port (0 or 1).
4:0	**GPX[4:0]**	These bits identify the bitmask. (the pin to be used for sleep control). Note that when writing to this register, the bitmask must contain only one bit set to ’1’, or the write operation will not be successful.

1.11.6 SLEEP_CTRL

Sleep Control Register

Individual Register Names and Addresses:

SLEEP_CTRL : 7Fh

	7	6	5	4	3	2	1	0
Access : FD	RW : 00		RW : 00	RW : 00				RW : 00
Bit Name	Enable		Bandgap	Sleep[1:0]				Mode

This register is used to set the sleep timer for low power applications. A sleep interval can be inserted between CapSense scans or GPIO sampling, so that the power consumption of the device can be reduced.

When the device is in deep sleep mode, only a GPIO interrupt can wake the device.

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of '0'.

Bit	Name	Description
7	**Enable**	Controls whether to enter periodically into sleep mode.
5	**Bandgap**	Controls whether to have the voltage bandgap powered during sleep in order to have faster wakeups.
4:3	**Sleep[1:0]**	The Sleep bits can be set according to the following table: **Sleep[1:0] / Sleep Interval** 00 – 1.95 ms (512 Hz) 01 – 15.6 ms (64 Hz) 10 – 125 ms (8 Hz) 11 – 1s (1 Hz) The sleep interval should be set to 8 or 1 Hz when saving to flash. The sequence should be: 1. Write configuration data to registers with sleep interval set to 8 or 1 Hz 2. Save the settings to flash 3. Change the sleep interval per design
0	**Mode**	Controls whether deep or normal sleep mode is enabled. 0 Normal sleep mode. 1 Deep sleep mode.

1.11.7 SLEEP_SA_CTR

Stay Awake Counter Register

Individual Register Names and Addresses:

SLEEP_SA_CTR : 80h

	7	6	5	4	3	2	1	0
Access : FD	RW : 00							
Bit Name	Bits[7:0]							

This register sets the number of sleep intervals during which the device needs to stay awake while it waits for events before returning to sleep. A new event (CapSense button press, GPIO interrupt, or I2C register read/write) resets the counter to this register value.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits are used to set the stay awake counter value.

1.12 CapSense Button Read-back Values Registers

1.12.1 CS_READ_BUTTON

Button Select Register

Individual Register Names and Addresses:

CS_READ_BUTTON : 81h

	7	6	5	4	3	2	1	0
Access : FD	RW : 0			RW : 00				
Bit Name	Port			GPX[4:0]				

This register is used to select the CapSense input pin to read the result values for registers 82h, 89h.

Only the pins defined as CapSense inputs in registers 06h-07h can be used with this set of registers. Trying to select other pins not defined as CapSense will not change the register value.

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
7	**Port**	This bit identifies the port (0 or 1).
4:0	**GPX[4:0]**	These bits identify the bitmask. Note that when writing to this register, the bitmask must contain only one bit set to ’1’, or the write operation will not be successful.

1.12.2 CS_READ_BL

Baseline Value MSB/LSB Registers

Individual Register Names and Addresses:

CS_READ_BLM : 82h CS_READ_BLL : 83h

	7	6	5	4	3	2	1	0
Access : FD	R : 00							
Bit Name	Bits[7:0]							

Reading from this register returns the 2-byte current baseline value for the selected CapSense switch.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits represent the baseline value.

1.12.3 CS_READ_DIFF

Sensor Difference Value MSB/LSB Registers

Individual Register Names and Addresses:

CS_READ_DIFFM : 84h CS_READ_DIFFL : 85h

	7	6	5	4	3	2	1	0
Access : FD	R : 00							
Bit Name	Bits[7:0]							

Reading from this register returns the 2-byte current sensor difference value for the selected CapSense switch.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits represent the sensor difference value.

1.12.4 CS_READ_RAW

Result Value MSB/LSB Registers

Individual Register Names and Addresses:

CS_READ_RAWM : 86h CS_READ_RAWL : 87h

	7	6	5	4	3	2	1	0
Access : FD	R : 00							
Bit Name	Bits[7:0]							

Reading from this register returns the 2-byte current raw count value for the selected CapSense switch.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits represent the raw count value.

1.12.5 CS_READ_STATUS

Sensors On Status Port 0/1 Registers

Individual Register Names and Addresses:

CS_READ_STATUS0 : 88h CS_READ_STATUS1 : 89h

	7	6	5	4	3	2	1	0
Access : FD				R : 00				
Bit Name				GP[4:0]				

Reading from this register returns the 2-byte current ON/OFF sensor status for all (up to 10) CapSense sensors. A ‘1’ is set for CapSense selected pins above the predefined finger threshold.

In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits must always be written with a value of ‘0’.

Bit	Name	Description
4:0	**GP[4:0]**	Used to represent sensor status. 0 Sensor OFF. 1 Sensor ON.

1.13 CapSense Slider Read-back Values Registers

1.13.1 CS_READ_CEN_POS

Centroid Position MSB/LSB Registers

Individual Register Names and Addresses:

CS_READ_CEN_POSM : 8Ah CS_READ_CEN_POSL : 8Bh

	7	6	5	4	3	2	1	0
Access : FD	R : 00							
Bit Name	Bits[7:0]							

Reading from this register returns the 2-byte current centroid position value for the CapSense slider.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits represent the centroid position.

1.13.2 CS_READ_CEN_PEAK

Centroid Peak MSB/LSB Registers

Individual Register Names and Addresses:

CS_READ_CEN_PEAKM : 8Ch CS_READ_CEN_PEAKL : 8Dh

	7	6	5	4	3	2	1	0
Access : FD	R : 00							
Bit Name	Bits[7:0]							

Reading from this register returns the 2-byte current centroid peak value for the CapSense slider. The centroid peak value corresponds to the maximum difference between raw counts and baseline for the sensors in the slider.

Bit	Name	Description
7:0	**Bits[7:0]**	These bits represent the centroid peak value.

1.13.3 COMMAND_REG

Command Register

Individual Register Names and Addresses:

COMMAND_REG : A0h

	7	6	5	4	3	2	1	0
Access : FD	W : 00							
Bit Name	Bits[7:0]							

Commands are executed by writing the command code to the Command register. Refer to Table 1-4, “Command Codes,” on page 59 for details on Command register opcodes.

Bit	Name	Description
7:0	**Bits[7:0]**	Refer to Table 1-4, “Command Codes,” on page 59 for details on Command register opcodes.

Table 1-4. Command Codes

Command Code	Name	Description
00h	Get Firmware Revision	The I2C buffer is loaded with the one-byte firmware revision value. Reading one byte after writing this command returns the firmware revision. The upper (MSB) four bits of the firmware revision byte are the major revision number and the lower (LSB) four bits are the minor revision number.
01h	Store Current Configuration to NVM	The current register settings are saved in nonvolatile memory (Flash). This setting is automatically loaded after the next device reset/power-up or if the Reconfigure Device (06h) command is issued. The sleep interval should be set to 8 or 1 Hz when saving to flash. The sequence should be: 1. Write configuration data to registers with sleep interval set to 8 or 1 Hz 2. Save the settings to flashJanuary 4, 2013 3. Change the sleep interval per design
02h	Restore Factory Configuration	Replaces the saved user configuration with the factory default configuration. Current settings are unaffected by this command. New settings are loaded after the next device reset/power up or if the 06h command is issued.
03h	Write POR Defaults	Sends new power-up defaults to the CapSense controller without changing current settings unless the 06h command is issued afterwards. This command is followed by 123 data bytes according to the POR Default Data Structure table[1]. The CRC is calculated as the XOR of the 122 data bytes (04h-80h excludes 76h,7Ah, and 7Bh). If the CRC check fails or an incomplete block is sent, the slave responds with a NAK and the data is not be saved to Flash. To define new POR defaults the user must: ■ Write command 03h ■ Write 122 data bytes with new values of registers ■ Write one CRC byte calculated as XOR of previous 122 data bytes
04h	Read POR Defaults	Reads the POR settings stored in the nonvolatile memory. To read POR defaults the user must: ■ Write command 04h ■ Read 122 data bytes ■ Read one CRC byte
05h	Read Device Configuration (RAM)	Reads the current device configuration. Gives the user "flat-address-space" access to all device settings. To read device configuration the user must: ■ Write command 05h ■ Read 122 data bytes ■ Read one CRC byte
06h	Reconfigure Device (POR)	Immediately reconfigures the device with actual POR defaults from Flash. Has the same effect on the registers as a POR. This command can only be executed in Setup Operation Mode (command code 08).
07h	Set Normal Operation Mode	Sets the device in normal operation mode. In this mode, CapSense pin assignments cannot be modified, as well as Settling Time, IDAC Setting, External Capacitor, and Sensor Auto-Reset.
08h	Set Setup Operation Mode	Sets the device in setup operation mode. In this mode, CapSense pin assignments can be changed as well as other parameters.
09h	Start CapSense Scanning	allows the user to start CSA scanning after it has been stopped using command 0x0A. Note that at POR, scanning is enabled and started by default if one or more sensors are enabled.
0Ah	Stop CapSense Scanning	Allows the user to stop CSA scanning. A system host controller might initiate this command before powering down the device to make sure that during power down no CapSense touches are detected. When CSA scanning is stopped by the user and the device is still in the valid VCC operating range, the following behavior is supported: ■ Any change to configuration can still be done (as long as VCC is in operating range). ■ Command code 0x06 overrides the status of stop/scan by enabling and starting CSA scanning if one or more sensors are enabled. ■ CapSense read-back values return 0x00.
0Bh	Returns CapSense Scanning Status	The I2C buffer is loaded with the one-byte CSA scanning status value. After writing the value 0Bh to the A0h register, reading one byte returns the CSA scanning status. It returns the LVD_STOP_SCAN and STOP_SCAN bits. LVD_STOP_SCAN is bit 3 - Set when CSA is stopped because VCC is outside the valid operating range. STOP_SCAN is bit 2 - Set when CSA is stopped by the user by writing command 0x0A.

1. POR Default Data Structure table is generated by PSoC Designer (in system level project) when you do the settings in properties GUI and click "OK" or "Apply to board" (In system level project, place the CapSense express driver and right-click on it, and then click on properties option to open the GUI). The generated table is saved in the <project folder name>/<project name>_config_through_flash.iic file.

Revision History

Table 2-1. CY8C201xx Register Reference Guide

Document Title: CY8C201xx Register Reference Guide Document Number: 001-45146				
Revision	**ECN#**	**Issue Date**	**Origin of Change**	**Description of Change**
**	2312491	04/08/2008	HMT	New specification.
*A	2554606	08/19/2008	HMT	Add PWM_ENABLE0, PWM_ENABLE1 (PWM_ENABLEx), PWM_MODE_DC, PWM_DELAY, and CS_FILTERING registers.
*B	3027740	09/11/2010	VED	Modified the definition of command code 03h in Table 1-4 on page 59.
*C	3040963	09/28/2010	AESA	Added footnote to Command Codes chapter on page 59. Added Figure 1-1 on page 14. Added Factory default value to all registers. In CS_LOW_BL_RST register on page 37: replaced text "It is generally used to correct the finger-on-at-startup condition" with "It is generally used to correct the false baseline initializations that may occur if the finger is already on the sensor when device is being powered (baseline may be initialized at higher value than what it should be). With this parameter the first touch which occurs before or during the power up will be ignored and successive touches will be detected".
*D	3242193	04/27/11	SLAN	No Change to Content. Minor template updates.
*E	3864590	01/10/2013	SLAN	Adding sleep interval settings when saving to flash on pages 48 and 58.
*F	4378389	05/13/2014	PRIA	No content update.
*G	4753824	05/04/2015	PRIA	Updated descriptions for the INT_MASKx and STATUS_HOLD_MSKx registers.
Distribution: External Web				