Toward Solving Multichannel RF-SoC Integration Issues Through Digital Fractional Division

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***Abstract*— In modern RF system on chips (SoCs), the digital content consumes up to 85% of the IC chip area. The recent push to integrate multiple RF-SoC cores is met with heavy resistance by the remaining RF/analog circuitry, which creates numerous strong aggressors and weak victims leading to RF performance degradation. A key such mechanism is injection pulling through parasitic coupling between various *LC*-tank oscillators as well as between them and strong transmitter (TX) outputs. Any static or dynamic frequency proximity between aggressors (i.e., oscillators and TX outputs) and victims (i.e., oscillators) that share the same die causes injection pulling, which produces unwanted spurs and/or modulation distortion. In this paper, we propose and demonstrate a new frequency planning technique of a multicore TX where each *LC*-tank oscillator is separated from other aggressors beyond its pulling range. This is done by breaking the integer harmonic frequency relationship of victims/aggressors within and between the RF transmission channels using digital fractional divider based on a phase rotation. Each oscillator's center frequency can be fractionally separated by ∼28% but, at the same time, both producing closely spaced frequencies at the phase rotator outputs. The injection-pulling spurs are so far away that they are insignificantly small (−80 dBc) and coincide with the second harmonic of the carrier. This method is experimentally verified in a two-channel system in 65-nm digital CMOS, each channel comprising a high-swing class-C oscillator, frequency divider, and phase rotator.**

***Index Terms*— Digital fractional divider, digitally controlled oscillator (DCO), frequency pulling, injection locking, multi-core radio, RF-SoC, system on chip (SoC).**

I. Introduction

THE abundance of wireless connectivity (e.g., WiFi and Bluetooth) and cellular (e.g., GSM, WCDMA, and LTE) communication standards has made the multiband multimode radios in mobile devices a pervasive trend. There is a relentless push toward a system-level integration, and recently, multicore radio integration enables manufacturing of less bulky equipment that is much cheaper and consumes less power. At the same time, allowing multiple radios to simultaneously coexist within a single silicon die leads to a hostile environment with various aggressors and victims affecting each other. An example of such a scenario could be a coexistence of LTE with 2.4-GHz WLAN and Bluetooth [1]. Moreover, modern radios need to support features such as frequency division duplex and carrier aggregation for high data rates, which further worsen the coupling problem.

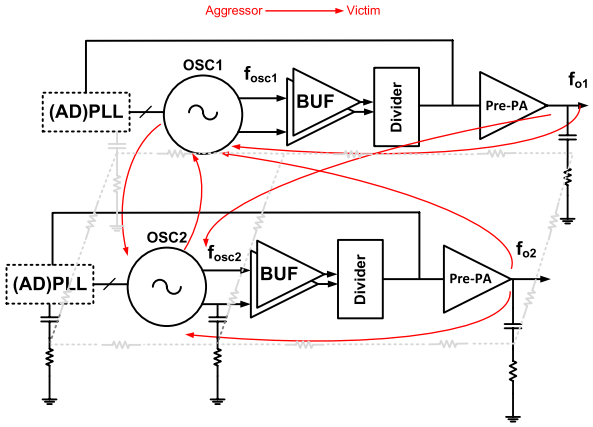

Fig. 1. System scenario of a two-core multiradio system and various pulling paths with aggressors and victims.

Furthermore, the use of nanoscale CMOS processes allows for an unprecedented degree of scaling and integration in digital circuitry, but complicates the implementation of traditional RF and analog circuits, of which linear transistor operation keeps on getting worse with each CMOS process node advancement in almost every aspect. On the other hand, the raw digital capability, in terms of processing sophistication and speed, is improving. Consequently, a need has arisen to find digital architectural solutions to the RF functions [2].

A major coexistence problem on the transmitter (TX) side is caused by injection pulling, which degrades signal integrity and creates unwanted emissions. Any oscillatory system, such as an *LC*-tank-based phase-locked loop (PLL), is generally vulnerable to injection pulling through parasitic coupling. This pulling will likely be the main cause for the degradation of spectral purity of the TX output [3].

Nowadays, there is a strong push to integrate a power amplifier (PA) with the rest of TX due to cost reasons. This has already happened in wireless connectivity (e.g., Bluetooth and WiFi) and is now happening in cellular mobiles. On the base station side, integrating a 200-W PA on the same die as the TX is not seriously considered yet. However, there are attempts

Manuscript received February 19, 2015; revised April 17, 2015; accepted May 19, 2015. Date of publication June 12, 2015; date of current version February 23, 2016. This work was supported by the European Union through the European Research Council Starting under Grant 307624.

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Digital Object Identifier 10.1109/TVLSI.2015.2436979

to integrate the RF front-end portion with the PA within the same package [4]. In these scenarios, the harmonics of the PA output or even the TX output driver are typically not attenuated enough and can injection-pull the oscillator. In practice, it has been shown that even very weak signals injected into the LC-tank oscillator can have dramatic consequences on the RF system performance [3]. Single-chip RF system solutions have the potential problem of signal integrity, stemming from the fact that the switching digital circuitry and the sensitive analog circuits share the same substrate. This issue is becoming exponentially more severe in multiradio systems that share the same die. In a single-radio RF system, the output PA can pull the oscillator; however, in multiradios, not only the output PAs but also all the oscillators can pull each other. In general, there are three sources of parasitic coupling [5]. As shown in Fig. 1, each oscillator and PA can couple resistively, magnetically, and capacitively to each other. In many cases, due to the low-resistivity substrate, which is the case for the scaled CMOS technology, noise/interference can pass throughout the entire chip. Thus, the analog circuits nearby the noise/interference sources will suffer the most. Fig. 1 shows the aggressor/victim scenarios in the most recent multicore radios.

In this paper, we first investigate the negative pulling effects in a two-channel system (Section II). Afterward, in Section III, we propose and investigate frequency planning by means of a *fractional* ratio ($f_{\text{osc}} \neq k \cdot f_o, k \in \mathbb{N}$) between the LC-tank oscillators resonating at f_{osc} and the PA stages operating at f_o. In this way, the near-integer harmonic relationship between the aggressors and the victims will be eliminated [6] and the pulling issues due to various multiple paths can be prevented. A low-power architectural solution for the fractional frequency translation is proposed in Section IV. Section V presents the detailed circuit implementation and measurement results providing insight into the selection of proper pulling countermeasures.

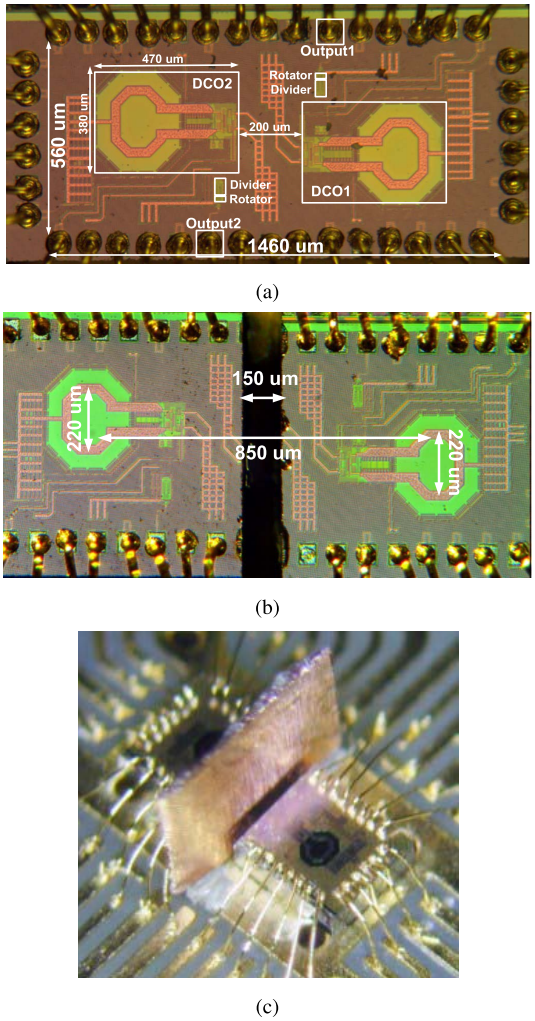


Fig. 2. Chip micrographs. (a) Common substrate. (b) Diced substrate. (c) Diced substrate with metal shield in between. Diced substrate shows a 10-dB reduction of injection pulling, and further using grounded metal shield reduces it by another 3 dB.

II. Injection-Pulling Effects

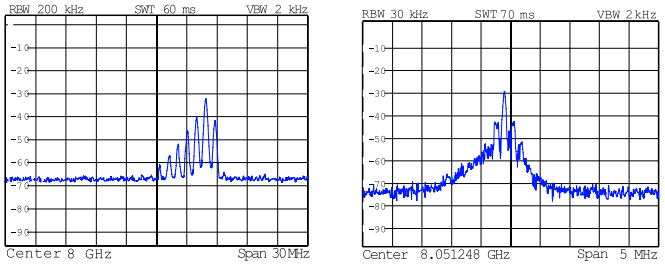
The effects of injection locking and pulling of an oscillator by a periodic signal were first studied in [7], and then thoroughly investigated in [8]–[11]. As elaborated in [8], the oscillator can maintain lock to the injected signal only within a limited frequency lock range (ω_L), which is estimated as

$$\omega_L = \frac{\omega_0}{2Q} \cdot \frac{I_{\text{inj}}}{I_{\text{osc}}} \cdot \frac{1}{\sqrt{1 - \frac{I_{\text{inj}}^2}{I_{\text{osc}}^2}}} \tag{1}$$

where $\omega_0 = 2\pi f_0$ is the natural angular resonant frequency of the tank and Q is its quality factor. The lock range depends on the injection current I_{inj} versus the oscillator current I_{osc} and Q-factor: the weaker the I_{inj}, the lower the chance for locking, and the lower the Q, the wider the locking range. The pulling phenomena have been studied for a single oscillator under injection. However, as mentioned above, mutual coupling between two or more oscillators will happen in increasingly more applications [9], [12].

Furthermore, integrated TXs contain a PA or its driver (pre-PA), whose large-swing signals can couple to various parts of the system including the sensitive LC-tank oscillators. An output power greater than just a few milliwatts might thus cause appreciable degradation during an eight-phase shift keying modulated transmission [13]–[15]. In order to study the serious effects of pulling in advanced integrated TXs and to offer potential solutions, a two-channel system with ~8-GHz oscillators is realized in 65-nm digital CMOS. Nondotted blocks in Fig. 1 were implemented on the IC, whose micrograph is shown in Fig. 2(a).

The two oscillators with overlapping tuning range are placed 200 μm apart on the same CMOS die (center-to-center distance between the inductors is 700 μm). This may correspond to the tight floorplanning environment of today's commercial multichannel SoCs. The two oscillators have separate bias and frequency tuning bits. It is important to stress that each oscillator simultaneously plays both aggressor and victim roles. The assigned roles are based on a context. If the injected frequency of the aggressor oscillator is out of the lock range, the victim oscillator can be pulled, and if it is near the lock range, the victim will be quasi-locked. By moving



(a) (b)

Fig. 3. Measured spectrum of the oscillator in Fig. 2(a) under injection. (a) Fast beat. (b) Quasi-lock. Injection is from the upper side.

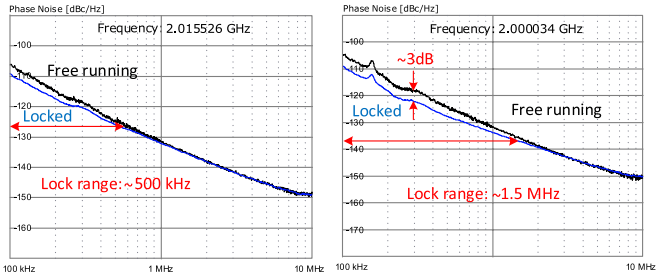


Fig. 4. Measured phase noise at the divider output. Left: diced with ground shielding. Right: common substrate.

the frequency just beyond the lock range, the oscillator will be in a fast beat mode [8]. The measured spectra of these two modes are shown in Fig. 3. Based on the calculations in [11], the spectrum is confirmed to be asymmetric and the sidebands on one side decay very rapidly. The power of the biggest injection-pulling spur under a weak injection can be calculated as

$$P(\omega_{\text{spur}}) \approx \left(\frac{\omega_0}{4Q} \cdot \frac{I_{\text{inj}}}{I_{\text{osc}}} \cdot \frac{1}{\omega_m}\right)^2. \tag{2}$$

For an injection signal far away from the lock range, the oscillator's center frequency ω_0 may not pull much; however, it creates spurs of equal power around ω_0 with an offset frequency of ω_m, with levels proportional to $1/\omega_m^2$. We verify this equation for three different cases. In the first test, the oscillators are on the same die [see Fig. 2(a)]. Then, the oscillators are separated by dicing the chip (with a saw) at its center [see Fig. 2(b)]. Finally, an additional grounded metal shield is inserted in between to reduce electromagnetic coupling [see Fig. 2(c)]. In this design, the ground and voltage supply lines of the two channels are completely separated on chip and are connected outside at the PCB. Moreover, the supply and ground pads of two oscillators have enough distance in order to avoid coupling to each other through their wirebonds.

It is well known that the phase noise of an injection-locked oscillator can improve if locked to a clean source. Intuitively, the injecting source can correct the zero crossings of the oscillator at regular intervals, thus lowering the accumulated jitter [8]. Phase noise improvement depends on the injection source power as long as it is within the locking range. Fig. 4 shows the measured phase noise, while free running

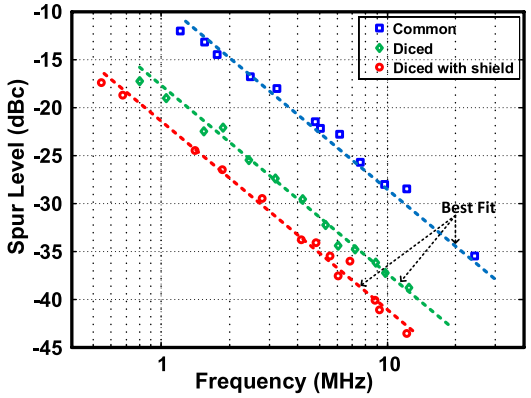


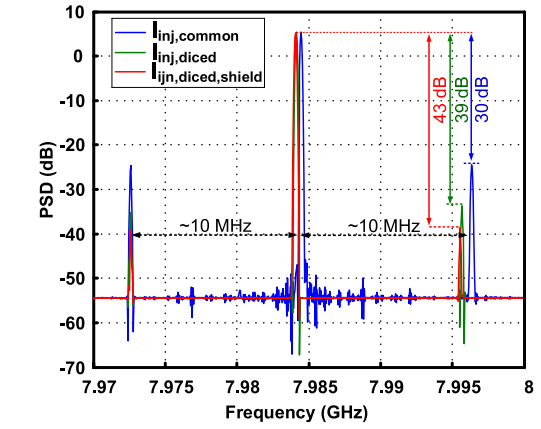
Fig. 5. Measured injection-pulling spurs at the oscillator output versus separation of the two carriers for three different test cases.

TABLE I
INJECTED CURRENT STRENGTH FOR DIFFERENT MEASUREMENTS EXTRACTED FROM FIG. 5

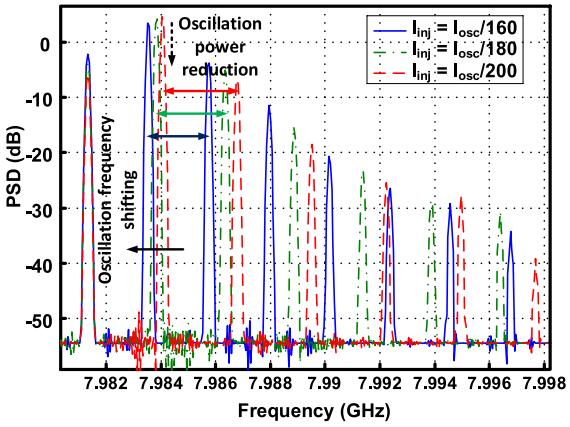
	Estimated injected current I_{inj} (μA)		
Spur frequency	Common	Diced	Diced and shielded
10 MHz	72	29	20

and in-locked conditions, in two scenarios, i.e., with the common substrate (right), and when the chip is diced and with the grounded shielding (left). Two interesting points can be observed when the coupling is reduced: 1) the locking range is reduced and 2) the amount of improvement in the phase noise is also decreased. According to (1), as the measured lock range is proportional to the injection current I_{inj}, which is proportional to the coupling strength, the coupling factor reduction is calculated to be three. Fig. 5 shows the measured highest generated spur power versus the frequency difference between the aggressor and victim. It confirms the 6-dB/octave slope evident from (2) and indicates that the substrate is the dominant coupling path. Coupling of the diced chips is reduced by ~8 dB. Moreover, by putting metal shield in between, another ~3 dB of spur reduction is achieved, which shows that a significant but nondominant part of the coupling is electromagnetic. This agrees with the locking range method in (1): $20\log_{10}(3) = 9.5$ dB, which is quite close to the measured $8 + 3 = 11$ dB. One might suspect that using a PLL around the oscillator can solve the pulling problem, but that would not be the case. As shown in [3] and [9], based on s-domain modeling and measurements, the injection pulling has a bandpass response in the PLL in which the sideband magnitudes vary with the frequency offset of injection and their magnitudes approach zero for both very near to and far away from the center frequency while having a peak in between exhibiting a bandpass behavior. This is because the PLL suppresses the effect of pulling if $(\omega_{\text{inj}} - \omega_0)$ is within the loop bandwidth and the oscillator pulling becomes less of an issue when $(\omega_{\text{inj}} - \omega_0)$ is large. The situation is exacerbated when the injection source has a variable envelope modulation (output of a PA or its driver in the case of a polar modulation). In that scenario, there will be a parasitic frequency modulation, which degrades the spectral purity.

Table I shows the injected current calculated based on the measurements and using (2) for three different test cases.



(a)



(b)

Fig. 6. Simulation results based on the model proposed in [16] for three different injection strengths. (a) Injection-pulling spurs based on the estimated parameters from the measurement results. (b) Effect of injection strength on victim oscillator frequency and amplitude (the lock range is 1.5 MHz).

It is evident that in the case of the common substrate, the injected current is much larger than in other cases. For example, comparing the common substrate with the one diced and shielded, the injected current is 4× smaller (which is close to the value calculated from the lock range, with the difference due to inaccuracy in estimating the exact value of the internal oscillator voltage swing and measuring the lock range since it is highly dependent on the biasing conditions).

The measurement results are also validated against a behavioral model suggested in [16]. Fig. 6(a) shows the simulation results for circuit parameters of an oscillator shown in Fig. 16 and the injected current of Table I, which is derived from (2). The simulated results are in agreement with the measured results in Fig. 5. To have an estimation on the oscillation center frequency shift (ω_{pulled}) and the pulling-induced spur locations, we repeat here, for convenience, [11, eqs. (11) and (23)] as (3) and (4). They are verified with the model mentioned above

$$\omega_b = \sqrt{\omega_m^2 - \left(\frac{\omega_0}{2Q} \cdot \frac{I_{\text{inj}}}{I_{\text{osc}}}\right)^2} \tag{3}$$

where ω_b is the beat frequency

$$\omega_{\text{pulled}} \approx \omega_0 + \frac{\omega_m}{2}\left(\frac{\omega_0}{2Q} \cdot \frac{I_{\text{inj}}}{I_{\text{osc}}} \cdot \frac{1}{\omega_m}\right)^2. \tag{4}$$

Injecting a current at a frequency close to the lock range will put the oscillator in a fast beat mode as in Figs. 3 and 6(b). (For simplicity, the injected current in this simulation is set larger than normal.)

It is evident from these equations and simulations that if the injection current is larger, the oscillator center frequency would be pulled in stronger. As a result, the amplitude of oscillation will decrease since the tank impedance also decreases due to this frequency shifting. In addition, spur spacing will decrease, therefore the stronger injection current creates more closely spacing spurs. In summary, if the internal voltage (V_{tank}) and current swings (I_{osc}) of the oscillator are low and the Q is low, the oscillator is more susceptible to pulling. Moreover, if the structure of the PA (in a direct conversion TX) is single ended, the oscillator is more easily pulled due to the existence of even-order harmonics.

III. Injection-Pulling Mitigation Methods

The previous section has demonstrated that the injection pulling produces strong unwanted spurs. There are well-known solutions attempting to reduce them. The most straightforward one is to reduce the coupling strength by increasing the physical distance between the strong aggressor and the sensitive victim and further isolating them with guard rings. Moreover, ground pickup connections can be used in between the two parts to absorb the interference. In addition, putting sensitive analog/RF parts in a deep N-well can be beneficial. These solutions, however, increase the chip fabrication cost, which is not desirable in high-volume consumer electronics.

Furthermore, multiple LC-tank oscillators will magnetically couple to each other. At the same time, an inductor present in the matching network of the last stage of a PA can also interact with other PAs or with the oscillators. Wire bondings of the adjacent critical pads can also magnetically couple. One solution to solve the magnetic coupling is to employ eight-shape inductors [17]. As reported in [18], 30 dB of magnetic coupling reduction could be achieved. However, other coupling paths remain unaffected in addition to a larger area and Q-factor degradation of the inductor. The third mechanism is through the interaction of the interconnects inside the chip as well as PCB traces that can capacitively couple to each other. The capacitive coupling should be reduced by a careful PCB layout design.

Considering the above experiments, analysis, and examples, the injection pulling cannot be realistically solved through physical isolation or merely through the coupling strength reduction. Consequently, the pulling *mitigation* via architectural transformation must be sought instead.

A. Fractional Divider

The injection pulling has been traditionally mitigated by operating the oscillator at integer multiples of the output RF carrier. Unfortunately, that arrangement does not entirely

eliminate the pulling since the PA harmonics still coincide with the oscillator center frequency. Another approach is to employ a fractional divider, which prevents the oscillator from both direct and harmonic pulling [19]–[22]. The fractional division could be achieved through a mixer following an oscillator [19]. It is then followed by a distribution network. However, this technique typically requires an LC bandpass filter or digital calibration to suppress the lower sideband spurs. In [20], a further modification was introduced, called inductor-less LO distribution, which eliminates filtering of harmonics in the LO path while not increasing the noise levels. However, that technique uses complicated analog circuits and consumes large area. Unfortunately, generated harmonics from the LO buffer and also the mixing of the oscillator harmonics and divider output is still a concern.

Another method to create the fractional frequency relationship is to use a frequency multiplier, $\times N$, following the oscillator, such that the PA harmonics would pull the oscillator. However, the generation of a quadrature output clock (e.g., required by the upconversion mixer) becomes more difficult. If, for example, polyphase filters were to be used, high insertion loss and high power consumption would be a major disadvantage [23].

The third method is using a digital technique known as a phase rotation approach. This technique is well suited for scaled CMOS. It is more power and area efficient but could require some calibration. There are various such structures, e.g., a multimodulus divider [24], but they are typically not suitable as they must lie on the direct feedforward RF path leading to an antenna. Phase switching divider [21], [22], [25]–[27] belongs to another group of fractional dividers. It has fewer elements operating at the full clock rate. The circuit generates equidistant phases, and then rotates selection between the different phases. Our proposed solution uses a reliable phase selection of the multiplexer. From the noise point of view, the choice of the phase generating circuit and multiplexer is of great importance. Previously reported pulling mitigation methods through a phase rotation introduce an excessive amount of noise since a number of devices are inserted in the RF feedforward path [21], [27]. For instance, Chandrashekar *et al.* [21] introduced a four-phase rotation in which each phase is divided by five using a Johnson counter (it contains five latches), whose output is sampled by the corresponding phase using a set–reset latch, each adding its own phase noise contribution. That might be acceptable for wireless connectivity applications but less so for cellular applications. In the next section, a low phase noise fractional divider will be introduced.

B. Frequency Planning

In this paper, we propose a digital fractional divider architecture suitable for the pulling-free frequency planning scheme for multichannel TXs. Fig. 7(top) shows the scenario in which the two oscillators operate at almost the same frequency.[1] Since the coupling strength is high, it leads to high spurious

[1]Their average frequencies could be identical, but, for example, due to modulation, they could be a bit different at a given time instance.

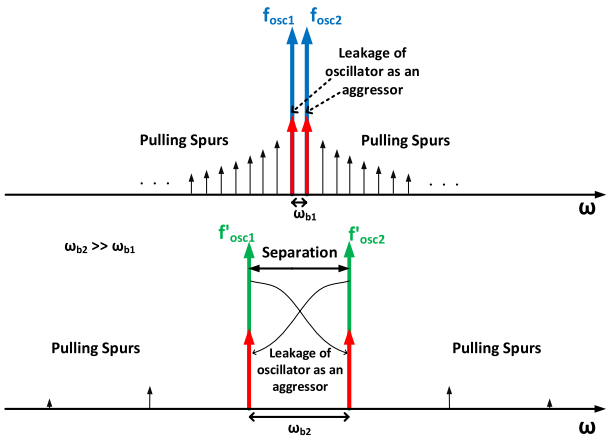


Fig. 7. Frequency planning concept for the pulling mitigation.

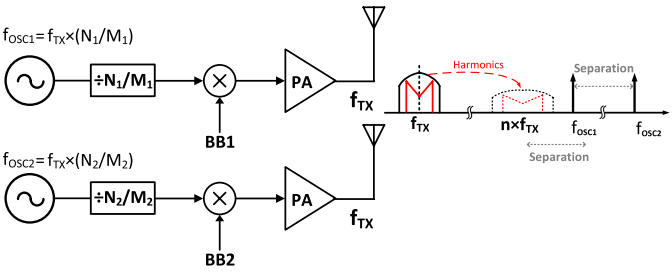


Fig. 8. Proposed fractional division in a two-channel TX.

content in the spectrum of both oscillators. If two oscillators' center frequencies are separated, as per (2), the coupling effects will decrease, as shown in Fig. 7(bottom). Since the output frequencies of the two channels need to be the same (on average), a noninteger (fractional) type divider should be used afterward. Employing a fractional frequency divider, as shown in Fig. 8, is the proposed method here to prevent both direct and harmonic PA pulling within and between the channels. As an example, consider a two-channel system with $f_{\mathrm{TX}} = 2$-GHz output. Employing an integer ÷4 divider leads to two oscillators with center frequencies at 8 GHz. However, using divide by $N_1/M_1 = 3.5$ and $N_2/M_2 = 4.5$ puts the center frequencies at $f_{\mathrm{osc1}} = 7$ GHz and $f_{\mathrm{osc2}} = 9$ GHz, which ensures enough separation, thus giving immunity to the injection pulling.

The reason for using an eight-phase rotation (÷4 and then phase rotator) is as follows: the integer ÷2 in Fig. 9(a) has a disadvantage of two oscillators operating at the same frequency, causing their strong mutual pulling. The second harmonic of the PA can also pull both oscillators. Using a higher integer division [÷4 in Fig. 9(b)] is beneficial from the PA harmonic power perspective, but it still exhibits another significant problem: the two oscillators' center frequencies coincide, which can create their mutual injection pulling. Here, the fourth harmonic of the PA has a lower energy than in Fig. 9(a) to pull the oscillators. However, the divider design could become difficult, although at this frequency inductors feature a higher Q-factor (at least at 65 nm and finer nodes), thus producing lower phase noise.

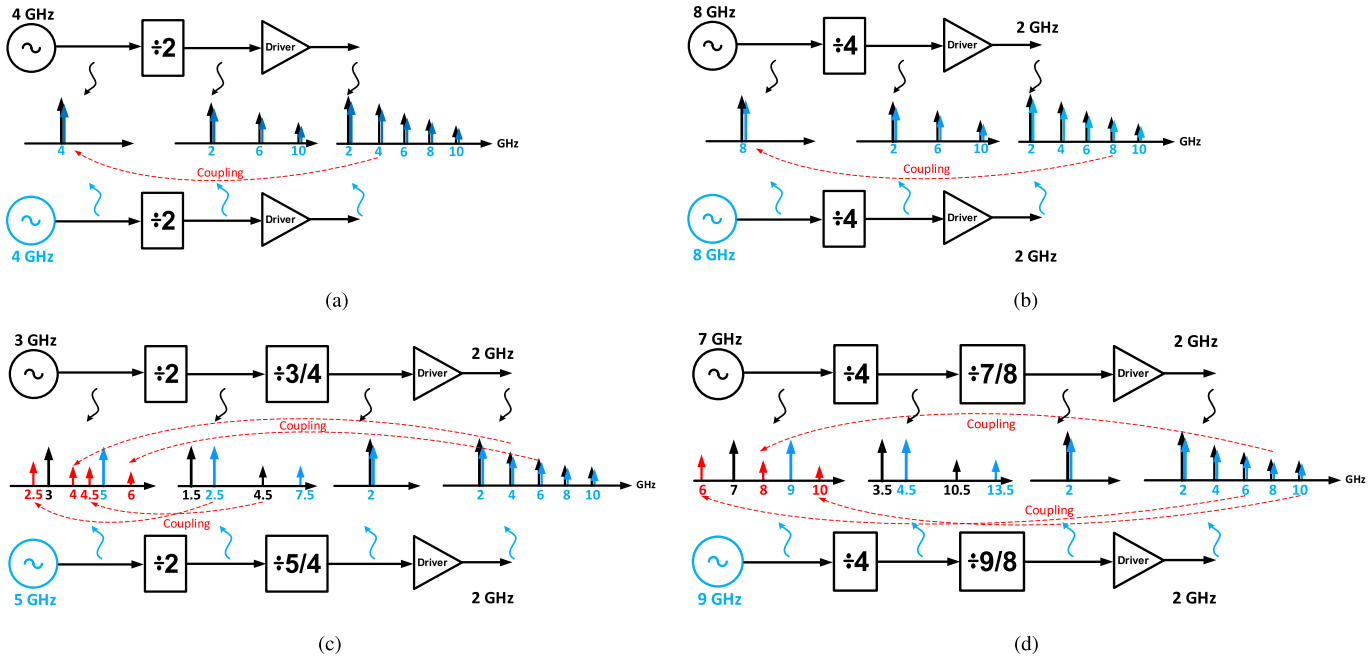


Fig. 9. Different frequency planning scenarios for multichannel pulling mitigation through digital dividers with an output frequency of about 2 GHz (e.g., coexistence of Bluetooth and WiFi). (a) Integer divide by 2. (b) Integer divide by 4. (c) Fractional divide by 2.5 and 1.5. (d) Fractional divide by 3.5 and 4.5.

Another option would be using a ÷2 followed by a four-phase rotator [see Fig. 9(c)]. Now, the two oscillators' center frequencies are well separated by 2 GHz and are thus immune to pulling. However, one of the output of the ÷2 divider could be 500 MHz away from the other oscillator, which could lead to pulling. Moreover, the third harmonic of the ÷2 divider can be placed again 500 MHz away from the oscillator. Another component comes from the second harmonics of the PA output, which places it 1 GHz away from both oscillators. Further disadvantage of this scheme is that one of the oscillators operates at 3 GHz, where the inductors are expected to have a lower Q-factor, thus worse phase noise performance. Fig. 9(d) shows the proposed method that uses a divide-by-four followed by an eight-phase rotator. In this way, we reap all the aforementioned advantages, and only the third, fourth, and fifth harmonics of the PA output are placed 1 GHz away from the oscillators, thus being sufficiently attenuated to be harmless.

IV. Proposed Fractional Divider for Pulling Mitigation

In this paper, we propose a low-power architectural solution that avoids the pulling problem altogether through a large fractional frequency translation of both the aggressor and victim circuits. Although this research specifically targets cellular base station TXs, the findings are applicable to cellular mobile applications, especially multicore RF-SoCs. Hence, the emphasis is on low phase-noise implementation. Fig. 10 contains two oscillators, each with an edge rotator [6]. This corresponds to the two-channel system of Fig. 1. The frequency translation direction depends on the edge rotation direction. The frequencies of the two channel outputs (OUT1 and OUT2) are the same ($f_{o1} = f_{o2} = f_{TX}$),

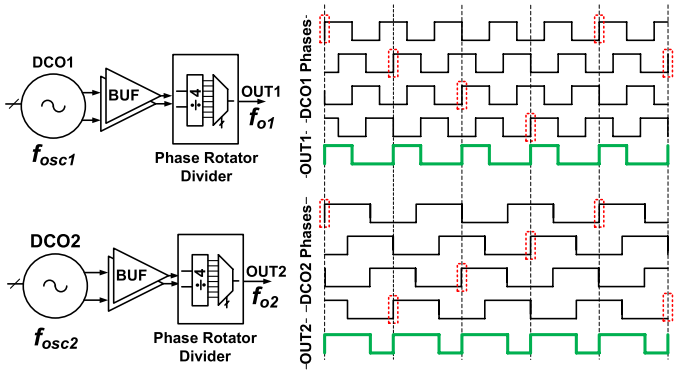


Fig. 10. Frequency translation through edge rotation in a two-core oscillator system as implemented in this IC chip. (For simplicity, only the four-phase rotation concept is shown.)

or very close to each other due to the modulation, but the center frequencies of the oscillators (f_{osc1} and f_{osc2}) are well separated. Thus, the coupling between the oscillators as well as between the outputs and the oscillators is no longer problematic. There will be the tradeoffs of choosing different ratios employed in the fractional divider to accomplish the pulling mitigation. Using higher number of phases is beneficial for two reasons. First, more variety of fractional ratios can be achieved. Second, in nanoscale CMOS technologies, peak inductor Q-factors are pushed to higher frequencies. From the above reasoning, the design of a high-purity oscillator favors higher division ratios. However, due to matching nonidealities of this type of divider, higher division ratios could lead to more close-in fractional spurs, which may violate the spectral mask. It also consumes more power. From the above reasoning, the ÷4 that generates eight phases was chosen here as the optimal tradeoff. Moreover, using a lower division

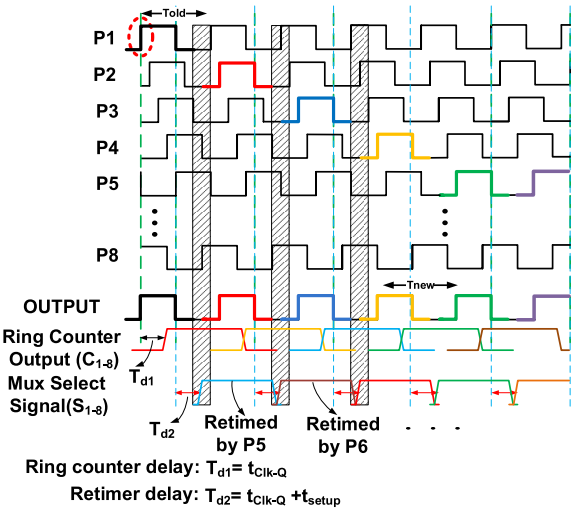


Fig. 11. Edge rotator timing waveforms for reliable select signal generation (divide-by-9/8 example).

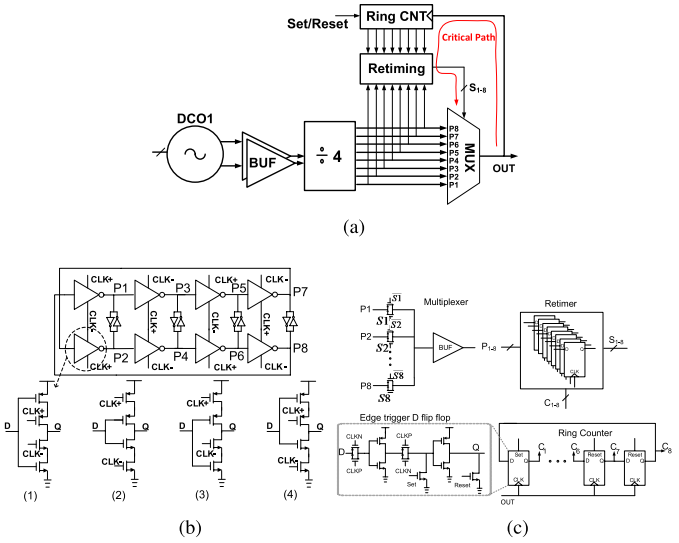


Fig. 12. (a) System-level diagram of the edge rotator divider. (b) Circuit details of the divider structure and different divider cell configurations. (c) Ring counter, multiplexer, retimer, and D-flip-flop.

ratio would place the oscillator center frequency closer to the PA harmonic, which makes it more prone to puling again (e.g., here the 5-GHz spacing will reduce to 1 GHz with ÷2).

Fig. 11 shows internal waveforms when the rotator in Fig. 10 is commanded to rotate its eight phases counterclockwise (i.e., constant phase retarding). By picking a rising edge of the next retarded divider phase, the output clock edges lag, thus resulting in the period increase by 1/8. The other rotator operates in the opposite direction.

System-level block diagram and circuit details of the phase rotator are shown in Fig. 12(a). The rail-to-rail CMOS ÷4 divider [see Fig. 12(b)] generates eight equidistant phases. Out of four different configurations, Fig. 12(b)(1) divider topology was chosen for its better noise performance and shorter propagation delay. Adding back-to-back inverters improves delay matching at the cost of small degradation in

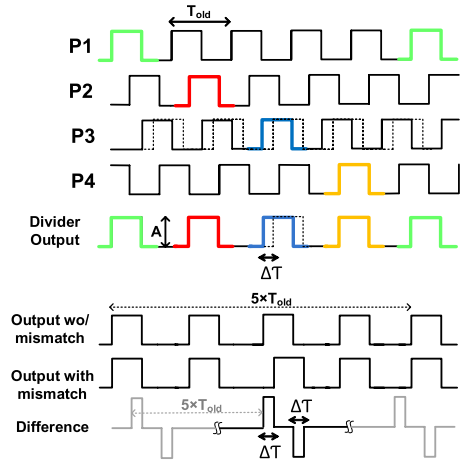


Fig. 13. Effect of timing mismatches on the divider output.

the phase noise. The rotating system contains a ring counter with set/reset to control the normal pass through or the fractional division (see Fig. 12). When set is asserted, only one of the mux select signals will be active and it operates as a normal ÷4. If reset is deasserted, logic 1 circulates in the ring counter and generates the proper selection signal. Edge-triggered D-flip-flops retime the ring counter outputs for the appropriate edge selection. The 8:1 mux uses complementary pass gates, whose eight outputs are wired OR, and the following internal buffer provides strong driving capability. As stressed above, to minimize the phase noise degradation of the output clock, extreme care must be taken to limit the device count on the feedforward path to the absolute minimum (which was not done in [21]), thus putting all the signal processing complexity on the noncritical feedback path. According to simple equations, ÷4 dividers can generate additional divide ratios of 4.5 and 3.5: $T_{\text{out1}} = 4 \times 9/8 \times T_{\text{osc1}} = 4.5 \times T_{\text{osc1}}$ and $T_{\text{out2}} = 4 \times 7/8 \times T_{\text{osc2}} = 3.5 \times T_{\text{osc2}}$.

In order to have a reliable selection (glitch free) of the edges, the multiplexer select signal should come in the shaded area of Fig. 11. To guarantee this, consideration of the worst case timing uncertainty is needed. The critical timing delay [see Fig. 12(a)] mainly comprises CLK-to-Q in the ring counter and CLK-to-Q delay for the retimer with enough setup time to have reliable selection in different process corners. In order to relax the timing, an edge-triggered flip-flop was chosen that exhibits small setup and hold times. Taking into account these delays results in choosing the appropriate signal phase ($P1$–$P8$) to retime the counter output to generate correct select signals for the multiplexer ($S1$–$S8$).

A. Analysis of the Mismatch

A disadvantage of the phase-rotating dividers is that they are sensitive to inherent mismatches and can generate significant spurs. Fig. 13 shows a four-phase rotation example (for the sake of simplicity) and the effect of the timing mismatch ΔT of one of its phases. The mismatch appears at the output every four cycles, therefore $f_{\text{spur}} = f_{\text{out}}/4$ (for the eight-phase rotation, it would happen every eight cycles).

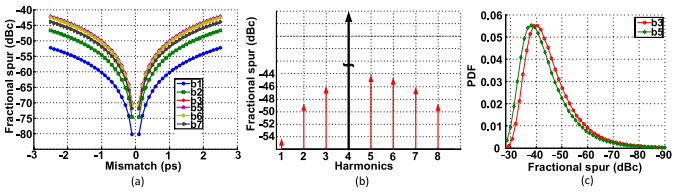


Fig. 14. Simulation results for four phases. (a) Fractional spurs versus phase mismatch. (b) 0.5% mismatch in single phase and related generated spur. (c) Statistical simulation results for the two largest harmonics with 0.5% mismatch in each of the four phases.

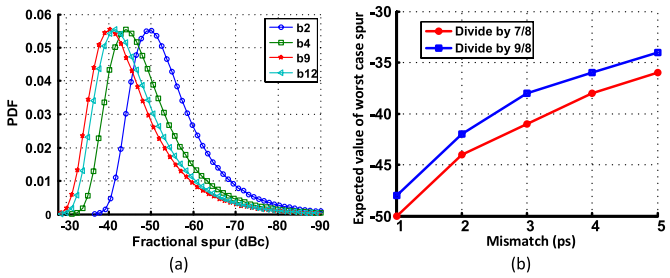


Fig. 15. Simulation results for eight phases. (a) Statistical simulation results for the four different coefficients with $\sigma = 0.54\%$ statistical mismatch in each of the eight phases. (b) Largest expected value for the fractional spur for two different divider modes.

It is possible to relate the maximum tolerable phase mismatch given the spurious-free dynamic range required at the output of the divider [28]. Another way to calculate the spur power is using Fourier series. In this paper, we use the Fourier method similar to [28] and derive a formula for phase-switched dividers. We consider a random mismatch in each phase, rather than only in a single phase as in [28].

Fig. 14 continues with the four-phase rotation of Fig. 13 considering the timing mismatch ΔT in the single phase. By taking Fourier series of the waveform derived from the difference between ideal output and output with mismatch and performing a number of simplifications, Fourier series coefficient b_k in (5) can be derived as

$$b_k = \frac{4A}{\pi k} \sin\left(\frac{k\pi}{2(N \pm 1)}\right) \sin\left(\frac{k\pi\,\Delta T}{(N \pm 1)T_{\text{old}}}\right) \tag{5}$$

where N (e.g., $N = 4$ and 8) is the number of divider phases, A is the amplitude, T_{old} is specified in Fig. 11, and the $\pm$ sign is either $+$ for up translation or $-$ for down translation. The signal $S(t)$ can be reconstructed as

$$S(t) = \sum_{k=1}^{\infty} b_k \cdot \sin\left(\frac{k\pi t}{(N \pm 1)T_{\text{old}}}\right). \tag{6}$$

Fig. 14(a) plots the first six coefficients that are normalized to the carrier (note that $k = 4$ corresponds to the fundamental frequency), indicating harmonic distortion versus the timing mismatch in the single phase. By considering 0.5% mismatch in a single phase (e.g., $T_{\text{old}} = 400$ ps), plotting different harmonics reveals that some of them have a stronger level [see Fig. 14(b)]. This is a simplified scenario, but in the practical case, the mismatch will appear at each phase. Hence, this may increase the spur power at one frequency location (e.g., $k = 6$), while the other locations (e.g., $k = 2$ and 3) are reduced.

In order to see the net effect of mismatch in each phase at the output, statistical simulation with 10^6 points was employed. Each mismatch is a random variable with a Gaussian distribution of $\sigma = 2$ ps. The results are shown in Fig. 14(c) for the two strongest spur levels. Fig. 15(a) shows the probability density function of the fractional spurs with the same statistical mismatches in each of the $N = 8$ phases. Fig. 15(b) shows the effect of the random mismatches on the worst case spur level in two modes of the divider (divide by 9/8 and 7/8). These spur levels are typically nonessential when the fractional dividers are used in the feedback path of a frequency synthesizer [22], [29].

The presented divider is obviously not limited to the 3.5 and 4.5 division ratios. By further modifying the selection path, other division ratios can be achieved. The closer inspection of the waveforms reveals that equations such as $T_{\text{new}} = T_{\text{old}} \times 2 + T_{\text{old}}/2$ and $T_{\text{new}} = T_{\text{old}} \times 2 + T_{\text{old}}/2 + T_{\text{old}}/8$ can be derived (T_{old} and T_{new} were specified in Fig. 11), which give ratios of 10 and 5.25. Further investigation proves that ratios of 4.75, 6, 7, 8, and 9 can also be achieved.

It should be mentioned that besides the injection-pulling mitigation, the fractional divider can be used to further extend the frequency range for multiband radios. It should be observed that based on (7), the location and the power of the divider output spurs can be estimated. For the $\div N$ division

$$S_{\text{div}}(t) = A \cdot \cos\left(\frac{2\pi f_c t}{N} + \frac{\beta \cdot \sin(2\pi f_m t)}{N}\right) \tag{7}$$

where $S_{\text{div}}(t)$ is the first Fourier component of the clock after the division and β is the spur level modeled as FM with f_c being a center frequency and f_m a modulating frequency. The frequency of the carrier is divided by N. However, the location of the spurs remains the same, but its power in decibels reduces by $20 \cdot \log(N)$.

In summary, the proposed techniques are applicable to single-chip radios using the fractional divider between the oscillator and the (pre-)PA, as well as to multiradio SoCs by operating such fractional dividers at different ratios in each path. In the latter case, the closest of the (pre-)PA output harmonics will be separated at least 1 GHz away from the oscillator. The resulting oscillator pulling will be very small, unlike in a conventional integer-N divider where some harmonics fall exactly on top of the oscillator, thus leading to a strong pulling.

V. Experimental Verification

The two oscillators, whose schematic is shown in Fig. 16, operate in a modified high-swing class-C architecture inspired from [30], in which the tail current source in [31] is removed. Instead, an automatic amplitude control is introduced to settle the oscillation voltage swing at the maximum swing. Two transistors in the current control circuit ($M3$ and $M4$) mirror the currents of the core transistors ($M1$ and $M2$). These currents are summed up and then compared with a reference current, I_{ref}. Then, they are RC low-pass filtered

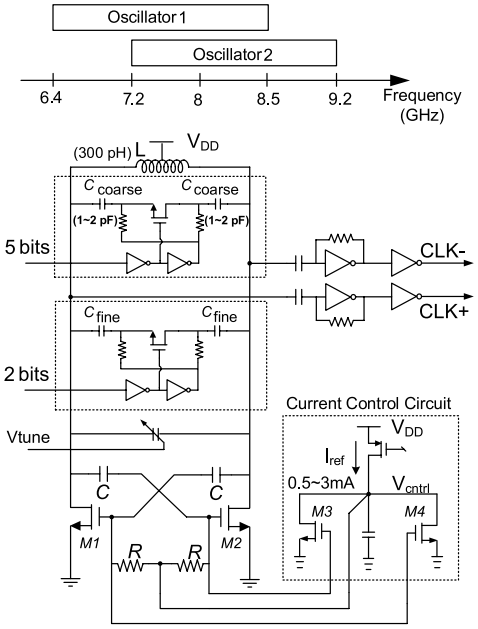


Fig. 16. Schematic of a class-C oscillator and resistive buffer. Two oscillators have overlapping tuning ranges.

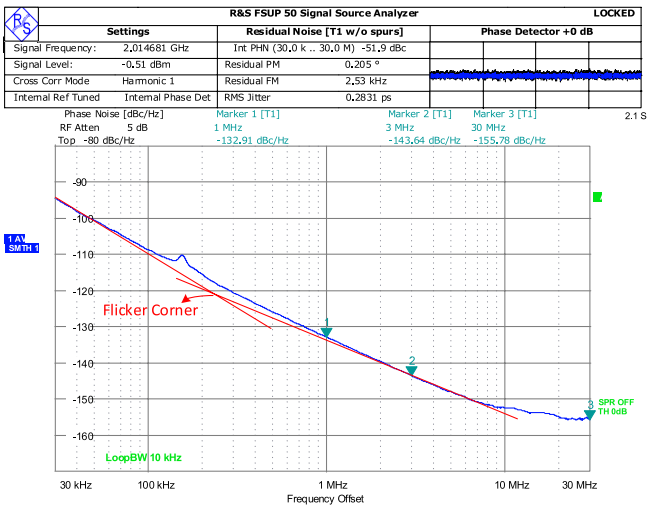


Fig. 17. Measured phase noise of the oscillator at the ÷4 divider output.

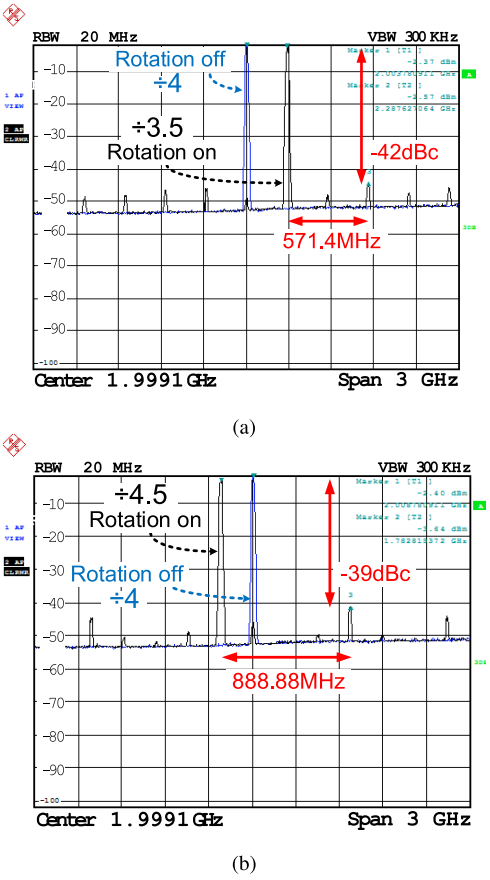


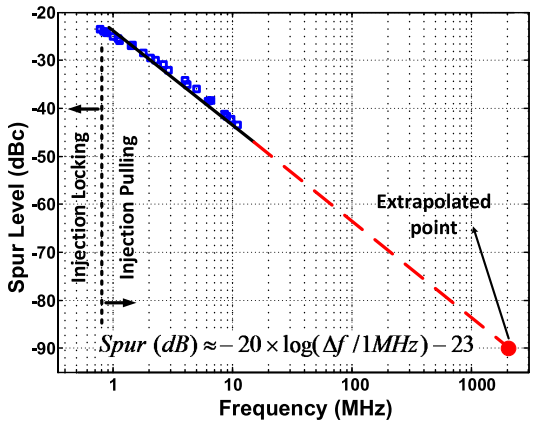
Fig. 18. Measured wide spectra showing fractional division spurs at the two modes of divider operation. (a) ÷3.5. (b) ÷4.5.

to generate V_{ctrl}, which is fed back to the oscillator core and biases the gates of ac-cross-coupled nMOS transistors. This forms a negative feedback loop to control the swing. In the steady state, the total dc current of the core is I_{ref} multiplied by the mirror ratio (i.e., $(W/L)_{1,2}/(W/L)_{3,4}$ which is four in this implementation). Hence, the power consumption and the oscillation amplitude can be controlled by adjusting I_{ref}.

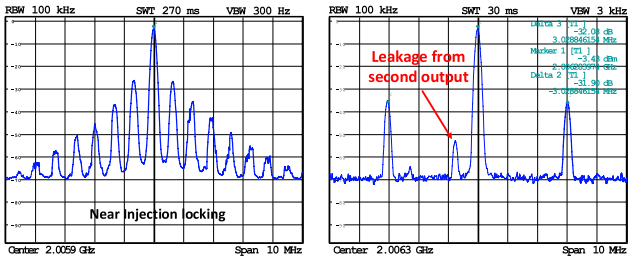
The headroom-enhancing transformer introduced in [30] was removed here in order to save area and improve Q-factor of the LC tank. Instead, a standard center-tapped inductor is used together with a switched-cap varactor bank. The whole tank's Q-factor is 16.

The two oscillators use overlapping tuning ranges [see Fig. 16(top)]. The first oscillator is tunable from 6.45 to 8.5 GHz and the second from 7.15 to 9.2 GHz. Thus, the measured tuning range of each oscillator is around 26%. Both oscillators have a 5-bit binary-weighted coarse method of moment (MOM) capacitor bank, a 2-bit fine MOM capacitor bank, and a linear varactor (only used expediently in this chip) for a continuous tuning range of 15 MHz. For reliability reasons, all the oscillator core transistors are thick oxide devices. The oscillator core area is 0.18 mm^2. An ac-coupled resistive-feedback inverter is cascaded with a digital inverter to drive a rail-to-rail CMOS ÷4 divider that generates the eight phases. The measured oscillator FoM at an offset of 3 MHz over the entire tuning range is 185 dB. Its phase noise is −143.6 dBc/Hz at an offset of 3 MHz from the divided 2-GHz output (see Fig. 17). Moreover, the noise floor measures −156 dBc/Hz and varies around 1 dB by activating the edge rotation. Simulation shows that the divide-by-four noise floor is about −160 dBc/Hz and the excess noise is coming from the rotator and output buffers. The measured current drain of each oscillator is 12 mA at 1.7 V and 1.3 mA at 1.2 V for each resistive buffer. The estimated (i.e., mixture of measurements and simulations) current drain is 2.5 mA for the ÷4 divider and 0.5 mA for the 2-GHz eight-phase rotator, both at 1.2 V.

The injection-pulling scheme has been successfully verified with RF performance satisfying the intended cellular base station TX system. Fig. 18(a) and (b) demonstrates the proper functionality of the two fractional dividers by shortening the output period by 1/8 for the first channel ($4\times f_{o1} = (8/7)f_{\text{osc1}}$)



(a)



(b)

Fig. 19. (a) Measured injection-pulling spurs at the divider output versus separation of the two carriers. (b) Spectrum of spurious tone (right) and near injection locking (left).

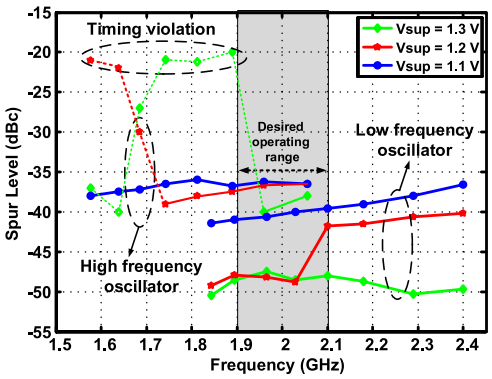


Fig. 20. Worst case spur through the entire tuning range for three different digital supply voltages.

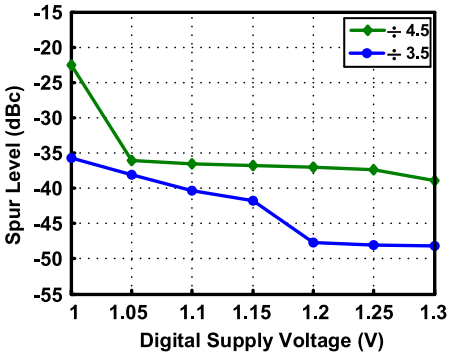


Fig. 21. Worst case spur power reduction of two dividers due to increasing power supply (at center frequencies of 2 GHz).

and elongating it by 1/8 for the second channel ($4 \times f_{o2} = (8/9) f_{\text{osc2}}$), respectively, when the rotators are engaged. The spurious tones due to the rotator timing mismatch are located at $k \cdot (f_{\text{osc1}}/4)/7$ for the up translator and $k \cdot (f_{\text{osc2}}/4)/9$ for the down translator, where k is the spur harmonic number. For $f_{\text{osc1}} = f_{\text{osc2}} = 8$ GHz, the fundamental spur locations are 285.7 and 222.22 MHz, respectively. The worst case measured spurious tones are -42 dBc for the up translation and -39 dBc for the down translation, which corresponds to around $\sigma = 2.5$-ps timing mismatch at each phase, based on the analysis of (5) with $N = 8$, which is shown in Fig. 15(a) and also in line with [28]. This spur level is acceptable for the intended operation in cellular base station TXs, which use large external cavity bandpass filters,[2] but it could be reduced for other applications using an adaptive delay mismatch calibration [22]. Note that the new nanoscale CMOS technology nodes will further improve this mismatch.

Since the two oscillators are separated by only 200 μm, their mutual coupling is expected to be high. The next set of experiments quantifies it. We first set the center frequencies of both oscillators at 8 GHz while measuring the spur level due to the injection pulling. Fig. 19 shows the relationship of the spur level versus frequency offset, which follows the 6 dB/octave fit of (2). With closer than 700-kHz separation (it will change with different injection power levels), the two oscillators experience injection locking. Fig. 19(b) (left) plots a spectrum of one oscillator just before it gets injection locked. Fig. 19(b) (right) shows the generated spurs due to the injection pulling at a given spacing from the carrier frequency. In order to avoid the injection locking and to suppress the injection pulling in the normal system operation, the phase rotators can be activated at the same time, but in the opposite directions, thus separating the resonant frequencies by about 2 GHz. As desired, both outputs are again at the same frequency, although at different duty cycles, which is corrected upstream in our intended system. However, the pulling is now almost nonexistent due to large separation (28%) of the two resonating frequencies. Through extrapolation of the injection pulling equation given in Fig. 19(a), the generated spur level would be insignificantly small below -80 dBc at the oscillator side and located 2 GHz away from the main carrier, which would anyway disappear in the second harmonic of the output.

Fig. 20 shows how the largest spur varies across the tuning range for both oscillators at three different supply voltages. It is clear that for the desired operating range with a nominal supply voltage of 1.2 V, there will be no timing violations. If an extended operation range is desired, putting the rotator at a lower supply voltage would be helpful. As shown in Fig. 11, in order to have the reliable selection, the select signal should come in the shaded area (best at the center). Setup and hold timing violations of the retimer or the multiplexer will result in

[2]The base station TX spurious requirements are extremely tough (e.g., -98 dBm in RBW = 100 kHz in GSM-900), hence large external cavity filters are used.

TABLE II
COMPARISON WITH OTHER PUBLISHED DIVIDERS

	[24]	[25]	[26]	[22]	[32]	**This Work**
Technology (nm)	250	350	700	45	65	**65**
Frequency (GHz)	5.5	2	1.7	4.75	2	**7.2/9.2**
Divide ratio	220 to 240	15/16	128/129	1.25	3-24	**3.5/4.5**
Number of phases	4	2×4	4	4	8	**8**
Power (mW)/V_{DD} (V)	59/2.2	2/1.5	24/3	9/1.1	0.6-1.6/1.2	**3/1.2**
Output noise floor (dBc/Hz)	N/A	-130	-142	-145[1]	N/A	**-156[2]**
Spur calibration	No	No	No	Yes	No	**No**
Area (mm^2)	0.09	0.04	N/A	N/A	0.00074	**0.0018**

[1]Including duty cycle correction buffers - [2]Including output buffers

significant spurs as this happens at some frequencies in Fig. 20 when the divider supply is increased to 1.3 V. It should be emphasized that these spurs are located very far from the main carrier and they will be filtered out downstream. At a midfrequency of 2 GHz, the supply voltage for both dividers is swept as shown in Fig. 21. Increasing the divider supply voltage improves the rising edges of the waveforms, which reduces mismatches between the branches, hence improving the spurious level. Table II compares this fractional divider with prior published work. This divider features the highest frequency of operation at the lowest power consumption and best noise performance.

VI. CONCLUSION

In this paper, various coupling mechanisms and methods to mitigate them for the purpose of multicore RF-SoC integration are studied and experimentally verified in a two-channel transmission subsystem realized in digital 65-nm CMOS. One of the consequences of the coupling is an injection pulling of an LC-tank oscillator, which creates unwanted spurs in the transmitted spectrum. Dicing the two-channel silicon die to physically separate two oscillators shows that the coupling through the common substrate is the most dominant coupling mechanism. In order to solve the problem of injection pulling, we propose a fractional divider based on an eight-phase rotator. Inserting the rotator between the oscillator and a PA or PA driver in a two-channel communication IC allows the oscillators to resonate at frequencies far away from each other (center frequencies separated by $\sim$28%) and from the common output frequency. In this way, the injection-pulling effect on the generated spurs would be virtually eliminated. In order to meet the noise floor requirements of wireless TXs, circuit complexity is put in the feedback path to relax the feedforward RF path. This produces a noise floor of only -156 dBc/Hz at $\sim$2 GHz. This proves attractiveness and competitiveness of the digital approach, whose goal is to replace RF functions with high-speed digital logic gates.

ACKNOWLEDGMENT

Authors would like to express their gratitude to NXP Semiconductors in Eindhoven, Netherlands, for financial support. Special thanks to Mark van der Heijden and his team at NXP Wireless Infrastructure for technical assistance. The authors would also like to thank R. Lotfi, I. Madadi, M. Alavi, and M. Babaie at the Delft University of Technology for the fruitful technical discussions, and A. Akhnoukh and W. Straver for their measurement support.

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