Variable Gain Amplifier With Output Optimization:

Professor Tai-Chang Chen
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Yumiko Kanasugi
Kendrick Tang
Hayley Garment
Jihoon Park

Introduction

The purpose of building a variable gain amplifier is to apply the all knowledge we have gained during the quarter about how to use the properties of BJT's to design different types amplifying circuits. Additionally, we have learned other applications of the transistor, namely current sources and active loads, and our design will utilize these features as well. In this final lab, we implement a three-stage operational amplifier with feedback loop using NPN and PNP BJT's.

Design Goals

Our design specifications are detailed below. In general the goal is to build a variable gain amplifier so the output is at least 0.5 W with low idling power.

Input signal specifications:

- Signal voltage: 100mV pkpk (min) – 5.6V pkpk (max)
- Signal source resistance 50 Ω

Minimum Design Specifications of the amplifier:

- Output power: 0.5W (minimum)
- Load Impedance (speaker): 8Ω
- Idling power: < 1W
- Distortion: No audible distortion in casual listening

Design and Simulation

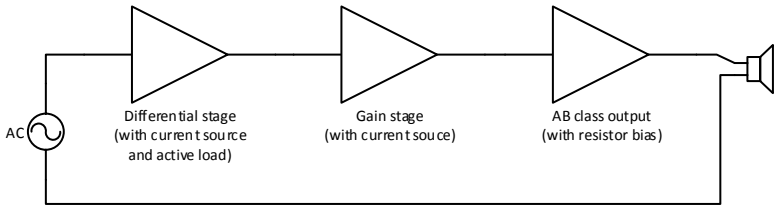

Figure 1 High level block diagram

The three stages of the amplifier are very interdependent. As a result, when doing the initial design in Multisim it was necessary to construct all three parts at the same time and bias each stage so the output would work well with the input to the next stage. It was also necessary to do everything with a standard non-inverting feedback loop to have finite and deterministic gain. Since the specifications require that the output deliver at minimum 0.5W to an 8Ω load, we know that our voltage has to be a minimum of 2V. With the input at a minimum of 100mV, this means that our amplifier must be able to deliver at least a gain of 20. As a result, the resistors R_s and R_f were picked to achieve a gain of at least 20.

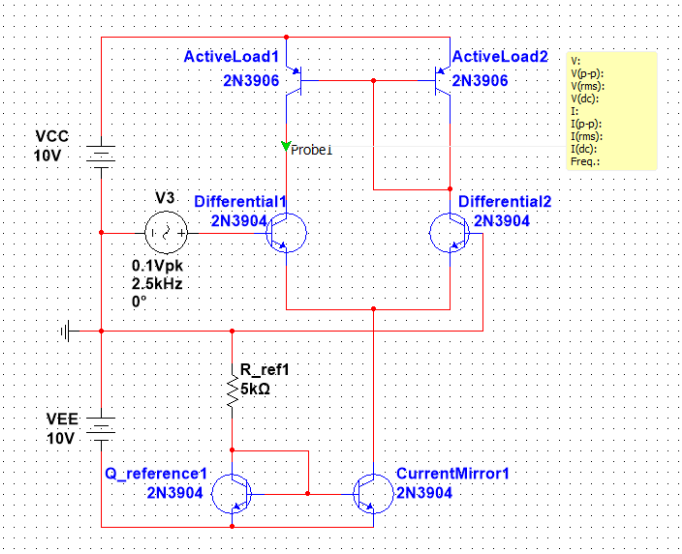

Figure 2 Stage 1 circuit topology

We first began by designing stage 1: the differential amplifier. The circuit configuration is shown as in Figure 2. The output is taken from the collector of the first half of the differential amplifier. The circuit topology consists of a standard NPN differential amplifier with a current mirror at the emitter, and a current mirror active load at the collectors. The current mirrors were used to bias the design to reduce the dependence on resistor biasing. The reference resistor in the first stage was chosen to be 5kΩ so that the current generated would be close to 2 mA. The active load is used to increase the gain of the first stage, which isn't really necessary because our DC rails are so small, but reduces the number of resistors in the first stage. The simulated and actual behavior of the first stage can be seen in Figure 6 in the testing section.

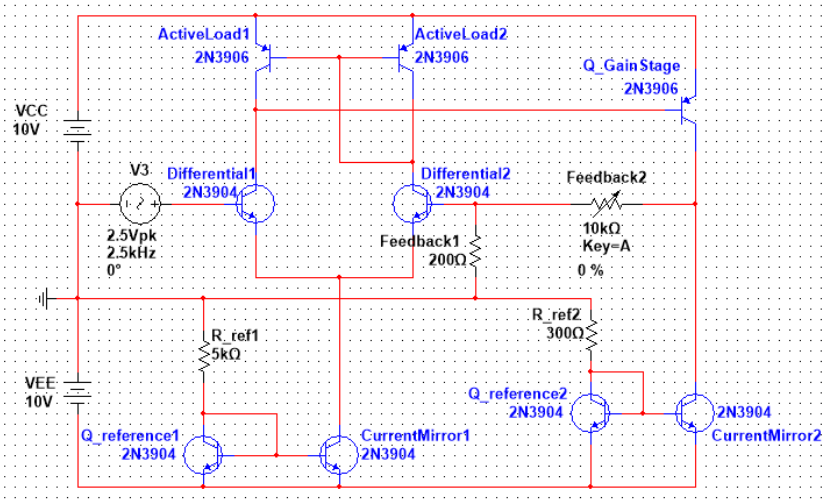

Figure 3 Stage 1 and 2 Circuit Topology

The second stage was a simple CE PNP amplifier with a current mirror generating the collector current. The configuration can be seen in figure 3. To have a significant amount

of gain, a 300Ω reference resistor was used. This would generate a current of approximately $\frac{10-0.7}{300} = 31$ mA. While this isn't that large, we used a power transistor anyway because our 2N3906 PNPs were mostly broken. The simulated and actual behavior of the first two stages can be seen in Figure 7 in the testing section.

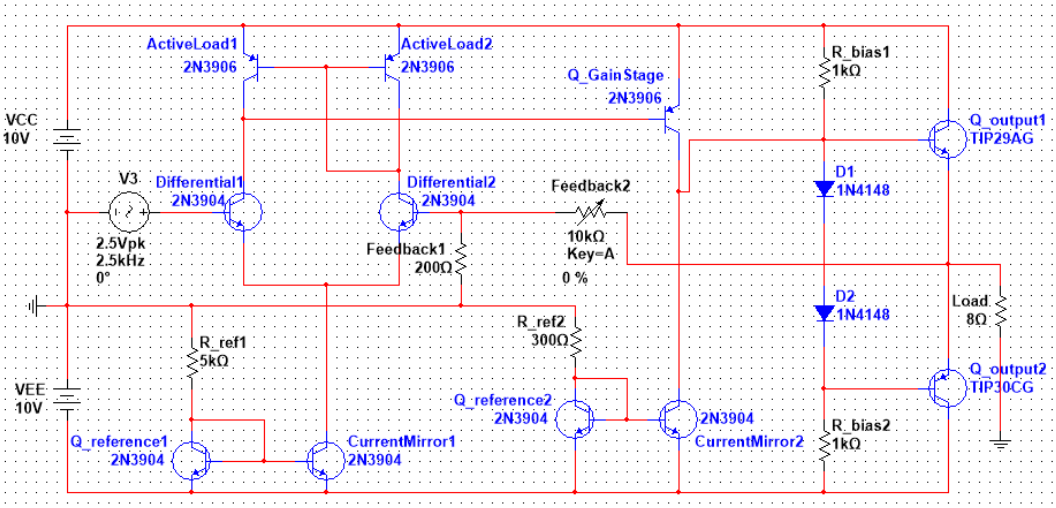

Figure 4 Final Circuit Topology

The final stage uses a standard AB class output. The final configuration can be seen in figure 4. The quiescent current is set by the bias 1kΩ resistors to be $\frac{10-0.7}{1000} = 9.3$ mA. We needed to keep the current large enough, yet also needed to keep the output range large enough to maintain at least 0.5 W. With 0.5 W being generated to an 8 ohm output, the currents through this output stage are very large. As a result, the NPN and PNP transistors used were TIP 29 and TIP 30, respectively, to provide proper heat dissipation and current ranges. The simulated behavior of all three stages with an 8 ohm load can be seen in Figure 5.

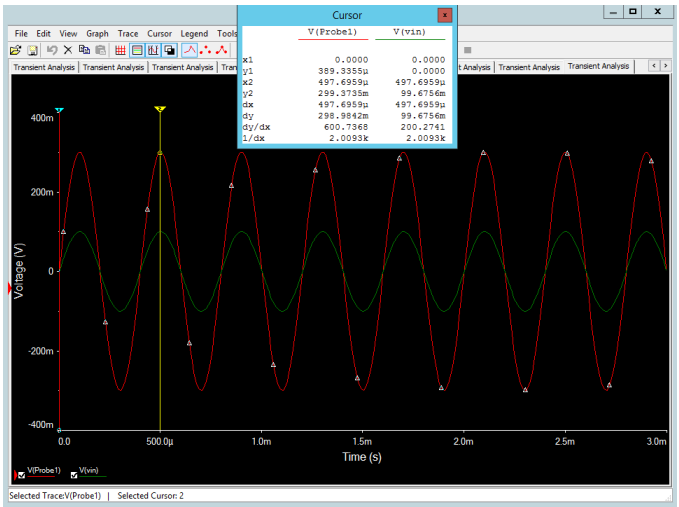

Figure 5 Final Amplifier Topology Simulated Behavior

Assembly

The first time the circuit was physically assembled, something went wrong at the second stage. After a frustrating night the group gave up and went home. The next day the circuit was dismantled, reassembled, and everything worked. We are not sure what happened. No design changes were made at this point.

Testing

The amplifier was tested in multiple stages. First, just the differential stage was tested with the inverting input grounded. As seen in the design section, the simulated and actual behavior matched pretty well so we deemed this a pass. Then the differential and gain stage were tested. Of course there was no load because didn't have the third stage yet. Instead, a standard non-inverting feedback loop was used to determine gain: $1 + \frac{R_f}{R_s}$. Again, the simulated and actual behavior matched. After the first two stages were deemed working, the output stage was added and tested with and without an 8 ohm load. After we were happy with the results, we put a standard speaker at the output and used the function generator to produce "music" because we didn't have access to the right cable. The final test results are in the results section.

The figures below compare the actual and simulated behavior up to the second stage. The final amplifier was tested with an oscilloscope, but the real test was with the speaker and real music.

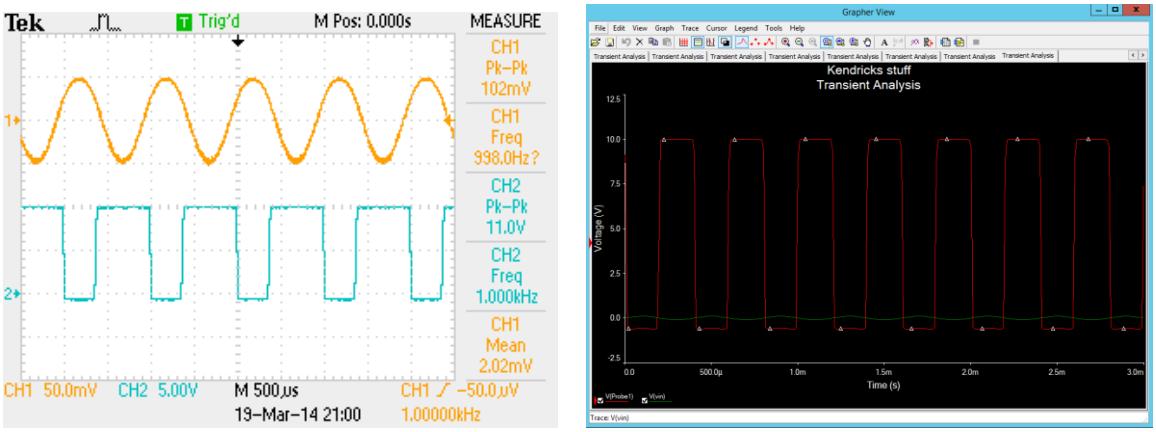

Figure 6 Stage 1 actual (left) and simulated (right) results

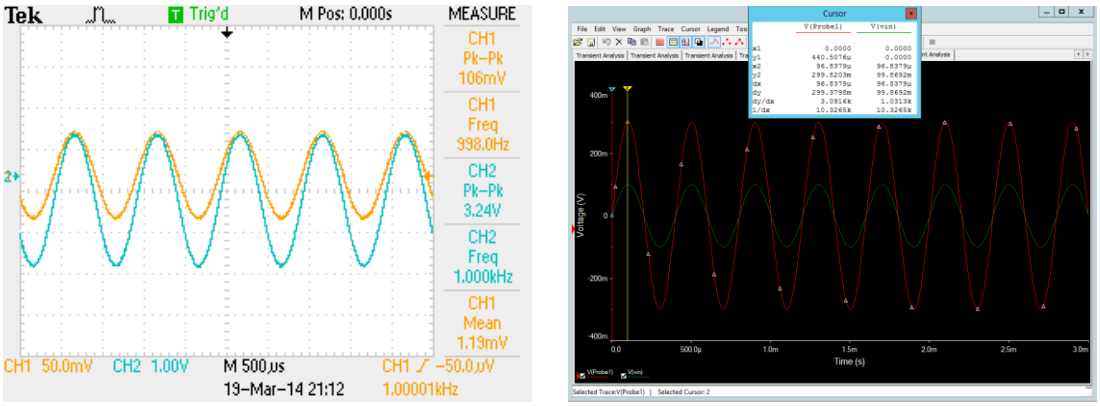

Figure 7 Stage 1 and 2 actual (left) and simulation (right) results

Results

This project was tricky because there were a few things needed to properly implement a three stage amplifier we didn't know about until someone read a few of the chapter in the textbook. Specifically, the need for a feedback loop at every stage to maintain a finite and deterministic gain, the use of power transistors at the output stage, and picking the right reference resistors so a 0.1 Vpp signal and 5 Vpp signal could be amplified without clipping. One other problem was that at one point the second stage produced a crazy amount of noise. We believe this had to do with some problem with the components or breadboard because when we rebuilt everything from scratch it worked almost perfectly.

The amplifier can vary its gain to produce at least a 0.5 W output with inputs ranging between 0.1 and 3 Vpp with an 8 ohm load. An idling current of 20 mA was drawn from the voltage source, which means, since $0.020A * 20V = 0.4\,W$, there is an idling power of 0.4 W.

Conclusion

A three stage variable gain amplifier was built. The amplifier utilized a differential stage, gain stage, an AB class output stage, and current mirrors to produce constant currents and active loads. It simulated very well and passed initial testing. During the demonstration a lower idling power was observed, a 0.5 W output power was obtained with a 0.1 Vpp signal and with the 3 Vpp signal. Sound was not achieved through the Bose speaker, but when we borrowed a store speaker after the professor left it produced very loud sound.