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Hw #4 CS 3340.501

1. MIPS Instruction

lui $t1, 0x03aa $t1 = 0x03aa0000

ori $t1, $t1, 0xcdef $t1 = 0x03aa0000 + 0x0000cdef => $t1 = 0x03aacdef

andi $t1, $t1, 0xffffcafe

0x03aacdef → 0000 0011 1010 1010 1100 1101 1110 1111 and
0xffffcafe → 1111 1111 1111 1111 1100 1010 1111 1110
0000 0011 1010 1010 1100 1000 1110 1110

0 3 a a c 8 e e

$t1 = 0x03aac8ee

sll $t1, $t1, 4 $t1 = 0x03aac8ee
= 0000 0011 1010 1010 1100 1000 1110 1110 shift 4
<< 4 = 0011 1010 1010 1100 1000 1110 1110 0000
= 3 a a c 8 e e 0
= 0x3aac8ee0

MIPS Instruction	$t1 value
lui $t1, 0x03aa	0x03aa
ori $t1, $t1, 0xcdef	0x03aacdef
andi $t1, $t1, 0xffffcafe	0x03aac8ee
sll $t1, $t1, 4	0x3aac8ee0