

Altium Designer ECG PCB Documentation

Ken Iiyoshi

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ENGR-UH 3611 Electronics

Using and Learning Altium Designer

Altium Designer can be used on a Mac by using virtual box or dual boot to Windows. The following youtube series was referenced for creating schematics, importing footprints, and generating a PCB layout:

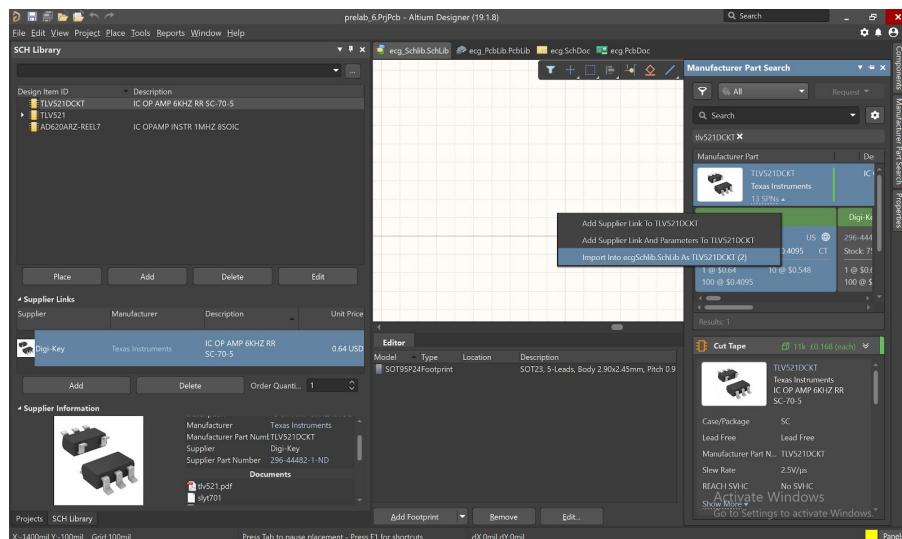
<https://www.youtube.com/watch?v=KpgTud1iQ-4>

Schematic and PCB Library creation

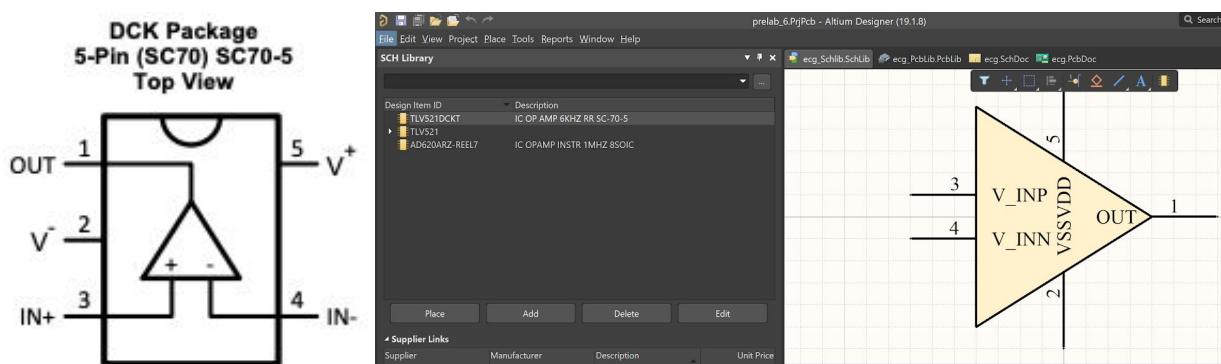
The PCB project consists of Schematic Library and PCB Library named “ecg”. Each library contains both the opamp and instrumentation amplifier.

Creating a schematic components for the Op amp

Ideally, we want to find from “manufacturer part search” TLV521DCKT including its pcb and schematic file. Although the component is available, the pcb and schematic files are not available. Thus, these files were manually created. The commercial component was first imported into the schematic library as shown below.

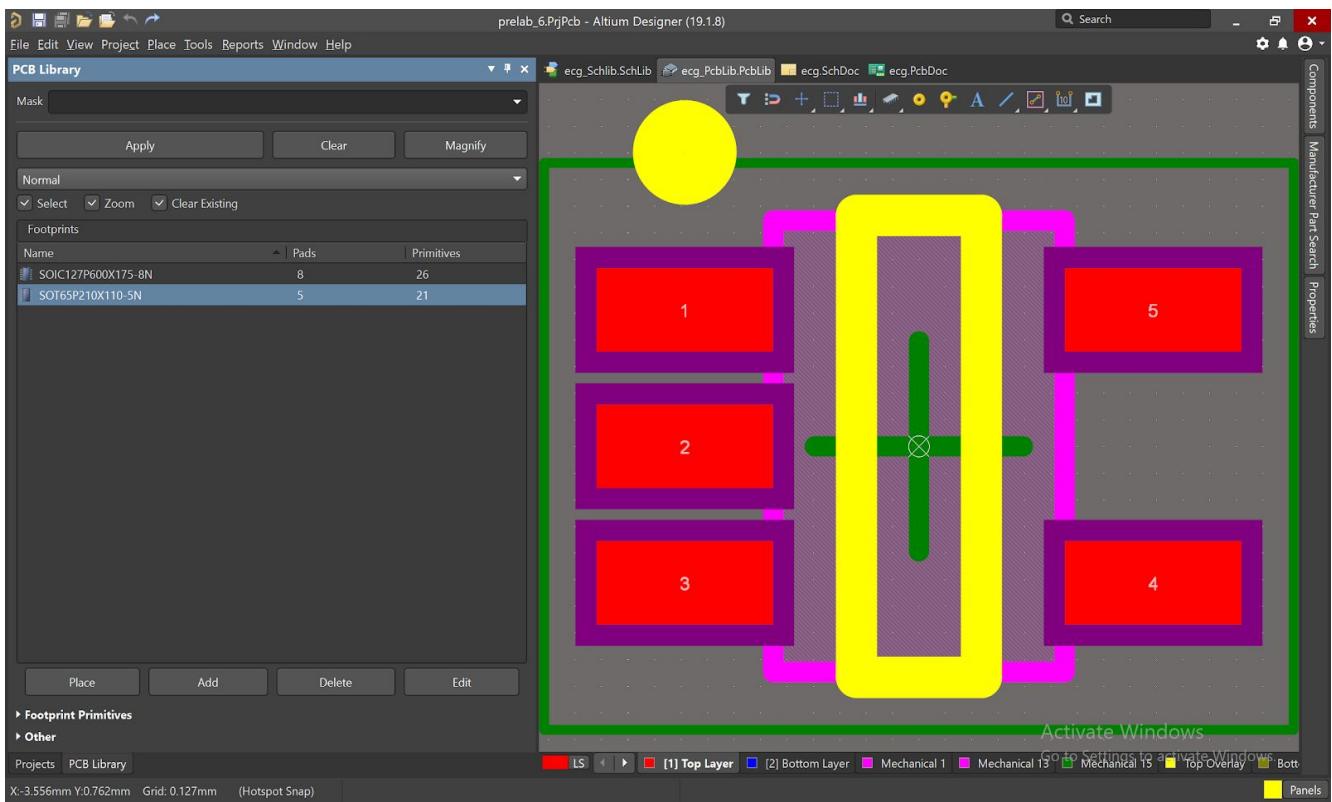
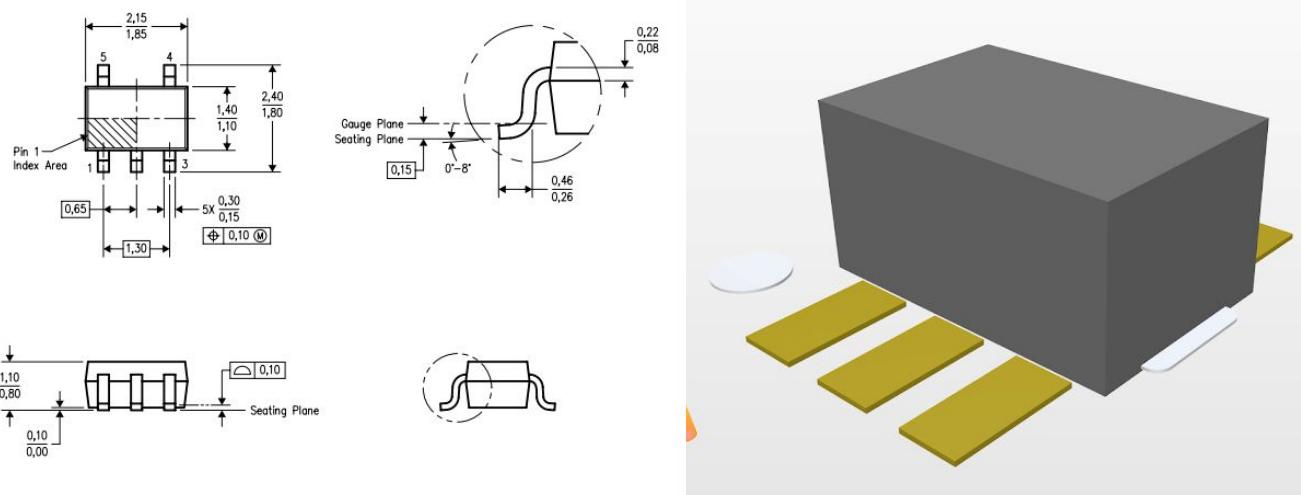


The pin configuration for the part via the component’s datasheet was used to construct the schematic for the opamp, as shown in the screenshot below



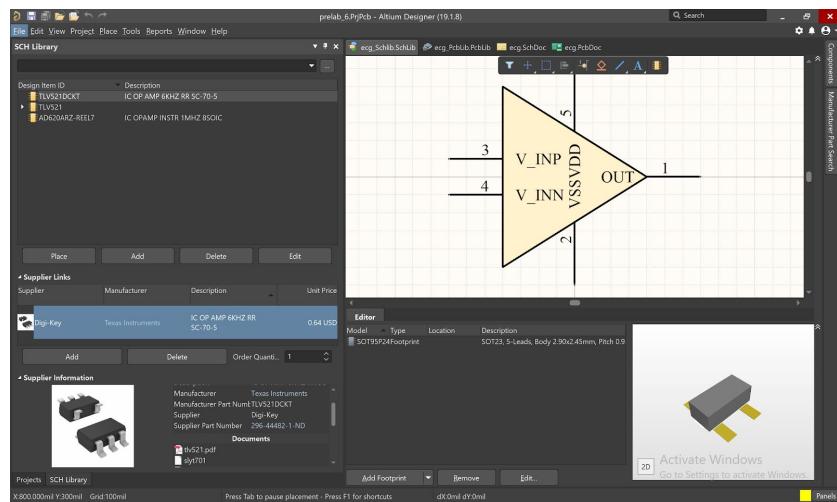
Creating a footprint for the Op amp schematic

According to the datasheet snippet shown below, TLV521DCKT is based on SOT23 Package (Small-outline transistor) with 5-Leads. Based on this, from the PCB library window, tools => IPC Compliant Footprint Wizard..., the footprint was imported with corresponding dimensions inputted. The resulting PCB footprint is shown in both 2D and 3D.



Attaching the footprint to the Opamp schematic

Attach this footprint to the schematic library into the schematic editor as shown below.



Repeating schematic and footprint creation/attachment for instrumentation amplifier

The process was repeated for the instrumentation amplifier, AD620ARZ-REEL7. The datasheet outlines the type of connections and footprints one can use. Note from the highlighted area that the IA is a SOIC (Small Outline Integrated Package). The following screenshot shows the resulting schematic for IA.

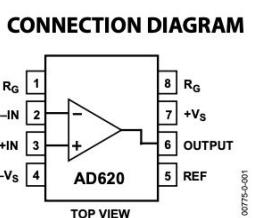
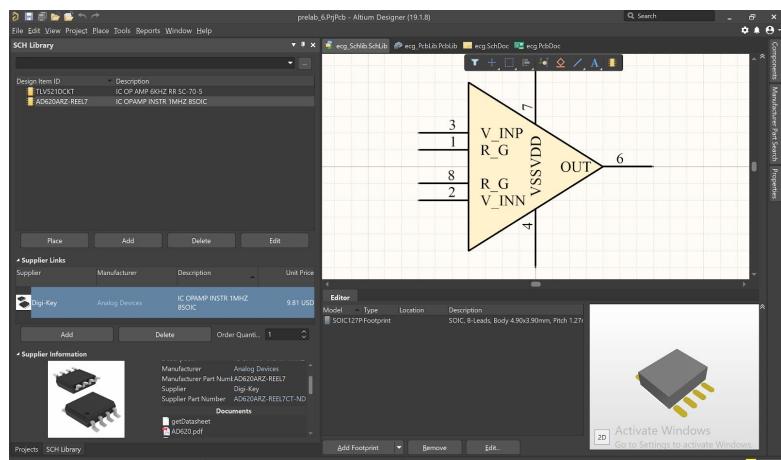


Figure 1. 8-Lead PDIP (N), CERDIP (Q), and SOIC (R) Packages

PRODUCT DESCRIPTION

The AD620 is a low cost, high accuracy instrumentation amplifier that requires only one external resistor to set gains of 1 to 10,000. Furthermore, the AD620 features 8-lead SOIC and DIP packaging that is smaller than discrete designs and offers lower power (only 1.3 mA max supply current), making it a good fit for battery-powered, portable (or remote) applications.



Based on the datasheet, just as with op amp, tools => IPC Compliant Footprint Wizard... was selected to import a footprint. The datasheet in the design data below was used for wizard's dimensions specifications. The following screenshot shows the footprint for the IA.

OUTLINE DIMENSIONS

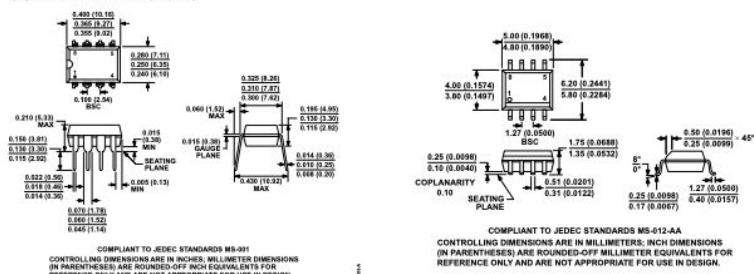


Figure 50. 8-Lead Plastic Dual In-Line Package (PDIP)
Narrow Body (N-8).
Dimensions shown in inches and (millimeters)

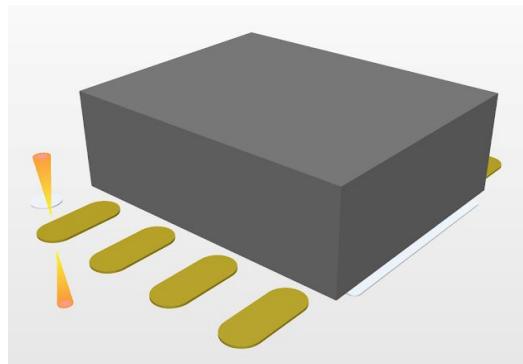
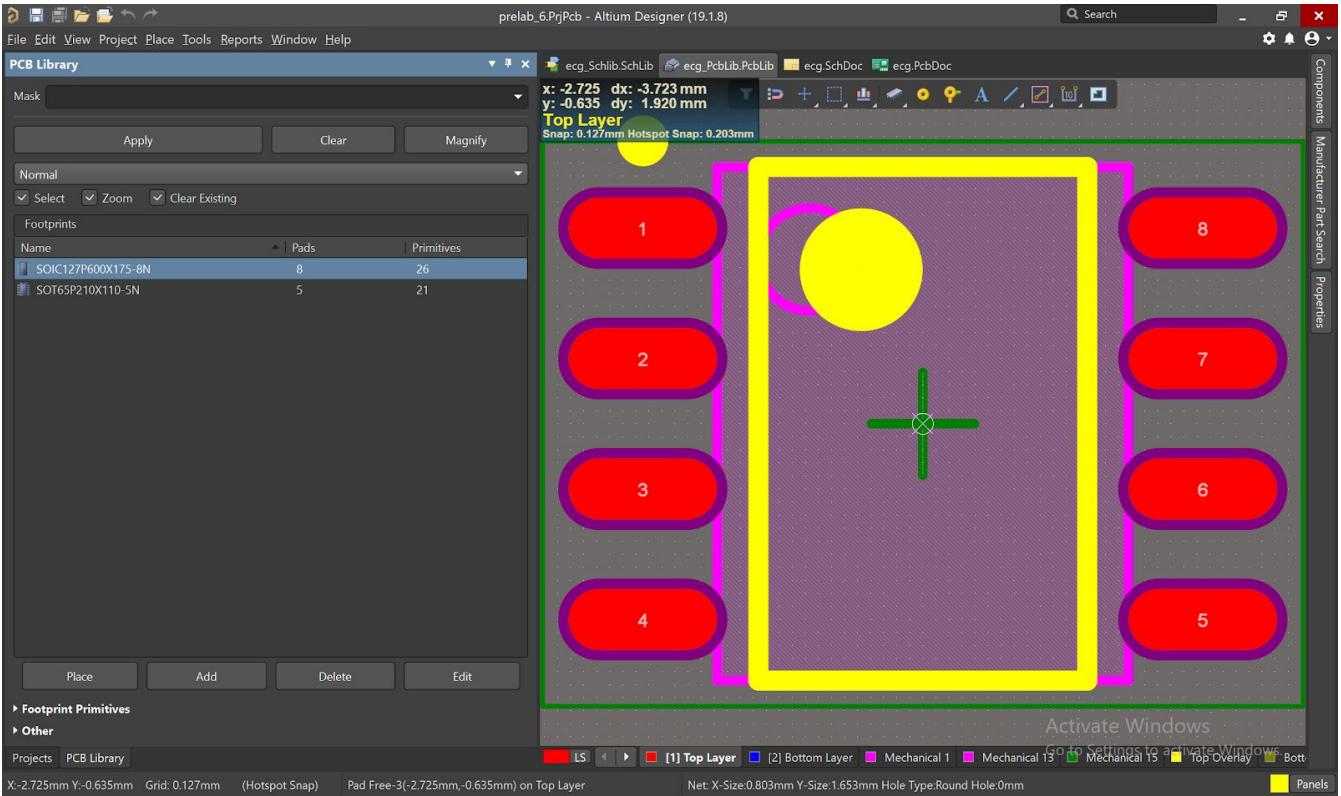
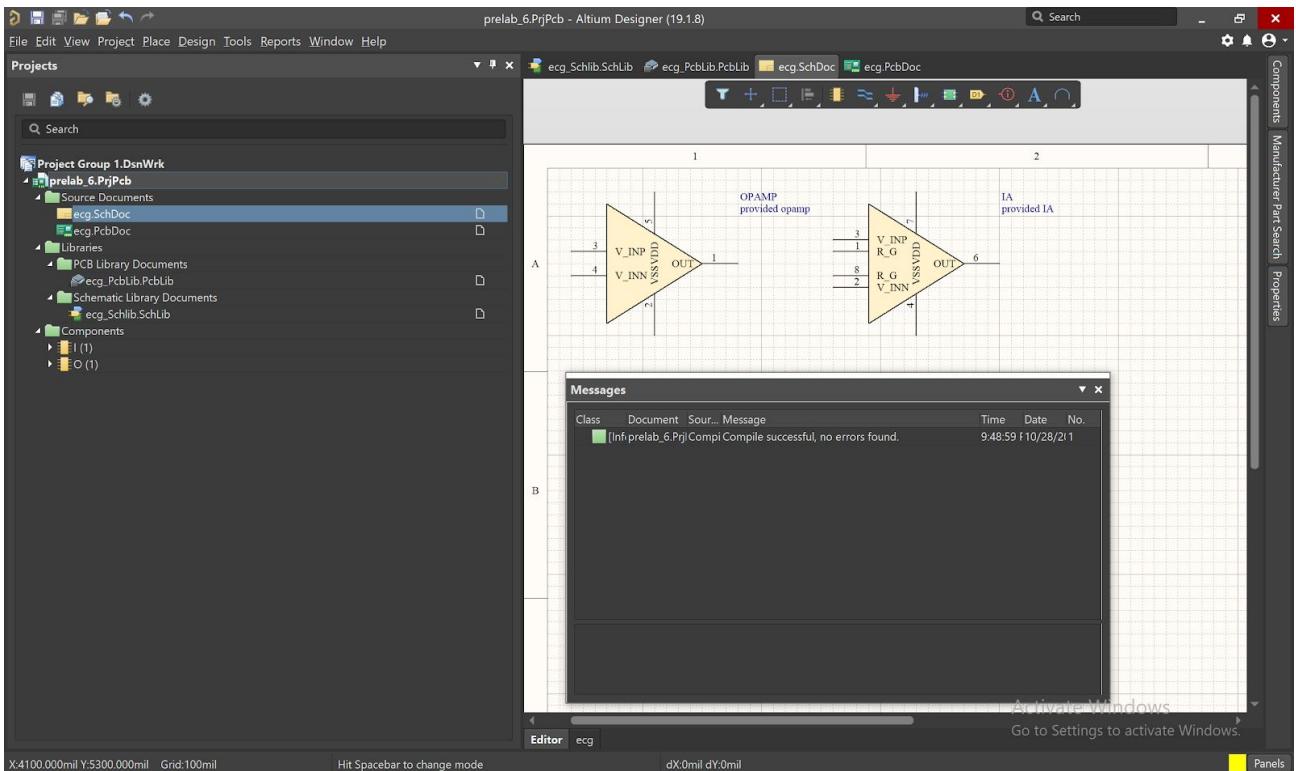


Figure 52. 8-Lead Plastic Dual In-Line Package (SOIC_N)
Narrow Body (N-8).
Dimensions shown in millimeters (and inches)



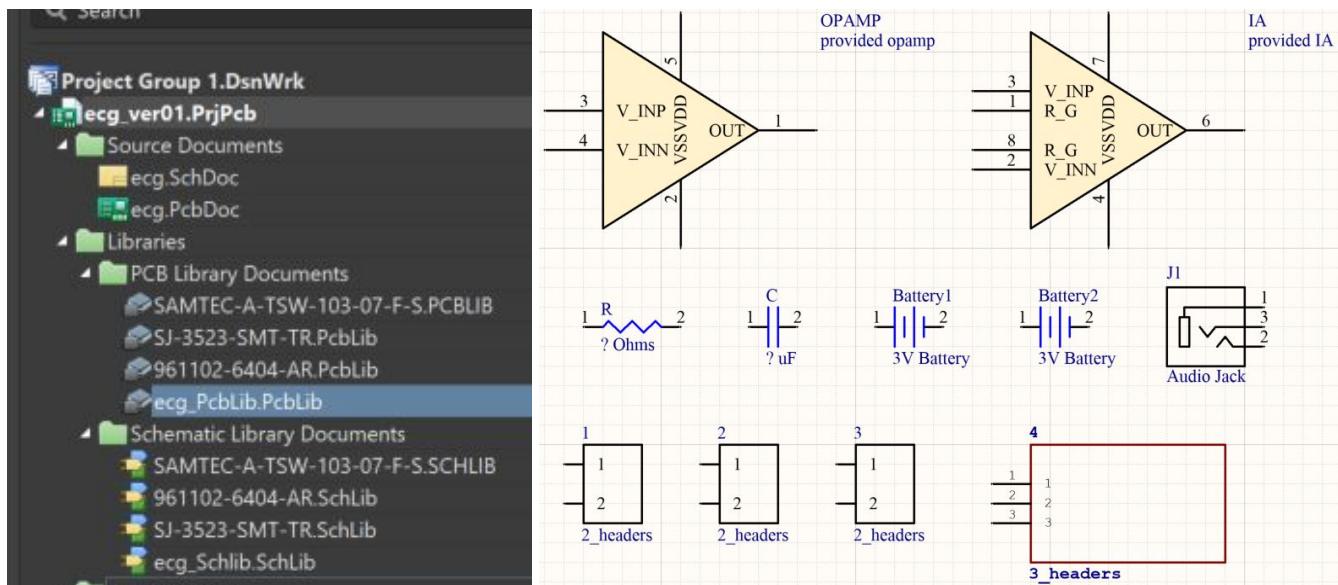
Instantiating the two components on a schematic

The instantiation of op amp and IA is shown below. The project was successfully compiled. Ecg schematic document can be updated (i.e. Design => Update Schematics command) to generate a PCB Document



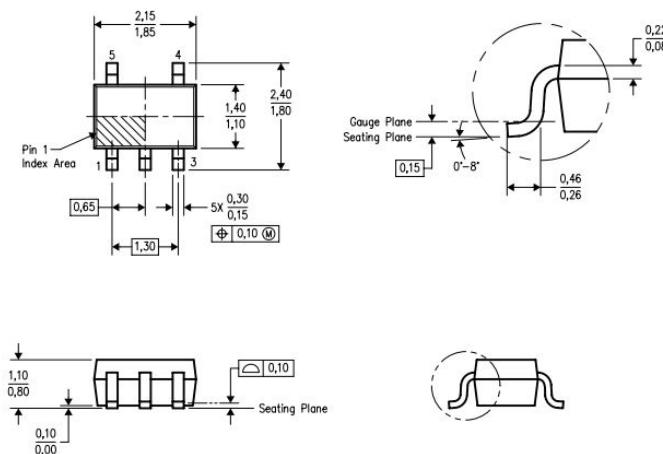
Overview + All Schematics Instantiation

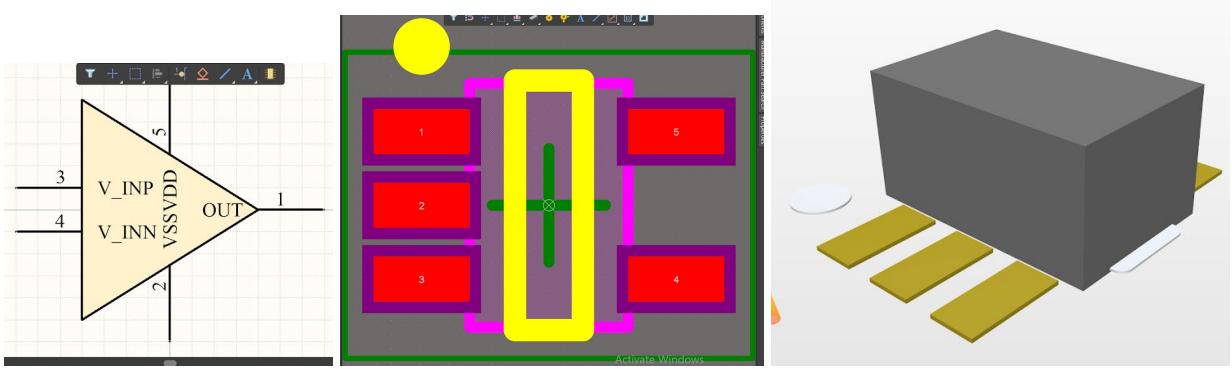
Opamp, IA, resistors, capacitors, and battery retainers were created within the `ecg_PcbLib` Library folder. Audio jack and 2 header pins, and 3 header pins were imported from existing libraries on Digi-Key, EasyEDA, or PCB3D.



Opamp Schematic & PCB

According to the datasheet snippet shown below, TLV521DCKT is based on SOT23 Package (Small-outline transistor) with 5-Leads. The resulting PCB footprint is shown in both 2D and 3D.





Instrumentation Amplifier Schematic & PCB

The data sheet for instrumentation amplifier, or AD620ARZ-REEL7, outlines the type of connections and footprints one can use. Note from the highlighted area that the IA is a SOIC (Small Outline Integrated Package). The following screenshot shows the resulting schematic for IA. Based on the datasheet, just as with op amp, the design data below was used for wizard's dimensions specifications. The following screenshot shows the footprint for the IA.

CONNECTION DIAGRAM

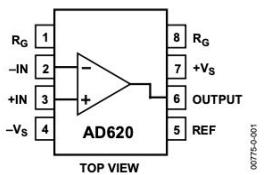


Figure 1. 8-Lead PDIP (N), CERDIP (Q), and SOIC (R) Packages

PRODUCT DESCRIPTION

The AD620 is a low cost, high accuracy instrumentation amplifier that requires only one external resistor to set gains of 1 to 10,000. Furthermore, the AD620 features 8-lead SOIC and DIP packaging that is smaller than discrete designs and offers lower power (only 1.3 mA max supply current), making it a good fit for battery-powered, portable (or remote) applications.

OUTLINE DIMENSIONS

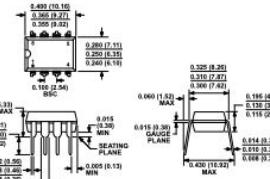


Figure 50. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body (N-8).
Dimensions shown in inches and (millimeters)

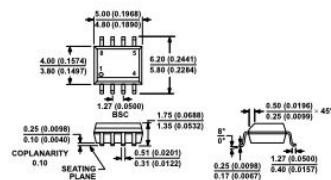
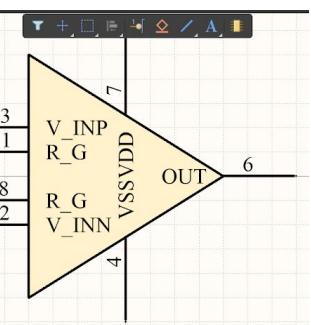
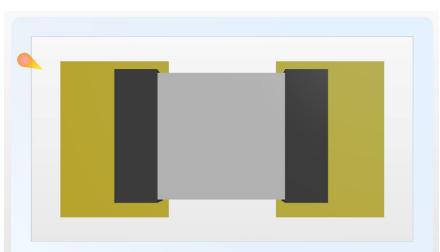
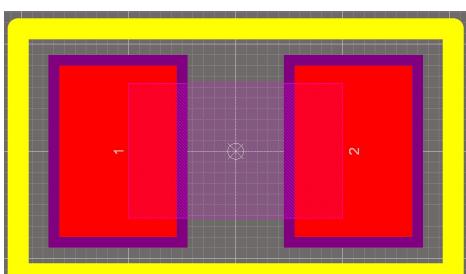


Figure 52. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (N-8).
Dimensions shown in millimeters and (inches)

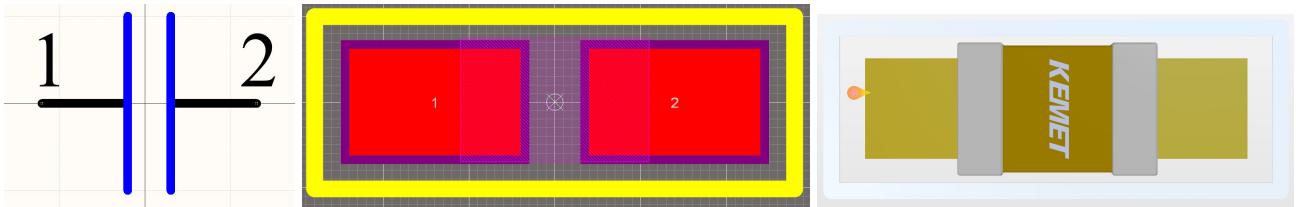
ESPEC-A



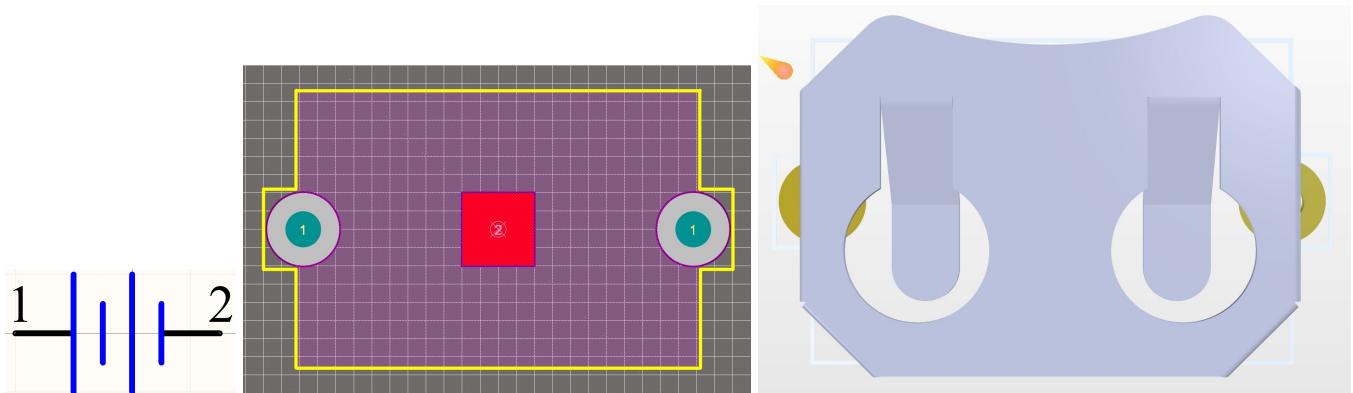
Resistor Schematic & PCB



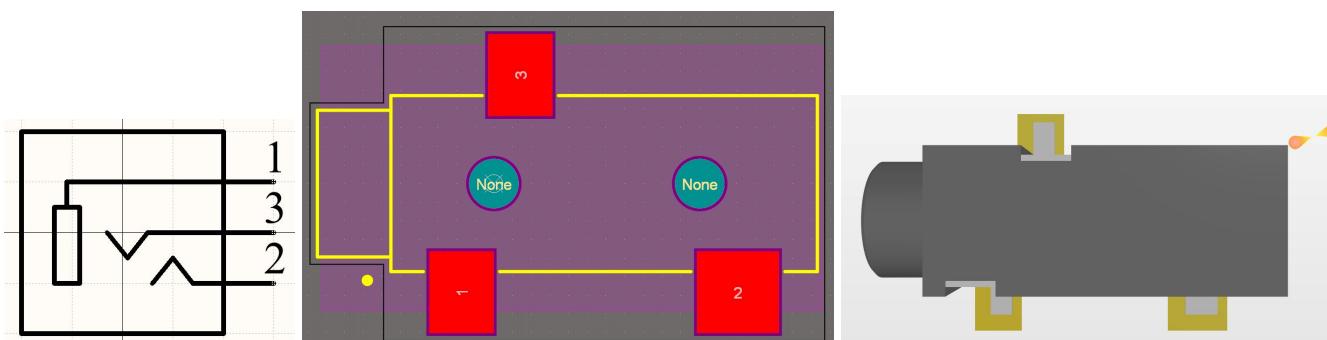
Capacitor Schematic & PCB



Battery Retainer Schematic & PCB

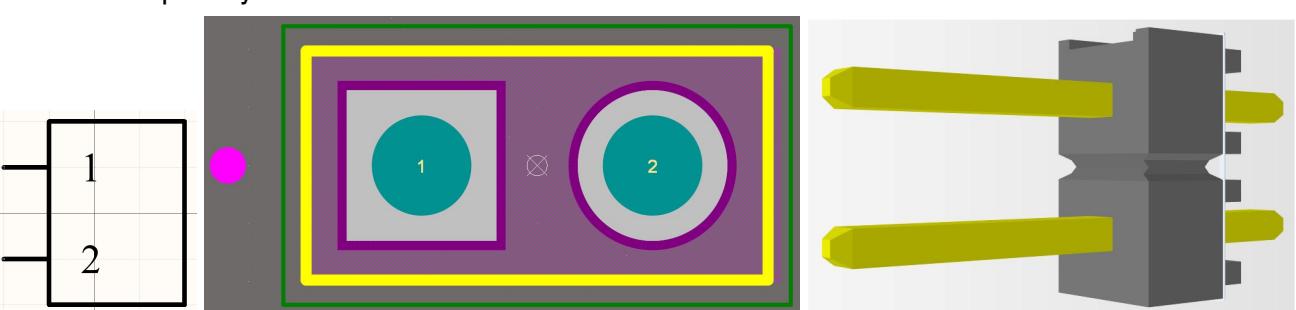


Audio Jack Schematic & PCB

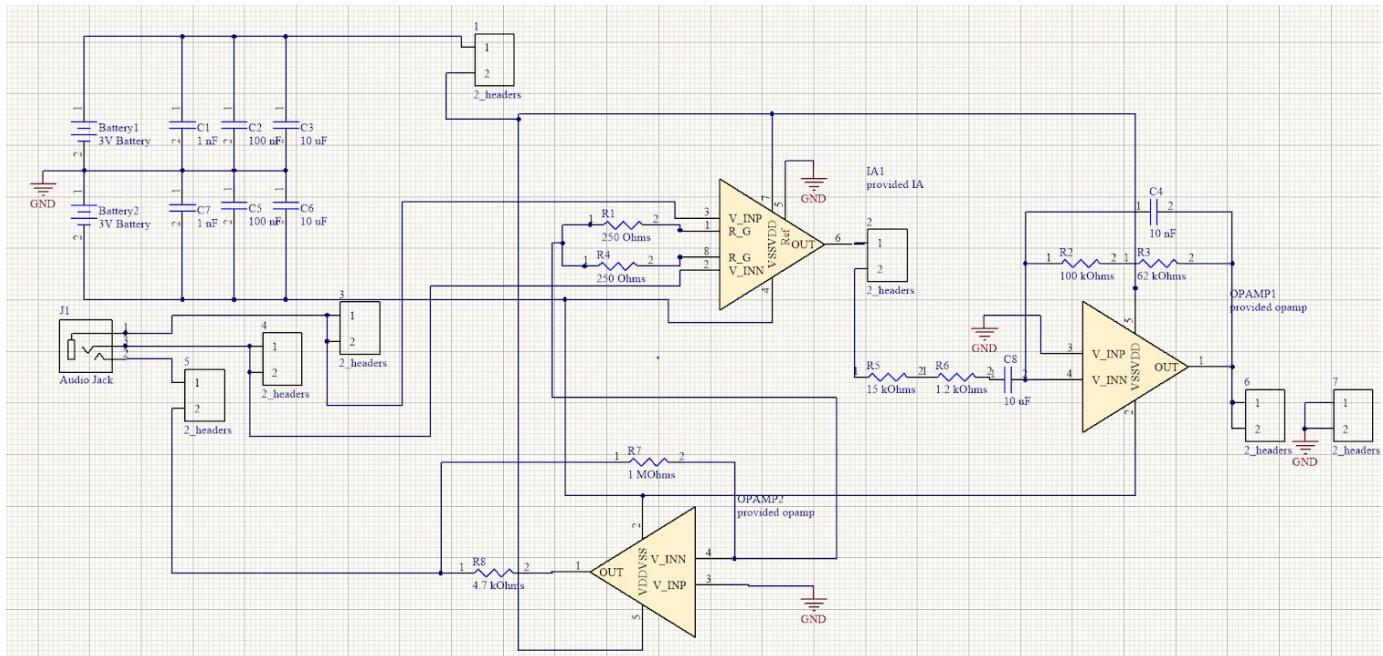


2 Header Pins Schematic & PCB

Header pins are used to probe output to oscilloscope as well as to any other external device". By having header pins between the IA and filter, the IA signals can be tested without the filter. We'll put a jumper on the header pins to connect the IA output to filter input. See the screenshot below for the header pin layout.

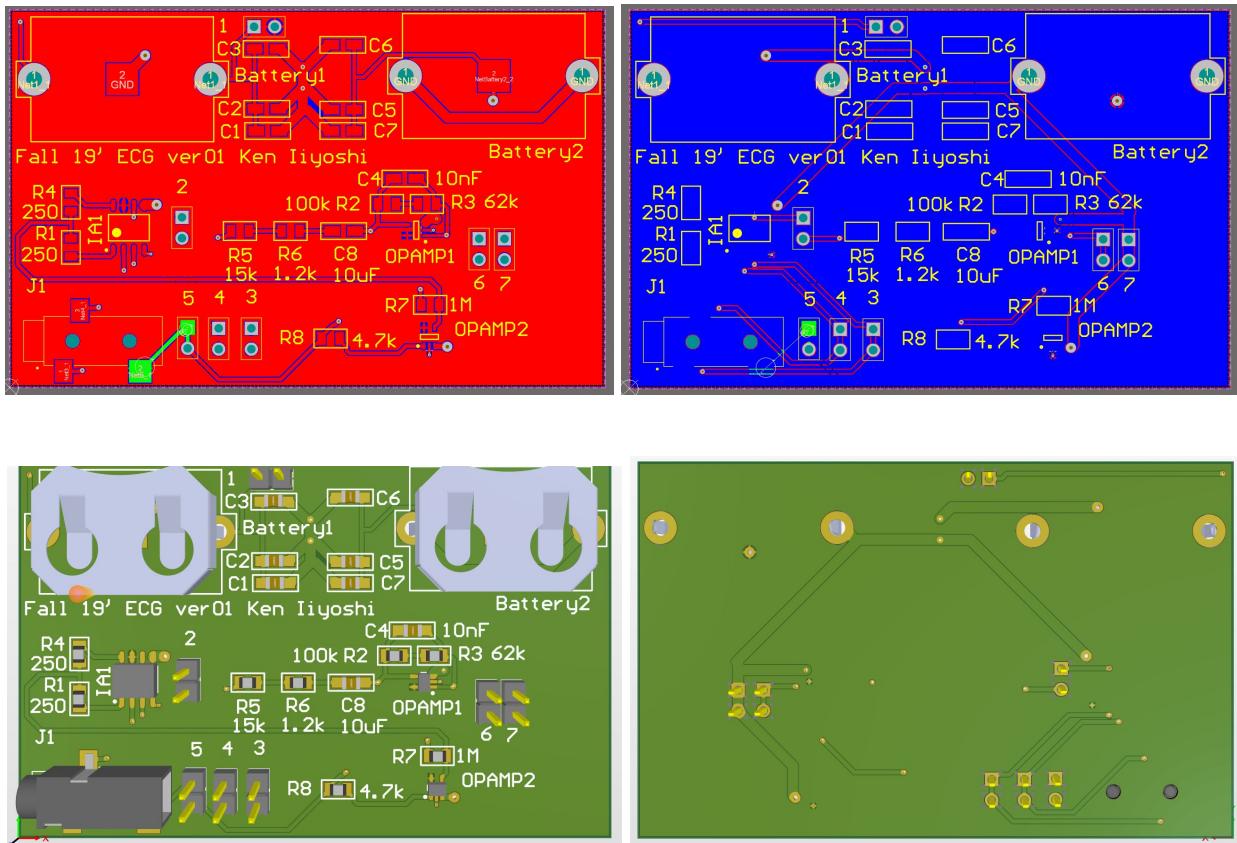


ECG Schematic Diagram



- GND ports are connected to each other by default when the pcb is fabricated.
 - Filter resistor/capacitor values: They are supposed to achieve gain=10 and 1~100Hz bandwidth. With IA gain = $1 + 50,000/54 = 927$, the ecg's total gain would be approx 10k.
 - R'' selected as $162k = 62k+100k$. Hence, $R' = 16.2k = 15k+1.2k$
 - $C' = 1/(2\pi \cdot 16.2k) = 10 \mu F$. Gain = 10 so $1000C'' = C'$. Thus, $C'' = 10nF$.
- Multiple capacitors(10u,100n,1nF - to cover different frequency bands). Empty spaces can be used for routing. Power line should as thick as possible.
- Bias voltage is most likely 0.2~0.3 V so the output voltage would range probs ± 2.7 .
 - Note that in lab we used $\pm 15V$ VDD/VSS. Our output was less than this so output signals weren't clipped. But, the battery only provides $\pm 3V$. So here's my suggestion for updating R_g :
 - INA121 Gain = $1 + 50k/R_g$
 - R_g for lab: $27 \text{ Ohms} \times 2$. Thus, gain = $1 + 50k/54 = 940$
 - Now, with filter gain = 10, the total gain for the ECG become 1k. I.e few mV ECG body signal amplifies to few Volts output
- You can use net names to help make the schematic look nice, just don't try to validate your design until you have multiple net labels for each net
 - Place → net
- Once your schematic is ready make sure to annotate your schematic
 - Tools -->annotate

PCB design:



Steps for PCB design

1. Create route

- PCB Layout: It's sensible to mirror the schematic design for the pcb layout, as seen in the screenshots below. Red is the top layer, blue is the bottom layer.
- Recommended default route width is 10mil (0.254mm). For ground, 50mil (1.27mm) The main focus is to minimize noise on the ECG signal route (i.e. make the connections wide and short).
- Use 50% neck-down option in the design rules so to fit the 0.2543mm line into the opamp pins. The minimum line width is 0.001mil (0.000254mm) btw according to one manufacturer (<https://www.sunstone.com/pcb-manufacturing-capabilities/detailed-capabilities>).
- One tool for checking missing connections is Tools->Design Rule Check... When you run it, it shows you message for any design warnings. (ignore Minimum Solder Mask Silver, as this detects opamp pins.)

2. Adjust board shape

3. Pour on both sides

- Recommended: VDD for top layer, VSS for bottom layer.
- Need vias for VSS

4. Add Keepout layer to make boundary for pcb company.

5. Generate output

- File -> smart PDF ->
- Deselect bill of materials
- Edit the PCB board outline thing so that there are two specific layers, top and bottom and that they both include the board outline