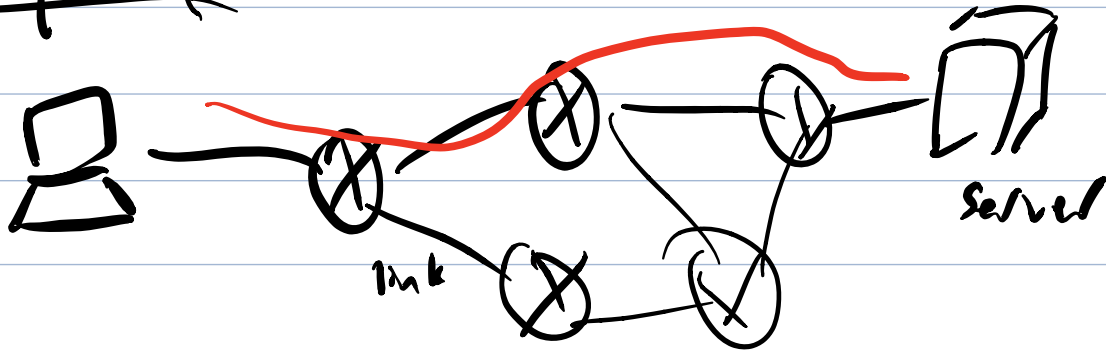


instance of app \leftrightarrow instance of app
process \leftrightarrow process
host \leftrightarrow host
hop \leftrightarrow hop



ARP: address resolution protocol $IP \rightarrow MAC$
host and routers: nodes

channels connecting adj. nodes: links (wired, wireless, LANs)

layer-2 packet: frame (encapsulated datagram)

data-link layer is responsible for fixing datagrams from one node to a physically adj. node

Network Datagram ↓

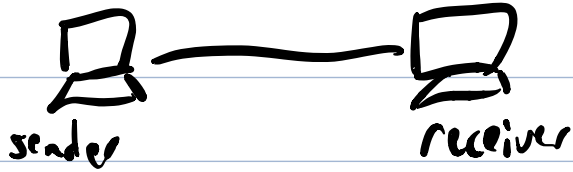
Link HL Datagram TL frame

- offers framing, link access

- reliable delivery between adj. nodes

Reliable data transfer means to deliver packets in order without errors

- flow control



↳ ensures that sender will not overwhelm the receiver buffers (implemented w/ feedback)

- error detection

↳ errors caused by signal attenuation & interference
↳ receiver detect presence of error

↳ signals sender for retransmit or drop frame

- error correction

↳ receiver identifies and corrects bit errors without resorting to re-tx

- half-duplex and full-duplex

↳ half-duplex: a node can either tx or rx

↳ full-duplex: a node can tx and rx at the same time

link layer implemented mostly in NIC.



each intf has an NIC in a router

EDC - error detection & correction bits

Error Detection



parity checking

→ detect single bit errors

odd parity

- add 1 bit to data s.t. # of 1s is odd

1011 → 10110

even parity

- add a parity bit to make #1s even

2D parity check

↳ assume e.g. odd parity

D = 1010 1100 1011

00100

1011	0
1100	1
1010	1
0010	0

10101 11011 10110 → rx

1	0	1	0
1	1	0	0
1	0	1	0
0	0	1	0

error
↳ flip to 1

Cyclic redundancy checking (CRC)

- more powerful, detect multiple bit flips

Sender receiver
 Agree generator $G: 1001$ $G: 1001$
 data D
 CRC R $\frac{D \parallel R}{G} \bmod 2 = 0$

$D \parallel R$ \longrightarrow
 CRC calculated s.t. $\frac{D \parallel R}{G} \bmod 2 = 0$ (no remainder)

Assume G has $r+1$ bits.
 Then size of CRC (R) will be r bits
 \Rightarrow Max # errors that we can detect is r

frame $D' \parallel R'$
 $\frac{D' \parallel R'}{G} \bmod 2 = r$
 0 1
 No error detected errors

e.g. data = 101110 sender side, compute CRC
 $G = 1001$

CRC size $r=3$ \uparrow = size of R
 $r+1=4$

LSL r bits left

$D \times 2^r$

$$R = \frac{D \cdot 2^r}{G} \bmod 2$$

$\rightarrow 101110000$

division mod 2:

- subtraction is XOR

w/o a borrow

- result of a division
mod 2 is the leading
bit of the dividend

$$R = \text{rem} \left(\frac{D \cdot 2^r}{n} \right) = \underline{011}$$

Sender transmits
frame D || R

101110011

$$\begin{array}{r} \overline{101011} \\ 1001 \overline{) 101110000} \\ \underline{1001} \\ 00101 \\ \underline{000} \\ 1010 \\ \underline{1001} \\ 00110 \\ \underline{000} \\ 1100 \\ \underline{1001} \\ 1010 \\ \underline{1001} \\ 011 \\ \underline{000} \\ R \end{array}$$