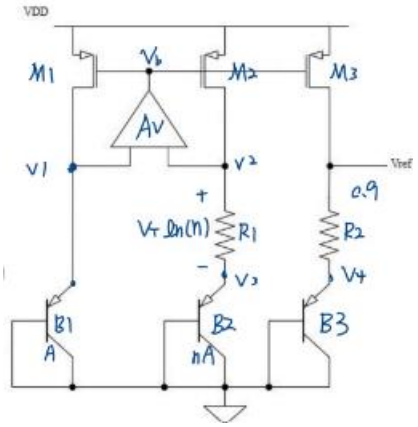
EE3235 Analog Integrated Circuit Analysis and Design I
Final Project

Part I - Bandgap Reference

Bandgap reference							
Working Item	SPEC			Your work			
Supply voltage VDD	1.98V	1.8V	1.62V		1.98V	1.8V	1.62V
T.C. from -40~125℃	< 20ppm/℃			TT	14.098	18.713	19.242
				SS	13.933	18.775	19.236
				FF	13.649	17.589	19.675
Bandgap voltage	1.36V			TT	1.3616	1.3627	1.3606
VDD	1.8V, -40~125℃						
PSR @ DC	< - 40dB			TT	-47.43 ~ -42.23		
				SS	-48.02 ~ -42.22		
				FF	-47.35 ~ -42.25		
PSR @ 10kHz	< - 30dB			TT	-46.90 ~ -42.23		
				SS	-47.13 ~ -42.26		
				FF	-46.14 ~ -42.27		
VDD	1.8V, 27℃, TT						
Power Consumption(μW)	<50μW			18.4562uW			

1. Design Consideration

(a) Determine the ratio of the two resistors through calculation and calculate the expected Vref.



Assume that the current of B1, B2 and B3 are same and the formula of PNP BJT is:

$$I_C = I_S * \exp\left(\frac{V_{BE}}{V_T}\right) \overset{\text{def}}{\cong} V_{BE} = V_T * ln\left(\frac{I_C}{I_S}\right)$$

The size of B2 is n times of PNP BJT

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln\left(\frac{n * I_C}{I_s}\right) - V_T \ln\left(\frac{I_C}{I_S}\right) = V_T \ln(n)$$

And we know $V_1 = V_1$ and $V_3 = V_{BE2}$, $V_1 = V_{BE1}$ ∴

$$R_1 = \frac{V_T \ln(n)}{I_{D2}} \leftrightarrow I_{D1} = I_{D2} = I_{D3} = \frac{V_T \ln(n)}{R_1}$$

And $V_{ref} = V_{BE2} + R_2 \times I_{D3} = V_{BE3} + \frac{R_2}{R_1} V_T \ln(n)$

When V_T = 26mV → $\frac{R_2}{R_1} = \frac{V_{ref} - V_{BE3}}{V_T \ln(n)} = \frac{38.46(V_{ref} - V_{BE3})}{\ln(n)}$

- Calculate V_{BE3} :

$$V_{BE3} = V_T \ln\left(\frac{I_c}{I_s}\right), I_s \approx 1.879 \times 10^{-18} A \ldots (1)$$

$$\frac{V_T \ln(n)}{R_1} = I_B + I_C = \frac{\beta + 1}{\beta} I_C, \beta \approx 1.37 \; in \; PNP_{X15_{V50}} \ldots (2)$$

$$when \; choosing \; n = 12, R_1 \approx 100k\Omega \sim 300\Omega, V_{BE} \; is \; about \; 0.6 \sim 0.7 \approx 0.65V$$

$$\rightarrow \frac{R_2}{R_1} \approx 38.46\left(\frac{(V_{ref} - 0.65V)}{\ln(n)}\right)$$

- T.C. calculation

$$V_{ref} = V_{BE} + \frac{R_2}{R_1} V_T \ln(n)$$

$$\frac{\partial V_{ref}}{\partial T} = 1 \times \frac{\partial V_{BE}}{\partial T} + \frac{R_2}{R_1} \times \ln(n) \times \frac{\partial V_T}{\partial T} should \; equal \; 0$$

$$\therefore \frac{R_2}{R_1} \times \ln(n) = -\frac{\partial V_{BE}}{\partial T} \div \frac{\partial V_T}{\partial T} \approx 2.4 \div 0.087 \approx 26.436$$

  - Why using 2.4 ?

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4 + m)V_T - \frac{E_q}{q}}{T}$$

So, when V_{BE} = 0.65V, $\frac{\partial V_{BE}}{\partial T} \approx -0.0024 V/K$

$$when \; choosing \; n = 12, \ln(n) \approx 2.5 \; \therefore \frac{R_1}{R2} \approx 10.57 \rightarrow choose \frac{R_1}{R_2} = 10.5$$

$$expected \; V_{ref} \; \therefore V_{BE3} + \frac{R_2}{R_1} V_T \ln(n) \approx 1.3606V$$

(b) Given the power consumption limitation, arrange the total current you can use carefully; by doing so, you can determine the absolute value of the two resistors, and be able to design the OPAMP based on the current budget you set.

$$\text{Power} = V_{DD} \times \left(I_{D1} + I_{D2} + I_{D3} + I_{opamp}\right) < 50uW$$

Assume that the power of OPAMP is about 48uA.

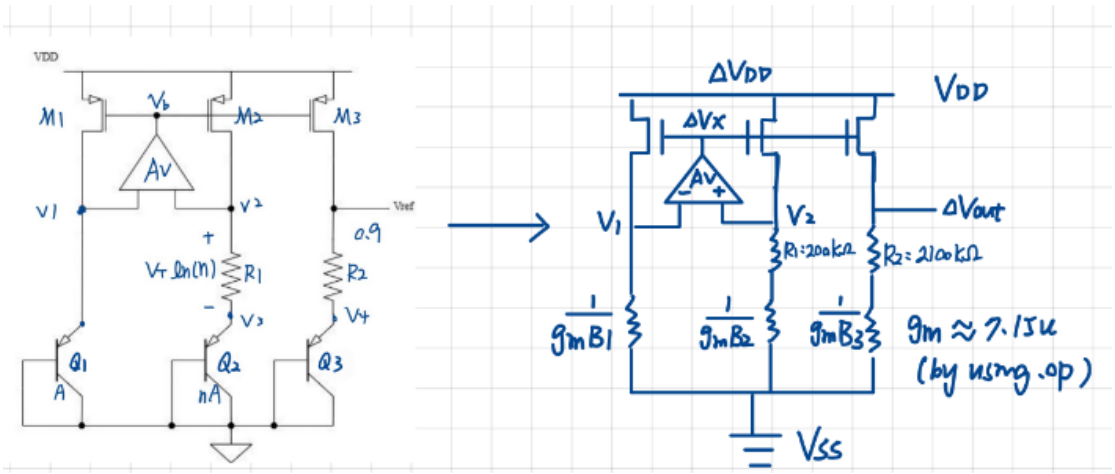
$\therefore I_{D1} = I_{D2} = I_{D3}$ $\therefore I_{D2} < 0.37$uA, and $R_1 = \frac{V_T \ln(n)}{I_{D2}}$

$$\therefore R_1 > \frac{V_T \ln(n)}{0.926uA} = 175k\Omega \rightarrow choose \; R_1 = 200k\Omega$$

$$\rightarrow R1 = 200k\Omega, R_2 = 2.1M\Omega, V_{REF} = 1.36V$$

$$power \; budget \; of \; OPAMP: 48UW$$

(c) PSR (Power Supply Rejection) is an important indicator for evaluating the quality of a bandgap reference circuit. Please analyze the aspects through which PSR can be improved and how the gain of the OPAMP would affect PSR. Use proper calculation and analysis to establish the specifications for the OPAMP.



$$\Delta V1 = g_{m1}(\Delta V_X - \Delta V_{DD})\left(\frac{1}{g_m Q_1} \parallel r_{o1}\right)$$

$$\Delta V2 = g_{m2}(\Delta V_X - \Delta V_{DD})\left(R_1 + \frac{1}{g_m Q_1} \parallel r_{o2}\right)$$

$$since\ M1 = M2 \rightarrow r_{o1} = r_{o2}\ ;\ Q1(A)g_m = Q2(nA)\ g_m \rightarrow g_{m1} = g_{m2} = g_{m3} = gm$$

$$(\Delta V_2 - \Delta V_1) \times A = \Delta V_x$$

$$\rightarrow g_m(\Delta V_x - \Delta V_{DD})R_1 A = \Delta V_X$$

$$\rightarrow (g_m R_1 A - 1)\Delta V_x = g_m R_1 A \Delta V_{DD}$$

$$\frac{\Delta V_x}{\Delta V_{VDD}} = \frac{g_m R_1 A}{g_m R_1 A - 1} \rightarrow (\Delta V_x - \Delta V_{DD}) = \frac{1}{g_m R_1 A - 1} \times V_{DD}$$

$$\Delta V_{out} = g_{m3}(\Delta V_x - V_{DD})\left(R_2 + \frac{1}{g_{m3}} \parallel r_{o3}\right)$$

$$= g_{m3}\left(\frac{1}{g_m R_1 A - 1}\right)\Delta V_{DD}\left(R_2 + \frac{1}{g_m} \parallel r_{o3}\right)$$

$$PSR = 20\log\left(\frac{\Delta V_{out}}{\Delta V_{DD}}\right) < -40dB \rightarrow \frac{\Delta V_{out}}{\Delta V_{DD}} < 0.01\ V/V$$

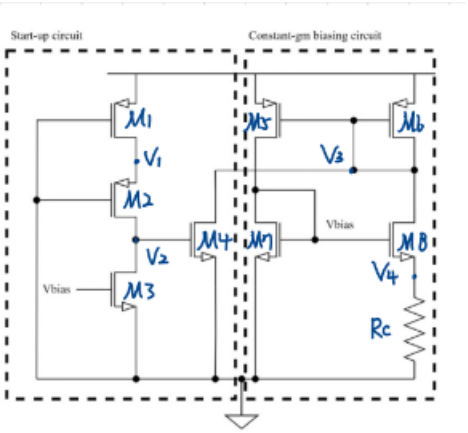
$$\frac{\Delta V_{out}}{\Delta V_{DD}} = g_{m3}\left(\frac{1}{g_m R_1 A - 1}\right)\left(R_2 + \frac{1}{g_m} \parallel r_{o3}\right) \approx gm\left(\frac{1}{g_m R_1 A - 1}\right) * R_2 < \frac{0.01V}{V}$$

$$\left(\frac{1}{g_m R_1 A - 1}\right) < 6.67 * 10^{-4} \rightarrow A > 1050.7V/V$$

So we should design the OPAMP which has gain larger than 1050V/V.

(d) Design the OPAMP based on the structure shown in Fig. 3. and Fig. 4. and, the analysis you did in the previous parts.

- Start-up Circuit



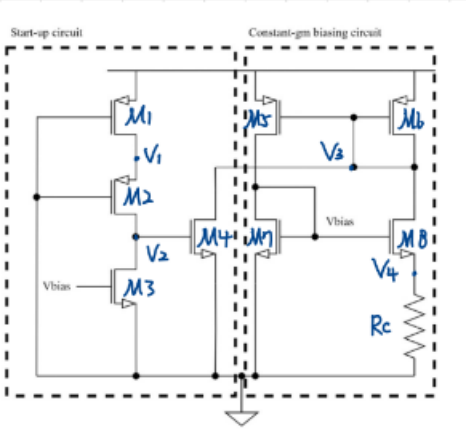
When V_{DD} is low, start-up circuit should turn on to increase the speed of turning on constant gm core and when V_{DD} is high, start-up circuit should turn off so it will not affect constant gm core and increase power consumption. When turning on, M1 ~ M4 should all in saturation (or subthreshold) and when turning off, M1 and M2 should cut off or in linear region and M3 or M4 should remain in saturation region to maintain the operation of constant gm core. When sizing each PMOS and NMOS, I first set the ratio of $W/L_{PMOS} = 3\ W/L_{NMOS}$ and we know:

$$I_D = 2unC_{ox}\frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}\right]^2 (1 \pm \lambda V_{DS})$$

$$P_{total} = V_{DD} * I_{total}$$

So, if the size of the transistor is too large, the power consumption might exceed our power budget, so I increase the length of each transistor to lower the current. Also, I decrease the width of each transistor to increase threshold voltage which makes current smaller. Finally, the size of M1 and M2 are W/L = 0.9um/20um and the size of M3 and M4 are W/L = 0.3um/20um.

- Constant gm core



Assume M7 and M8 have same current, and the width of M8 is k times of M7. Assume k is 4 and M7 and 8 satisfy square law.

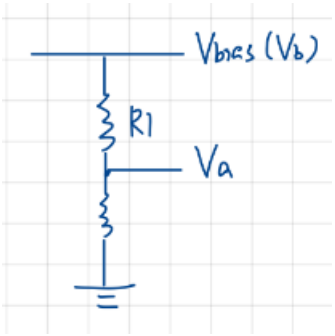
$$\therefore V_{ov8} = \frac{V_{ov7}}{2}$$

So, we know that:

$$R_C = \frac{V_{ov7}}{2}$$
$$I_D = \frac{V_{ov8}}{R_c}$$
$$V_{ov8} = \frac{2I_{D2}}{g_{m8}}$$
$$\rightarrow g_{m8} * R_C = 2 \; and \; g_{m6} * R = 1$$

In contrast to being exclusively a constant gm circuit, it actually functions as a constant g_m * Rc circuit. The current passing through M7, regardless of process variations, corner conditions, temperature fluctuations, or supply voltage changes, upholds the characteristic of gm=1/R. This consistent gm is particularly advantageous for our amplifier design, ensuring a relatively stable bandwidth. Based on the aforementioned analysis and adhering to the 3:1 mobility sizing rule, the sizes for M5, M7 (PMOS) are set to 3um/1um, and the size for M6 (NMOS) is set to 1um/1um. Given that K is designated as 4 for the square law behavior mentioned earlier, the size for M8 is established at 4um/1um.

- Voltage divider for V_{bias}

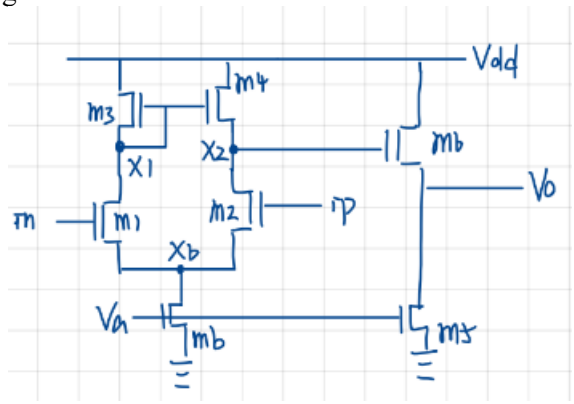


To achieve the desired biasing for the two-stage OPAMP design in BGR, adjustments to the V_{bias} output from the constant-gm core with the start-up circuit are necessary. The typical Vbias output ranges between 0.6 to 0.8V, making it challenging to raise it to 1.2V for PMOS biasing or lower it to 0.4V for direct NMOS biasing. Opting for a single-ended single-biasing point two-stage OPAMP simplifies the requirement to a single low biasing voltage.

For the biasing of the tail current NMOS in the two-stage OPAMP design, a biasing voltage of approximately 0.3 to 0.4V is preferred. To achieve this, I decided to implement a voltage divider using large resistors. The goal is to split the original Vbias output from the constant-gm core and start-up circuit in half. This approach not only satisfies the biasing requirements for the two-stage OPAMP design but also ensures that Vbias remains temperature-independent. By splitting the voltage to ground rather than the temperature-dependent V, temperature independence is maintained.

I selected resistors $R1$ and $R2$ for the voltage divider, both set to 5MΩ. Choosing large resistors minimizes current flow, thereby reducing the impact on the voltage divider's influence on the constant-gm core. This strategy ensures the stability of the constant-gm core output around 0.6V and maintains temperature independence which let V_a satisfy the specification (< 20ppm/℃).

- Two-stage OPAMP



I choose a single-ended second stage and a single biasing voltage two-stage OPAMP, considering the constant-gm core with the start-up circuit provides only a single low biasing voltage, Vbias. This configuration simplifies the design, utilizing the given Vbias to produce a non-differential output voltage.
When designing the sizing for this two-stage OPAMP, I set the size of PMOS 3um/1um, and the size of NMOS 1um/1um since the mobility of NMOS and PMOS is 3:1. Finally, the tail current transistor is sized at 2um/1um since the current will flow to 2 NMOS of first stage amplifier.

And the gain of this 2-stage amplifier is:

$$A_V = A_{v1} * A_{V1} = \left(g_{m1,2} * r_{o3,4}\right) * (gm_6 * (r_{o5} \parallel \text{r\_o6})) \approx 4852V/V$$

The gain is larger than 1050V/V.

(e) Complete the whole bandgap reference circuit design.
From (a) to (d) I design the size of BJT, transistors in start-up circuit, constant gm core and two stage OPAMP and the resistors in BGR and constant gm core, so the only part that I haven't designed yet is the size of the transistors in BGR.

- Size of M1, M2 and M3
  At the beginning, I set the size of three PMOS transistors 3um/1um, then I found there is a serious channel length modulation effect which will affect the stability of the circuit. So, I increased the size of M1, M2 and M3 to 30um/10um.
  When increase the Length of transistors:
  - $r_o = \frac{V_A}{I_D} = \frac{1}{\lambda I_D}$. Increasing L can increase Av so ro can be larger which decrease the effect of channel length modulation.
  - $gain = g_m r_o = \sqrt{2\mu n C_{ox}\left(\frac{W}{L}\right)} \times \frac{1}{\lambda I_D}$ so, if the length increases, λ will decrease and gain will increase.
  - Larger transistors are generally less sensitive to manufacturing process variations, like oxide thickness, doping levels.
  - Since the length is larger, it will be less affected by the short channel length effect.
  - The parasitic transistors can be smaller.

  Therefore, I design W/L=30um/10um so the circuit can be more stable.

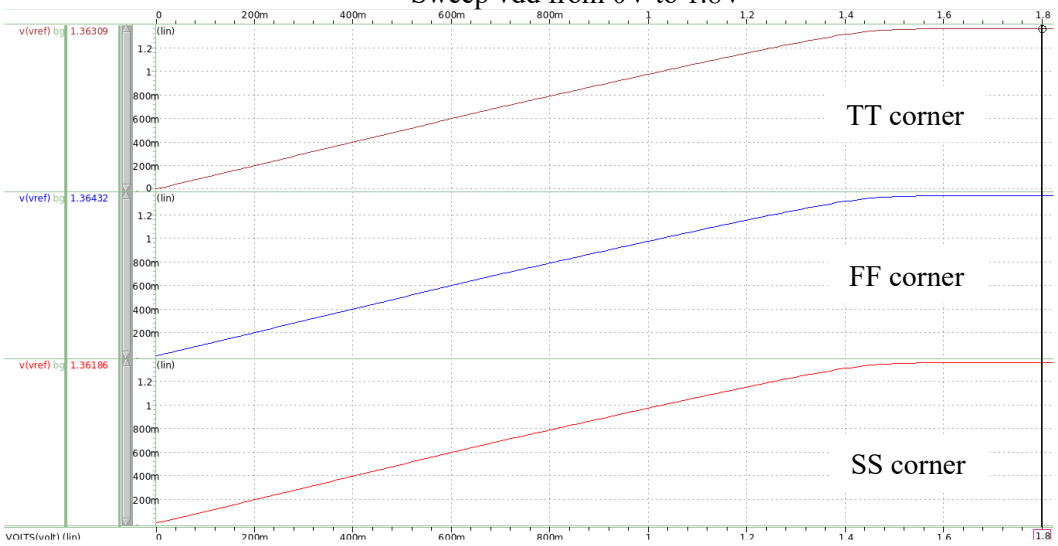
So we complete the whole design, each parameter is shown below.

Bandgap reference					
M1	30um/10um	M2	30um/10um	M3	30um/10um
Q1	m=1	Q2	m=12	Q3	m=1
R1	200kΩ	R2	2.1MΩ	-	-
Start-up circuit					
M1	0.9um/20um		M2	0.9/20um	
M3	0.3um/20um		M4	0.3um/20um	
Constant gm core					
M4	3um/1um		M5	3um/1um	
M6	1im/1um		M7	4im/1um	
Rcgm	150kΩ		-	-	
Two stage OPAMP					
M1	1um/1um		M2	1um/1um	
M3	3um/1um		M4	3um/1um	
M5	1um/1um		M6	3um/1um	
Mb	2um/1um		-	-	
R1	5MΩ		R2	5MΩ	

2. Simulation result

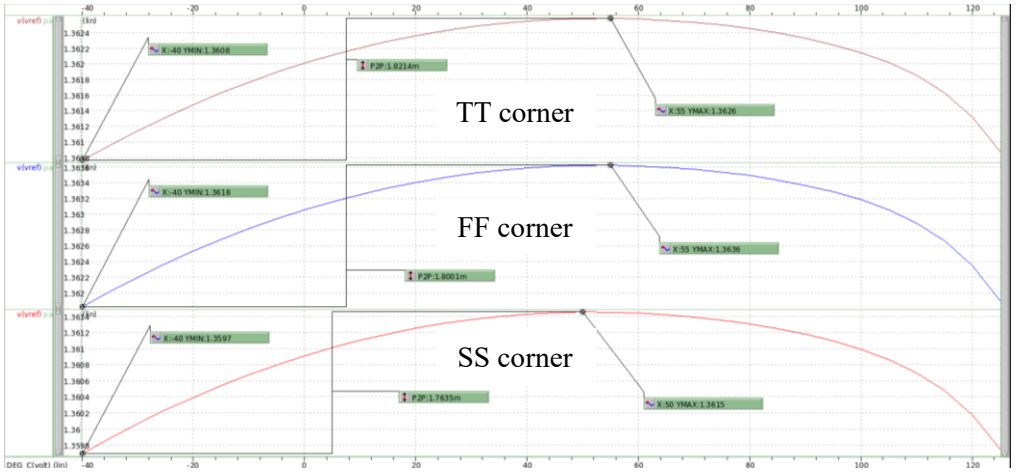
(a) .DC

Sweep vdd from 0V to 1.8V



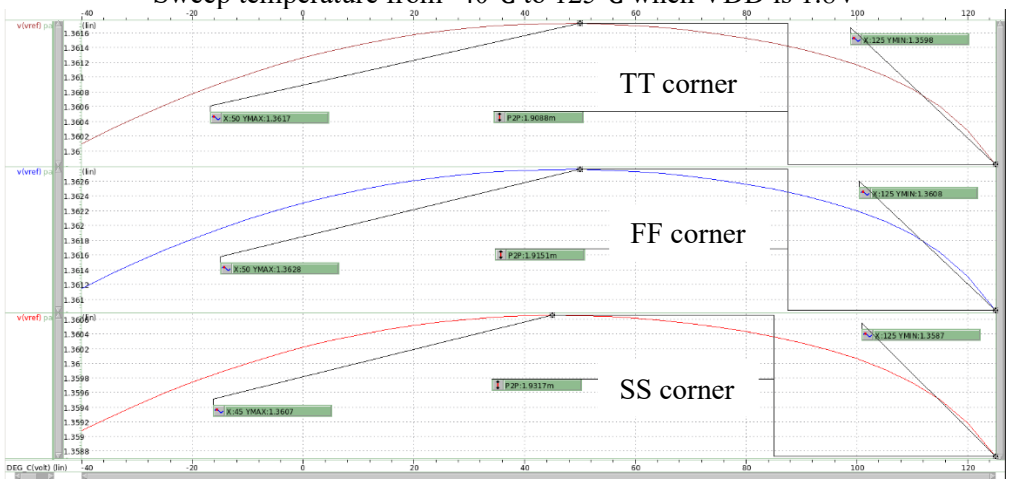
x-axis: Vdd (V) – y-axis: vref (V)

Sweep temperature from -40℃ to 125℃ when VDD is 1.98V



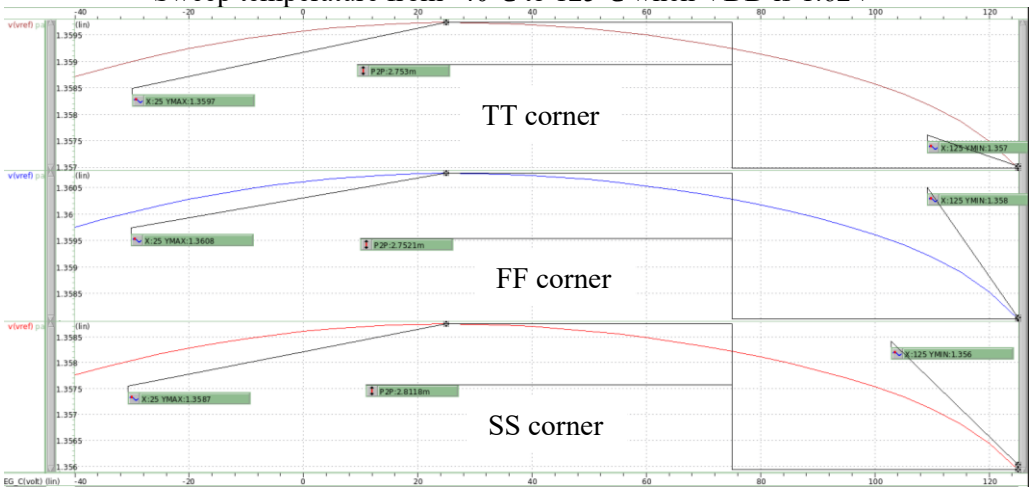
x-axis: temperature (℃) – y-axis: vref (V)

Sweep temperature from -40℃ to 125℃ when VDD is 1.8V



x-axis: temperature (℃) – y-axis: vref (V)

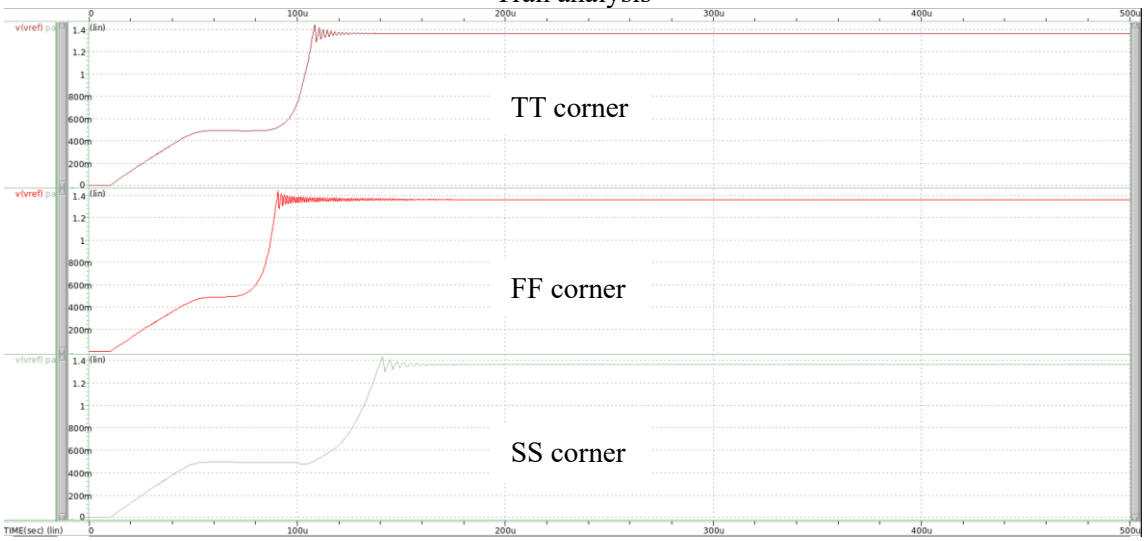
Sweep temperature from -40℃ to 125℃ when VDD is 1.62V



x-axis: temperature (℃) – y-axis: vref (V)

(b) .Tran

Tran analysis



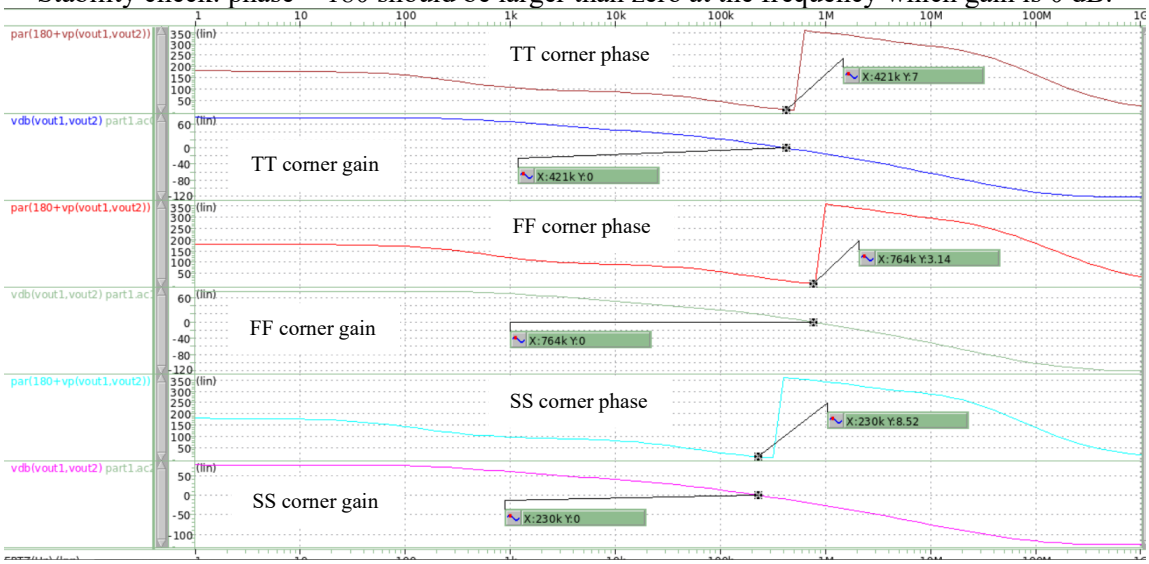
x-axis: time (μs) – y-axis: vref(v)

we can see V_{ref} has a sharp increase and finally become stable at about 1.3616V.

(c) .AC

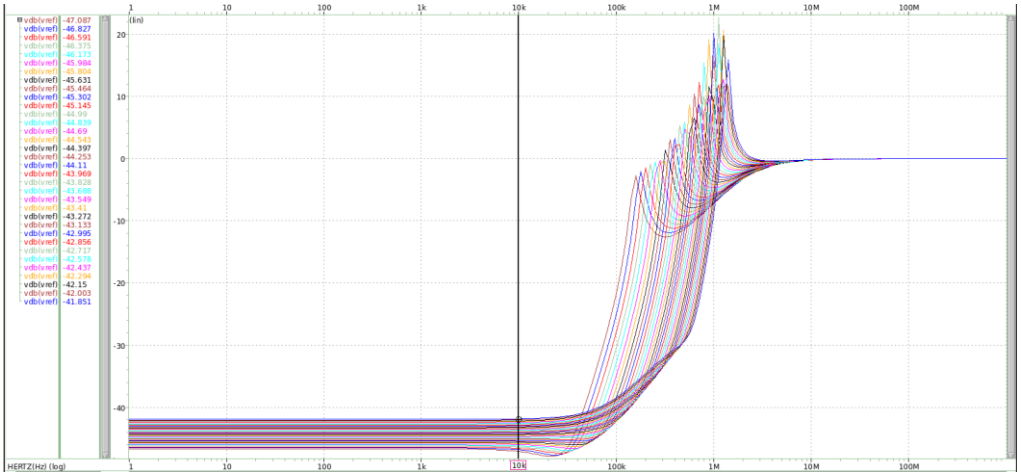
Check the stability of circuit by using the circuit below.

Stability check: phase + 180 should be larger than zero at the frequency which gain is 0 dB.



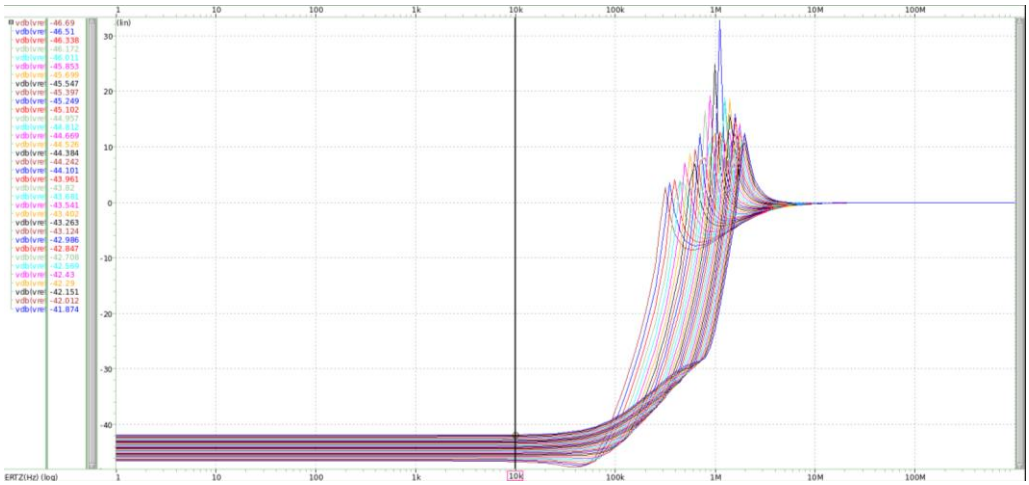
x-axis: frequency in log (Hz) – y-axis: phase (degree), gain (dB)

PSR in TT corner



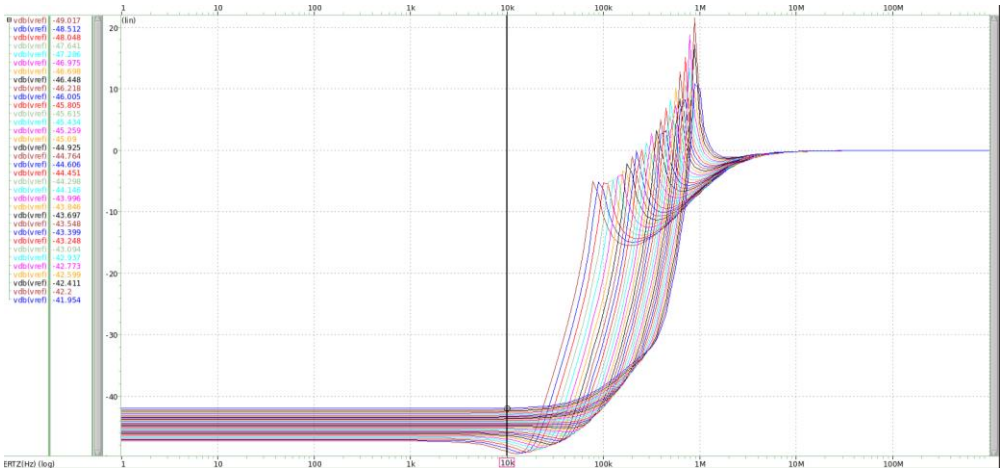
x-axis: frequency in log (Hz) – y-axis: gain of Vref in dB

PSR in FF corner



x-axis: frequency in log (Hz) – y-axis: gain of Vref in dB

PSR in SS corner

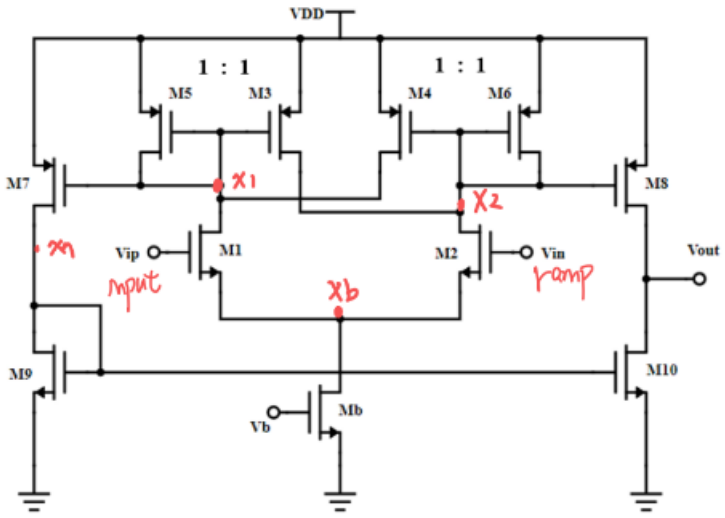


x-axis: frequency in log (Hz) – y-axis: gain of Vref in dB

Part II - Single Slope ADC (SSADC)

1. Design consideration

(a) Please observe the operation of the SSADC and discuss the operational requirements that the comparator must meet (e.g. setting time, input range)



Following the SPEC of BGR and SSADC, we can see that the input is about $0.95V_{ref}$ ~$0.25V_{ref}$ and the V_{ref} we generate in part1 is about 1.3606V, so the input range is about 0.34V ~ 1.3V. So, in the testbench, we should set ramp_max = 1.3 and ramp_min=0.35

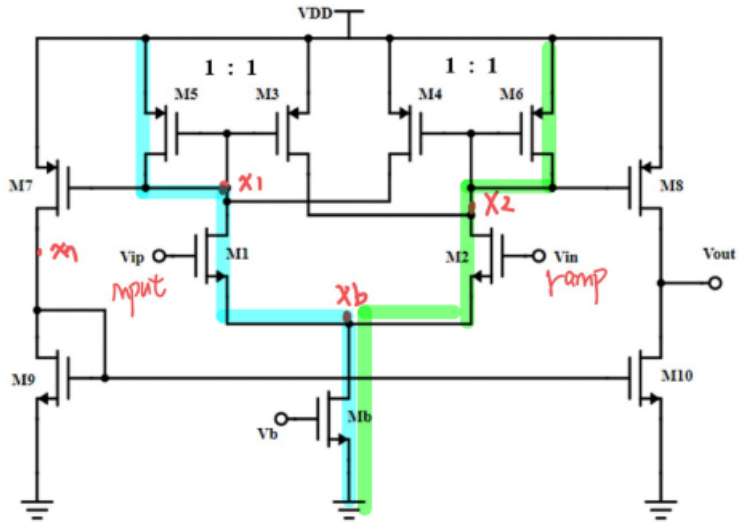
To meet the requirements of settling time of comparator, we need to shorten the output transition time, which should at least be smaller than clock time. And we can see the frequency of clock is 1.594MHz in testbench.

$$\therefore \text{clock period} = 627.4\text{ns}$$

So, we need to design a comparator with output rise time smaller than 627.4ns.

(b) Complete the design of the comparator (An OPAMP connected with an inverter chain) and describe your design in detail, including the schematic, operation point of all transistors (you should draw your schematic and mark the DC voltage and current on it), and how you run the simulations.

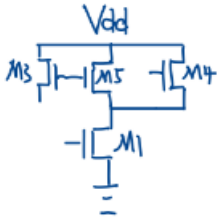
The comparator design above looks like a two-stage amplifier. We can design it like we design amplifier, but the input voltage to the comparator is DC. Let's first look at the two cases of input voltage.



- Vrampin > Vsample
  M2 flows more current than M1, which makes M3,5 turn off and M4,6 turn on. The V_{DS5} is close to zero, so the voltage at x1 is larger than x2. In the second stage, it amplifies the differential voltage at x1 and x2. Since x1 is larger than x2, Vout would be high and ID6 is approximately equal to tail current.
- Vrampin < Vsample
  M1 flows more current than M2, which makes M3,5 turn on and M4,6 turn off. And since the voltage across M3,5 will lower the voltage at x1, which makes Vx1<Vx2. So, in the second stage, it pulls Vout to negative rail potential which means pull to low and ID5 is approximately equal to tail current.

When sizing, I didn't use a 3:1 ratio in NMOS and PMOS. It is because when looking at NMOS transistor M1, its drain is connected to the drain M4 and M5 and M5 is connected to M3. That is, we can look at the PMOS side as 3 PMOS transistors in parallel. If mobility of NMOS is three times of PMOS than

$$3 * mobility\ of\ PMOS * width\ of\ PMOS = 1 * mobility\ of\ NMOS * width\ of\ NMOS$$



This means we can use the same width and length on NMOS and PMOS.

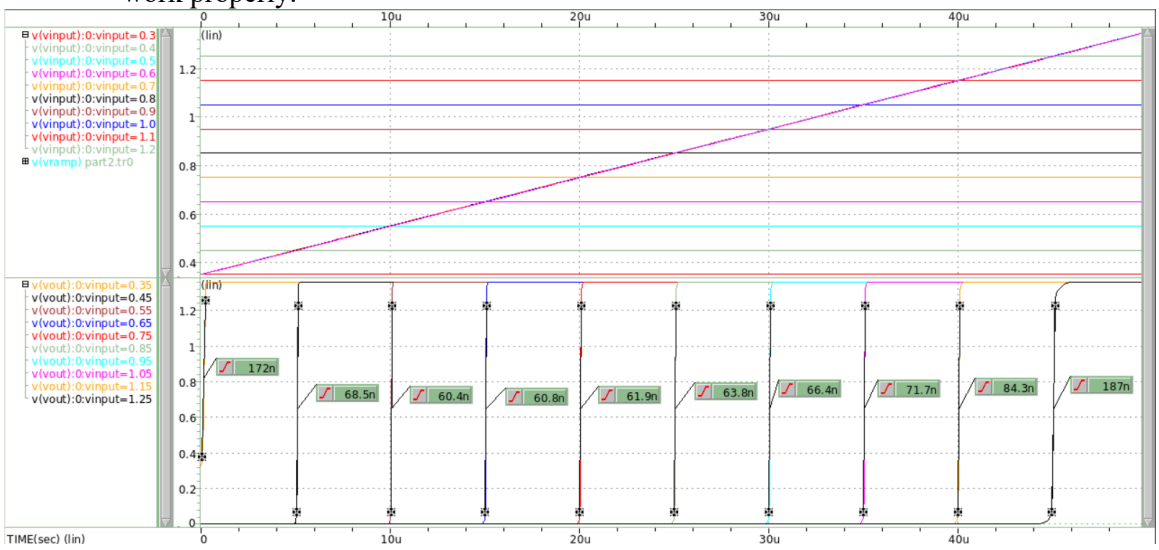
And since the current will be divided in two paths (M1 and M2), I designed the width of Mb two times of M1,2 at first. However, by the analysis above, we can see that no matter in which situation, there is only one path that will flow current, so I change Mb to the same size as M1,2.

In the analysis above, I decided the ratio of all transistors be the same. Then I adjust the length and width of all transistors together. To lower the rise time of the circuit the current variation should be large enough at second stage so the circuit be more sensitive such

that we can shorten the rise and fall time. And according to the equation of Id in saturation below:

$$I_D = \frac{1}{2} u_n C_{ox} \frac{W}{L} [(V_{GS} - V_{th})]^2 (1 \pm \lambda V_{DS})$$

We can increase current by increasing the ratio of W and L, however when L is smaller and W is larger, Vth would be too large, so Id might decrease, so we should also increase the length. Knowing Vb is 0.5 in testbench, I finally adjust the size equal 0.6um/0.6um so Mb will in saturation region and provide enough current, and other transistors will work properly.

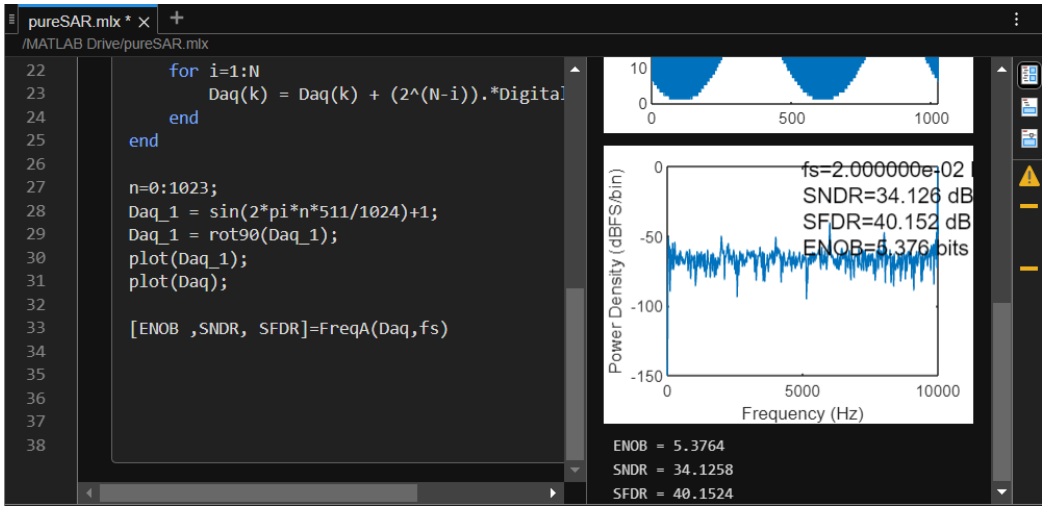


Rise time of different input(0.35V~1.3V): x-axis: time(sec) – y-axis: voltage(V)

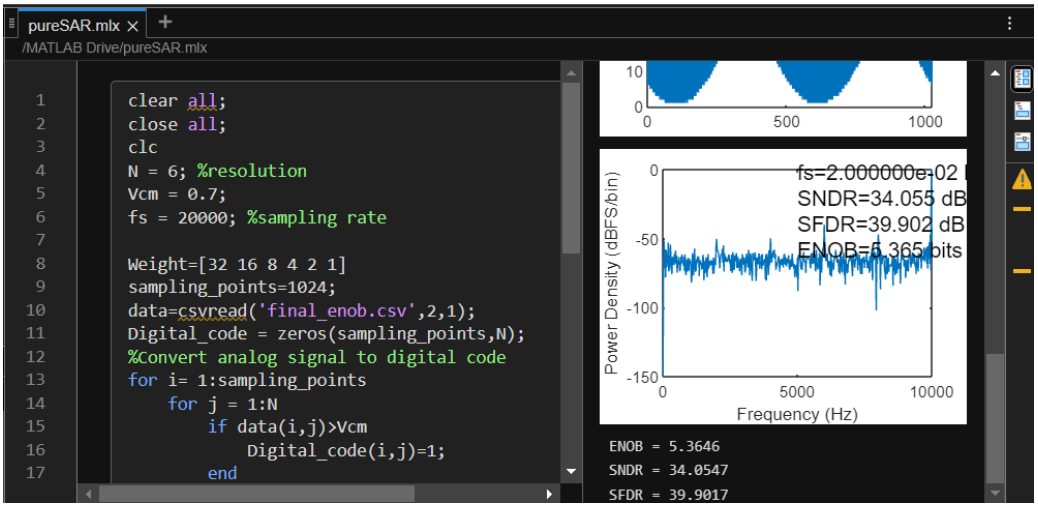
Size of Comparator			
M1	0.6um/0.6um	M2	0.6um/0.6um
M3	0.6um/0.6um	M4	0.6um/0.6um
M5	0.6um/0.6um	M6	0.6um/0.6um
M7	0.6um/0.6um	M8	0.6um/0.6um
M9	0.6um/0.6um	M10	0.6um/0.6um
Mb	0.6um/0.6um	-	-

2. SPICE code submission

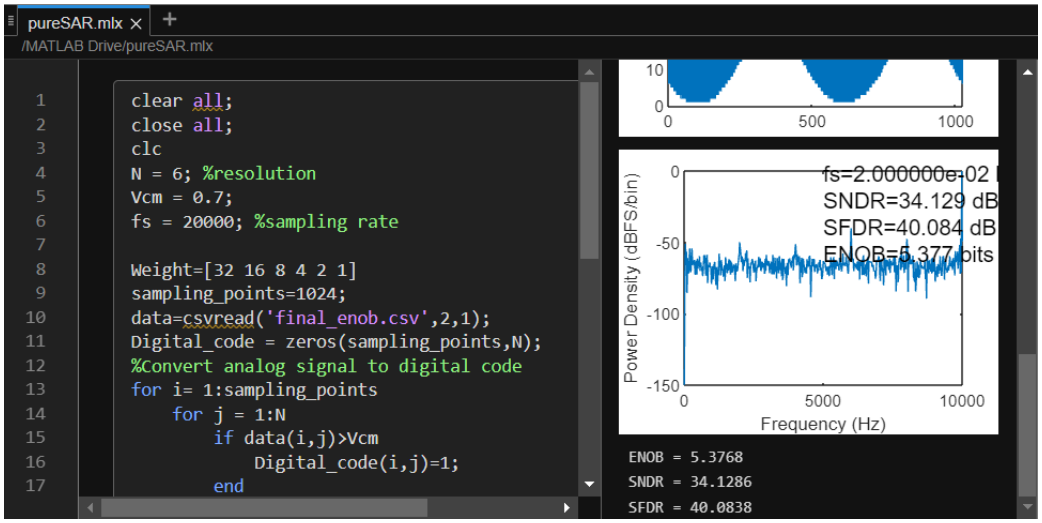
3. Measure the ENOB



VDD = 1.8V



VDD = 1.62V



VDD = 1.92V

We can see the results are very close to each other. I think it is because our output voltage Vref of BGR is almost the same in different condition.

Part III – Experience Sharing

I think the final project is quite interesting. In this project, we can know how our circuit can be used in application, not only be used as an amplifier. But in this course, we only use Hspice run simulation, so it is possible that our design may not work.

There are a few suggestions I would like to make to this course. First, I think we should learn more about how to design circuits in the course, not just learning how to analysis. It is wonderful that Professor Tang introduced many kinds of circuits in class and analysis them in detail. However, when designing the circuit in homework, I still usually don't know how to begin my design. Second, I think TA should tell us what they want to see in the report before we submit homework. Sometimes, I only write down what the assignment required in the report, but TA still takes out my points because I didn't write them in detail or just what I wrote is not what TA wants to see. I think the question in the homework can be more concrete like what detail should I provide in the report.

Having said that, it is still a very good course and I want to thank Professor Tang and all TAs for this semester's AIC course and have a happy winter break.