EE3235 Analog Integrated Circuit Analysis and Design I

Homework 4
Ideal OP circuit
Due date: 2023.11.29 (Wed.) 13:20 (upload to eeclass system)

Suppose V_{DD}=1.8V, temperature=25°C, TT corner in this homework.

Please note that:

> 1. **No delay allowed**.
> 2. Please hand in your report using eeclass system.
> 3. Please generate your report with **pdf** format, name your report as
> HWX_studentID_name.pdf.
> 4. Please hand in the spice code file (.sp) for each work. Do not include output file.
> 5. Please print waveform with white background, and make sure the X, and Y
> labels are clear.
> 6. Please do not zip your report.

In this homework, you have to build an ideal op model(with finite gain=60dB) by SPICE and use this model to construct the following four circuits, including: **Unity-Gain Amplifier, Noninverting Amplifier, Inverting Amplifier, Voltage Adder and Integrator**
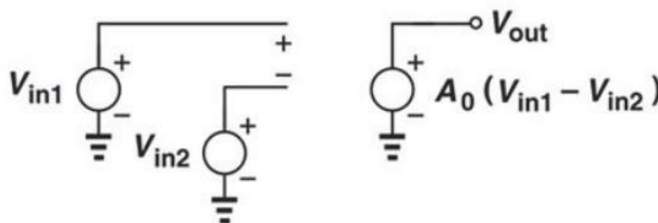

Fig. 1. Ideal op model

You have to build an ideal op model as show in Fig. 1. and **let A₀ = 60dB** (Hint：use E element to build an ideal model). **In the question below, all parts that need to be calculated must consider op as finite gain**, otherwise no points will be given.

Please submit a sp file for each part, a total of 4 sp files, named as: UGA.sp, NIA.sp, IA.sp, and VAI.sp. If you don't submit the assignments in accordance with the above regulations, no points will be given.
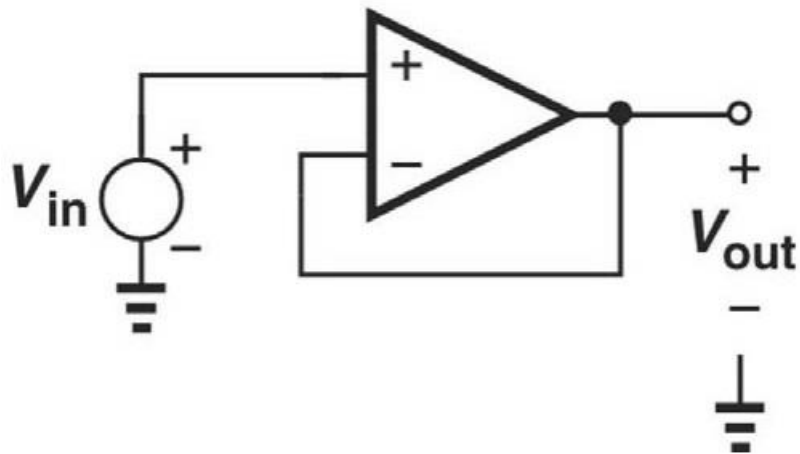
1. **Unity-gain Amplifier**

Fig. 2. Unity-gain amplifier

Use your ideal op model to construct an unity gain amplifier as shown in Fig. 2.

(a) DC Sweep

Please probe V_{out} v.s. V_{in} (sweep V_{in} from $0V \sim 5V$) and measure the derivative of V_{out} when V_{in} is 2.5V.

(b) TF Analysis

Please run the .TF command in HSPICE to measure the I/O impedance and DC gain A_v. Calculate the **DC gain** and compare it to the simulation result.
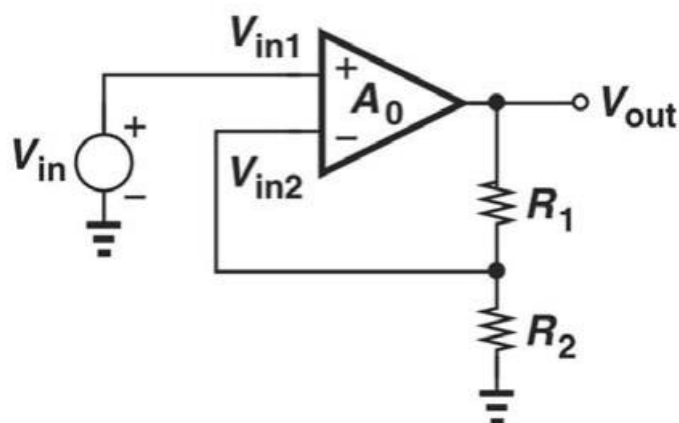
2. **Noninverting Amplifier**

Fig. 3. Noninverting Amplifier

Use your ideal op model to design an Noninverting Amplifier as shown in Fig. 3. **With closed-loop gain = 30 (error < 1%).**

(a) DC Sweep

Please probe V_{out} v.s. V_{in} (sweep V_{in} from 0V~5V) and measure the derivative of V_{out} when V_{in} is 2.5V.

(b) TF Analysis

Please run the .TF command in HSPICE to measure the I/O impedance and DC gain A_v. Calculate the **DC gain** and compare it to the simulation result.

(c) How do you design your circuit to meet the SPEC? Describe your design considerations.
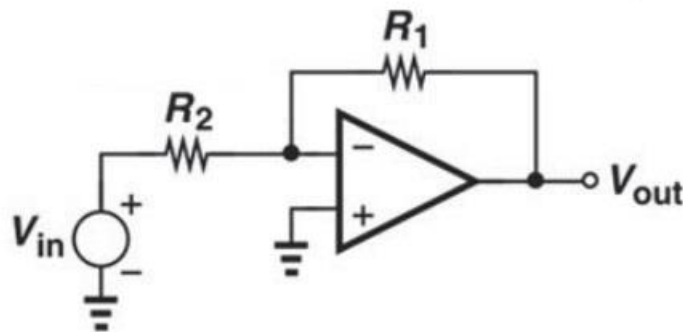
3. **Inverting Amplifier**

Fig. 4. inverting Amplifier

Use your ideal op model to design an inverting Amplifier as shown in Fig. 4. **With closed-loop gain = 30 (error < 1%).**

(a) DC Sweep

Please probe V_{out} v.s. V_{in} (sweep V_{in} from 0V~5V) and measure the derivative of V_{out} when V_{in} is 2.5V.

(b) TF Analysis

Please run the .TF command in HSPICE to measure the I/O impedance and DC gain A_v. Calculate the **DC gain** and compare it to the simulation result.

(c) How do you design your circuit to meet the SPEC? Describe your design considerations.
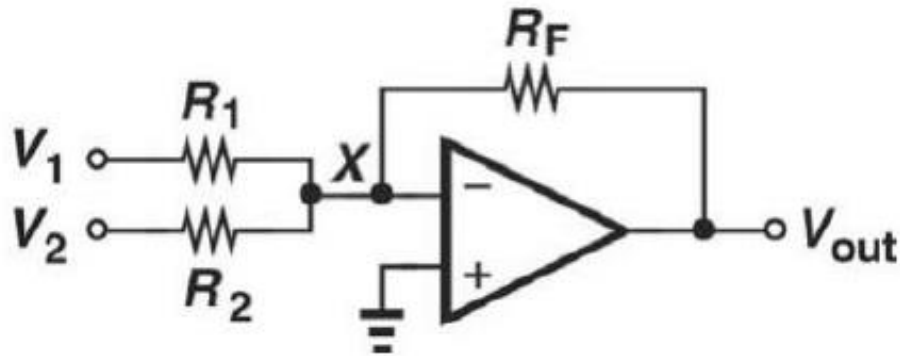
4. Voltage Adder + Integrator
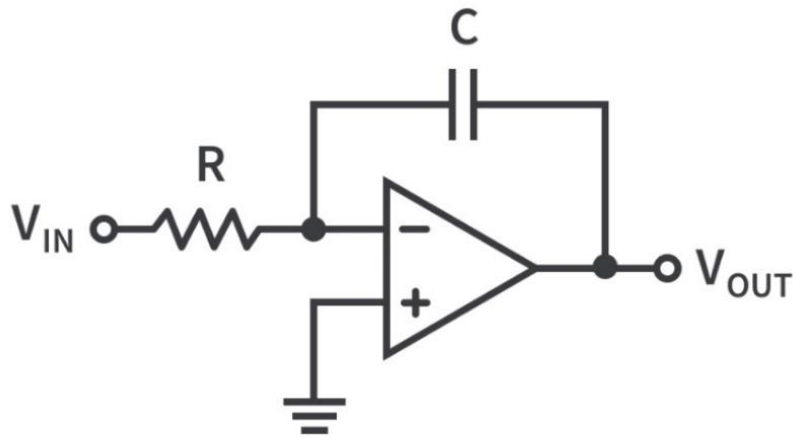

Fig. 5. Voltage Adder Circuit

Fig. 6. Integrator

The voltage adder is shown in Fig. 5 and the integrator is shown in Fig.6. Use only your ideal op model, 2 integrators, and 1 voltage adder to design a circuit satisfied the following equation.

$$V_y(t) = \int \left(\int -600V_x(t) - 1200V_y(t)dt \right) dt$$

(a) Describe your design consideration and show the schemetic.

(b) Suppose all initial conditions are 0 and $V_x(t)$ is an unit step input. Please do hand calculation to find the transient response of $V_y(t)$ and the period of the waveform at $V_y(t)$.

(c) Let $V_x(t)$ be an unit step input. Plot the transient response of $V_y(t)$ and measure the period of $V_y(t)$. The output waveform should looks like Fig. 7.

The unit step input **has to** be generated using the following instruction and the transient response time **has to** be larger than 6(s).

<div align="center">Vin   Vx   GND   PULSE   0   1   5   1n   1n   10</div>

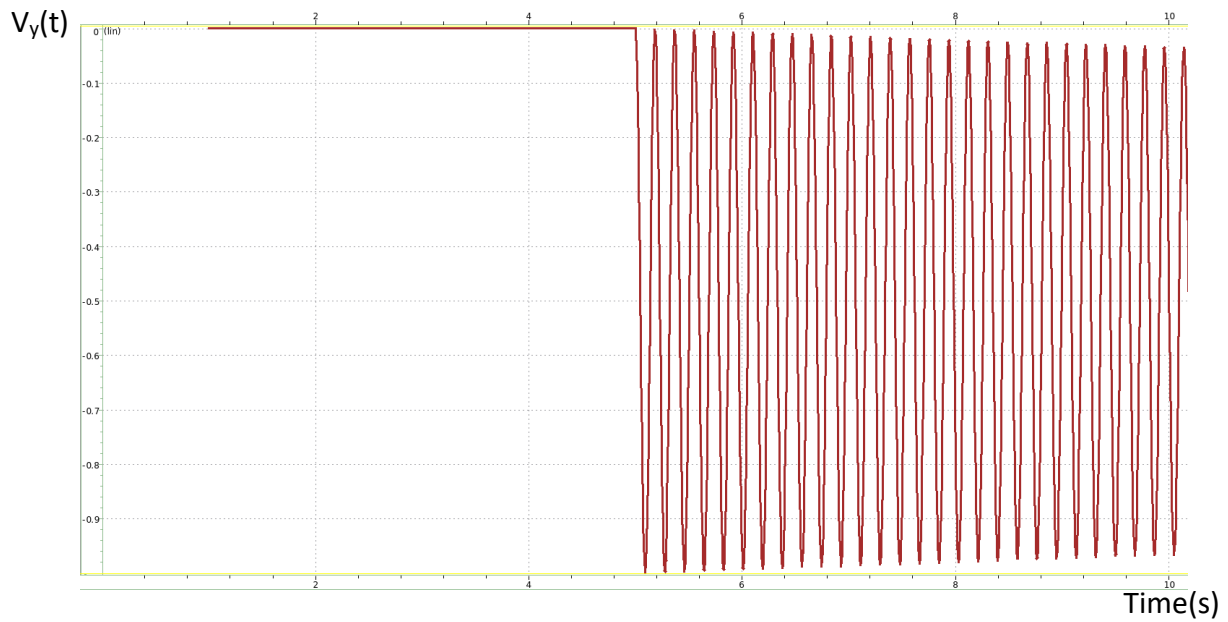(d) What is the error between calculated waveform period and the simulation waveform period?

Fig. 7. $V_y(t)$ waveform in 4.(b)