EE3225 Analog Integrated Circuit Analysis and Design HW3

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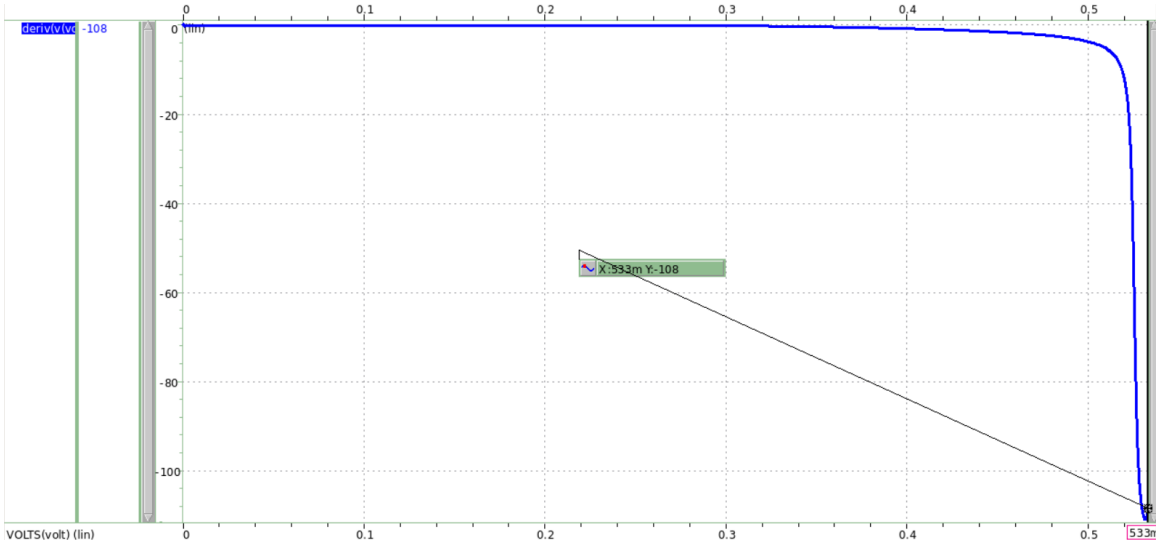
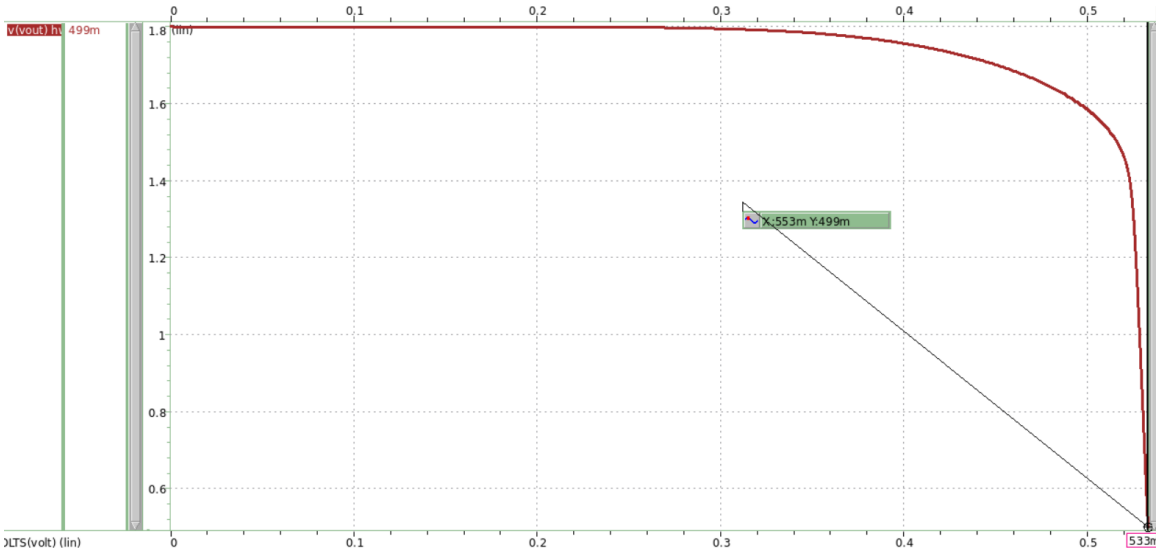
Part I-Cascade Amplifier

(a)



X axis: Vin(V) – Y axis: Gain(V/V)



X axis: Vin(V) – Y axis: Vout(V)

```
** 110061217 王彥智 hw3_a

****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:vbl     = 900.0000m 0:vdd     =   1.8000  0:vin     = 533.0000m
+0:vout    = 499.4235m


**** voltage sources

subckt
element  0:vin      0:vbl      0:vdd
 volts    533.0000m  900.0000m    1.8000
 current    0.         0.        -5.1118u
 power      0.         0.         9.2012u

    total voltage source power dissipation=    9.2012u       watts
```

Operating point and voltage source

- Vout = 0.499V(0.5V ± 10mv)
- $|A_1|$ = 108V/V(>100V/V)
- Vin = 0.533V
- Vb1 = 0.9V
- $(\frac{W}{L})_{NMOS} = (\frac{W}{L})_{PMOS} = \frac{3um}{3um}$

How I design:

- Step1: designable parameters: Vin, Vb1, (W/L) of NMOS and PMOS
- Step2: gain should larger than 100:

$$|A_1| = g_{mnmos}(r_{onmos}||r_{opmos}) \approx g_{mnmos}r_{opmos}$$

$$= \frac{2I_D}{V_{in} - V_{th}} * \frac{1}{\lambda_{pmos}I_D} = \frac{2}{(V_{in} - V_{th})\lambda_{pmos}} > 100V/V$$

  To increase gain, we should

  1. Decrease Vin, and PMOS and NMOS should stay in saturation region (maintain I_d), so when decreasing Vin, we should also increase W/L of NMOS and PMOS. Also, we should consider if Vin is larger than Vth or not.
  2. Decrease λ_{pmos} by increasing L of PMOS.
- Step3: from step2, to have a large gain, I design Vin ≅ 0.55, which is a little bit larger than Vth in this process. Also, from step2, W/L of NMOS and PMOS should be large enough and L also should be large enough to have a larger gain, so I design W/L = 3um/3um.

- Step4: Do .dc analysis to find Vb1 which make Vout = 0.5V. If there is no Vb1 that satisfy the condition, adjust Vin and do .dc analysis again. Finally, Vin = 0.533 and Vb1 = 0.9.
- Step5: check the result. Use .dc to check that gain is larger than 100. Use .op to check Vout = 0.5V and both NMOS and PMOS are in saturation region.

(b)

```
**** mosfets


subckt
element  0:mp       0:mn
model    0:p_18.1   0:n_18.1
region   Saturation Saturation
 id        -5.1118u    5.1118u
 ibs      6.208e-22 -1.008e-21
 ibd      227.8188a -142.0151a
 vgs     -900.0000m  533.0000m
 vds       -1.3006   499.4235m
 vbs         0.          0.
 vth     -476.2435m  340.8760m
 vdsat   -368.6683m  173.2277m
 vod     -423.7565m  192.1240m
 beta      64.6455u  302.0019u
 gam eff  557.0846m  507.4460m
 gm        21.8546u   47.1123u
 gds       52.5553n  392.3847n
 gmb        7.1252u    9.2323u
 cdtot      3.2640f    4.3769f
 cgtot     57.5294f   59.9554f
 cstot     65.6636f   63.1053f
 cbtot     23.4601f   21.7777f
 cgs       52.6225f   54.1463f
 cgd        1.0851f    1.0554f
```

```
****     small-signal transfer characteristics

     v(vout)/vin                               = -105.8835
     input resistance at            vin        =  1.000e+20
     output resistance at v(vout)              =    2.2476x
```

Gain and small signal parameters

Hand calculation: I connect gate of NMOS to ground and gate of PMOS to 1.8V, so we don't need to consider body effect.

$$|A_1| = g_{mnmos}(r_{onmos}||r_{opmos}) = g_{mnmos}(\frac{1}{g_{dsnmos}}||\frac{1}{g_{dspmos}})$$

$$= \frac{g_{mnmos}}{g_{dsnmos} + g_{dspmos}} = \frac{47.1123u}{392.3847n + 52.5553n} = 105.8851$$

Check NMOS in saturation:

$$V_{gs} = 533mV > V_{th} = 340.8760mV$$

$$V_{gs} - V_{ds} = 533mV - 392.3847mV = 140.6153mV < V_{th} = 340.8760mV$$

Check PMOS in saturation:

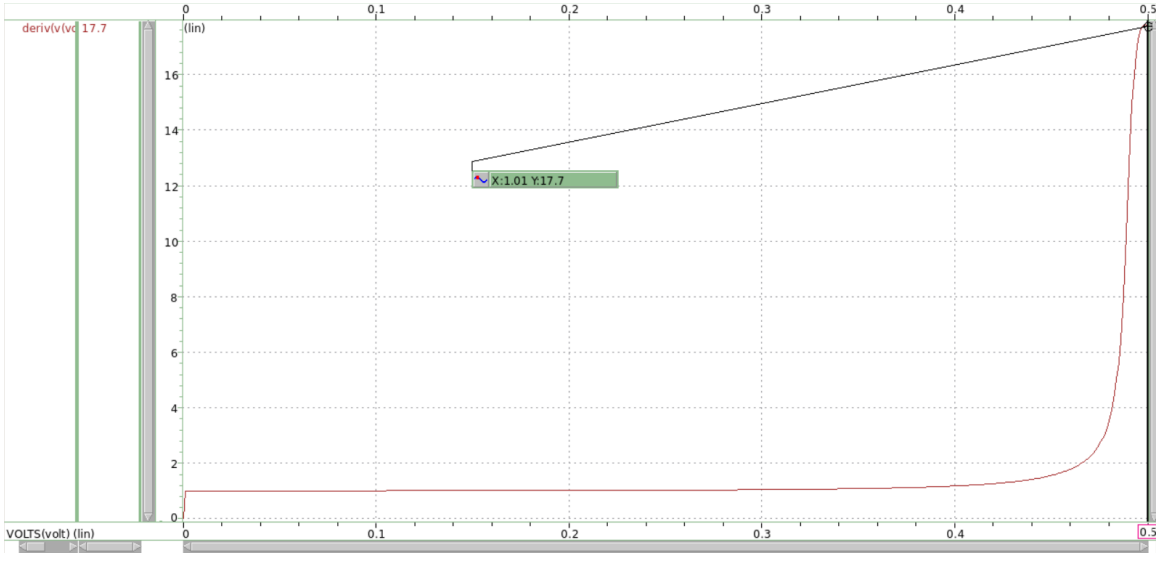
$$|V_{gs}| = 900mV > |V_{th}| = 476.2435mV$$

$$|V_{gs} - V_{ds}| = 900mV - 1300.6mV = -400.6mV < V_{th} = 476.2435mV$$

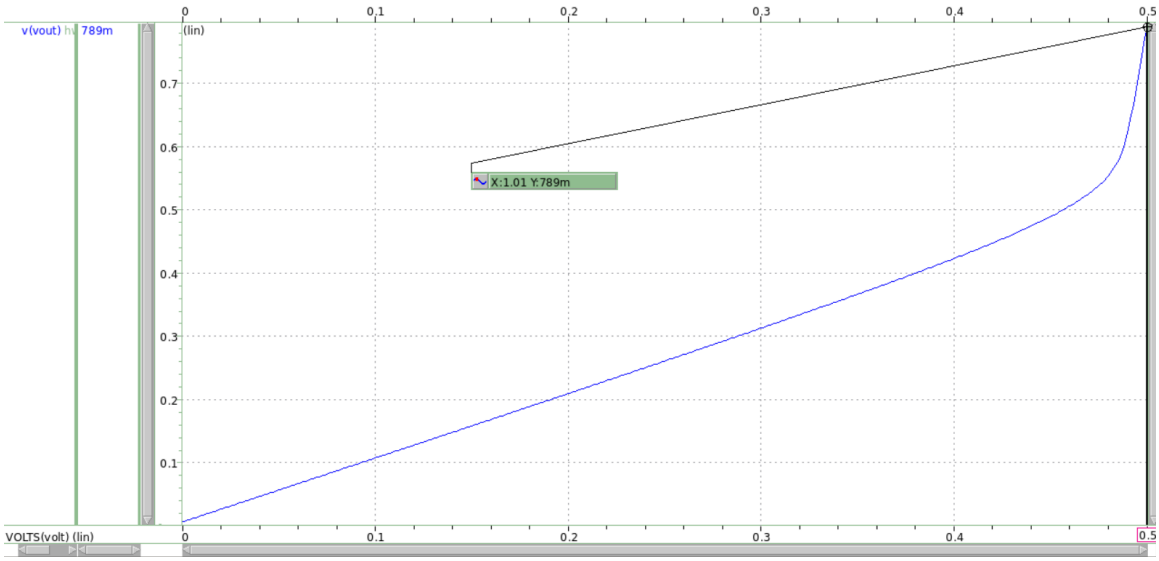
Error:

$$\frac{105.8835 - 105.8851}{105.8851} = -1.5 * 10^{-3}\%$$

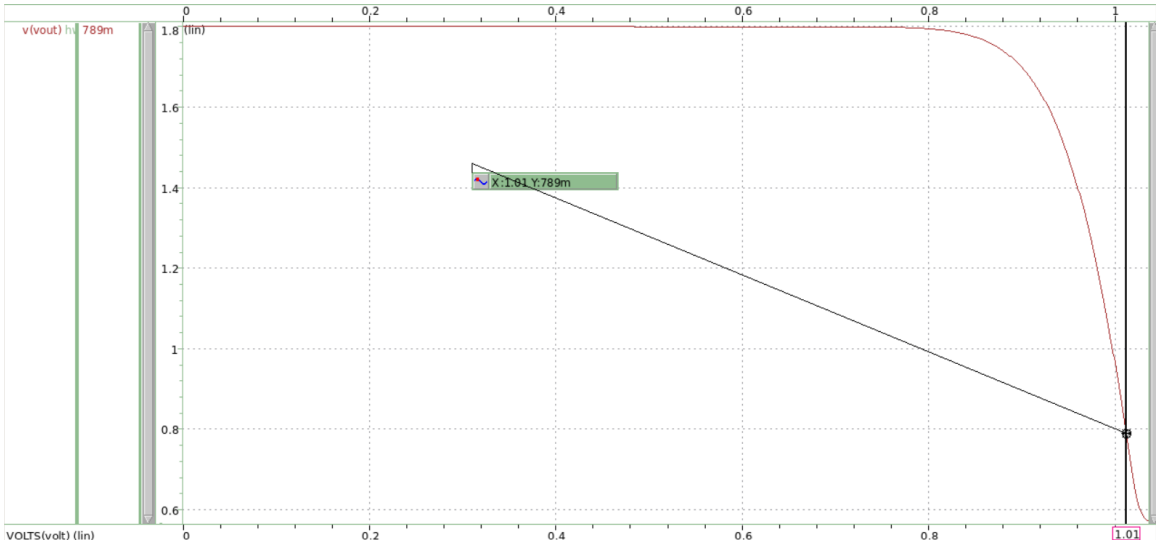
(c)



X axis: Vin(V) – Y axis: gain(V/V)



X axis: Vin(V) – Y axis: Vout(V/V)



X axis: Vb2(V) – Y axis: Vout(V)

```
** 110061217 王彥智 hw3_b

****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:vb2     =   1.0120  0:vdd     =   1.8000  0:vin     = 500.0000m
+0:vout    = 788.7143m


**** voltage sources

subckt
element  0:vin      0:vb2      0:vdd
 volts    500.0000m    1.0120     1.8000
 current   10.1129u    0.       -10.1129u
 power     -5.0564u    0.        18.2031u

    total voltage source power dissipation=   13.1467u       watts
```

Operating point and voltage source

- I_D = 10.1129μA(error: $\frac{10.1129-10}{10}10$ = 1.11% < 5%)
- $|A_2|$ = 17.7 V/V(>15V/V)
- Vin = 0.5V
- Vb2 = 1.012V
- Vout = 0.788V
- $(\frac{W}{L})_{NMOS} = \frac{15um}{1um}$

How I design:

- Step1: designable parameters: Vb2, (W/L) of NMOS
- Step2: gain should larger than 15:

$$|A_2| = g_m(r_{onmos}||R_D \approx g_m R_D = \frac{2I_D}{V_{gs}-V_{th}} * R_D = \frac{2}{(V_{b2}- V_{in} - V_{th})} > 15V/V$$

  To increase gain, we should

  1. Decrease Vb2, but NMOS should stay in saturation region, so when decreasing Vb2, we should also increase W/L of NMOS to maintain I_d.
  2. Decrease V_{th} by increasing L of NMOS, but it's not the main factor of the gain.
- Step3: from step2, to have a large gain, I design Vb2 ≅ 1.05, which is a little bit larger than (Vth + Vin = 0.55 + 0.5). Also, W/L of NMOS should be large enough to maintain I_d, so I design W/L = 15um/1um.

- Step4: Do .dc analysis to find Vb2 which make Vout = 0.8V($I_d = \frac{V_{dd}-V_{out}}{R_D} = \frac{1.8-V_{out}}{100k\Omega} = 10uA \rightarrow Vout = 0.8V$). Finally, Vb2 = 1.012V. If there is not Vb2 that satisfy the condition, change W/L and do .dc analysis Vb2 again.
- Step5: check the result. Use .dc to check that gain is larger than 15. Use .op to check $I_d = 10uA$ and NMOS is in saturation region.

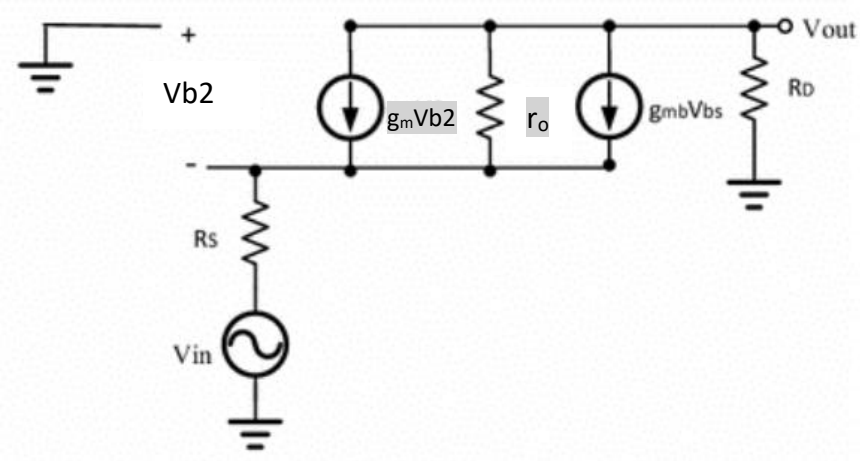
(d)

```
**** mosfets


subckt
element  0:mn
model    0:n_18.1
region   Saturation
 id        10.1129u
 ibs     -565.3016a
 ibd     -891.7188a
 vgs      512.0000m
 vds      288.7143m
 vbs     -500.0000m
 vth      479.9309m
 vdsat     81.5058m
 vod       32.0691m
 beta       4.7083m
 gam eff  519.9006m
 gm       196.1642u
 gds        2.9998u
 gmb       31.1424u
 cdtot     19.7335f
 cgtot     85.8967f
 cstot     89.4453f
 cbtot     48.2201f
 cgs       70.5705f
 cgd        5.3514f
```

```
****     small-signal transfer characteristics

    v(vout)/vin                               =   17.7157
    input resistance at            vin        =    5.6447k
    output resistance at v(vout)              =   76.9247k
```

Gain and small signal parameters

Hand calculation: since I connected the body to ground, so I should consider body effect. Considering the following small signal model.



* there is no Rs in our circuit

By KCL at node of Vout: -(gm+gmb)Vin + (Vout-Vin)/r_o +Vout/R_D = 0

So

$$|A_2| = \frac{V_{out}}{V_{in}} = \frac{g_m + g_{mb} + \frac{1}{r_o}}{\frac{1}{r_o} + \frac{1}{R_D}} = \frac{196.1642u + 31.1424u + 2.9998u}{2.9998u + 1/100k} = 17.7160V/V$$

Check NMOS in saturation region:

$$V_{gs} = 512mV > V_{th} = 479.9309mV$$

$$V_{gs} - V_{ds} = 512mV - 223.2857mV = 140.6153mV < V_{th} = 479.9309mV$$

Error:

$$\frac{17.7157 - 17.7160}{17.7160} = -1.69 * 10^{-3}\%$$

(e)

i. yes.

- Vx = 0.500635 ≅0.5V
- Vout of (a) = 0.4994235≅0.5V
- Vin of (b) = 0.5

$$\text{Error: } \frac{0.500635 - 0.4994235}{0.4994235} = 0.24\%$$

```
** 110061217 王彥智 hw3_c

****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:vb1     = 900.0000m 0:vb2     =   1.0120  0:vdd     =   1.8000
+0:vin     = 533.0000m 0:vout    = 799.9460m 0:vx      = 500.6350m
```

Operating point

ii. No, overall gain doesn't equal A_1 * A_2.

```
****     small-signal transfer characteristics

     v(vout)/vin                               =   -4.6995
     input resistance at            vin        =  1.000e+20
     output resistance at v(vout)              =   99.9431k
```

Overall gain

- $|A1 * A2| = 105.8835 * 17.7157 = 1875.8003$V/V
- $|A_{cascade}| = 4.6995$V/V

Why not equal: we neglect the input impedance and output impedance. That is, input impedance is not zero and output impedance is not infinite in this case.

Output impedance of common source amplifier (without considering body effect):

$$R_{out} = r_{onmos} \,||r_{opmos} = \frac{1}{g_{dsnmos} + g_{dspmos}} = \frac{1}{392.3847n + 52.5553n} = 2.2475 * 10\text{^}6\Omega$$

Input impedance of common gate amplifier(considering body effect):

$$R_{in} = \frac{R_D + \frac{1}{g_{ds}}}{\frac{gm + gmb}{gds} + 1}$$

$$= (100k + \frac{1}{2.9998u})/(\frac{196.1642u + 31.1424u}{2.9998u} + 1) = 5645.667\Omega$$

So, the overall gain should equal:

$$|A_{cascade}| = |A1 * A2| * \frac{R_{in}}{R_{in} + R_{out}}$$

$$= 1875.8003 * \frac{5645.667\Omega}{5645.667\Omega + 2247500\Omega} = 4.7001V/V$$

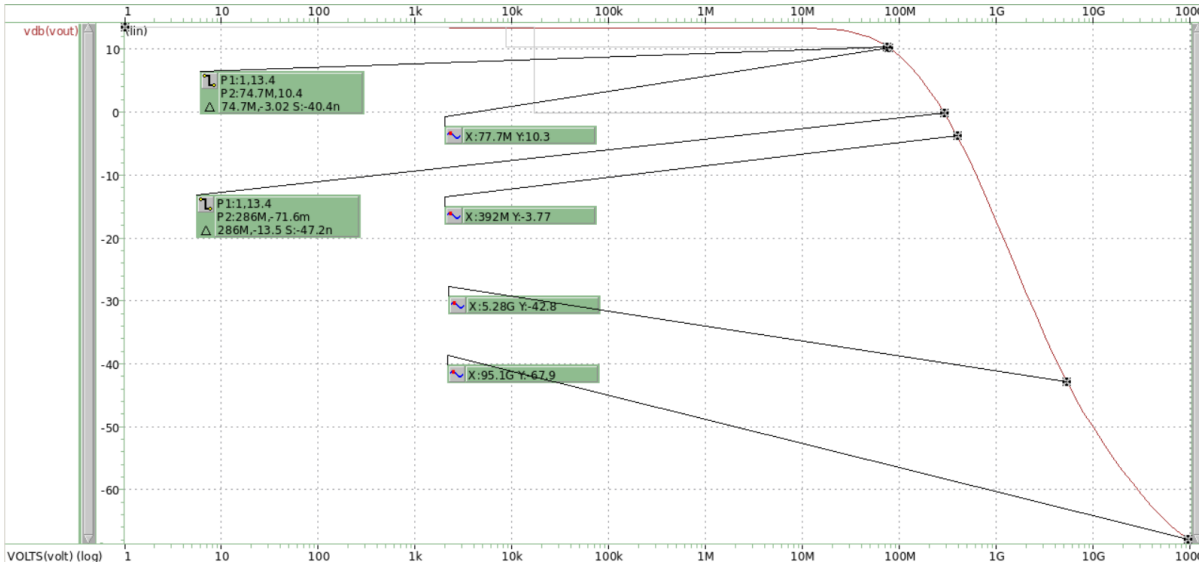
Error:

$$\frac{4.6995 - 4.7001}{4.7001} = 0.031\%$$

(f)

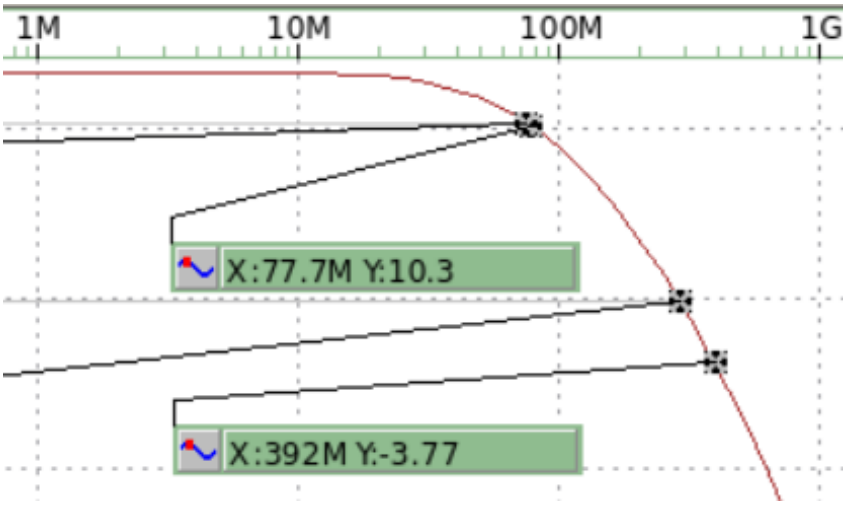
```
******   pole/zero analysis


   input =  0:vin          output = v(vout)

      poles (rad/sec)                poles ( hertz)
real            imag            real            imag
-488.343x       0.              -77.7222x       0.
-2.46198g       0.              -391.837x       0.

      zeros (rad/sec)                zeros ( hertz)
real            imag            real            imag
33.2042g        0.              5.28462g        0.
597.299g        0.              95.0631g        0.

 ***** constant factor = 284.892u
******
** 110061217 王彥智 hw3_c

****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgain_in_db=  13.4411     at=   1.5849
            from=   1.0000     to= 100.0000g
bw=  74.7237x
ugb= 286.3280x
```

Pole/zero analysis and ac analysis



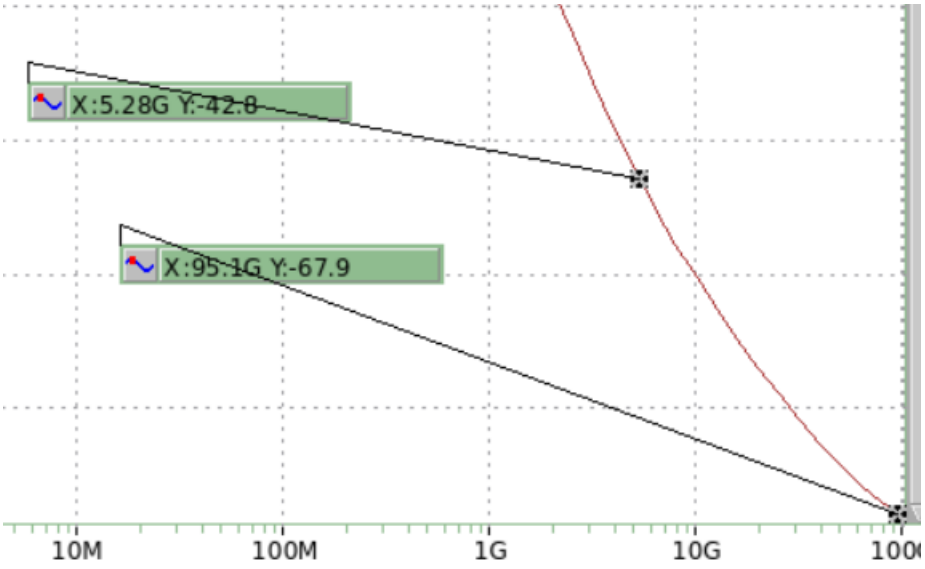
Frequency response of cascade amplifier

X axis: frequency(Hz) – Y axis: Vout(Vdb)



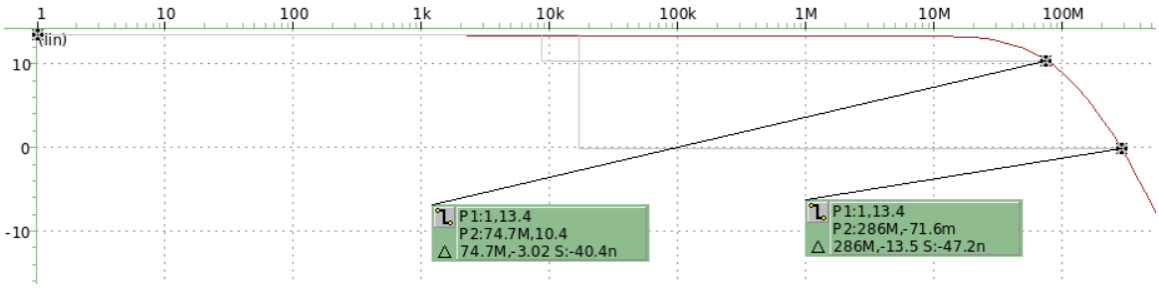
1st Pole: 77.7M; 2nd pole: 392M

X axis: frequency(Hz) – Y axis: Vout(Vdb)



1st Zero: 2.28G; 2nd zero: 95.1G

X axis: frequency(Hz) – Y axis: Vout(Vdb)



Unit-gain bandwidth: 392M; -3db bandwidth: 74.7M

X axis: frequency(Hz) – Y axis: Vout(Vdb)

(g)

Hand calculations:

```
****     small-signal transfer characteristics

v(vout)/vin                              =   -4.6995
input resistance at            vin       =  1.000e+20
output resistance at v(vout)             =   99.9431k
```

Output resistance (Rout)

```
   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:vb1     =  57.5295f 0:vb2     =  85.5747f 0:vdd     =  89.1242f
+0:vin     =  59.9547f 0:vout    =  19.6828f 0:vx      =  96.7049f
```

Capacitance table: we can find Cout here

So, the dominant pole is:

$$\frac{1}{2\pi * R_{out} * C_{out}} = \frac{1}{2\pi * 99943.1\Omega * 19.6828fF} = 80.9469MHz$$

The definition of dominant pole is the pole with lowest frequency, so the dominant pole we measured is 77.7222MHz.

$$\text{Error:}\frac{77.7222-80.9469}{80.9469} = -3.983\%$$

Error is a little bit large, but acceptable. I think it is because we only consider the node of output, not every node of the circuit.

(h)

Table I Performance Table

Work item	Unit	Specification	Simulation	Calculation
Vdd	V	1.8		
Common Source Amplifier				
Vin	V	-	0.533	
Vb1	V	-	0.9	
Vo	V	0.5	0.4994235	
Gain($\lvert A_1 \rvert$)	V/V	>100	105.8835	105.8851
Common Gate Amplifier				
Vin	V	0.5	0.5	
Vo	V	-	0.7887143	
I	μA	10	10.1129	
Gain($\lvert A_2 \rvert$)	V/V	>15	17.7157	17.7160
Cascade Amplifier				
Vin	V	-	0.533	
Vx	V	0.5	0.500635	
Vo	V	-	0.7999460	
Gain($\lvert A_1 * A_2 \rvert$)	V/V	>1	4.6995	4.7001
Dominate Pole	MHz	>40	77.7222	80.9469
Unit Gain Bandwidth	MHz	>70	286.3280	