# EE3235 Analog Integrated Circuit Analysis and design I

## Homework 4

## Ideal OP circuit

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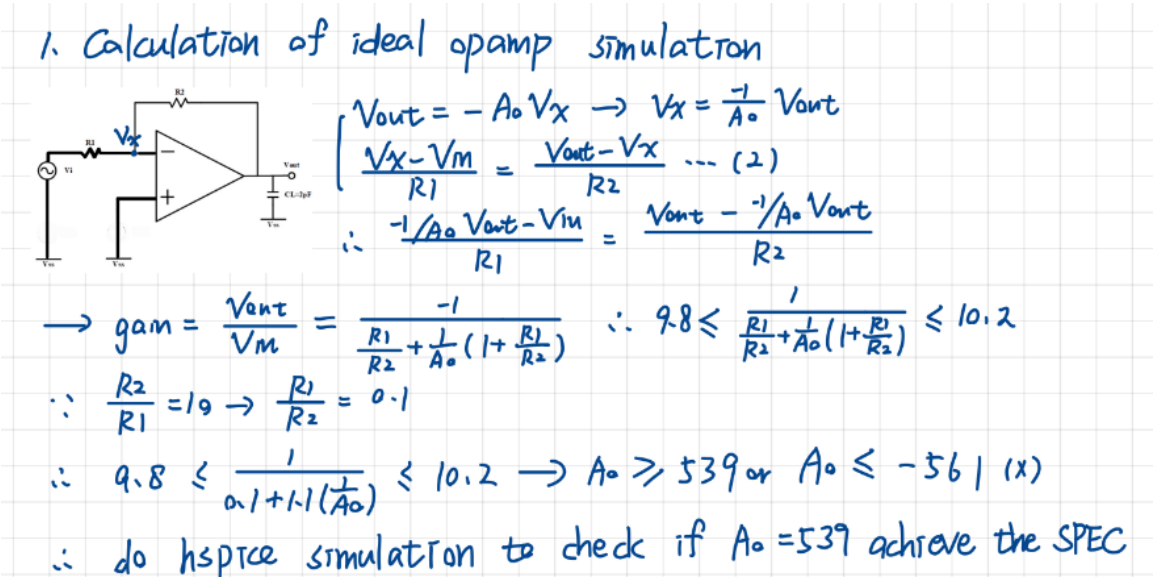
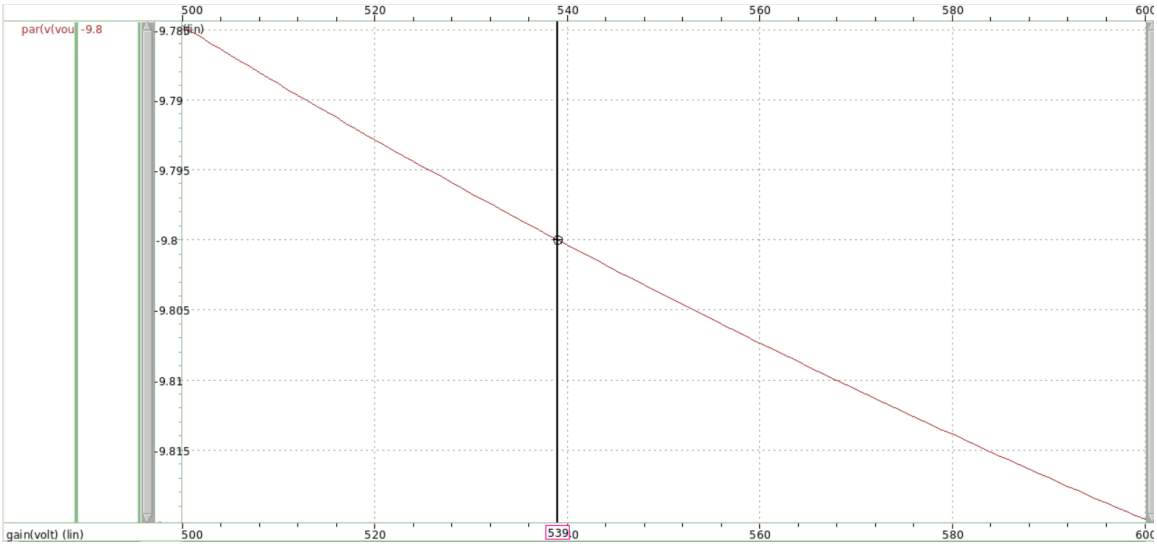
PART1：Design the amplifier in Fig. 2

1. Ideal operational amplifier simulation



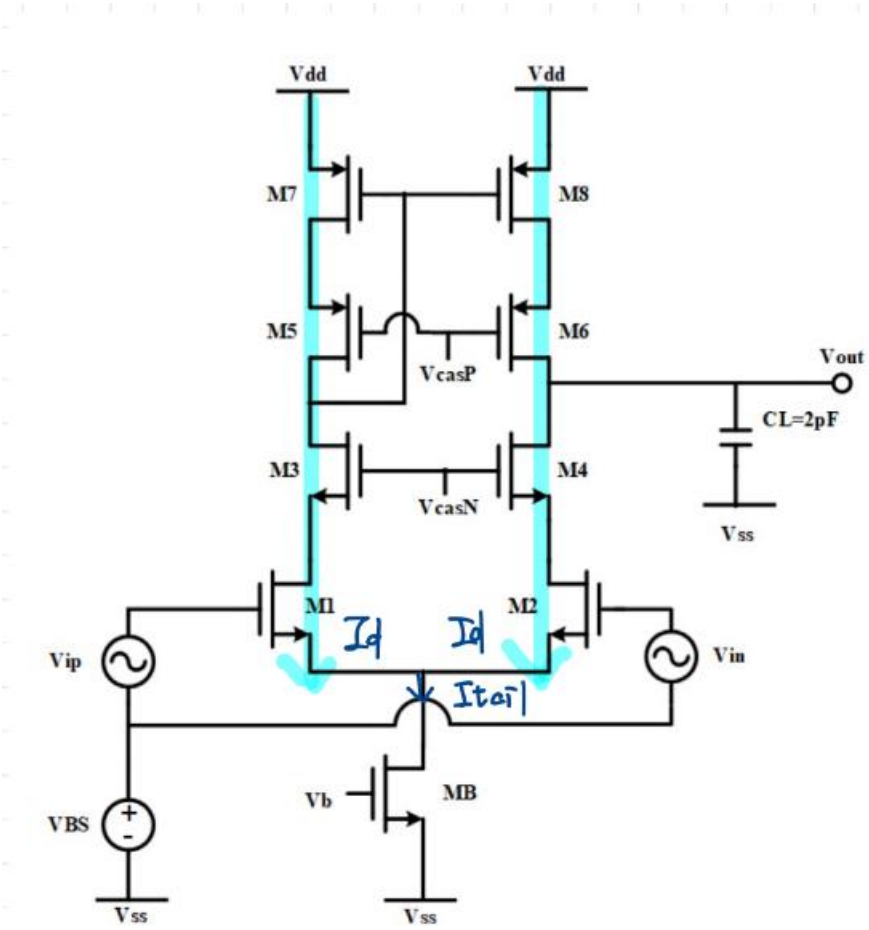

Hand calculation.

To verify the results, I run Hspice with an ideal amplifier(E) and two resister (R1=1kΩ, R2=10kΩ) and sweep the gain of ideal amplifier from 500 to 600 to see when close loop gain equals 9.8(v/v).




X axis: open loop gain(V/V)-Y axis: closed loop gain(V/V)

2. Circuit Design




Step1. Check out the speculation and circuit architecture.

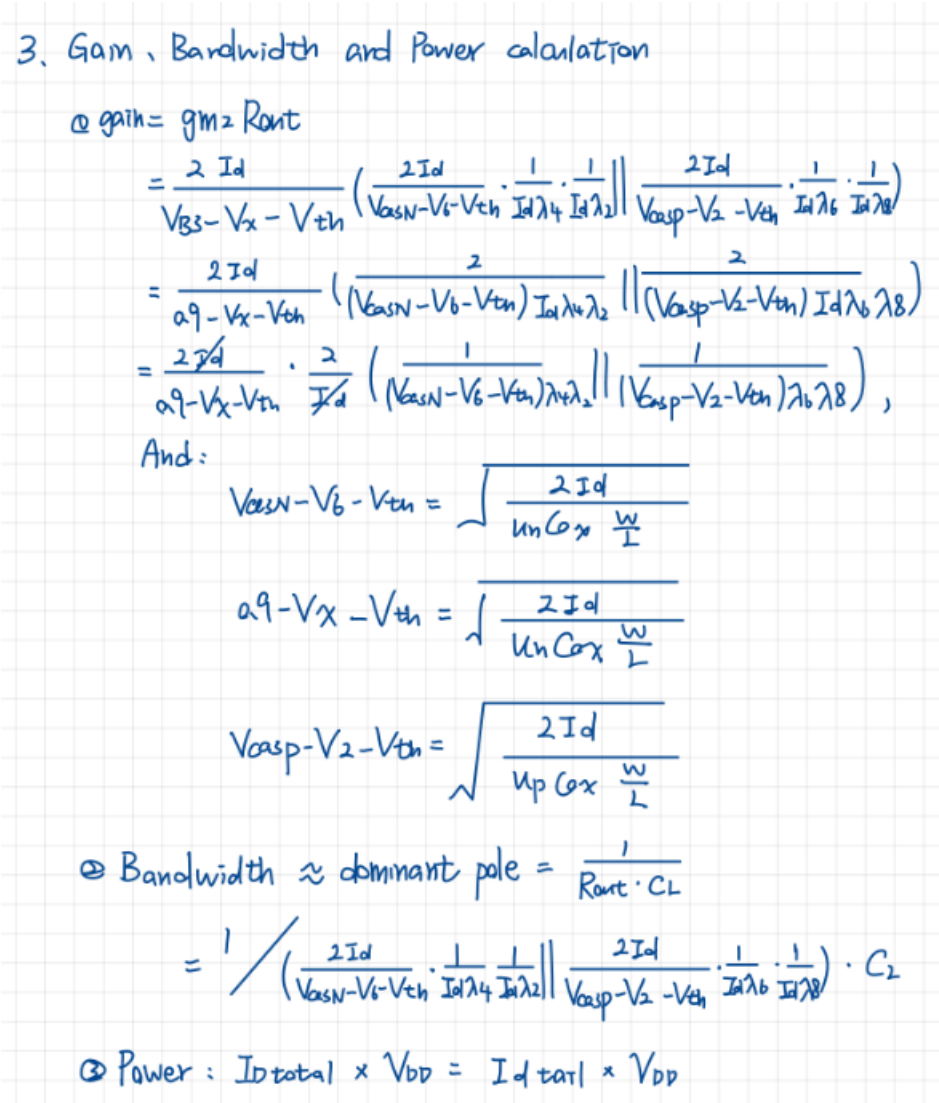
- All NMOS and PMOS should be in saturation region.

- Gain should be larger than 539(V/V)
- -3dB bandwidth should be larger than 7kHz
- Symmetric circuit: minimize common mode noise.
- Cascade: increase output gain

Step 2. Simplify estimation and calculation

- Make length and width of M1 to M8 same, so W/L of all transistor are same, all NMOS parameters (e.g. beta value) are same, and also all PMOS parameters are same
- Tail current is decide by MB and Vb, so I replaced it by an ideal current source (after determine current value, I will change it back). And so:

Step 3. Gain bandwidth and power calculations.



3. Gain, Bandwidth and Power calculation

① gain = $g_{m2} R_{out}$

$$= \frac{2I_d}{V_{B3} - V_x - V_{th}} \left( \frac{2I_d}{V_{GSN} - V_b - V_{th}} \cdot \frac{1}{I_d \lambda_4} \cdot \frac{1}{I_d \lambda_2} \right) \left\| \frac{2I_d}{V_{GSP} - V_2 - V_{th}} \cdot \frac{1}{I_d \lambda_6} \cdot \frac{1}{I_d \lambda_8} \right)$$

$$= \frac{2I_d}{a9 - V_x - V_{th}} \left( \frac{2}{(V_{GSN} - V_b - V_{th}) I_d \lambda_4 \lambda_2} \right\| \frac{2}{(V_{GSP} - V_2 - V_{th}) I_d \lambda_6 \lambda_8} \right)$$

$$= \frac{2\cancel{I_d}}{a9 - V_x - V_{th}} \cdot \frac{2}{\cancel{I_d}} \left( \frac{1}{(V_{GSN} - V_b - V_{th}) \lambda_4 \lambda_2} \right\| \frac{1}{(V_{GSP} - V_2 - V_{th}) \lambda_6 \lambda_8} \right),$$

And:

$$V_{GSN} - V_b - V_{th} = \sqrt{\frac{2I_d}{\mu_n C_{ox} \frac{W}{L}}}$$

$$a9 - V_x - V_{th} = \sqrt{\frac{2I_d}{\mu_n C_{ox} \frac{W}{L}}}$$

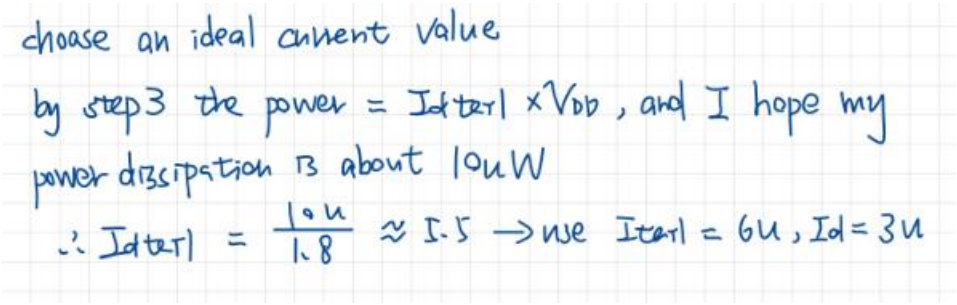
$$V_{GSP} - V_2 - V_{th} = \sqrt{\frac{2I_d}{\mu_p C_{ox} \frac{W}{L}}}$$

② Bandwidth ≈ dominant pole = $\frac{1}{R_{out} \cdot C_L}$

$$= 1 \Big/ \left( \frac{2I_d}{V_{GSN} - V_b - V_{th}} \cdot \frac{1}{I_d \lambda_4} \cdot \frac{1}{I_d \lambda_2} \right\| \frac{2I_d}{V_{GSP} - V_2 - V_{th}} \cdot \frac{1}{I_d \lambda_6} \cdot \frac{1}{I_d \lambda_8} \right) \cdot C_L$$

③ Power : $I_{D\,total} \times V_{DD} = I_{d\,tail} \times V_{DD}$

Step 4. Choose the ideal current value (if I can't adjust a proper parameter to achieve the speculation in the following steps, I will go back to this step to increase the current a little bit):



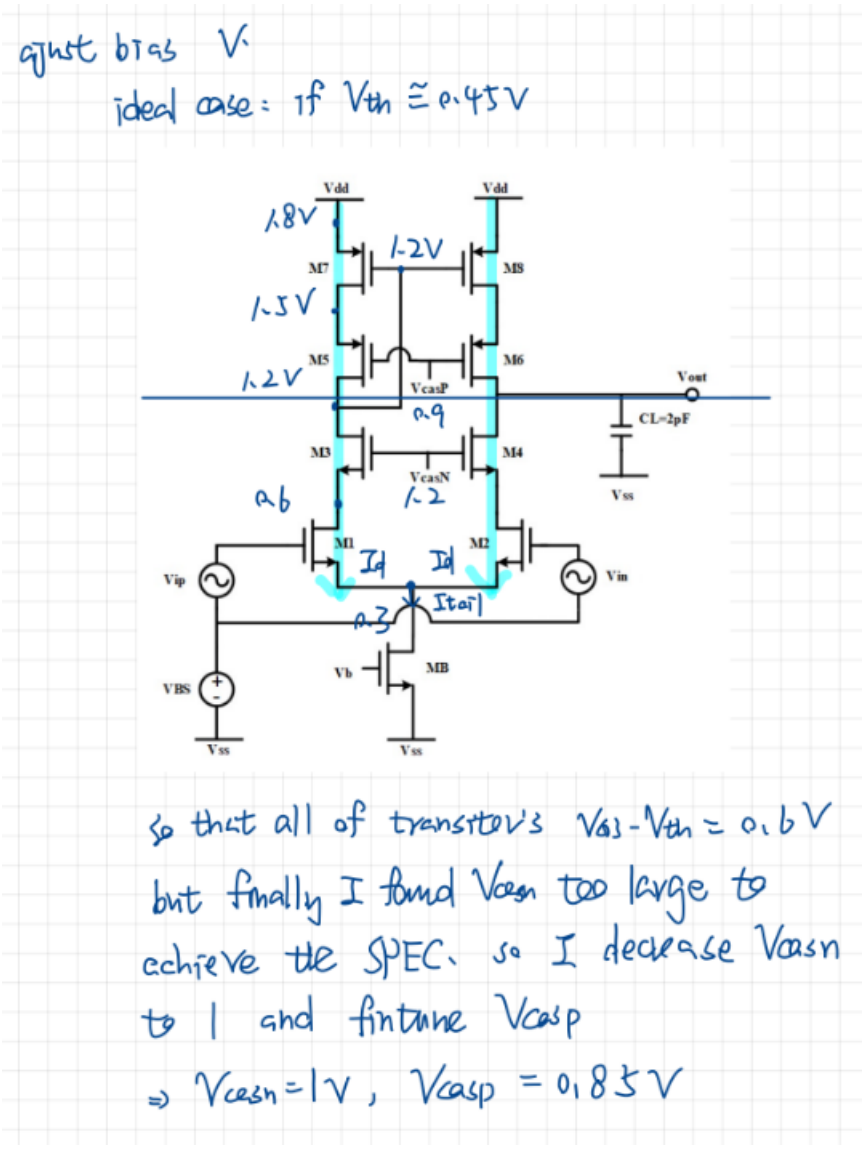

Step 5. Choose size of NMOS and PMOS:

- L should not be too small, or the threshold voltage will be too large, and it will be more difficult to keep all transistors in saturation region
- I use the following test to check out the relationship between $r_o$ ($1/g_{ds}$) and W/L, we can see $r_o$ is approximately proportional to W/L and from the gain and bandwidth equation in step3., if $r_o$ increases(W/L increases), gain increases and bandwidth decreases, so we should let W/L a proper value so that gain will not be too small, and bandwidth will not be to small.
- I use the following test to check out the relationship between beta and W/L, we can see beta is approximately proportional to W/L and from the gain and bandwidth equation in step3., if beta increases(W/L increases), gain decrease and bandwidth increases, so we should let W/L a proper value so that gain will not be too small, and bandwidth will not be too small.
- Finally, I choose L=0.5um, W=2um

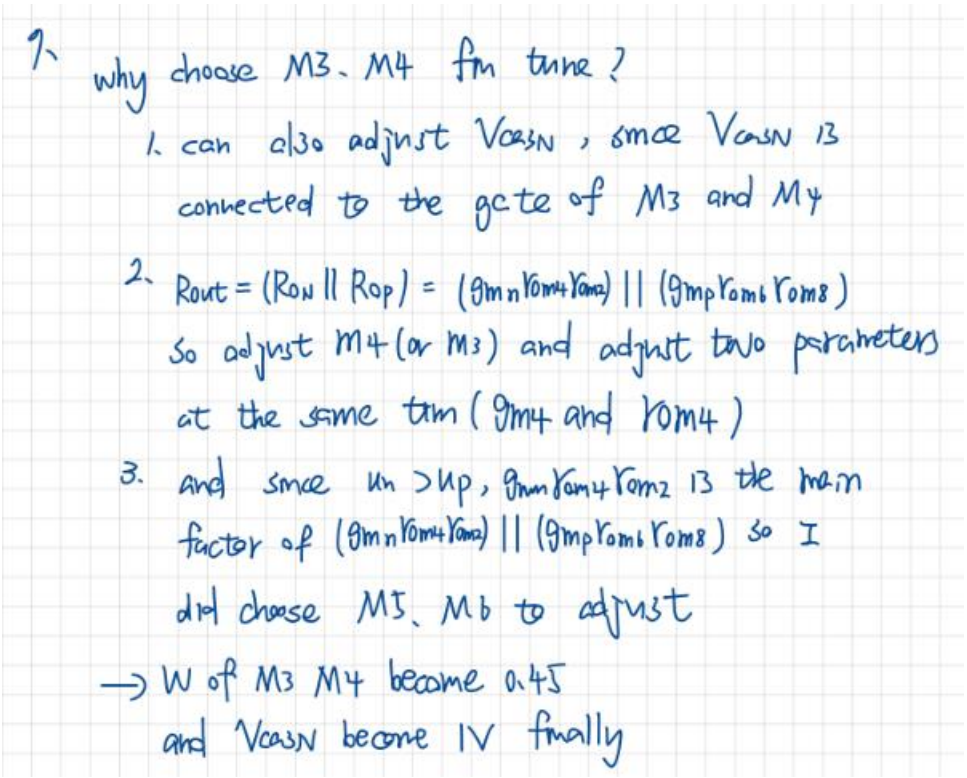
```
m1 vdd vb gnd gnd n_18 l=.5u  w=2u
m2 vdd vb gnd gnd n_18 l=.5u  w=4u
m3 vdd vb gnd gnd n_18 l=1u   w=2u
m4 vdd vb gnd gnd n_18 l=1u   w=4u
```

| subckt | | | | |
|---|---|---|---|---|
| element | 0:m1 | 0:m2 | 0:m3 | 0:m4 |
| model | 0:n_18.1 | 0:n_18.1 | 0:n_18.1 | 0:n_18.1 |
| region | Saturation | Saturation | Saturation | Saturation |
| id | 20.2036u | 42.2446u | 14.3959u | 29.9079u |
| ibs | -4.493e-21 | -7.796e-21 | -3.202e-21 | -5.519e-21 |
| ibd | -384.9075a | -638.7762a | -384.9088a | -638.7785a |
| vgs | 600.0000m | 600.0000m | 600.0000m | 600.0000m |
| vds | 1.8000 | 1.8000 | 1.8000 | 1.8000 |
| vbs | 0. | 0. | 0. | 0. |
| vth | 433.7470m | 429.1863m | 383.5547m | 379.1470m |
| vdsat | 170.9181m | 173.8957m | 198.5977m | 201.8223m |
| vod | 166.2530m | 170.8137m | 216.4453m | 220.8530m |
| beta | 1.2934m | 2.5909m | 621.5332u | 1.2461m |
| gam eff | 507.4465m | 507.4465m | 507.4463m | 507.4464m |
| gm | 198.0789u | 405.5012u | 116.2023u | 237.2249u |
| gds | 2.7004u | 5.5150u | 1.2484u | 2.5516u |
| gmb | 36.4279u | 74.5801u | 22.1406u | 45.1905u |
| cdtot | 2.3923f | 4.6882f | 2.3927f | 4.6889f |
| cgtot | 7.3336f | 14.6710f | 13.7824f | 27.5612f |
| cstot | 9.0229f | 17.9135f | 15.5462f | 30.9591f |
| cbtot | 5.6081f | 10.9787f | 7.2572f | 14.2758f |
| cgs | 6.0299f | 12.0690f | 12.0137f | 24.0318f |
| cgd | 720.4754a | 1.4412f | 707.3906a | 1.4150f |

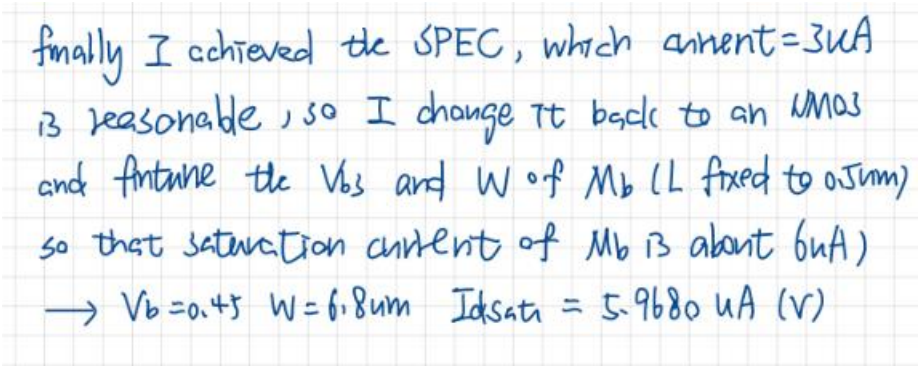
Step 6. Adjust bias voltage: $V_{casn,}$ $V_{casp}$




Step 7. I found that adjust bias voltage will affect gain and bandwidth a lot, so if the gain or bandwidth is really closed to speculation, I will fin tune the size of M3 and M4.




Step 8. Change the ideal current source back to a NMOS.



```
vdd vdd   0 1.8
vss vss   0 0
vb  vb    0 0.45
vn vcasn 0 1
vp  vcasp 0 0.85

vcm   vcm   vss dc=0.9
vdiff vdiff vss dc=0  ac=1
Ep    vip   vcm vdiff vss  0.5
En    vin   vcm vdiff vss -0.5

mb vmb  vb    vss vss n_18 l=.5u  w=6.8u
m1 vm1  vip   vmb vss n_18 l=.5u   w=2u
m2 vm2  vin   vmb vss n_18 l=.5u   w=2u
m3 vm3  vcasn vm1 vss n_18 l=.5u   w=2.2u
m4 vout vcasn vm2 vss n_18 l=.5u   w=2.2u
m5 vm3  vcasp vm7 vdd p_18 l=.5u   w=2u
m6 vout vcasp vm8 vdd p_18 l=.5u   w=2u
m7 vm7  vm3   vdd vdd p_18 l=.5u   w=2u
m8 vm8  vm3   vdd vdd p_18 l=.5u   w=2u

cl vss vout 2p
```

Circuit design

| subckt | | | | | | | subckt | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| element | 0:mb | 0:m1 | 0:m2 | 0:m3 | 0:m4 | 0:m5 | element | 0:m6 | 0:m7 | 0:m8 |
| model | 0:n_18.1 | 0:n_18.1 | 0:n_18.1 | 0:n_18.1 | 0:n_18.1 | 0:p_18.1 | model | 0:p_18.1 | 0:p_18.1 | 0:p_18.1 |
| region | Saturation | Saturation | Saturation | Saturation | Saturation | Saturation | region | Saturation | Saturation | Saturation |
| id | 5.9680u | 2.9840u | 2.9840u | 2.9840u | 2.9840u | -2.9840u | id | -2.9840u | -2.9840u | -2.9840u |
| ibs | -1.008e-21 | -74.3876a | -74.3876a | -103.1978a | -103.1978a | 30.7773a | ibs | 30.7773a | 4.078e-22 | 4.078e-22 |
| ibd | -192.1361a | -96.8112a | -96.8112a | -261.2117a | -261.2117a | 85.9470a | ibd | 85.9470a | 30.7765a | 30.7765a |
| vgs | 450.0000m | 552.1373m | 552.1373m | 547.2695m | 547.2695m | -715.7911m | vgs | -715.7911m | -654.0502m | -654.0502m |
| vds | 347.8627m | 104.8678m | 104.8678m | 693.2193m | 693.2193m | -419.8413m | vds | -419.8413m | -234.2089m | -234.2089m |
| vbs | 0. | -347.8627m | -347.8627m | -452.7305m | -452.7305m | 234.2089m | vbs | 234.2089m | 0. | 0. |
| vth | 445.9782m | 517.7428m | 517.7428m | 524.2083m | 524.2083m | -583.3432m | vth | -583.3432m | -520.2438m | -520.2438m |
| vdsat | 71.3830m | 88.4556m | 88.4556m | 83.0515m | 83.0515m | -161.4173m | vdsat | -161.4173m | -158.7329m | -158.7329m |
| vod | 4.0218m | 34.3945m | 34.3945m | 23.0612m | 23.0612m | -132.4479m | vod | -132.4479m | -133.8064m | -133.8064m |
| beta | 4.4031m | 1.2972m | 1.2972m | 1.4292m | 1.4292m | 265.3957u | beta | 265.3957u | 277.7935u | 277.7935u |
| gam eff | 507.4460m | 516.3919m | 516.3919m | 518.8320m | 518.8320m | 555.4719m | gam eff | 555.4719m | 557.0846m | 557.0846m |
| gm | 123.5472u | 52.8838u | 52.8838u | 57.9531u | 57.9531u | 33.7945u | gm | 33.7945u | 33.3259u | 33.3259u |
| gds | 2.1685u | 6.2841u | 6.2841u | 944.1748n | 944.1748n | 390.8122n | gds | 390.8122n | 991.9044n | 991.9044n |
| gmb | 24.3493u | 8.1358u | 8.1358u | 8.2234u | 8.2234u | 8.8742u | gmb | 8.8742u | 9.7457u | 9.7457u |
| cdtot | 9.7511f | 3.0363f | 3.0363f | 2.8205f | 2.8205f | 2.4432f | cdtot | 2.4432f | 2.7716f | 2.7716f |
| cgtot | 18.1781f | 6.3942f | 6.3942f | 6.5206f | 6.5206f | 6.7490f | cgtot | 6.7490f | 6.8192f | 6.8192f |
| cstot | 21.3434f | 7.2906f | 7.2906f | 7.4486f | 7.4486f | 8.1918f | cstot | 8.1918f | 8.5184f | 8.5184f |
| cbtot | 20.3305f | 5.5944f | 5.5944f | 5.6506f | 5.6506f | 5.2388f | cbtot | 5.2388f | 5.8816f | 5.8816f |
| cgs | 12.2889f | 4.9116f | 4.9116f | 4.8798f | 4.8798f | 5.5812f | cgs | 5.5812f | 5.5856f | 5.5856f |
| cgd | 2.5423f | 789.0279a | 789.0279a | 803.7885a | 803.7885a | 723.1107a | cgd | 723.1107a | 757.3319a | 757.3319a |

All transistors operate in saturation region.

```
****     small-signal transfer characteristics

     v(vout)/vdiff                              =  539.4155
     input resistance at              vdiff     =  1.000e+20
     output resistance at v(vout)               =   11.1712x
```

Small signal transfer transfer characteristics

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
gain_db=  54.6387     at=   1.0000
            from=   1.0000     to=   1.0000g
bandwidth=   7.0871k
```

Ac analysis

```
**** voltage sources

subckt
element  0:vdiff    0:vb       0:vcm      0:vdd      0:vn       0:vp
 volts      0.       450.0000m  900.0000m    1.8000     1.0000   850.0000m
 current    0.         0.         0.        -5.9680u    0.         0.
 power      0.         0.         0.        10.7424u    0.         0.

subckt
element  0:vss
 volts      0.
 current    5.9680u
 power      0.

    total voltage source power dissipation=   10.7424u       watts
```

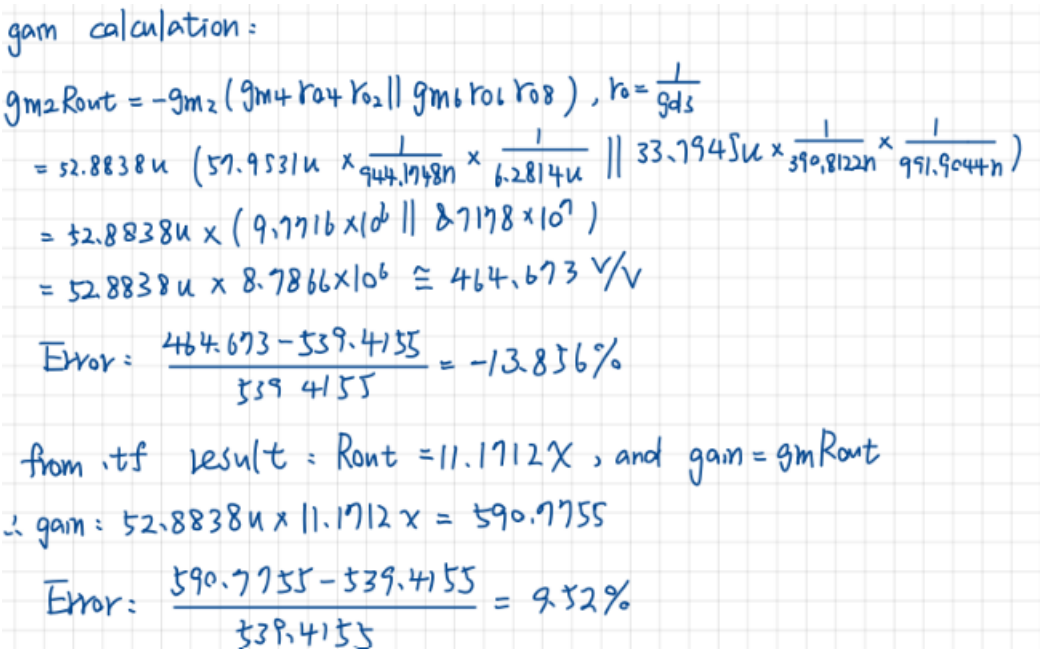
Power dissipation

Power hand calculation: 1.8*5.9680u=10.7424uW

3. Differential Mode

```
****     small-signal transfer characteristics

     v(vout)/vdiff                              =  539.4155
     input resistance at             vdiff      =  1.000e+20
     output resistance at v(vout)               =   11.1712x
```

Measured gain value: 539.4155(V/V)




Hand calculation gain value

Reason of gain error:

- When using small signal parameters to calculate gain, I didn't consider body effect (body of NMOS/PMOS is connected to ground/vdd)
- When use Rout to calculate gain, we should use effective Gm to calculate gain value, because the current source(Mb) is not ideal which means it has a resistance.

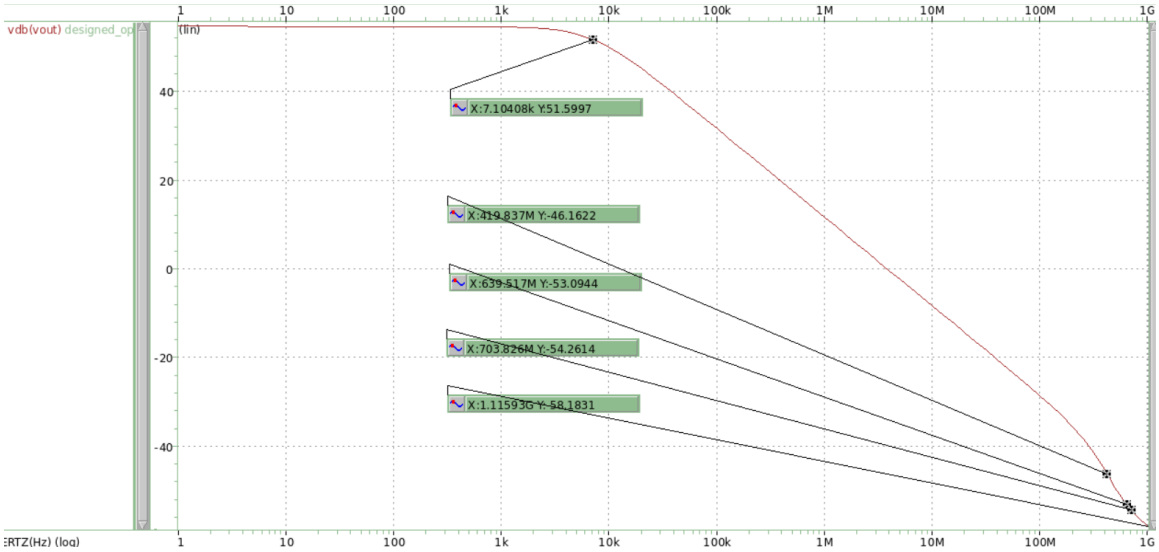
4. Frequency Response/Pole and zero

```
**************************************************
  ******   pole/zero analysis


   input =  0:vdiff          output = v(vout)

      poles (rad/sec)                 poles ( hertz)
real             imag             real             imag
-44.6363k        0.               -7.10408k        0.
-2.07008g        -1.63504g        -329.464x        -260.225x
-2.07008g        1.63504g         -329.464x        260.225x
-4.01821g        0.               -639.517x        0.
-4.42227g        0.               -703.826x        0.
-7.01161g        0.               -1.11593g        0.
-8.15773g        0.               -1.29834g        0.

      zeros (rad/sec)                 zeros ( hertz)
real             imag             real             imag
-1.98363g        -3.15855g        -315.705x        -502.698x
-1.98363g        3.15855g         -315.705x        502.698x
-4.01801g        0.               -639.486x        0.
-4.42233g        0.               -703.836x        0.
-8.16157g        0.               -1.29895g        0.
52.3583g         0.               8.33308g         0.
```

Pole and zero

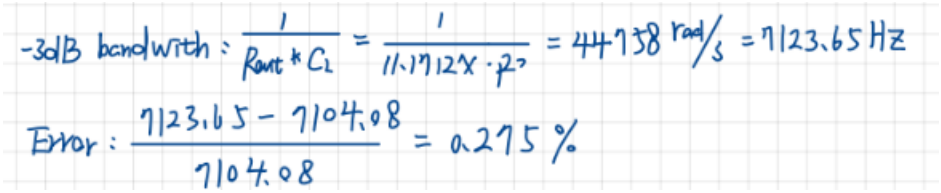
```
****** ac analysis tnom=  25.000 temp=  25.000 ******
gain_db=  54.6387     at=   1.0000
            from=   1.0000     to=   1.0000g
bandwidth=   7.0871k
```

Bandwidth: 7.0871kHz




X axis: frequency (log (Hz)) – Y axis: open loop gain(dB)

Hand calculation of -3dB bandwidth (dominant pole):




*Unit is MHz

Reason of bandwidth error:

- Although the first pole dominates the bandwidth value, the bandwidth is affected by all the poles. Therefore, if we only consider the first pole, there will be some errors.

5. Specification

| Device size | | | |
|---|---|---|---|
| M1(W/L, m) | 2um/0.5um | M5(W/L, m) | 2um/0.5um |
| M2(W/L, m) | 2um/0.5um | M6(W/L, m) | 2um/0.5um |
| M3(W/L, m) | 2.2um/0.5um | M7(W/L, m) | 2um/0.5um |
| M4(W/L, m) | 2.2um/0.5um | M9(W/L, m) | 2um/0.5um |
| Mb(W/L, m) | 6.8um/0.5um | | |

Table 1

```
    total voltage source power dissipation=   10.7424u       watts
```

Fig. 3 Power dissipation: 10.7424watts

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
gain_db=  54.6387     at=   1.0000
            from=   1.0000     to=   1.0000g
bandwidth=   7.0871k
```

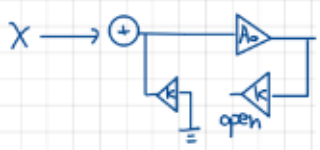
Falt-band gain: 54.6387dB

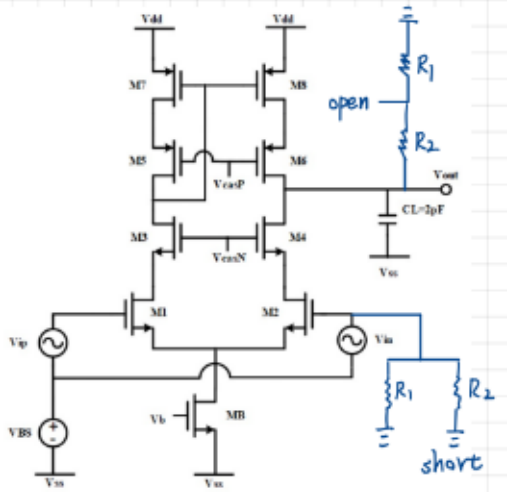
Part2

1. Discuss how I determine the value of R1 and R2

We need to consider the effect of feedback on I/O impedance:

It's an V-V amplifier, so we can break the ckt like this:




gain: $\dfrac{g_{m2}(g_{m6}r_{o6}r_{o8}\,||\,g_{m4}r_{o4}r_{o2}\,||\,(R_1+R_2))}{1+g_{m2}(g_{m6}r_{o6}r_{o8}\,||\,g_{m4}r_{o4}r_{o2}\,||\,(R_1+R_2))\left(\frac{R_1}{R_1+R_2}\right)}$

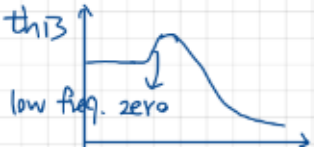
So if $R_1$, $R_2$ too small it will affect Rout and therefore decrease the gain.

dominant pole: $\dfrac{1}{(g_{m6}r_{o6}r_{o8}\,||\,g_{m4}r_{o4}r_{o2}\,||\,(R_1+R_2))\,C_L}$

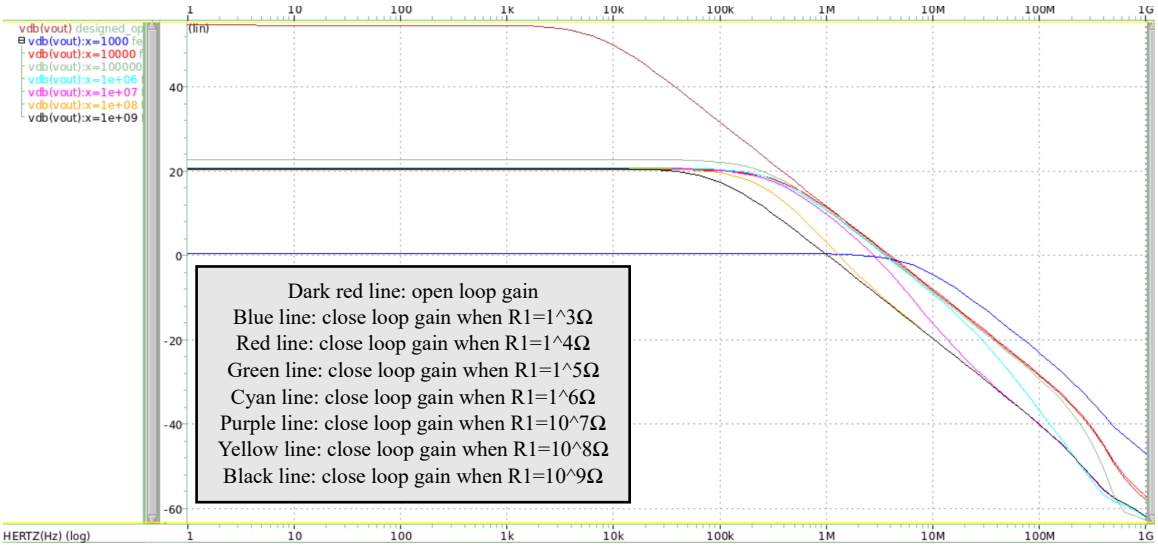
so if $R_1$, $R_2$ too large it will affect Rout and therefore decrease dominant pde value ( bandwidth ↓ )

zero: $\dfrac{1}{C_m(R_m+(R_1\,||\,R_2))}$

so if $R_1$, $R_2$ too large it will decrease the zero of mput node, so the graph will be like this



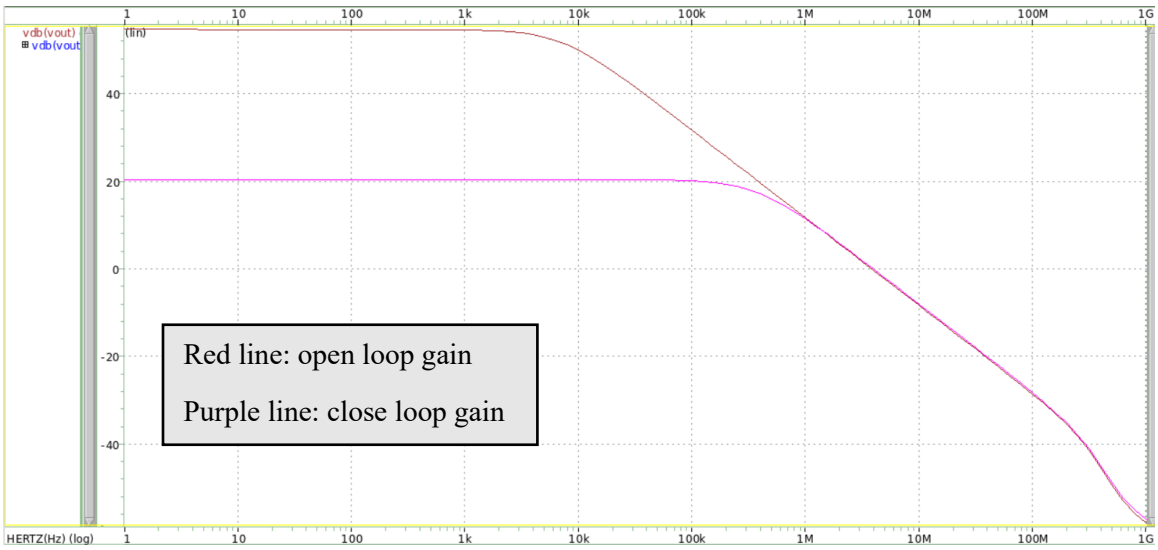

So, to find proper r value I use dc sweep from 1000Ω to 10^9Ω, and we can see when r1=10kΩ, the graph is the most ideal.




X axis: frequency(log (Hz)) – Y axis: open loop gain(dB)

```
****     small-signal transfer characteristics

     v(vout)/vdiff                          =   10.4395
     input resistance at          vdiff     =   1.000e+20
     output resistance at v(vout)           =   207.5418k
```

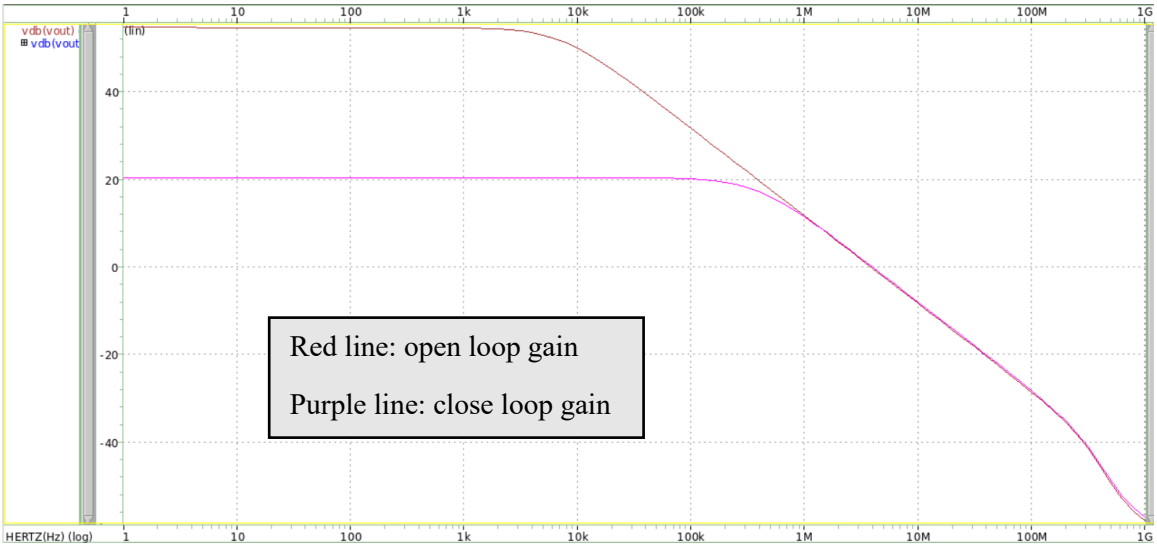
But, when I look at the small-signal transfer characteristics, the gain doesn't achieve the speculation. Therefore, I sweep r1(9000 Ω, 9100 Ω, 9200 Ω …… 11000Ω), then I found that when r1=9.8k Ω, r2=98k Ω, the curve will be the most ideal and the gain is really close to 10(V/V).




X axis: frequency (log (Hz)) – Y axis: open loop gain(dB)

```
****     small-signal transfer characteristics

     v(vout)/vdiff                              =   10.0715
     input resistance at            vdiff       =  1.000e+20
     output resistance at v(vout)               =  199.8550k
```

2. Observe the frequency response, you will see the gain change after we connect the feedback loop. Please mark the flat-band gain in both two curves and hand calculate the gain change, the flat-band gain after closed-loop as well as gain error.




X axis: frequency (log (Hz)) – Y axis: open loop gain(dB)

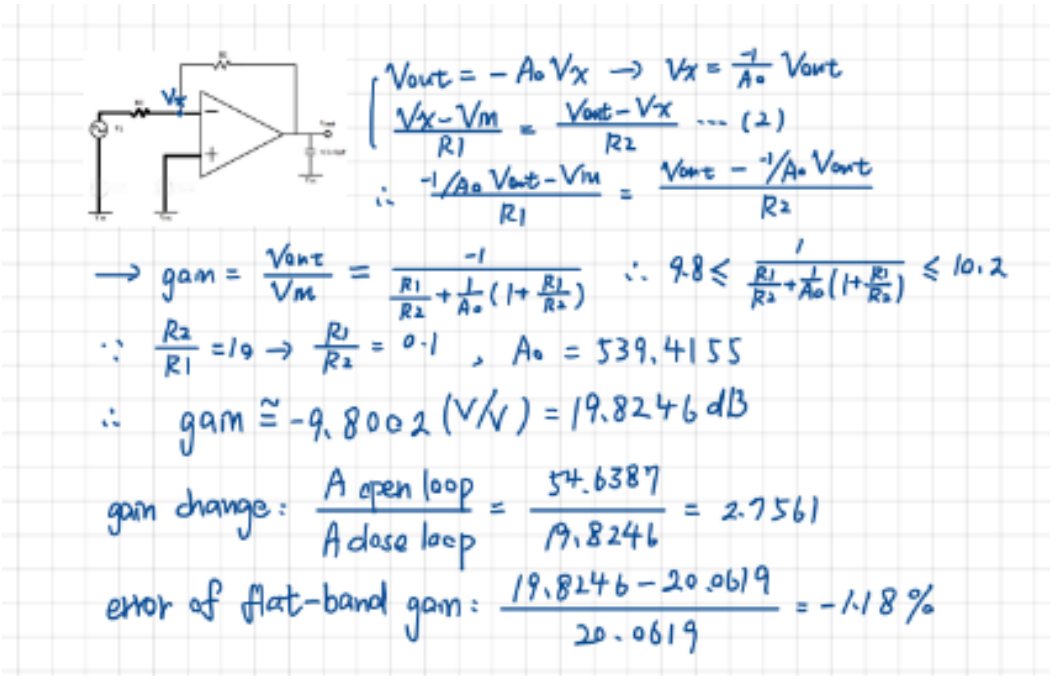
```
****** ac analysis tnom=  25.000 temp=  25.000 ******
gain_db=  54.6387     at=   1.0000
          from=   1.0000     to=   1.0000g
bandwidth=   7.0871k
```

Open loop flat-band gain: 54.6387dB

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
 *** parameter x =     1.0000k       ***

gain_db=  20.0619     at=   1.0000
          from=   1.0000     to=   1.0000g
bandwidth= 395.6924k
```

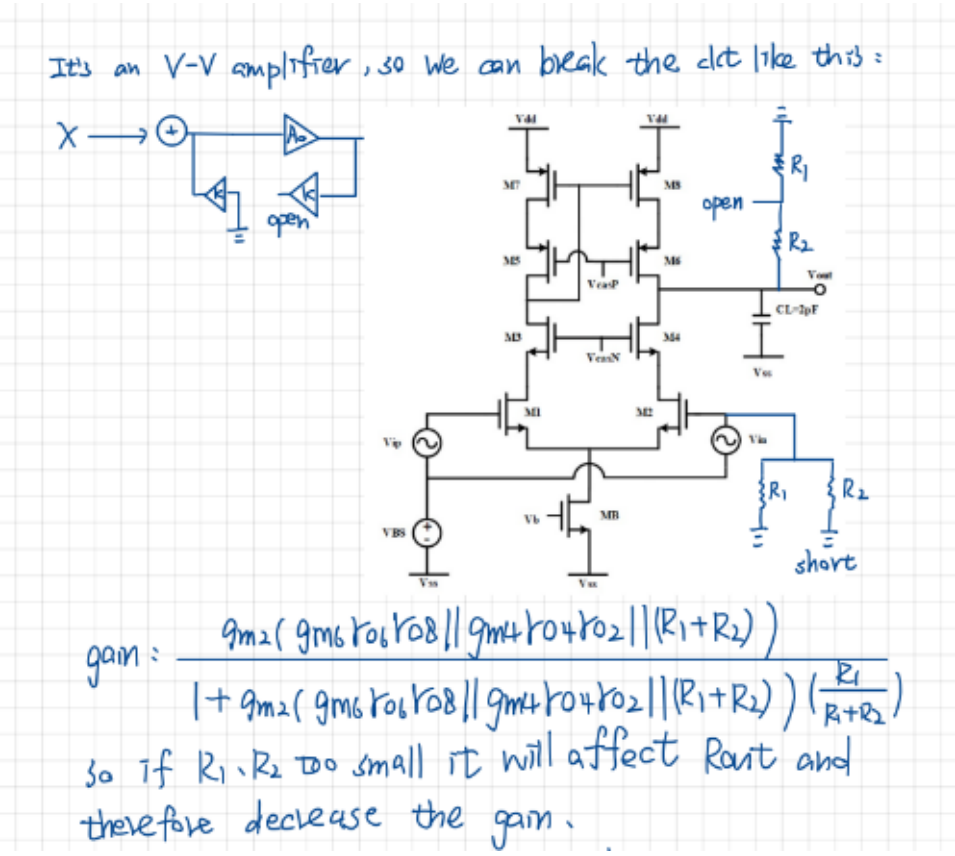
Close loop flat-band gain: 20.0619dB

Hand calculation of gain:

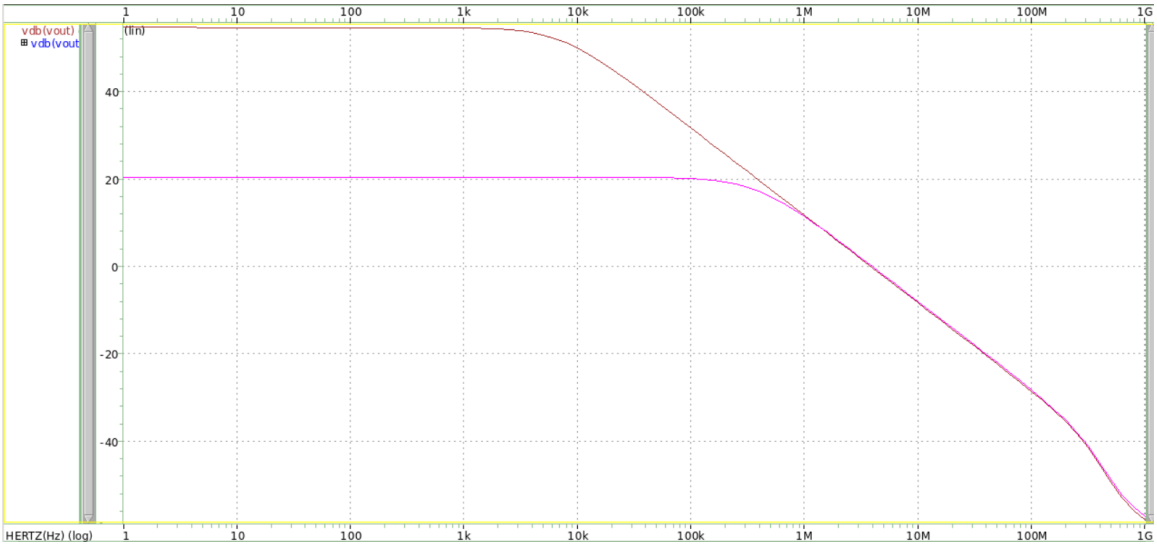



Error reason:

The feedback loop will affect original opamp, but we didn't take it into consideration:



3. Closed-loop gain is obviously lower than open-loop gain. Then, why do we need the feedback loop? How does it favor our needs?
    - Gain desensitization against open loop gain variations due to process and temperature variations.
      With feedback, the closed-loop gain relies less on the value of $A_v$. For example, in our circuit, the closed-loop gain is primarily determined by the ratio of r1 and r2.
    - Increase the bandwidth of the circuit.
      Although the gain decrease, the bandwidth of the circuit increase(tradeoff)




X axis: frequency (log (Hz)) – Y axis: open loop gain(dB)

    - Insensitive to load variations.
      The negative feedback creates a more consistent output, so the load impedance will not affect the circuit.
    - Improve the linearity of the circuit.
      The negative feedback reduces the common mode noise and also reduce the nonlinearities in the output signal.
4. Observe the frequency response. How does the dominant pole change after connecting feedback loop? And hand calculates the dominant pole after connecting feedback loop.

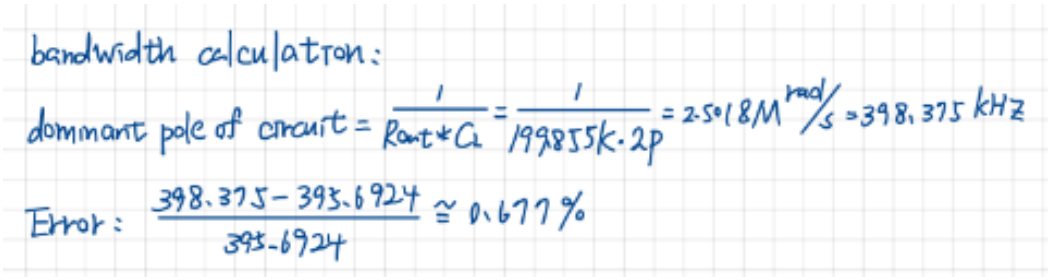
```
**************************************************
  ******   pole/zero analysis


   input =  0:vdiff          output = v(vout)

      poles (rad/sec)                 poles ( hertz)
real             imag             real             imag
-44.6363k        0.               -7.10408k        0.
-2.07008g        -1.63504g        -329.464x        -260.225x
-2.07008g        1.63504g         -329.464x        260.225x
-4.01821g        0.               -639.517x        0.
-4.42227g        0.               -703.826x        0.
-7.01161g        0.               -1.11593g        0.
-8.15773g        0.               -1.29834g        0.

      zeros (rad/sec)                 zeros ( hertz)
real             imag             real             imag
-1.98363g        -3.15855g        -315.705x        -502.698x
-1.98363g        3.15855g         -315.705x        502.698x
-4.01801g        0.               -639.486x        0.
-4.42233g        0.               -703.836x        0.
-8.16157g        0.               -1.29895g        0.
52.3583g         0.               8.33308g         0.
```

Dominant pole of open-loop: 7.10408kHz

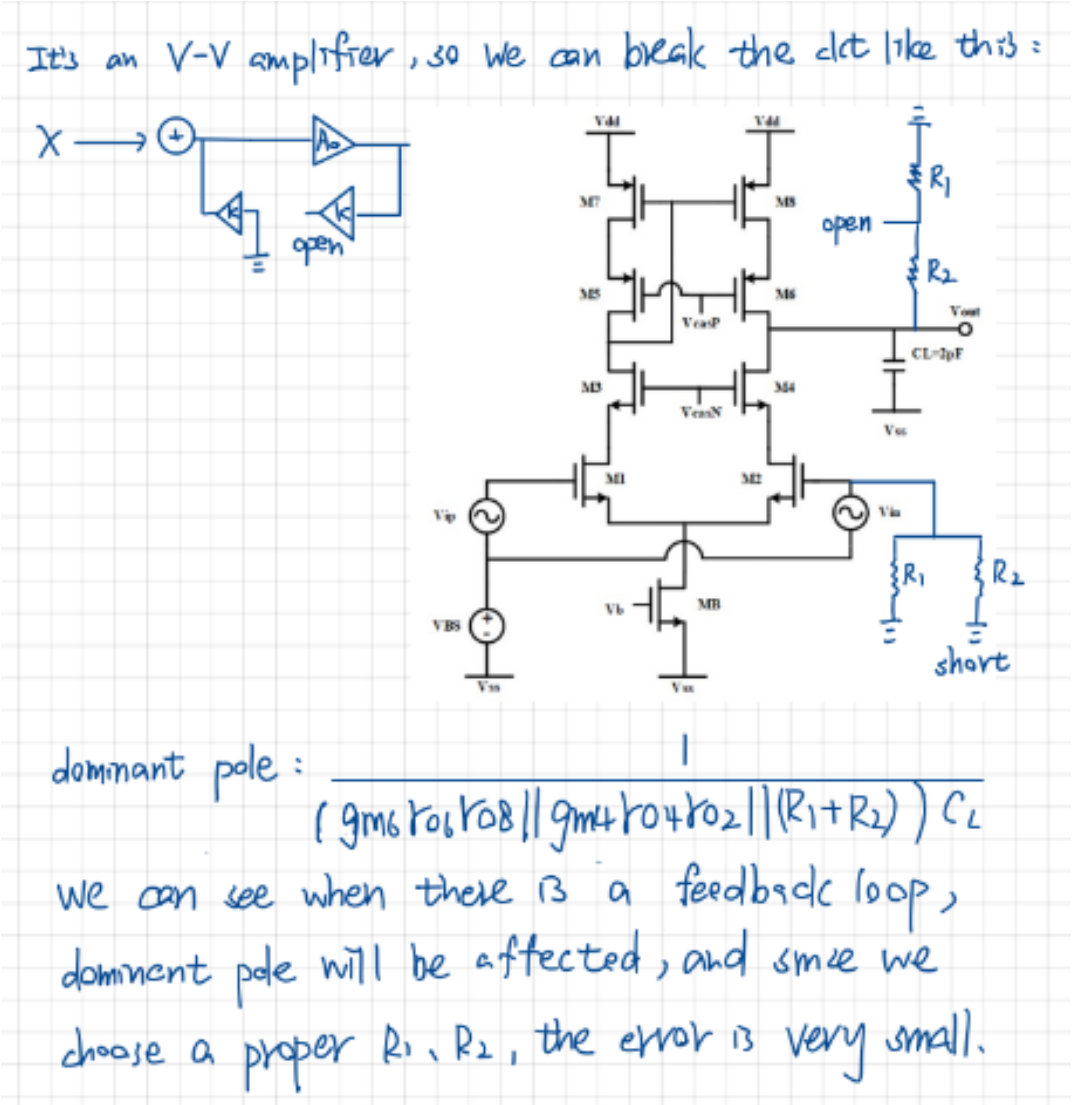
```
******   pole/zero analysis


   input =  0:vdiff          output = v(vout)

      poles (rad/sec)                  poles ( hertz)
real             imag             real             imag
-2.49224x        0.               -396.652k        0.
-2.07823g        -1.64084g        -330.760x        -261.149x
-2.07823g        1.64084g         -330.760x        261.149x
-4.07554g        0.               -648.643x        0.
-4.61715g        0.               -734.842x        0.
-6.78916g        0.               -1.08053g        0.
-8.24254g        0.               -1.31184g        0.
-20.2500g        0.               -3.22289g        0.

      zeros (rad/sec)                  zeros ( hertz)
real             imag             real             imag
-1.92463g        -3.08556g        -306.315x        -491.082x
-1.92463g        3.08556g         -306.315x        491.082x
-4.06236g        0.               -646.544x        0.
-4.58028g        0.               -728.974x        0.
-8.31779g        0.               -1.32382g        0.
-17.5708g        0.               -2.79649g        0.
52.3609g         0.               8.33349g         0.
```

Dominant pole of open-loop: 396.652kHz

Hand calculation of dominant pole after connecting feedback loop.




Reason of error:




Summary table

| Part1: open-loop simulation | | | |
|---|---|---|---|
| Working item | specification | simulation | calculation |
| Tail current | (uA) | 5.968 | - |
| Gain | >539(V/V) | 539.4155 | 590.7755 |
| Tial current bias | VBS(V) | 0.45 | - |
| Input common mode | Vb(V) | 0.9 | - |
| -3dB bandwidth | >7kHz | 7.0871 | 7.12365 |
| Power dissipation | uW | 10.7424 | 10.7424 |
| Part2: closed-loop simulation | | | |
| Working item | specification | simulation | calculation |
| Closed loop gain | 10(V/V) | 10.0715 | 9.8002 |