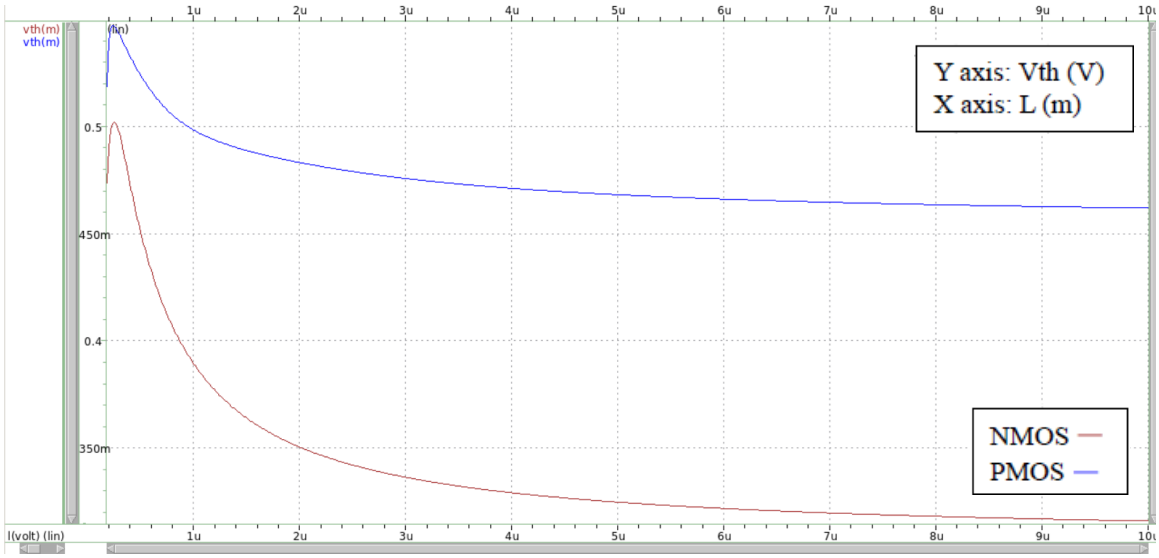
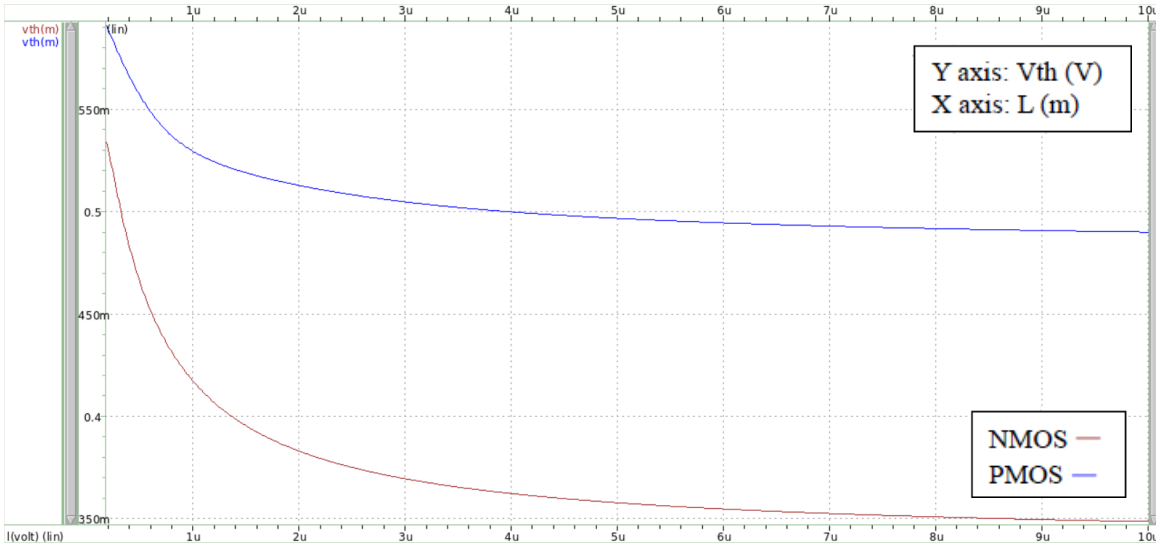
EE323500 HW1 report

110061217 王彥智

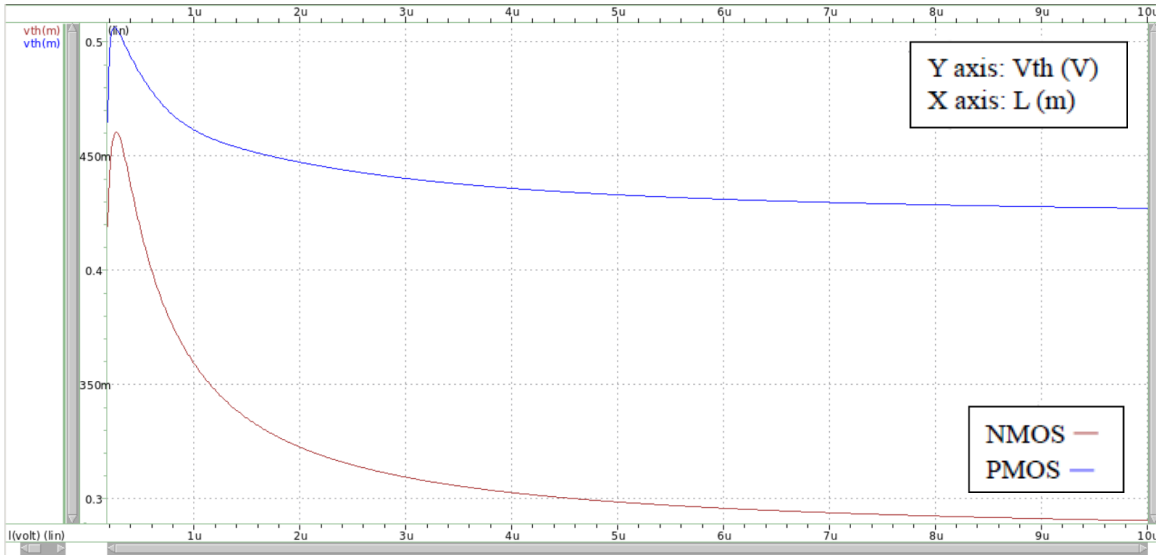
- Part1: red line represents NMOS, blue line represents PMOS.
  - Threshold voltage
    - When channel length is shorter than 0.2um, V_{th} increases with channel length because of short-channel effect. When channel length is longer, V_{th} and channel length is negatively correlated because of reverse short-channel effect. When channel length is even longer, V_{th} becomes a constant.
    - In ss corner, there is no short-channel effect, and the v_{th} is larger than tt corner, since the carrier mobility of NMOS and PMOS is lower than normal. In ff corner, the short-channel effect is more severe, and the V_{th} is smaller than tt mode, since the carrier mobility of NMOS and PMOS is higher than normal.
    - V_{th} of NMOS is always lower than v_{th} of PMOS. The reason is the mobility of electronics is higher than holes.



tt corner: Threshold voltage(volt)-Channel length(meter)

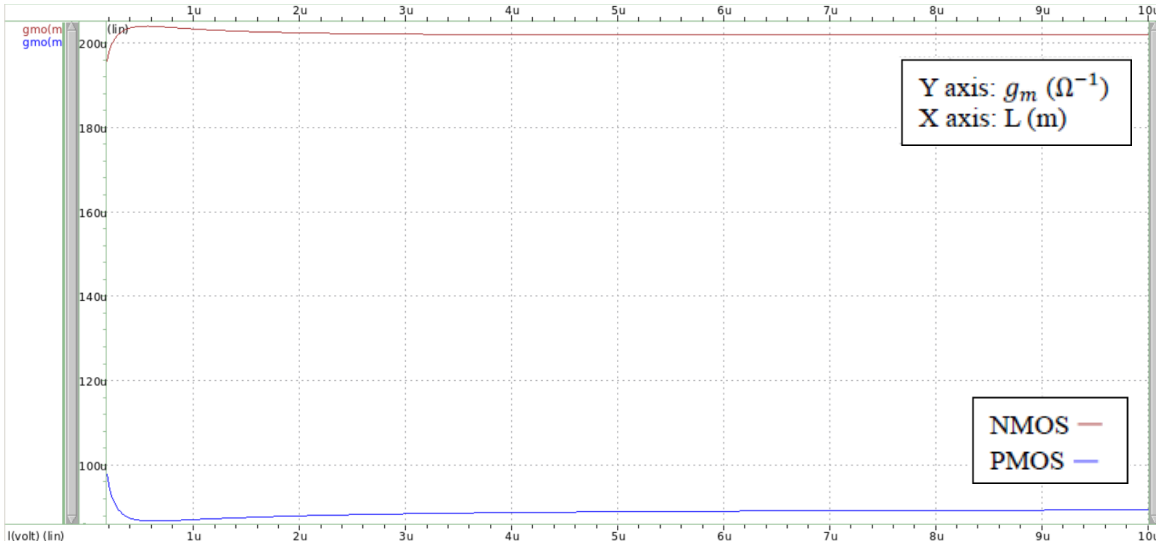


ss corner: Threshold voltage(volt)-Channel length(meter)



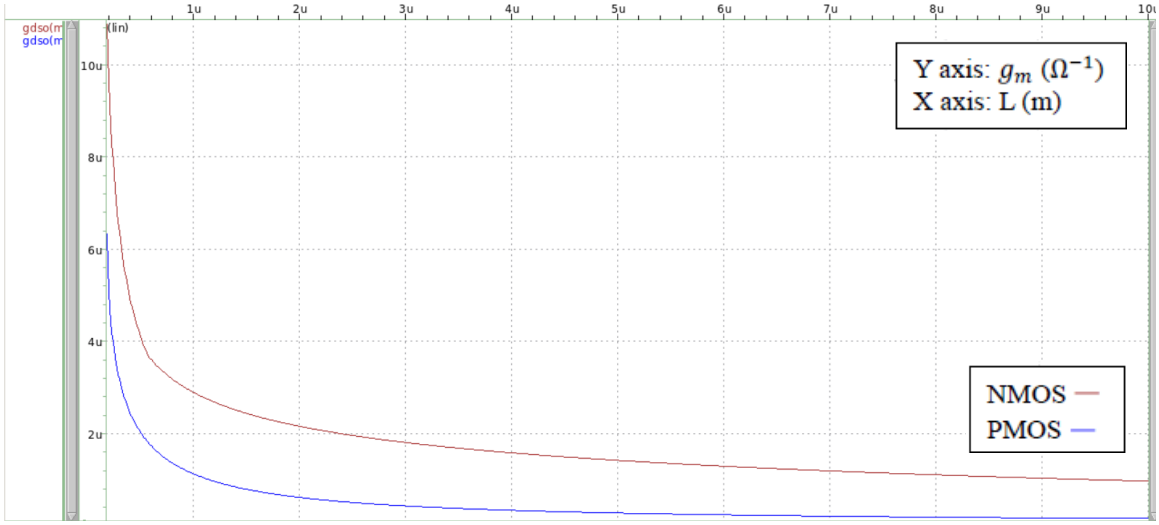
ff corner: Threshold voltage(volt)-Channel length(meter)

- Transconductance:
  - $g_m = \mu_n C_{ox} \frac{W}{L} V_{ov}$
  - The transconductance of NMOS is always larger than PMOS, since mobility of electronics is higher than holes.
  - When channel length is shorter, transconductance of NMOS is proportional to channel length and transconductance od PMOS is inversely proportional to channel length.



Transconductance(siemens)-channel length(meter)

- Output conductance:
  - $g_{ds} = \frac{dIs}{dV_{gs}} = \mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th} - V_{ds})$: output conductance is inversely proportional to channel length.
  - Output conductance of NMOS is always higher than PMOS, since mobility of electronics is higher than holes.

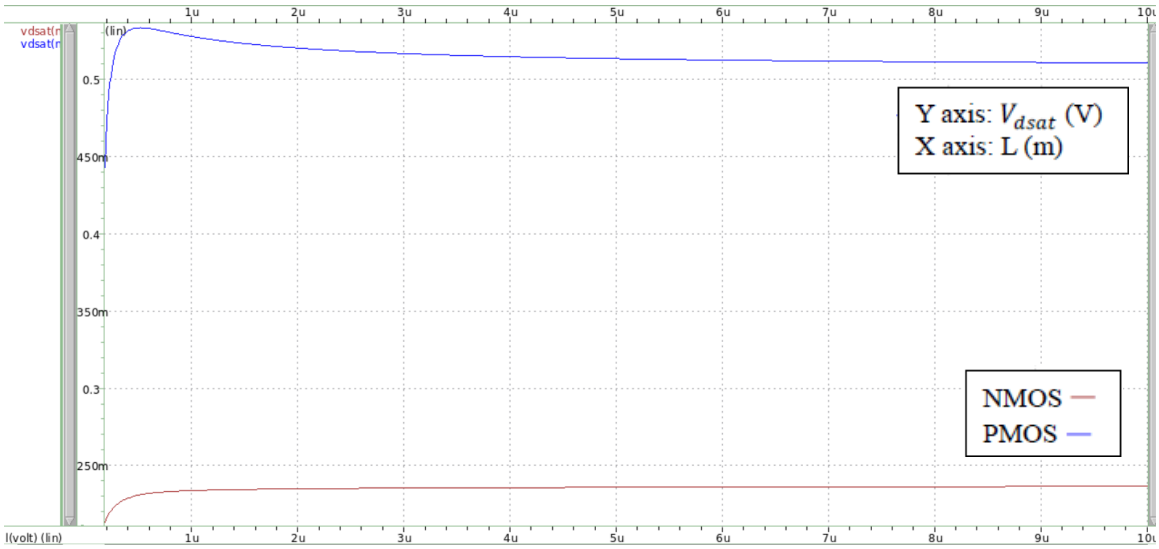


Output conductance(siemens)-channel length(meter)

- Saturation drain voltage:
  - $V_{dsat} = (\frac{m}{V_{gs}-V_T} + \frac{1}{\varepsilon_{sat} L})^{-1}$ saturation voltage will increase and finally saturate to a fixed value as the channel length increase. It is

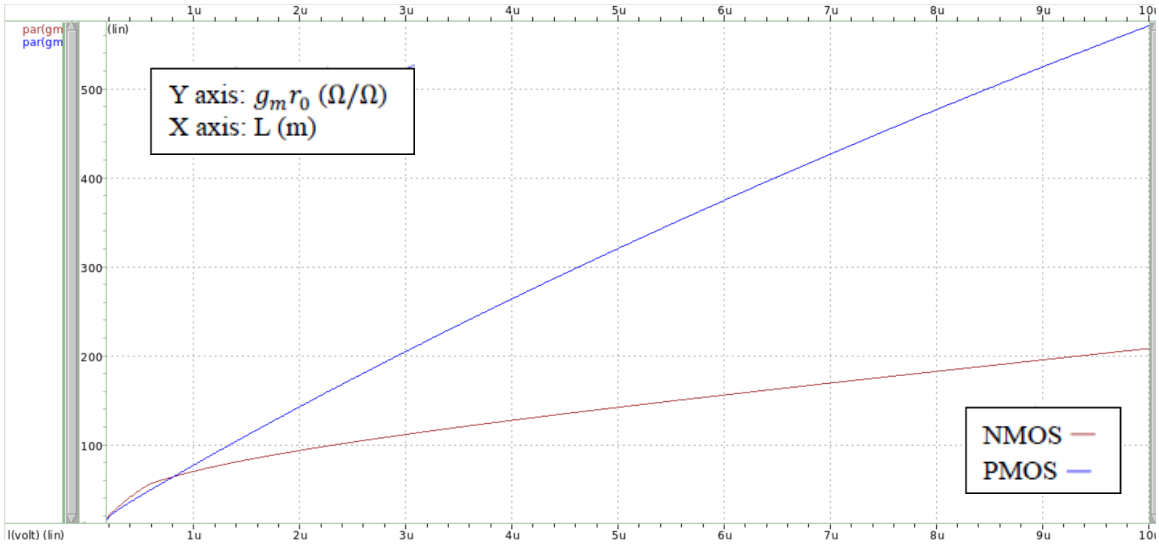
because the increase of V_{dsat} is dominated by $\frac{m}{V_{gs}-V_T}$, so V_{dsat} reaches a constants when channel length is longer.

- PMOS saturation voltage is always higher than NMOS saturation voltage, since mobility of electronics is higher than holes.



Saturation drain voltage(volt)-channel length(meter)

- Intrinsic gain: the intrinsic gain increases as the channel length increase, and when channel length is short, NMOS intrinsic gain is higher, and when channel length is longer, PMOS intrinsic gain is higher.



intrinsic gain-channel length(meter)

- Power efficiency:

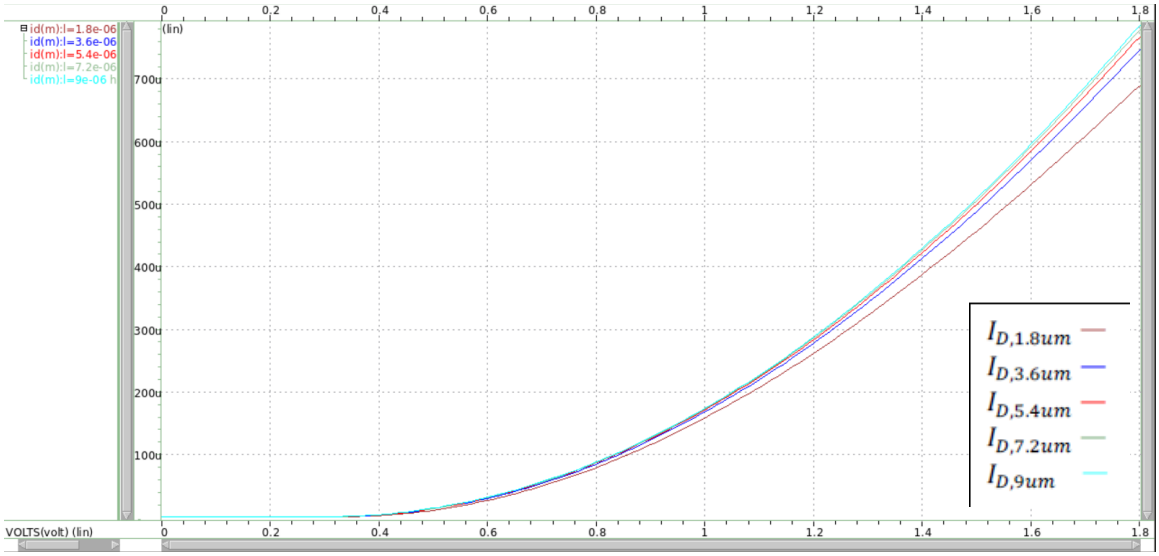
- Power of PMOS is always negative since the definition of drain current. Therefore, we use abs () to set the power to positive.
- When L<1um, both NMOS and PMOS gradually converge to a constant.
- NMOS is more power efficient since mobility of electronics is higher than holes.

power efficiency(I/volt)-channel length

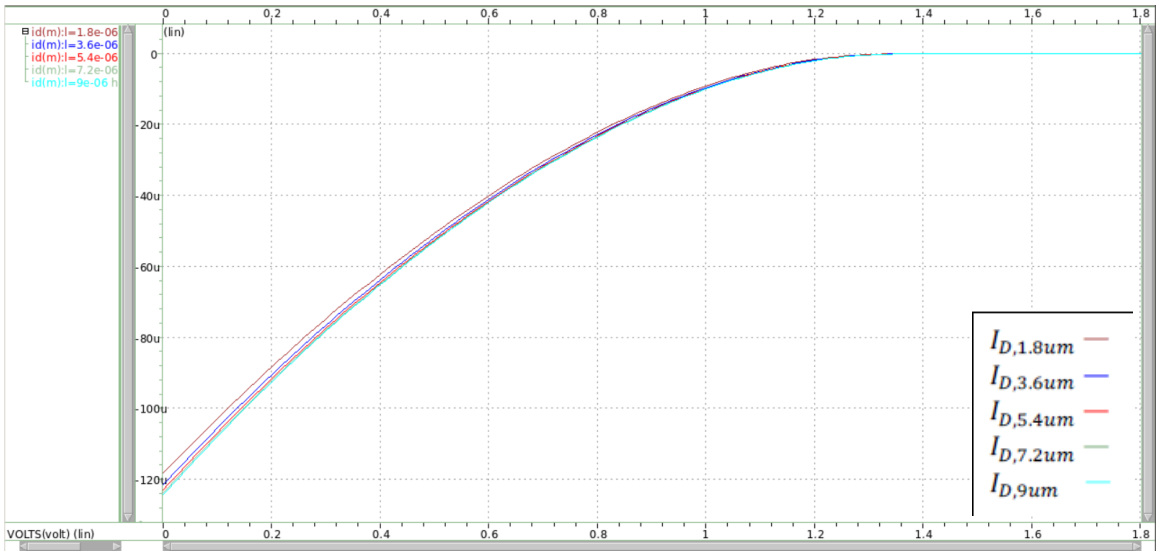
- Speed
  - $I = C(\frac{dV}{dt}) \rightarrow speed = change\ of\ output\ voltage = \frac{dV}{dt} = \frac{I}{C}$ and I_d is proportional to g_m, so $\frac{g_m}{C}$ represents speed.
  - the speed will decrease a lot as the channel length increases, since the gate capacity is proportional to the area of gate which is equal to channel length multiples width, so capacity increase as channel length increase, and the speed decrease.
  - NMOS speed is always faster than PMOS since mobility of electronics is higher than holes.

Speed(I/second)-channel length(meter)

- Part2
  - Regardless of NMOS or PMOS, Drain Current is positively related to Gate voltage.
  - When the Gate voltage is fixed, the longer the Channel length is, the greater the Drain Current is .
  - Due to the definition of the current direction, the PMOS curve has a negative sign.



NMOS: drain current(ampere)-gate voltage(volt)



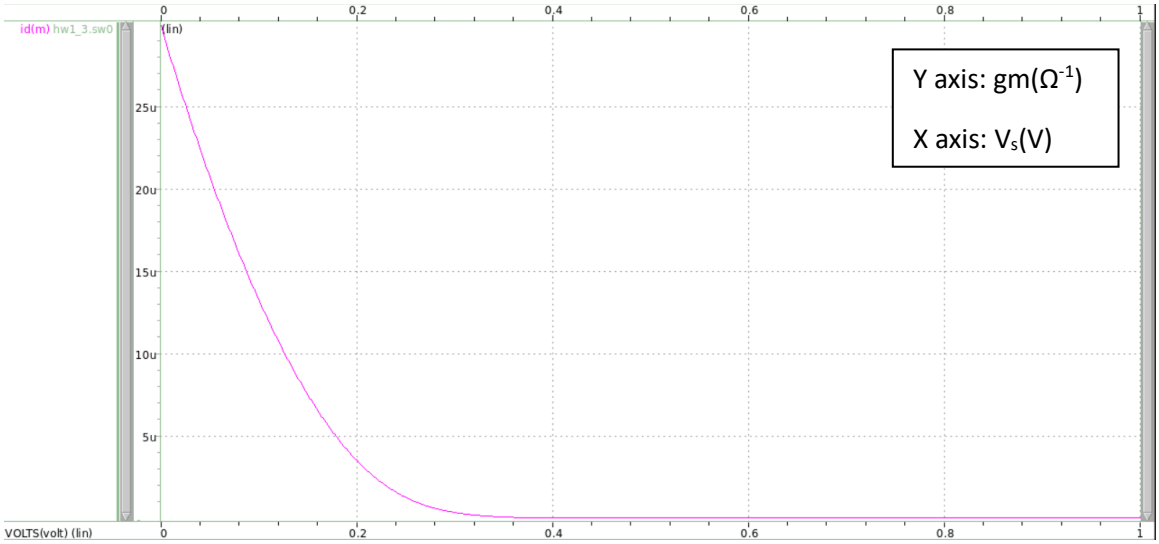
PMOS: drain current(ampere)-gate volage(volt)

- Part3
  - Correct size: L = 1.2u, W/L = 2
  - Observation:
    - As the V_s increase, the threshold voltage increases because of the body effect.

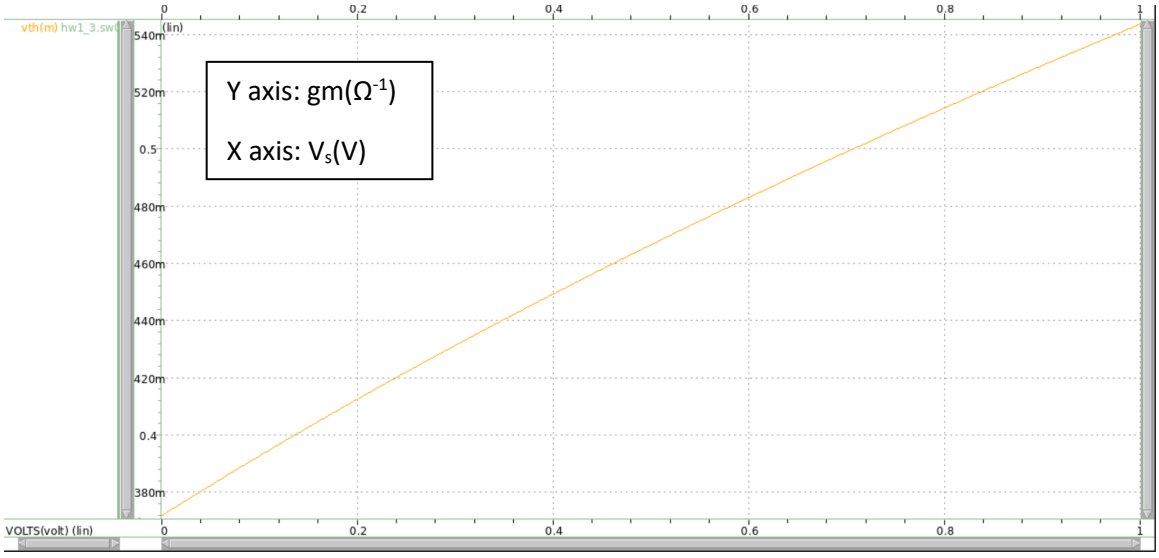
      $$V_{th} = V_{th0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|})$$

      When V_s increases, V_{SB} increases, so V_{th} will increase.

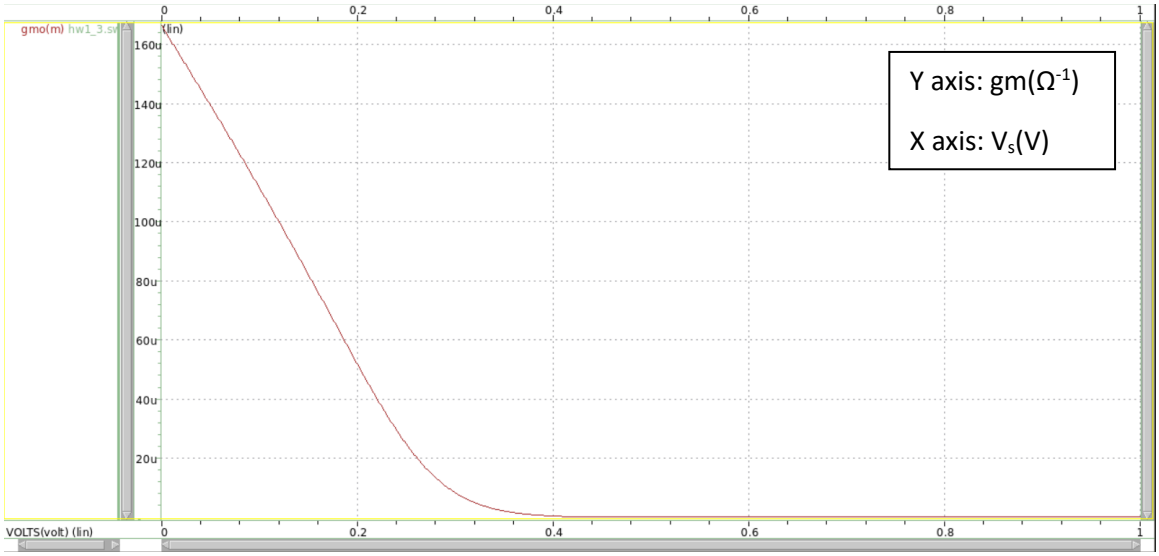
    - Also, Vgs = V_g (0.7v) – V_s deceases, so V_{gs} will be closer to V_{th}. When V_{gs} is not larger than Vth, the MOSFET turn off, so there will be no drain current. Also, since $g_m = \sqrt{2u_n C_{ox}\frac{W}{L}I_D}$, so $g_m \propto I_D$, gm will be zero when V_s increases.



drain current(ampere)-source voltage(volt)

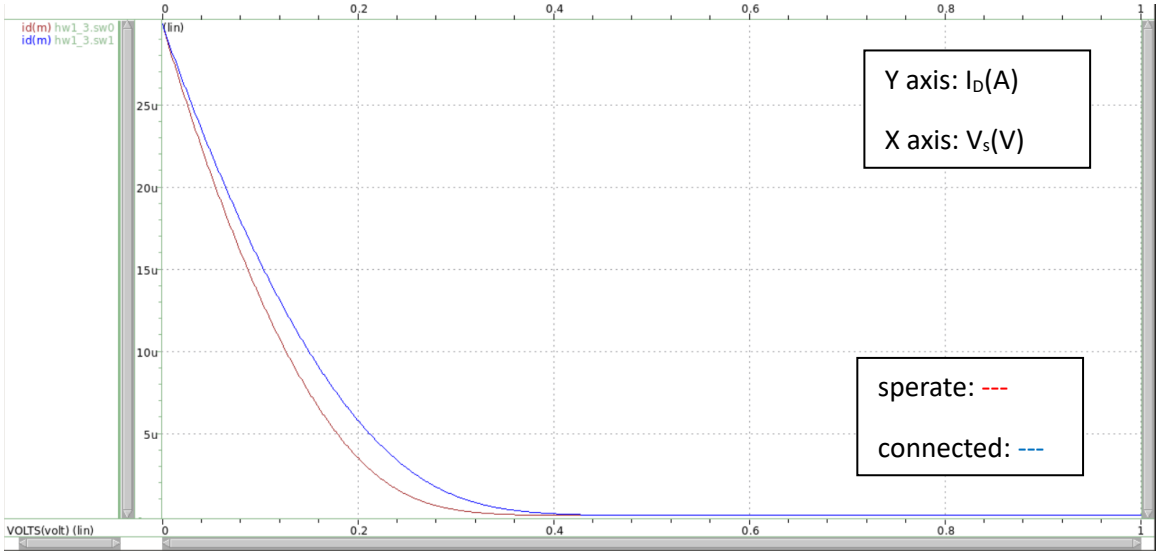


threshold voltage(volt)-source voltage(volt)

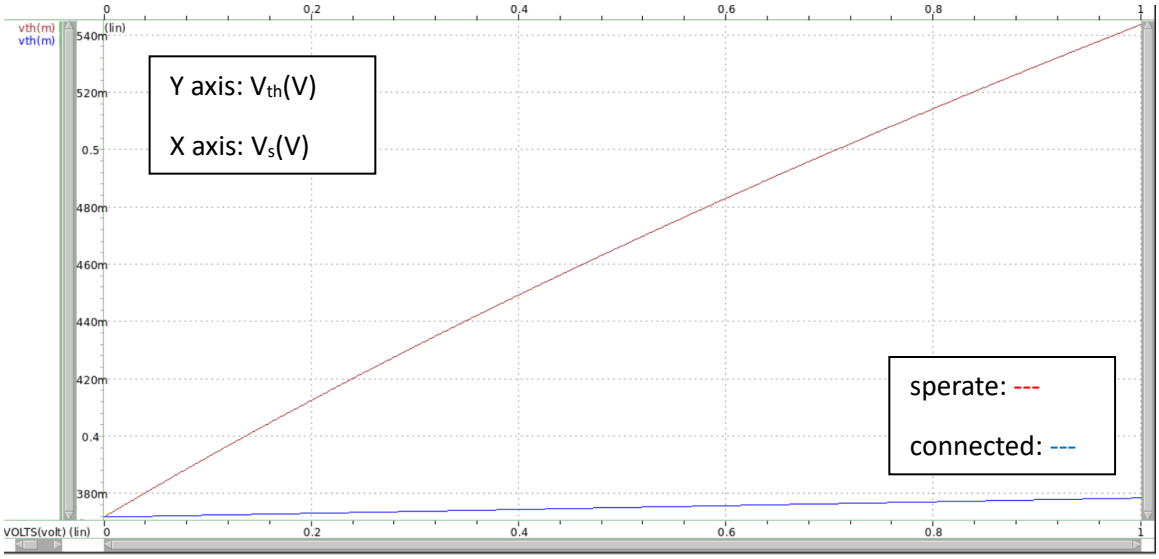


transconductance(siemens)-source voltage(volt)

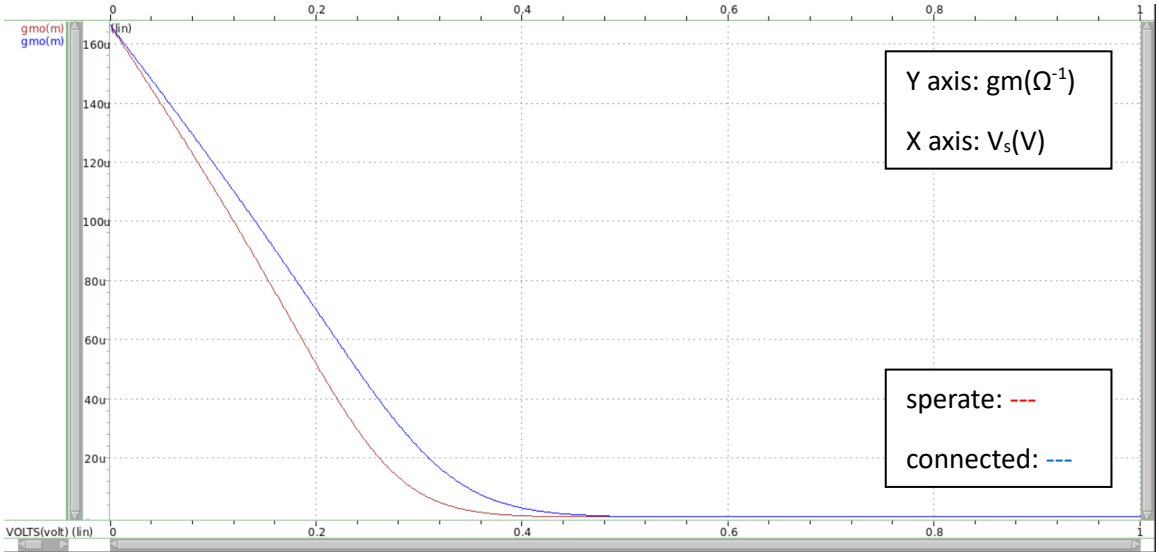
- Observation (red line represents source and body not connected, blue line represents connected): when the source and body are connected, there will not have body effect, so V_{th} will not change, but V_{gs} will also decrease as V_s increase. Therefore, V_{gs} will get close to V_{th} in a lower speed when body and source are connected, so we can see the blue line is higher than red line in the graph of drain current and transconductance.



drain current(ampere)-source voltage(volt)



threshold voltage(volt)-source voltage(volt)



transconductance(siemens)-source voltage(volt)