Analog Integrated Circuit Analysis and Design I

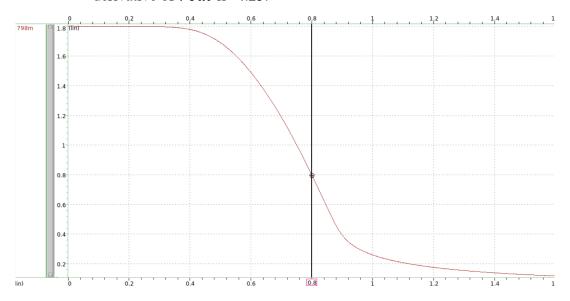
Homework 2

110061217 王彥智

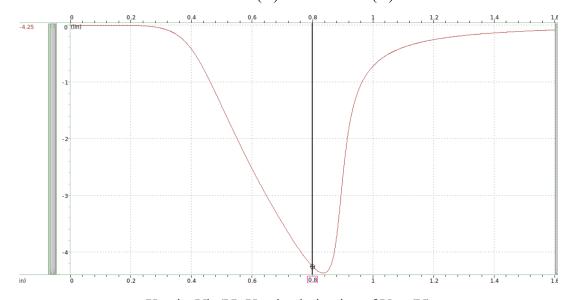
• Part 1

o DC sweep:

We can see when Vin is 0.8V, *Vout* is 0.798V(error: 0.25%) and the derivative of *Vout* is -4.25.



X axis: Vin(V)-Y axis: Vout (V)



X axis: Vin(V)-Y axis: derivative of Vout(V)

o TF analysis

The following table is the TF analysis result, we can see Av is -4.2563 when Vin is 0.8V. We can compare the result of DC sweep and TF analysis. In DC sweep, the meaning $\frac{\partial Vout}{\partial Vin}$ is "how Vout change when Vin change a little bit." In TF analysis, we give some AC small signal on the DC operating point to see the output change. Therefore, the result of two analyses are basically the same, since the meaning of two operation are the same.

Vin(V)	$Rin(\Omega)$	$\operatorname{Rout}(\Omega)$	Av(V/V)
797.0000m	1.000e+20	43.8850k	-4.2394
798.0000m 799.0000m	1.000e+20 1.000e+20	43.8627k 43.8400k	-4.2451 -4.2507
800.0000m	1.000e+20	43.8168k	-4.2563
801.0000m 802.0000m	1.000e+20 1.000e+20	43.7931k 43.7689k	-4.2617 -4.2671
803.0000m	1.000e+20	43.7442k	-4.2724

TF Analysis

Hand Calculation and Discussion

```
**info** dc convergence successful at Newton-Raphson method 1****** PrimeSim HSPICE -- R-2020.12-SP2 linux64 (May 24 2021 7074677) ******
 ** 110061217 hw2 part1
 ****** operating point information thom= 25.000 temp= 25.000 ******
 ****** operating point status is all simulation time is node =voltage node =voltage node =voltage
              = 1.8000 0:vin
                                      = 800.0000m 0:vout
                                                                    = 798.3265m
 +0:vdd
 **** voltage sources
 element O:vin
  volts 800.0000m 1.8000
current 0. -21.3122u
0. 38.3620u
                       0:vdd
      total voltage source power dissipation= 38.3620u
                                                                           watts
 **** resistors
 subckt
 element 0:rd
  r value 47.0000k
              1.0017
21.3122u
21.3479u
  v drop
  current
  power
```

Operating point

subckt element 0:mn 0:n_18.1 mode1 Saturation 21.3122u -6.353e-21 region ibs -114.4098a i bd 800.0000m 798.3265m vgs vds vbs 398.5086m vth . 332.9477m vdsat 401.4914m vod 308.1817u beta 507.4472m 97.1615u gam eff 1.5461u 18.3993u gmb cdtot cgtot cstot 7.8613f 3.8609f cbtot 6.0654f 358.0754a cgs cgd

NMOS

Working item	SPEC	Your Design	Hand Calculation
V_{DD}	1.8V	1.8V	1.8V
$V_{in,DC}$	0.8V	0.8V	0.8V
$V_{out,DC}$	0.8V	798.3265mV	798.3266V
Gain A _V	>3.2(V/V)	4.2563(V/V)	4.2572(V/V)
R_D	<90k Ω	47k Ω	
I_D	<30uA	21.3122uA	
$M_b W/L$		1um/1um	

COMMON SOURCE PERFORMANCE TABLE

$$V_{out} = V_{DD} - I_d * R_D = 1.8 - 21.3122uA * 47k\Omega = 0.7983266V$$

$$Error = \frac{(0.7983265 - 0.7983266)}{0.7983266} * 100\% = -1.252 * 10^{(-3)}\%$$

$$A_V = \frac{\partial Vout}{\partial Vin} = -g_m R_D = -97.1615u \left(\frac{1}{\Omega}\right) * 47k\Omega = -4.5665(V/V)$$

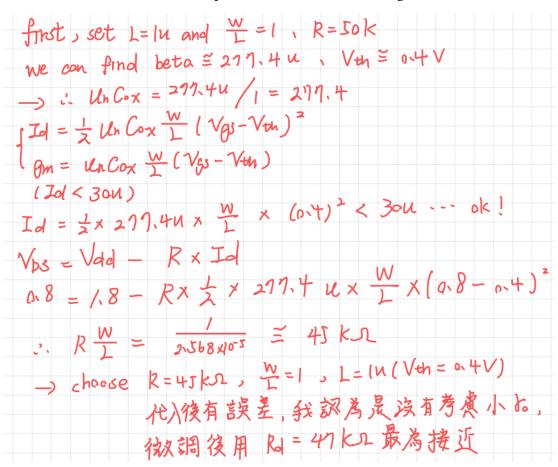
$$Error = \frac{(4.2563 - 4.5665)}{4.5665} * 100\% = -7.28\%$$

$$R_{out} = (R_D \parallel \frac{1}{g_{ds}}) = (47K \parallel 646788.6941) = \frac{43816.0334\Omega}{43.8160}$$

$$Error = (43.8168 - 43.8160) / 43.8160 * 100\% = 0.0017\%$$

Discussion

How I design the amplifier? First, I choose L = 1um, since it should not be too small, or it will have short-channel effect. Also, I don't want L to be too large, or it will waste the space of circuit. Second, I use a random W, L and R_D value to run hspice, I can get beta value($\frac{beta}{W/L} = u_n C_{ox}$), and Vth value. Third, I use W/L = 1, since $I_D = \frac{\frac{1}{2}\mu_n C_{ox}W}{L(V_{in}-V_{th})^2} < 30uA$. Then, I use $R_D = 50$ k Ω to run hspice, and use $Id = \frac{1}{2} * \frac{u_n C_{ox}W}{L} * (V_{gs} - V_{th})$ and $V_{out} = V_{DD} - I_d * R_D$ to find correct R_D . Finally, use new R_D to run hspice again, since I don't consider r_o , there will be some error, so I adjust it a little bit. The final R_D is 47k Ω .



My calculation for design

• Why the hand calculation of A_V is different from the result?

I use the following formula to calculate the result:

$$V_{out} = V_{DD} - I_d * R_D = V_{DD} - \frac{1}{2} * u_n C_{ox} \frac{W}{L} * (V_{in} - V_{th})^2 * R_D$$

$$\rightarrow \frac{\partial Vout}{\partial Vin} = -u_n C_{ox} \frac{W}{L} * (V_{in} - V_{th}) * R_D$$

And, when in saturation, $g_m = u_n C_{ox} \frac{W}{L} (Vin - Vth)$

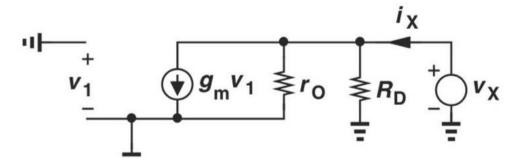
So,
$$A_V = \frac{\partial Vout}{\partial Vin} = -g_m R_D = -97.1615u \left(\frac{1}{\Omega}\right) * 47k\Omega = -4.5665$$

However, by using small signal analysis, we should consider channel-length modulation effect, and by the following small signal module:

$$A_V = -gm * R_{out} = -gm * (R_D \parallel r_o)$$

= -97.1615 u $\left(\frac{1}{\Omega}\right) \times 43.8168$ k $\Omega = \frac{V}{V}$

Error can be reduce to $\frac{(4.2563 - 4.2572)}{4.2572} * 100\% = -0.0211\%$

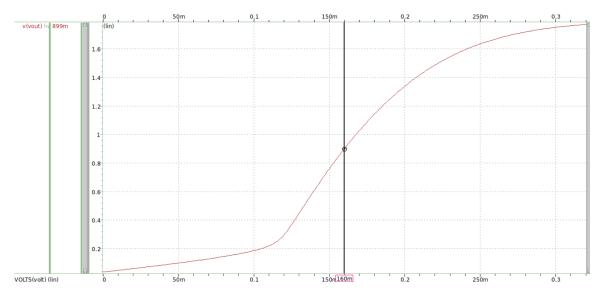


Small signal Model of Common Source Amplifier

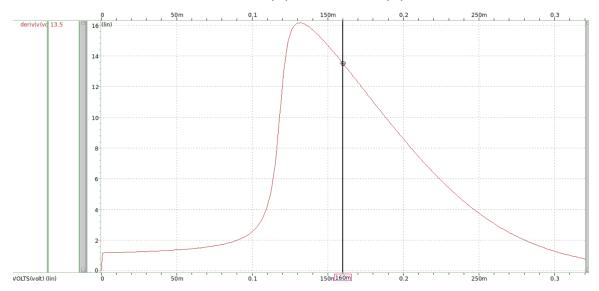
• Part 2

o DC sweep

We can see when Vin is 0.16V, *Vout* is 0.899V(error: 0.11%) and the derivative of *Vout* is 13.5.



X axis: Vin(V)-Y axis: Vout (V)



X axis: Vin(V)-Y axis: derivative of *Vout* (V)

o TF analysis

The following table is the TF analysis result, we can see Av is 13.4464 when Vin is 0.16V. Comparing the result of DC sweep and TF analysis, we can see the result of two analyses are basically the same.

Vin(V)	$Rin(\Omega)$	$\operatorname{Rout}(\Omega)$	Av(V/V)
155.0000m	5.1964k	61.9412k	14.0483
156.0000m	5.2408k	62.0637k	13.9293
157.0000m	5.2862k	62.1844k	13.8095
158.0000m	5.3327k	62.3034k	13.6891
159.0000m	5.3803k	62.4209k	13.5680
160.0000m	5.4290k	62.5370k	13.4464
161.0000m	5.4787k	62.6518k	13.3242
162.0000m	5.5296k	62.7654k	13.2016
163.0000m	5.5817k	62.8779k	13.0786
164.0000m	5.6348k	62.9893k	12.9552
_165.0000m	5.6892k	63.0998k	12.8314

TF Analysis

Hand Calculation

```
**info** dc convergence successful at Newton-Raphson method 1****** PrimeSim HSPICE -- R-2020.12-SP2 linux64 (May 24 2021 7074677) ******
 ** 110061217 hw2 part2
 ****** operating point information tnom= 25.000 temp= 25.000 ******

****** operating point status is all simulation time is 0.

node =voltage node =voltage node =voltage
                      = 600.0000m 0:vdd
= 899.3692m
                                                                 = 1.8000 0:vin
 +0:vb
                                                                                                                     = 160.0000m
 +0:vout
 **** voltage sources
  subckt

        SUDCKI

        element
        0:vin
        0:vb
        0:vaa

        volts
        160.0000m
        600.0000m
        1.8000

        current
        12.3374u
        0.
        -12.3374u

        power
        -1.9740u
        0.
        22.2073u

          total voltage source power dissipation= 20.2333u
                                                                                                                                  watts
  **** resistors
  subckt
 element 0:rd
r value 73.0000k
v drop 900.6308m
current 12.3374u
   power
                       11.1115u
```

Operating point

subckt 0:mn element 0:n_18.1 mode1 Saturation ibs i bd 440.0000m vds vth vdsat 56.0176m vod beta gam eff 507.4460m 212.7323u 2.2920u 43.5106u 15.8434f gm gds gmb cdtot cstot cbtot cgs cgd

NMOS

Working item	SPEC	Your Design	Hand Calculation
V_{DD}	1.8V	1.8V	1.8V
$V_{in,DC}$	0.16V	0.16V	0.16V
$V_{out,DC}$	0.9V	899.3692mV	899.3698mV
Gain A _V	>10(V/V)	13.4464(V/V)	13.448 (V/V)
R_D	<90k Ω	73k Ω	
I_D	<30uA	13.3374uA	
V_b		0.6V	
$M_b W/L$		12um/1um	

COMMON GATE PERFORMANCE TABLE

$$V_{out} = V_{DD} - I_d * R_D = 1.8 - 12.3374uA * 73k\Omega = 0.8993698V$$

$$Error = \frac{899.3692 - 899.3698}{899.3698} * 100\% = -6.67 * 10^{(-4)}\%$$

$$A_V = \frac{\partial Vout}{\partial Vin} = g_m R_D = 212.7323u \left(\frac{1}{\Omega}\right) * 73k\Omega = 15.5294(V/V)$$

$$Error = \frac{13.4464 - 15.5294}{15.5294} * 100\% = -13.41\%$$

$$R_{out} = (R_D \parallel \frac{1}{g_{ds}}) = (73K \parallel 436300.1745) = 62536.622\Omega$$

$$Error = \frac{(62537 - 62536.622)}{62536.622} * 100\% = 2.5 * 10^{(-8)}\%$$

$$R_{in} = \frac{R_D + \frac{1}{g_{ds}}}{g_m ro + 1} = \frac{73000 + 436300}{212.7323u * 436300 + 1} = \frac{5428.7630}{5428.763}$$

$$Error = \frac{(5429 - 5428.763)}{5428.763} * 100\% = 0.00435\%$$

o Discussion

How I design the amplifier? First, I choose L = 1um, since it should not be too small, or it will have short-channel effect. Also, I don't want L to be too large, or it will waste the space of circuit. Second, I use a random W, L and R_D value to run hspice, I can get beta value($\frac{beta}{W/L} = u_n C_{ox}$), and Vth value. Third, to let NMOS operated in saturation region, $V_b > V_{th} + V_{in} \approx 0.56V$, I use $V_b = 0.6V$ to bias the NMOS. Third, since $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{th})^2 = \frac{1}{2} 400 \frac{W}{L} (0.04)^2 < 30uA$, and the required gain is large, so I use W/L = 12. Then, I use random R_D to run hspice, and use $Id = \frac{1}{2} * \frac{u_n C_{ox} W}{L} * (V_{gs} - V_{th})$ and $V_{out} = V_{DD} - I_d * R_D$ to find correct R_D . Finally, use new R_D to run hspice again, since I don't consider r_o , there will be some error, so I adjust

*I connect the source and body here since I don't want to have body effect.

*I choose $V_b = 0.6v$ since I don't want NMOS enter subthreshold region. Also, leg room can be lower(more space to operate).

• Why the hand calculation of A_V is different from the result?

I use the following formula to calculate the result:

$$V_{out} = V_{DD} - I_d * R_D = V_{DD} - \frac{1}{2} * u_n C_{ox} \frac{W}{L} * (V_b - V_{in} - V_{th})^2 * R_D$$

$$\to \frac{\partial Vout}{\partial Vin} = -u_n C_{ox} \frac{W}{L} * (V_b - V_{in} - V_{th}) * R_D$$

it a little bit. The final R_D is 73k Ω .

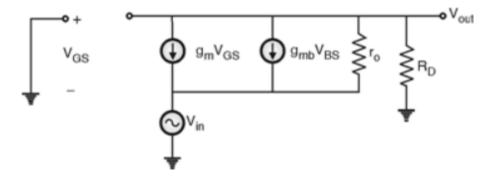
And, when in saturation, $g_m = u_n C_{ox} \frac{W}{L} (V_b - Vin - Vth)$

So,
$$A_V = \frac{\partial Vout}{\partial Vin} = g_m R_D = 212.7323u \left(\frac{1}{\Omega}\right) * 73k\Omega = 15.5294$$

However, by using small signal analysis, we should consider channel-length modulation effect and Rin (neglect g_{mb} here, since I connect body and source so V_{bs} is 0 here). By the following small signal module:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{1 + g_m r_o}{R_{in}(1 + g_m r_o)} * R_D = \frac{13.448(\text{V/V})}{12.448(\text{V/V})}$$

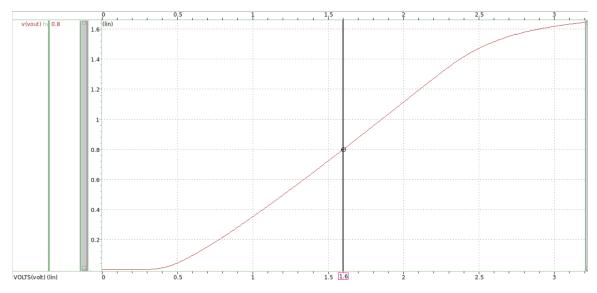
Error can be reduce to
$$\frac{(13.4464 - 13.448)}{13.448} * 100\% = -6.5 * 10^{(-5)}\%$$



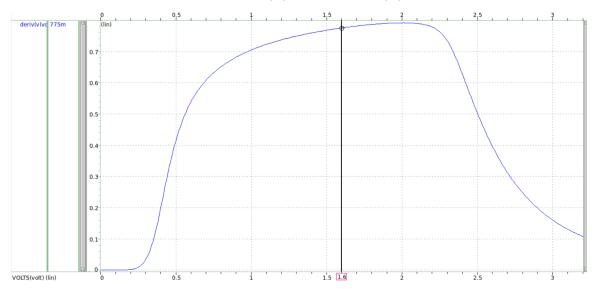
Small signal Model of Common Gate Amplifier

• Part 3

DC sweep We can see when Vin is 1.6V, Vout is 0.8V(error: almost 0%) and the derivative of Vout is 0.775.



X axis: Vin(V)-Y axis: Vout (V)



X axis: Vin(V)-Y axis: derivative of *Vout* (V)

TF analysis

The following table is the TF analysis result, we can see Av is 0.7757681 when Vin is 1.6V. Comparing the result of DC sweep and TF analysis, we can see the result of two analyses are basically the same.

Vin(V)	$Rin(\Omega)$	$\operatorname{Rout}(\Omega)$	Av(V/V)
1.5500	1.000e+20	8.0436k	772.2784m
1.5600	1.000e+20	8.0144k	772.9999m
1.5700	1.000e+20	7.9855k	773.7096m
1.5800	1.000e+20	7.9570k	774.4074m
1.5900	1.000e+20	7.9289k	775.0936m
1.6000	1.000e+20	7.9011k	775.7681m
1.6100	1.000e+20	7.8737k	776.4311m
1.6200	1.000e+20	7.8466k	777.0826m
1.6300	1.000e+20	7.8198k	777.7226m
1.6400	1.000e+20	7.7934k	778.3513m
1.6500	1.000e+20	7.7673k	778.9685m

TF Analysis

Hand Calculation

```
***info** dc convergence successful at Newton-Raphson method

1****** PrimeSim HSPICE -- R-2020.12-SP2 linux64 (May 24 2021 7074677) *****

*** 110061217 hw2 part3

****** operating point information tnom= 25.000 temp= 25.000 *****

****** operating point status is all simulation time is 0.

node =voltage node =voltage node =voltage

+0:vdd = 1.8000 0:vin = 1.6000 0:vout = 799.8416m

***** voltage sources

subckt element 0:vin 0:vdd volts 1.6000 1.8000 current 0. -21.6173u power 0. 38.9112u

total voltage source power dissipation= 38.9112u watts

***** resistors

subckt element 0:rs r value 37.0000k v drop 799.8416m current 21.6173u power 17.2905u
```

Operating point

**** mosfets

subckt element model region id ibs ibd vgs vds vbs vth vdsat vod beta gam eff gm gds gmb cdtot cgtot cstot cbtot cgs	0:mn 0:n_18.1 Saturation 21.6173u -6.444e-21 -143.3363a 800.1584m 1.0002 0. 396.9768m 334.1528m 403.1816m 308.2048u 507.4472m 98.2088u 1.3530u 18.4990u 1.3716f 6.8796f 7.8579f 3.8176f 6.0601f
cgd	355.4636a

NMOS

Working item	SPEC	Your Design	Hand Calculation
V_{DD}	1.8V	1.8V	1.8V
$V_{in,DC}$	1.6V	1.6V	1.6V
$V_{out,DC}$	0.8V	799.8416mV	799.8401mV
Gain A _V	>0.75(V/V)	775.7681m(V/V)	784.1909m(V/V)
$R_{\scriptscriptstyle S}$	<90k Ω	37k Ω	
I_D	<30uA	13.3374uA	_
$M_b W/L$		1um/1um	

SOURCE FOLLOWER PERFORMANCE TABLE

$$V_{out} = I_d * R_s = 21.6173uA * 37k\Omega = 0.7998401V$$

$$Error = \frac{(799.8416 - 799.8401)}{799.8401} * 100\% = 1.8753 * 10^{(-4)}\%$$

$$A_V = \frac{\partial Vout}{\partial Vin} = \frac{g_m R_S}{1 + g_m R_S} = \frac{37K\Omega}{1 + 98.2088u * 37K\Omega} = 0.7984935(V/V)$$

$$Error = \frac{(799.8416 - 798.4935)}{798.4935} * 100\% = 0.16\%$$

$$R_{out} = \frac{1}{g_m} ||R_S| = \frac{1}{98.2088u + \frac{1}{37k}} = 8386.741\Omega$$

$$Error = \frac{(7901 - 8386.741)}{8386.741} * 100\% = -6.1384\%$$

Discussion

• How I design the amplifier?

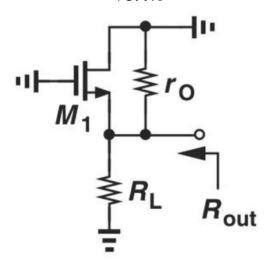
First, I choose L = 1um, since it should not be too small, or it will have short-channel effect. Also, I don't want L to be too large, or it will waste the space of circuit. Second, I use a random W, L and R_D value to run hspice, I can get beta value $(\frac{beta}{W/L} = u_n C_{ox})$, and Vth value. Third, since $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{th})^2 < 30uA$, and the required gain is not large, so I use W/L = 1. Then, I use random R_D to run hspice, and use $Id = \frac{1}{2} * \frac{u_n C_{ox} W}{L} * (V_{gs} - V_{th})$ and $V_{out} = I_d * R_s$ to find correct R_s . Finally, use new R_s to run hspice again, since I don't consider r_o , there will be some error, so I adjust it a little bit. The final R_D is 37k Ω .

*I connect the body and source here since I don't want to have body effect.

• Why the hand calculation of R_{out} is different from the result? We should also consider R_s in the circuit(channel length modulation), so by the following circuit which is in the course materials:

$$R_{out} = \frac{1}{g_m} || r_o || R_s = \frac{1}{\frac{1}{982088u} + \frac{1}{13530u} + \frac{1}{37000}} = 7899.40$$

Error can be reduce to
$$\frac{(7901 - 7899.4)}{7899.4} * 100\% = 0.0205\%$$



Source follower output impedance