EE3230 VLSI Design HW #3 report

110061217 王彥智

1. Please design an inverter chain with either even or odd number of inverters with the following conditions:
   - V_{DD} = 1.8V
   - The size of the first inverter is fixed. $(W/L)_N$ = 1u/0.18um, and $(W/L)_P$ = 1u/0.18um
   - The inverter chain drives a capacitor load of 20 pF.
   - The rise and fall time of the input is 2 ns, and the frequency is 50 MHz.

   a. Perform hand analysis and estimate the prQopagation delay vs. the number of stages n with n = 1~10. (Of course, for each n, you'd carefully resize the inverters.)

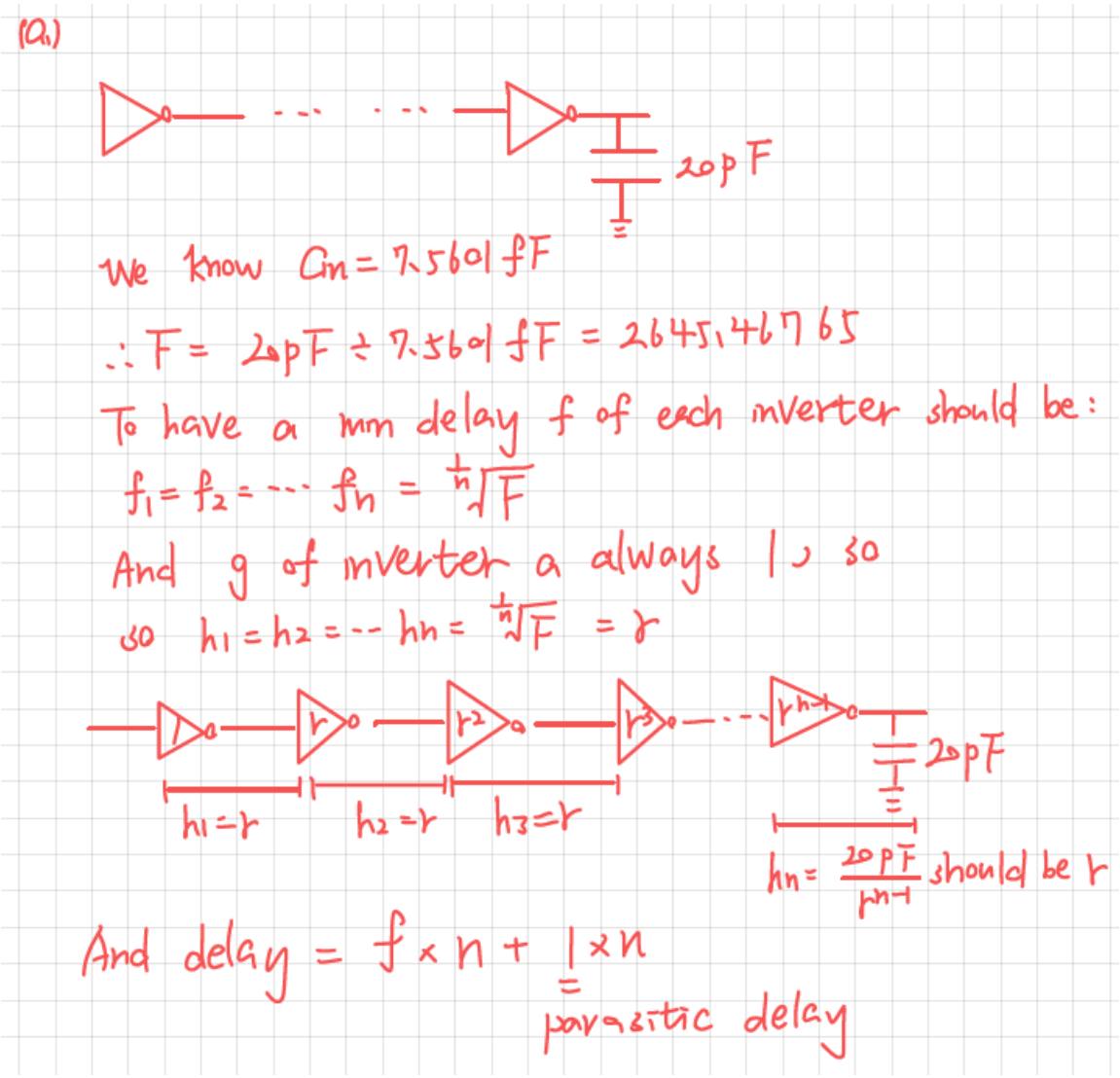
   Step1. Measure Cin and Cout of the first inverter.

subckt		
element	0:mnt0	0:mpt0
model	0:n_18.1	0:p_18.1
region	Saturation	Saturation
id	130.2454u	-130.2454u
ibs	-3.883e-20	1.582e-20
ibd	-111.7678a	178.6348a
vgs	900.0000m	-900.0000m
vds	780.1185m	-1.0199
vbs	0.	0.
vth	493.4697m	-531.4272m
vdsat	283.0096m	-376.0720m
vod	406.5303m	-368.5728m
beta	1.9554m	1.6895m
gam eff	507.4535m	557.0840m
gm	451.3344u	515.8957u
gds	29.8971u	26.6596u
gmb	61.2200u	163.6610u
cdtot	1.4167f	3.3680f
cgtot	1.8600f	5.7006f
cstot	2.7766f	8.1662f
cbtot	2.6279f	6.6821f
cgs	1.3337f	4.2776f
cgd	360.8722a	1.0609f

Cin = 1.86fF+5.7006fF = 7.5601fF

Cout = 1.4167fF + 3.368fF = 4.7847fF

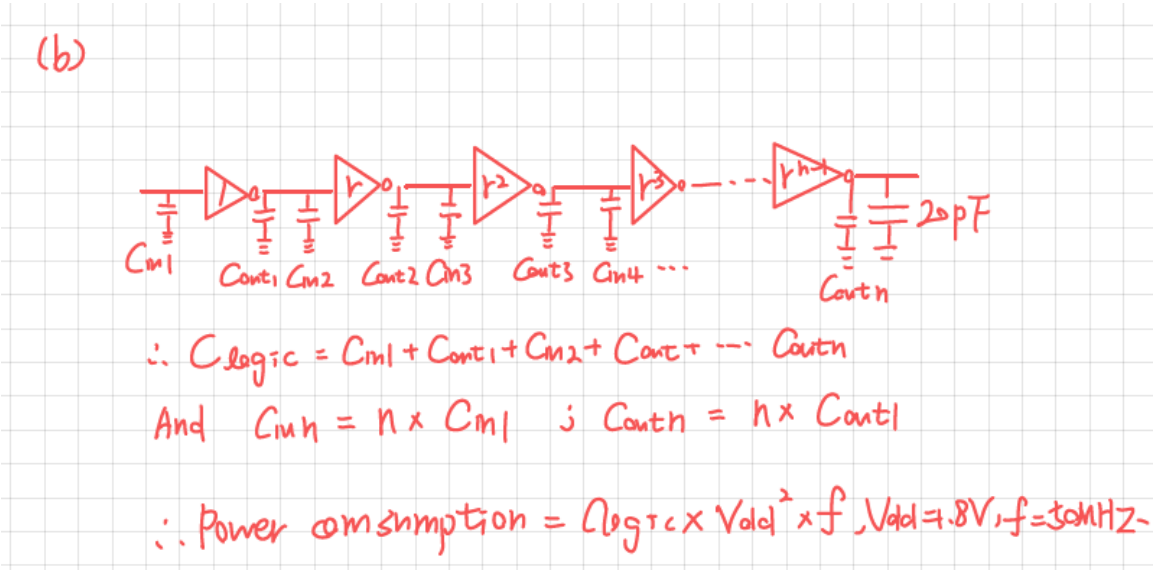
Step2. Derive the equation of delay.



Step3. Calculate the estimated delay.

n	F = Cout/Cin	f = F^(1/n) = 2645.45765^(1/n) = gh	D = n*f + n*1
1	2645.46765	2645.467653	2646.467653
2	2645.46765	51.43410982	104.8682196
3	2645.46765	13.83038124	44.49114373
4	2645.46765	7.171757791	32.68703116
5	2645.46765	4.836158112	29.18079056
6	2645.46765	3.718922054	28.31353232
7	2645.46765	3.082683389	28.57878372
8	2645.46765	2.678013777	29.42411022
9	2645.46765	2.400369228	30.60332305
10	2645.46765	2.19912667	31.9912667

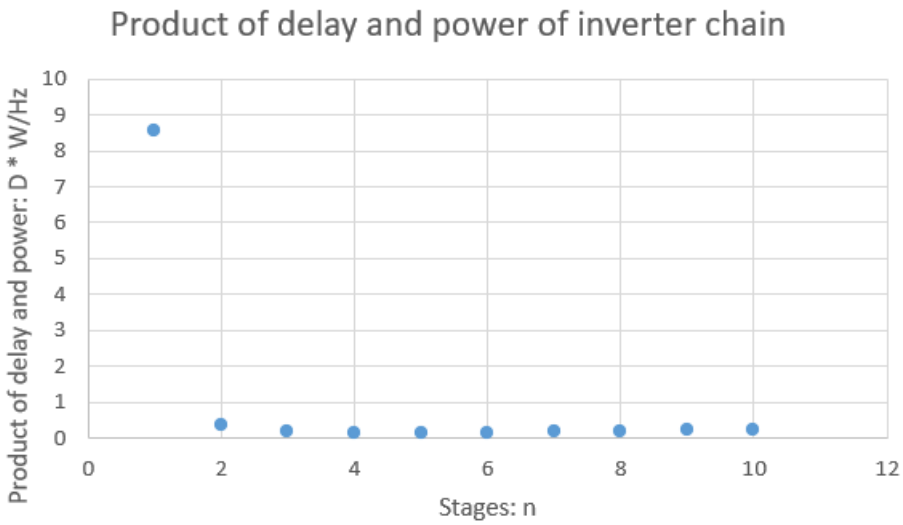
b. Perform hand analysis and estimate the power consumption vs. the number of stages n with n = 1~10. (Of course, for each n, you'd carefully resize the inverters.)
Step1. Derive the equation of power consumption.

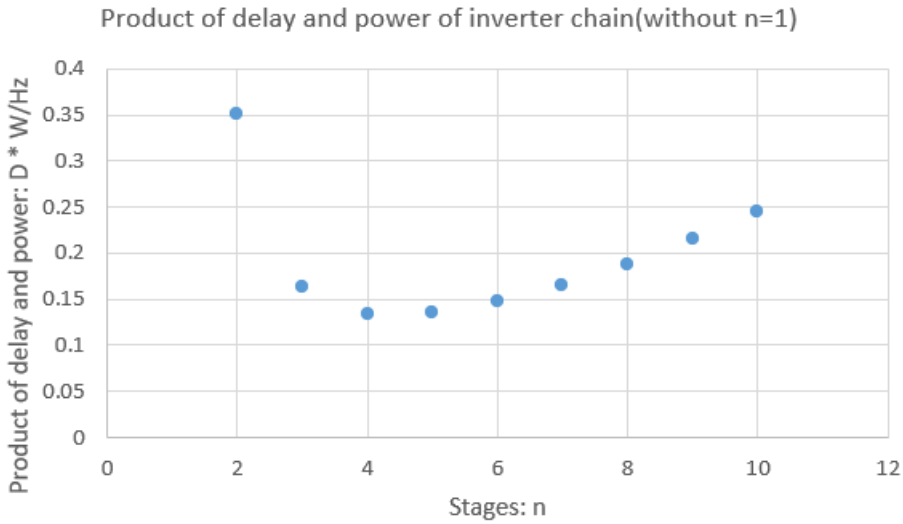


Step2. Calculate the estimated power consumption.

n	Clogic(fF)	power comsuption(W/Hz) = C * V^2*f
1	20012.34	0.003242
2	20647.29	0.003344861
3	22544.38	0.00365219
4	25289.49	0.004096897
5	28509.93	0.004618608
6	32006.75	0.005185094
7	35674.69	0.0057793
8	39454.8	0.006391678
9	43312.01	0.007016546
10	47224.33	0.007650342

c. Plot the product of power consumption and propagation delay for each n value vs. n. What is the n number for the minimum 'power-delay product'? Is it larger or smaller than the number of stages that gives the minimum delay? Explain your results clearly.

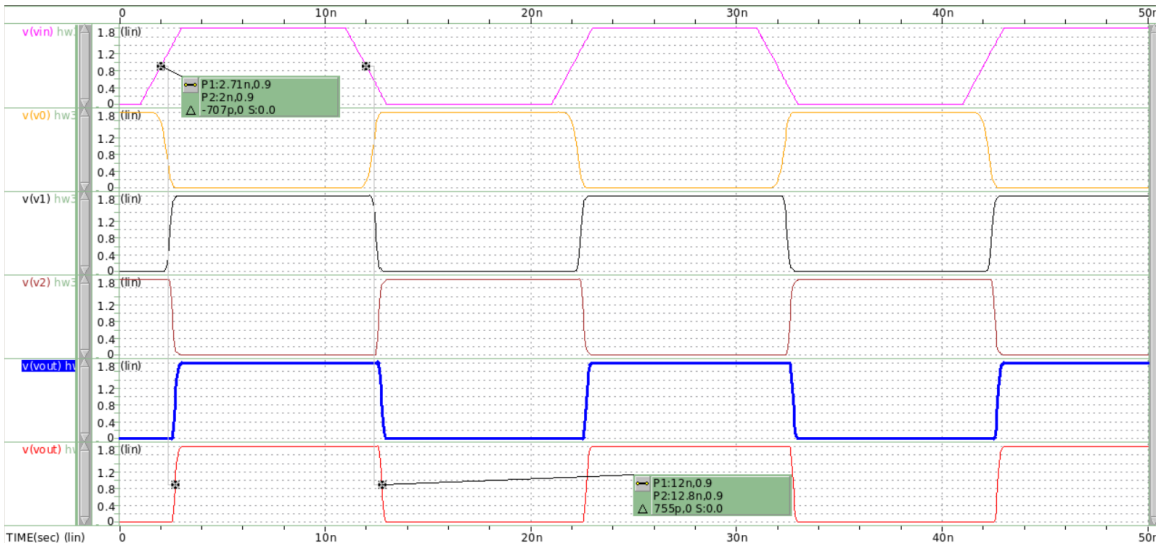




When n is 4, the inverter chain has minimum product of delay and power. It is smaller than the number of stages that gives the minimum delay.

When using 6 inverters, we can have minimum delay, but we use 6 inverters which may consume more power. Therefore, it's a tradeoff that we use 4 inverters only to make the minimum value of the product of power and delay.

d. With n that gives you the minimum 'power-delay product', simulate and plot the waveforms for each node, including the input, for 50 ns. Use one row for each waveform. Label key data points and show the propagation delays for both the rising and falling inputs. What is the difference between the simulation result and the hand calculations in terms of delay? Explain why they are different with reasons as clearly as possible.



waveforms for each node, including the input, for 50 ns

Hand analysis:

Step1. Find the parasitic delay of a unit inverter. I use the following circuit and measure function to measure the delay. (using 3 inverter and measuring the final stage delay make the value more accurate)

```
va va gnd pulse(0 1.8 0 2n 2n 8n 20n)
*va va gnd 0.9
vin vin gnd pulse(0 1.8 0 2n 2n 8n 20n)

mnt0 vb va gnd gnd n_18 l=.18u w=1u m=1
mpt0 vb va vdd vdd p_18 l=.18u w=3u m=1

mnt1 vc vb gnd gnd n_18 l=.18u w=1u m=1
mpt1 vc vb vdd vdd p_18 l=.18u w=3u m=1

mnt2 vd vc gnd gnd n_18 l=.18u w=1u m=1
mpt2 vd vc vdd vdd p_18 l=.18u w=3u m=1
```

circuit

```
.meas tran tpr_par trig v(vc) val='0.9' fall=1 targ v(vd) val='0.9' rise=1
.meas tran tpd_par trig v(vc) val='0.9' rise=1 targ v(vd) val='0.9' fall=1
```

measure function

tpr_par	tpd_par	tpr	tpd
poer_avg	power_0	power_1	power_2
power_3	temper	alter#	
2.012e-11	2.621e-11	7.060e-10	7.544e-10
4.425e-03	1.706e-05	7.800e-05	5.106e-04
3.803e-03	25.0000	1	

measure value

Step2. In (a.) we estimate the delay, and the unit of D is the parasitic delay of a unit inverter, so by multiplying D and measure value, we can get the hand analysis delay.

$$32.6870312 * \frac{(2.012 * 10^{-11} + 2.621 * 10^{-11})}{2} = 7.5719 * 10^{-10}$$

Simulation result:

```
cout vout gnd 20p

mn0 v0 vin gnd gnd n_18 l=.18u w=1u m=1
mp0 v0 vin vdd vdd p_18 l=.18u w=3u m=1

mn1 v1 v0 gnd gnd n_18 l=.18u w=1u m=7
mp1 v1 v0 vdd vdd p_18 l=.18u w=3u m=7

mn2 v2 v1 gnd gnd n_18 l=.18u w=1u m=49
mp2 v2 v1 vdd vdd p_18 l=.18u w=3u m=49

mn3 vout v2 gnd gnd n_18 l=.18u w=1u m=343
mp3 vout v2 vdd vdd p_18 l=.18u w=3u m=343
```

circuit

```
.meas tran tpr trig v(vin) val='0.9' rise=1 targ v(vout) val='0.9' rise=1
.meas tran tpd trig v(vin) val='0.9' fall=1 targ v(vout) val='0.9' fall=1
```

measure function

tpr_par	tpd_par	tpr	tpd
poer_avg	power_0	power_1	power_2
power_3	temper	alter#	
2.012e-11	2.621e-11	7.060e-10	7.544e-10
4.425e-03	1.706e-05	7.800e-05	5.106e-04
3.803e-03	25.0000	1	

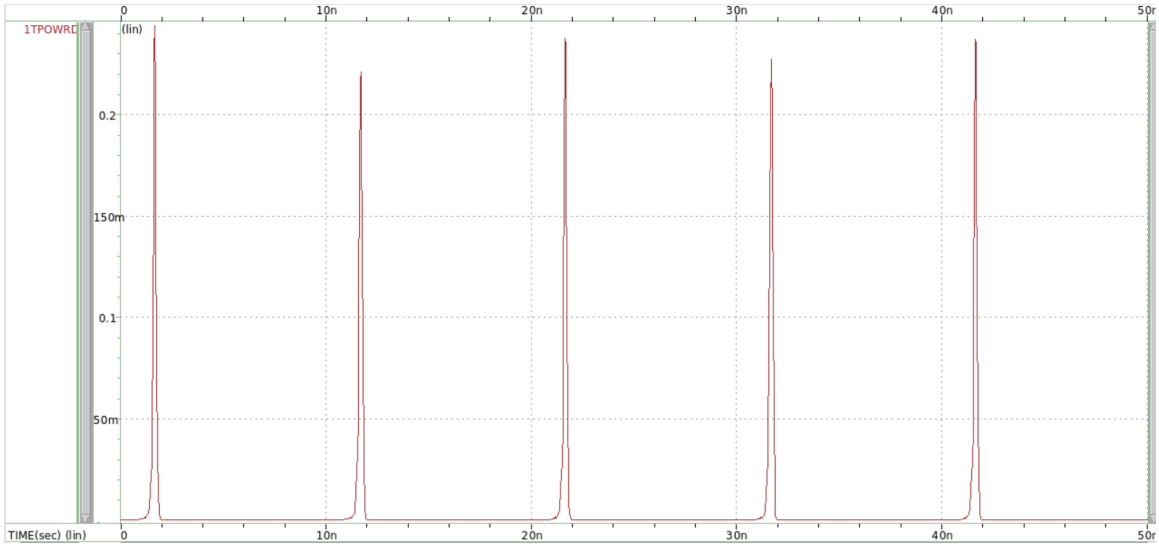
measure value

$$\frac{7.060 * 10^{-10} + 7.544 * 10^{-10}}{2} = 7.302 * 10^{-10}$$

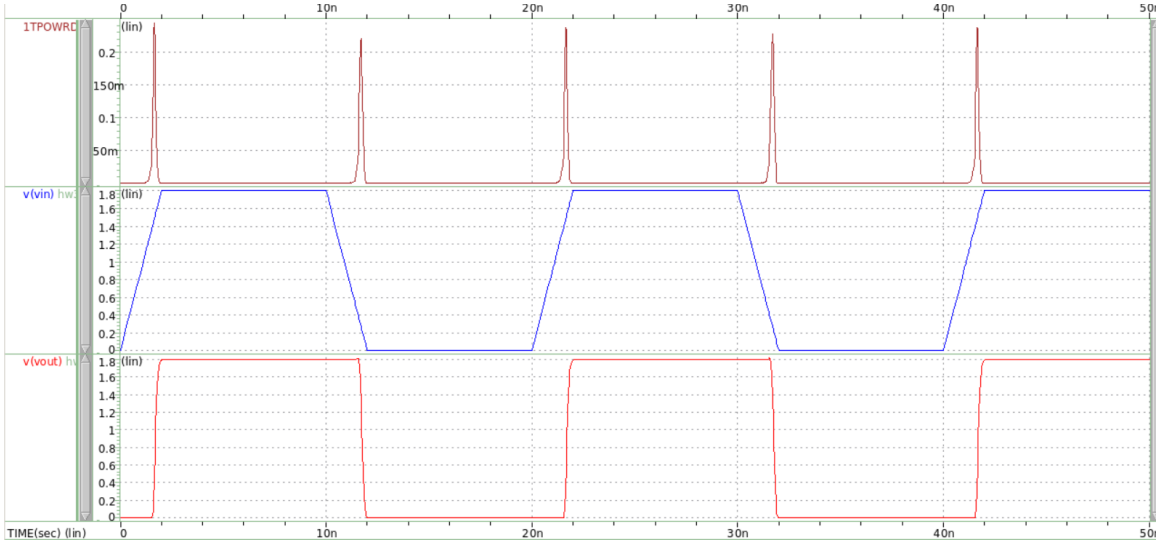
Error: $\frac{7.5719-7.302}{7.302} = 3.68\%$

The simulation result and hand analysis are almost the same.

e. Simulation power consumption vs. time of the inverter chain. Following the previous question, simulate and plot the instant power consumption vs. time of this inverter chain, and measure the average power for the time duration from t=30~50 ns. What is the difference between the simulation result and the hand calculations? Explain why they are different with reasons as clearly as possible.



Power consumption from 0ns to 50ns



Comparing with input and output

tpr_par	tpd_par	tpr	tpd
poer_avg	power_0	power_1	power_2
power_3	temper	alter#	
2.012e-11	2.621e-11	7.060e-10	7.544e-10
4.425e-03	1.706e-05	7.800e-05	5.106e-04

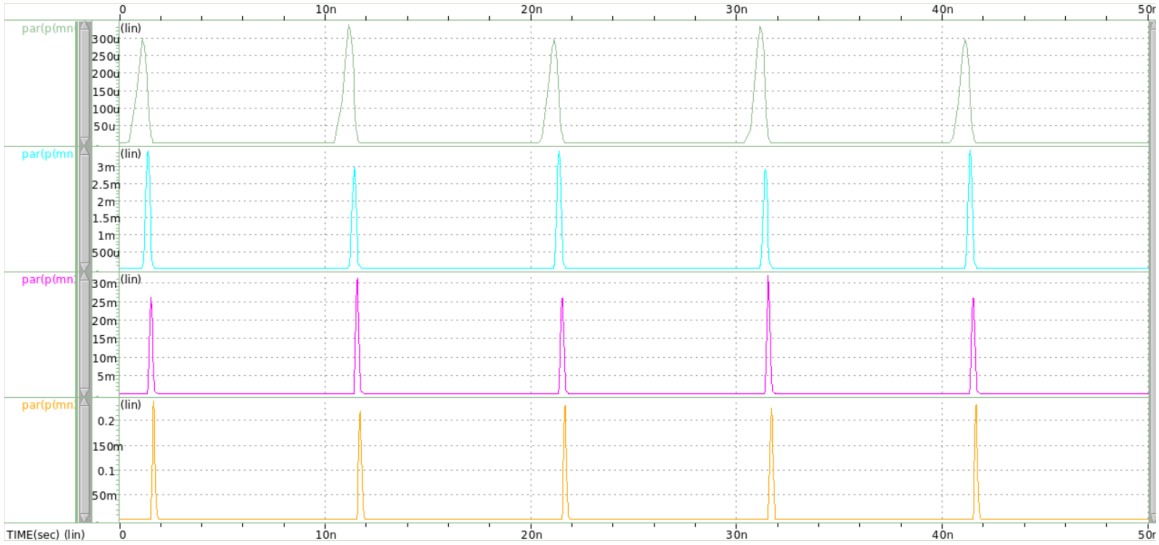
measure value

In (b.) We estimate power consumption 0.004096897W/Hz

$$\text{Error: } \frac{0.004096897-0.004425}{0.004225} = -7.414\%$$

f. For the average power, perform any simulation and/or analysis required to answer the following questions. Provide detailed data and explanations to support your answer.

i. Which stage consumes the most average power?

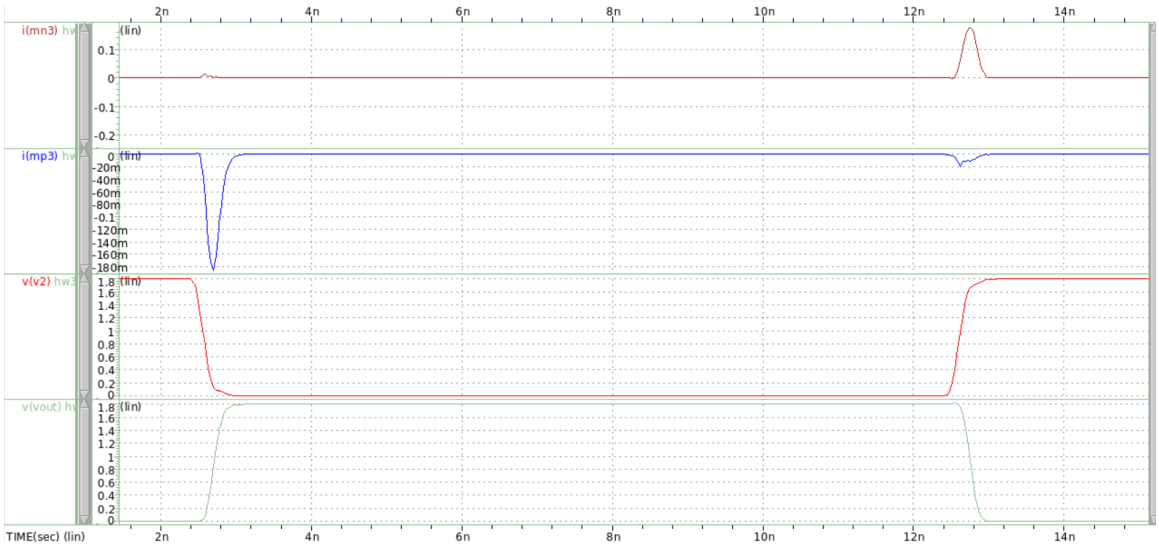


Power consumption in different stage (stage1 to stage4 from above to below)

tpr_par	tpd_par	tpr	tpd
poer_avg	power_0	power_1	power_2
power_3	temper	alter#	
2.012e-11	2.621e-11	7.060e-10	7.544e-10
4.425e-03	1.706e-05	7.800e-05	5.106e-04
3.803e-03	25.0000	1	

Stage4 consumes the most average power(3.803mW) since the size of the PMOS and NMOS is the largest in stage 4.

ii. For this most-power-consuming stage, how much average power is consumed by charging/discharging the output power? How much average power is consumed by short-circuit current? How much average power is consumed by leakage?




```
.meas tran charge integ'(-(v(vdd)-v(vout))*i(mp3))/20n' from=2.2n to=3.2n
.meas tran discharge integ'(v(vout)*i(mn3))/20n' from=12.4n to=13.2n

.meas tran shortcktn integ'((v(vout))*i(mn3))' from=2.2n to 3.2n
.meas tran shortcktp integ'((-v(vdd)+v(vout))*i(mp3))' from=12.4n to=13.2n
.meas tran shortckt_avg param='(shortcktn+shortcktp)/20n'

.meas tran leakage1 integ'-v(vdd)*i(mp3)' from=1n to=2.3n
.meas tran leakage2 integ'v(vdd)*i(mn3)' from=3.2n to=12.4n
.meas tran leakage3 integ'-v(vdd)*i(mp3)' from=13.2n to=21n

.meas tran leakage_avg param='(leakage1+leakage2+leakage3)/20n'
```

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '** 110061217 王彥智 hw3_1'
 tpr_par          tpd_par          tpr              tpd
 poer_avg         power_0          power_1          power_2
 power_3          charge           discharge        shortcktn
 shortcktp        shortckt_avg     leakage1         leakage2
 leakage3         leakage_avg      temper           alter#
  2.084e-11        2.293e-11        7.075e-10        7.547e-10
  4.435e-03        1.678e-05        7.810e-05        5.089e-04
  3.815e-03        1.725e-03        1.858e-03        2.970e-12
  2.013e-12        2.491e-04        3.569e-15        1.431e-15
  8.931e-17        2.545e-07         25.0000         1
```

Charge: 1.725*10^-3

Discharge: 1.858*10^-3

Short circuit current: 2.491*10^-4

Leakage: 2.515*10^-7

2. Repeat Q1, but, this time, replace the inverters with 2-input NAND gates. For the first 2-input NAND gates, design the transistor sizes so that it exhibits the same input capacitance as your first inverter in Q1. (Show data to support your size

choice). Also, set the P/N ratio such that, when the two-inputs are tied together, the input-output transfer function gives VOUT of 0.5 VDD with VIN set to 0.5 VDD. For questions d, e, and f, also compare and explain the difference (with reasons as clear as possible) between this design and the design in Q1.

a. Perform hand analysis and estimate the propagation delay vs. the number of stages n with n = 1~10. (Of course, for each n, you'd carefully resize the inverters.)

   Design the NAND2 size:

   1. Find P/N ratio such that when the two-inputs are tied together, the input-output transfer function gives VOUT of 0.5 VDD with VIN set to 0.5 VDD. Ratio: width of P / width of N = 1.218

```
****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:va      =   0.       0:vb      =   1.8000  0:vc      =  19.3743n
+0:vd      =   1.8000   0:vdd     =   1.8000  0:vm      = 900.0000m
+0:vmo     = 894.2654m  0:vx0     =  65.3158m 0:vx1     =   9.6872n
+0:vx2     =  65.3158m  0:vxm     = 130.6509m
```

   2. Adjust the size such that Cin equal Cin in 1.
      Size: NMOS: 0.87u; PMOS: 0.87u * 1.218 = 1.06u

```
vm vm gnd 0.9

mpma vmo  vm vdd vdd p_18 l=.18u w=.87u  m=1
mpmb vmo  vm vdd vdd p_18 l=.18u w=.87u  m=1
mnma vmo  vm vxm gnd n_18 l=.18u w=1.06u m=1
mnmb vxm  vm gnd gnd n_18 l=.18u w=1.06u m=1
```

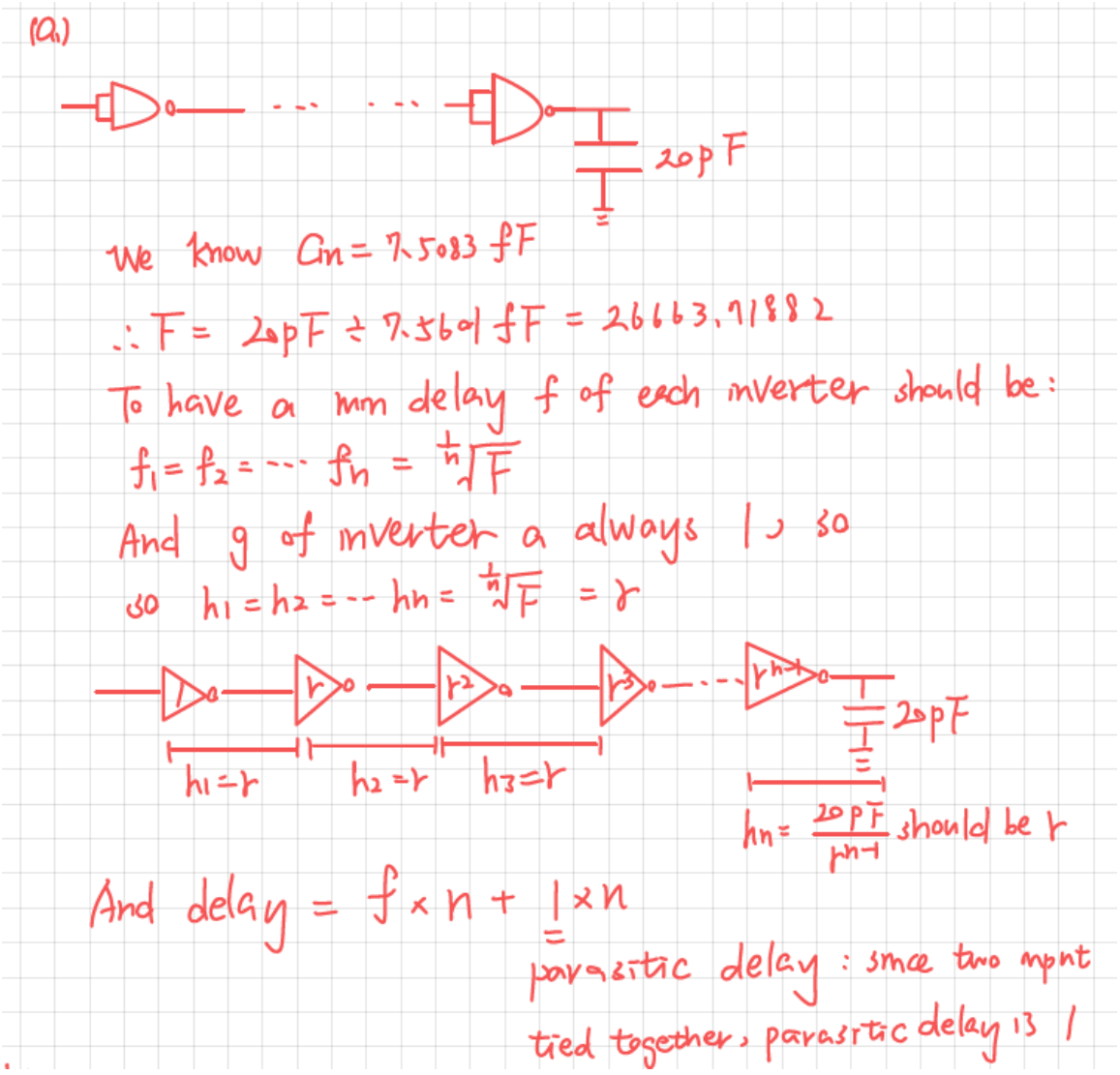
subckt					
element	0:mpma	0:mpmb	0:mnma	0:mnmb	
model	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1	
region	Saturation	Saturation	Saturation	Linear	
id	-35.5893u	-35.5893u	71.1785u	71.1785u	
ibs	6.974e-21	6.974e-21	-19.2983a	-2.061e-20	
ibd	74.2263a	74.2263a	-131.9293a	-19.2571a	
vgs	-900.0000m	-900.0000m	769.3491m	900.0000m	
vds	-905.7346m	-905.7346m	763.6146m	130.6509m	
vbs	0.	0.	-130.6509m	0.	
vth	-527.5612m	-527.5612m	512.7166m	517.7007m	
vdsat	-384.2836m	-384.2836m	223.6423m	274.5441m	
vod	-372.4388m	-372.4388m	256.6325m	382.2993m	
beta	451.9273u	451.9273u	2.1010m	2.0664m	
gam eff	557.0840m	557.0840m	510.9862m	507.4498m	
gm	142.9913u	142.9913u	403.2133u	206.5924u	
gds	8.3569u	8.3569u	21.4810u	376.6266u	
gmb	45.7708u	45.7708u	50.1478u	30.1899u	
cdtot	1.0911f	1.0911f	1.4664f	2.7204f	
cgtot	1.6541f	1.6541f	1.9707f	2.2294f	
cstot	2.4963f	2.4963f	2.8527f	3.0491f	
cbtot	2.1788f	2.1788f	2.6520f	3.0134f	
cgs	1.2424f	1.2424f	1.4234f	1.2744f	
cgd	307.9419a	307.9419a	380.9146a	821.6247a	

Step1. Find Cin and Cout of the first NAND2.

Cin = 1.6541fF+1.6541fF+1.9707fF+2.2294fF = 7.5083fF

Cout = 1.0911fF+1.0911fF+1.4664fF+2.7204fF = 6.3690fF

Step2. Derive the equation of delay.

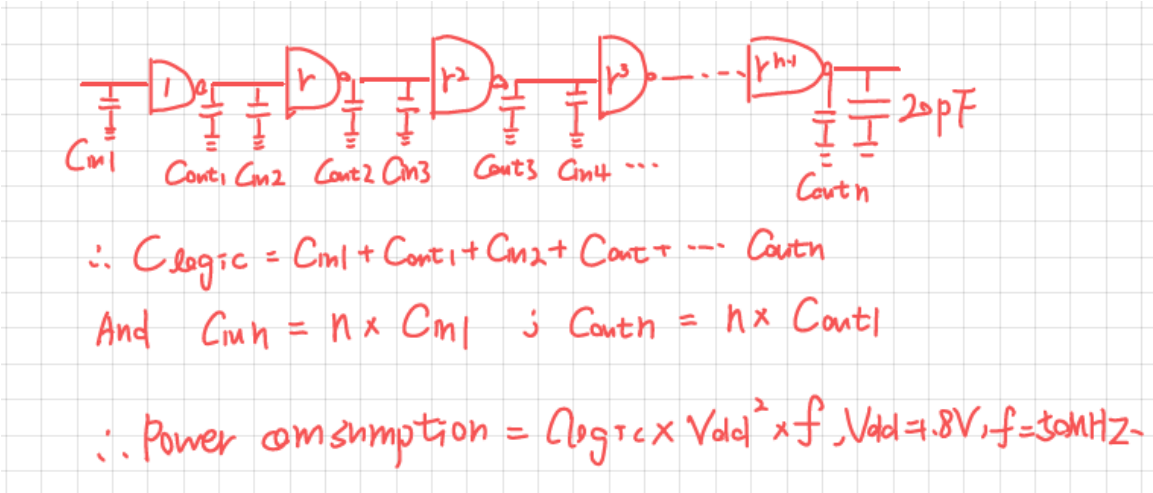


Step3. Calculate the estimated delay.

n		f = F^(1/n) = 2663.71882^(1/n) = gh	D = n*f + n*1
1		2663.718818	2664.71882
2		51.61122763	105.222455
3		13.86211379	44.5863414
4		7.184095464	32.7363819
5		4.842812735	29.2140637
6		3.723185973	28.3391158
7		3.085712663	28.5999886
8		2.680316299	29.4425304
9		2.402203635	30.6198327
10		2.200639165	32.0063917

b. Perform hand analysis and estimate the power consumption vs. the number of stages n with n = 1~10. (Of course, for each n, you'd carefully resize the inverters.)

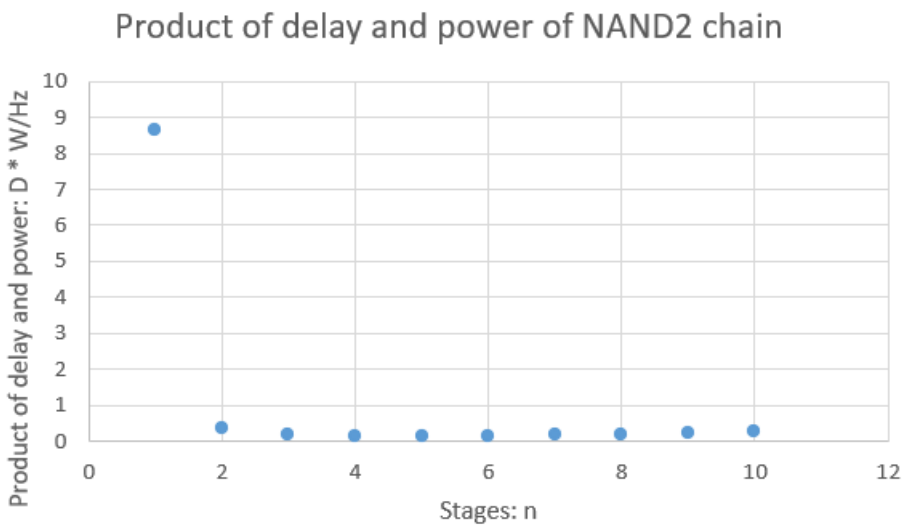
Step1. Derive the equation of power consumption.

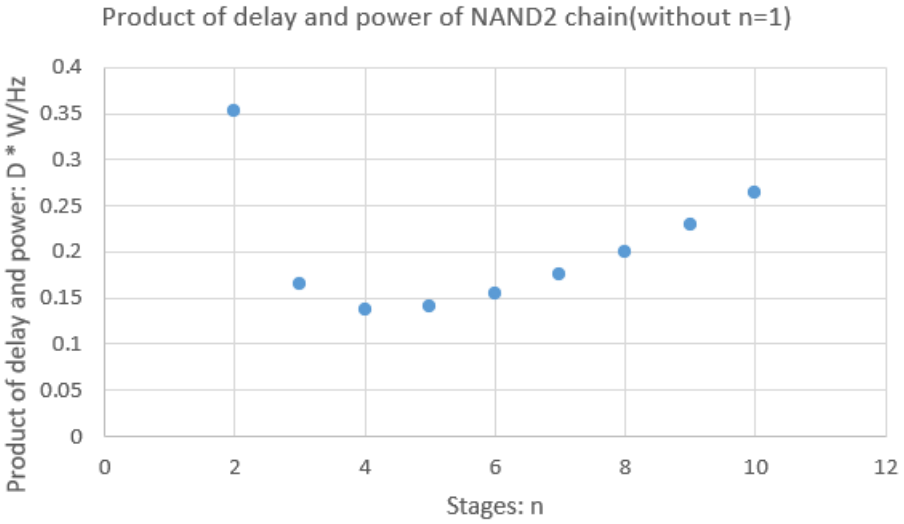


Step2. Calculate the estimated power consumption.

n	Clogic	power comsuption = C * V^2*f
1	20013.88	0.003242248
2	20730.1	0.003358276
3	22872.88	0.003705407
4	25975.22	0.004207986
5	29615.7	0.004797744
6	33569.16	0.005438204
7	37716.41	0.006110059
8	41990.71	0.006802495
9	46352.34	0.007509079
10	50776.4	0.008225776

c. Plot the product of power consumption and propagation delay for each n value vs. n. What is the n number for the minimum 'power-delay product'? Is it larger or smaller than the number of stages that gives the minimum delay? Explain your results clearly.





When n is 4, the NAND2 chain has minimum product of delay and power. It is smaller than the number of stages that gives the minimum delay. When using 6 NAND2, we can have minimum delay, but we use 6 NAND2 gates which may consume more power. Therefore, it's a tradeoff that we use inverters only to make the minimum value of the product of power and delay.

d. With n that gives you the minimum 'power-delay product', simulate and plot the waveforms for each node, including the input, for 50 ns. Use one row for each waveform. Label key data points and show the propagation delays for both the rising and falling inputs. What is the difference between the simulation

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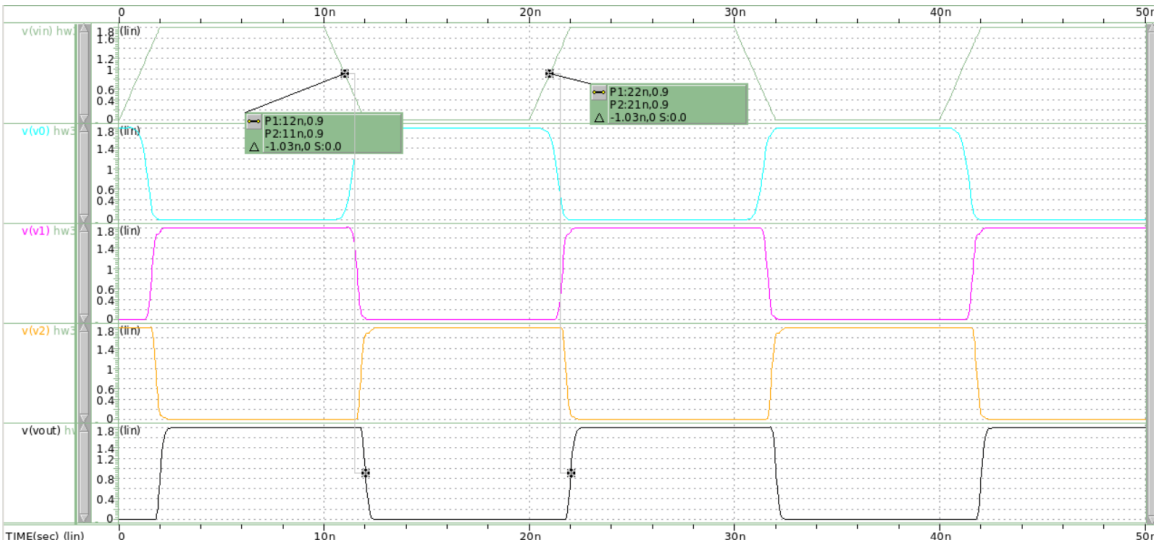


Hand analysis:

Step1. Find the parasitic delay of a unit inverter. I use the following circuit and measure function to measure the delay. (using 3 inverter and measuring the final stage delay make the value more accurate)

```
mpma vmo  vm vdd vdd p_18 l=.18u w=.87u  m=1
mpmb vmo  vm vdd vdd p_18 l=.18u w=.87u  m=1
mnma vmo  vm vxm gnd n_18 l=.18u w=1.06u m=1
mnmb vxm  vm gnd gnd n_18 l=.18u w=1.06u m=1

mpt0a vb  va vdd vdd p_18 l=.18u w=.87u  m=1
mpt0b vb  va vdd vdd p_18 l=.18u w=.87u  m=1
mnt0a vb  va vx0 gnd n_18 l=.18u w=1.06u m=1
mnt0b vx0 va gnd gnd n_18 l=.18u w=1.06u m=1

mpt1a vc  vb vdd vdd p_18 l=.18u w=.87u  m=1
mpt1b vc  vb vdd vdd p_18 l=.18u w=.87u  m=1
mnt1a vc  vb vx1 gnd n_18 l=.18u w=1.06u m=1
mnt1b vx1 vb gnd gnd n_18 l=.18u w=1.06u m=1

mpt2a vd  vc vdd vdd p_18 l=.18u w=.87u  m=1
mpt2b vd  vc vdd vdd p_18 l=.18u w=.87u  m=1
mnt2a vd  vc vx2 gnd n_18 l=.18u w=1.06u m=1
mnt2b vx2 vc gnd gnd n_18 l=.18u w=1.06u m=1

.tran 1p 50n
.meas tran tpr_par trig v(vc) val='0.9' fall=1 targ v(vd) val='0.9' rise=1
.meas tran tpd_par trig v(vc) val='0.9' rise=1 targ v(vd) val='0.9' fall=1
```

Circuit and measure function

tpr_par	tpd_par	temper	alter#
3.208e-11	3.097e-11	25.0000	1

measure function

Step2. In (a.) we estimate the delay, and the unit of D is the parasitic delay of a unit inverter, so by multiplying D and measure value, we can get the hand analysis delay.

$$32.7363819 * \frac{(3.208 * 10^{-11} + 3.097 * 10^{-11})}{2} = 1.032 * 10^{-9}$$

Simulation result:

tpr	tpd	power	power_0
power_1	power_2	power_3	temper
alter#			
1.033e-09	1.029e-09	4.223e-03	1.218e-05
6.778e-05	4.584e-04	3.685e-03	25.0000

measure result

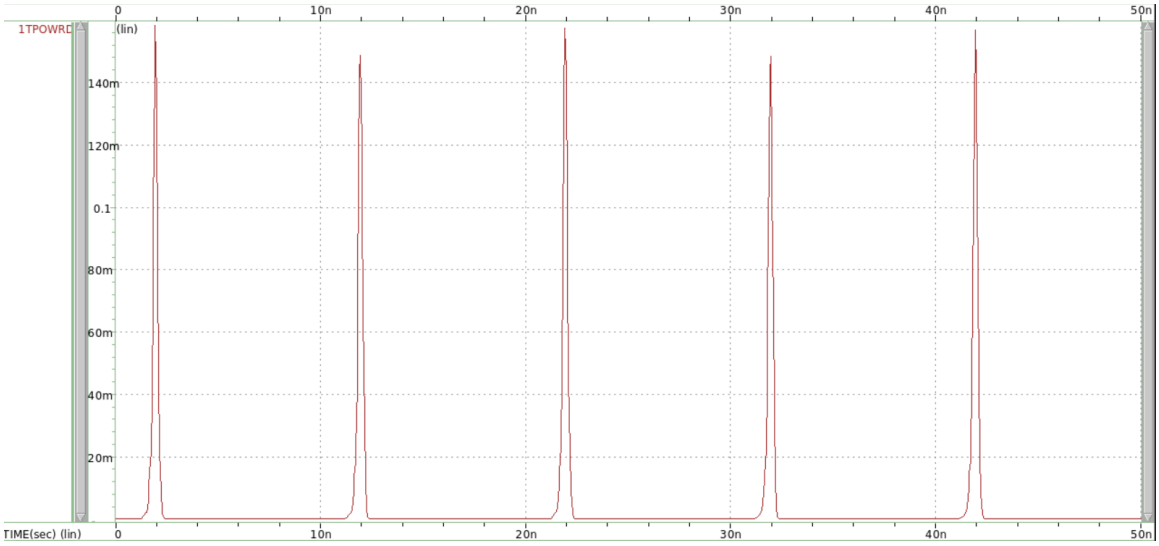
$$\frac{1.033 * 10^{-9} + 1.029 * 10^{-9}}{2} = 1.031 * 10^{-9}$$

Error: $\frac{1.032-1.031}{1.031} = 0.97\%$

The simulation result and hand analysis are almost the same.

The result is slower than inverter chain, I think it is because the Cin of NAND2 is a little bit smaller than inverter(7.5083 < 7.5601). So F of NAND2 chain is larger than inverter chain, which means it needs more time to charge or discharge.

e. Following the previous question, simulate and plot the instant power consumption vs. time of this inverter chain, and measure the average power for the time duration from t=30~50 ns. What is the difference between the simulation result and the hand calculations? Explain why they are different with reasons as clear as possible.



instant power consumption vs. time of this inverter chain, and measure the average power for the time duration from t=30~50 ns

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '** 110061217 王彥智 hw3_2'
 tpr              tpd              power            power_0
 power_1          power_2          power_3          temper
 alter#
  1.033e-09        1.029e-09        4.223e-03        1.218e-05
  6.778e-05        4.584e-04        3.685e-03         25.0000
```

In (b.) We estimate power consumption 0.004207986W/Hz

$$\text{Error: } \frac{0.004096897-0.004223}{0.004223} = -2.988\%$$

The power consumption of NAND2 chain is a little bit smaller than inverter chain, since Cin of NAND2 is a little bit smaller than Cin of inverter, so it needs less power to charge or discharge.

f. For the average power, perform any simulation and/or analysis required to answer the following questions. Provide detailed data and explanations to support your answer.
   i. Which stage consumes the most average power?

Power consumption in different stage (stage1 to stage4 from above to below)

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '** 110061217 王彥智 hw3_2'
 tpr                tpd                power              power_0
 power_1            power_2            power_3            temper
 alter#
  1.033e-09          1.029e-09          4.223e-03          1.218e-05
  6.778e-05          4.584e-04          3.685e-03           25.0000
```

Stage4 consumes the most average power(3.685mW) since the size of the PMOS and NMOS is the largest in stage 4.

Both NAND and inverter chain consume most power in the last stage, because according to out design, the logic gate in last stage is the largest, so it may consume the most power.

ii. For this most-power-consuming stage, how much average power is consumed by charging/discharging the output power? How much average power is consumed by short-circuit current? How much average power is consumed by leakage?


```
.meas tran charge integ'((v(vdd)-v(vout))*(abs(i(mp3a))+abs(i(mp3b))))/20n' from=1.7n to=2.7n
.meas tran discharge integ'(v(vout)*abs(i(mn3a)))/20n' from=11.5n to=12.5n

.meas tran shortcktn integ'v(vout)*(abs(i(mn3a))+abs(i(mn3b)))' from=1.7n to 2.7n
.meas tran shortcktp integ'(v(vdd)-v(vout))*(abs(i(mp3a))+abs(i(mp3b)))' from=11.5n to=12.5n
.meas tran shortckt_avg param='(shortcktn+shortcktp)/20n'

.meas tran leakage1 integ'v(vdd)*(abs(i(mp3a))+abs(i(mp3b)))' from=0n to=1.7n
.meas tran leakage2 integ'v(vdd)*abs(i(mn3a))' from=2.7n to=11.5n
.meas tran leakage3 integ'v(vdd)*(abs(i(mp3a))+abs(i(mp3b)))' from=12.5n to=20n


.meas tran leakage_avg param='(leakage1+leakage2+leakage3)/20n'
```

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '** 110061217 王彥智 hw3_2'
 tpr              tpd              power            power_0
 power_1          power_2          power_3          charge
 discharge        shortcktn        shortcktp        shortckt_avg
 leakage1         leakage2         leakage3         leakage_avg
 temper           alter#
  1.033e-09        1.029e-09        4.223e-03        1.218e-05
  6.778e-05        4.584e-04        3.685e-03        1.763e-03
  1.773e-03        8.857e-13        1.270e-12        1.078e-04
  1.116e-14        4.087e-13        4.639e-13        4.419e-05
   25.0000         1
```

Charge: 1.763*10^-3

Discharge: 1.773*10^-3

Short circuit current: 1.078*10^-4

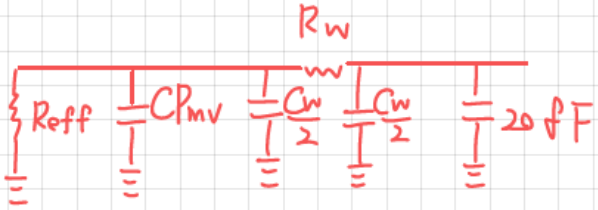
Leakage: 4.419*10^-5

For both NAND2 and inverter chain, most of the power is consumed to charge and discharge the node.

3. For an isolated, minimum-width, 5-mm long M1 wire, consider the following:
   - V_{DD} = 1.8V
   - The size of the first inverter and the load are fixed. $(W/L)_N$ = 1u/0.18um, and $(W/L)_P$ = 1u/0.18um
   - The inverter chain drives a capacitor load of 20 fF.
   - The rise and fall time of the input is 2 ns, and the frequency is 50 MHz.

   a. Inverter with wire
      1) Hand-calculate the signal delay (from input to the driver to input of the load) and power consumption. Explain the assumptions and details of your analysis clearly.

3a.



$$\text{delay} : R_{eff}\left(C_{Pmv} + \frac{C_w}{2} + \frac{C_w}{2} + 20f\right) + R_w\left(\frac{C_w}{2} + 20f\right)$$

$$\text{power} : \left(C_{Pm} + \frac{C_w}{2} + \frac{C_w}{2} + 20f\right) V_{dd}^2 \times f$$

∵ $R_{eff} = 2327.48\,\Omega$, $C = 7.8143$ fF] by doing an inverter layout (without wire) and add the R and C value in pex file of Vout node

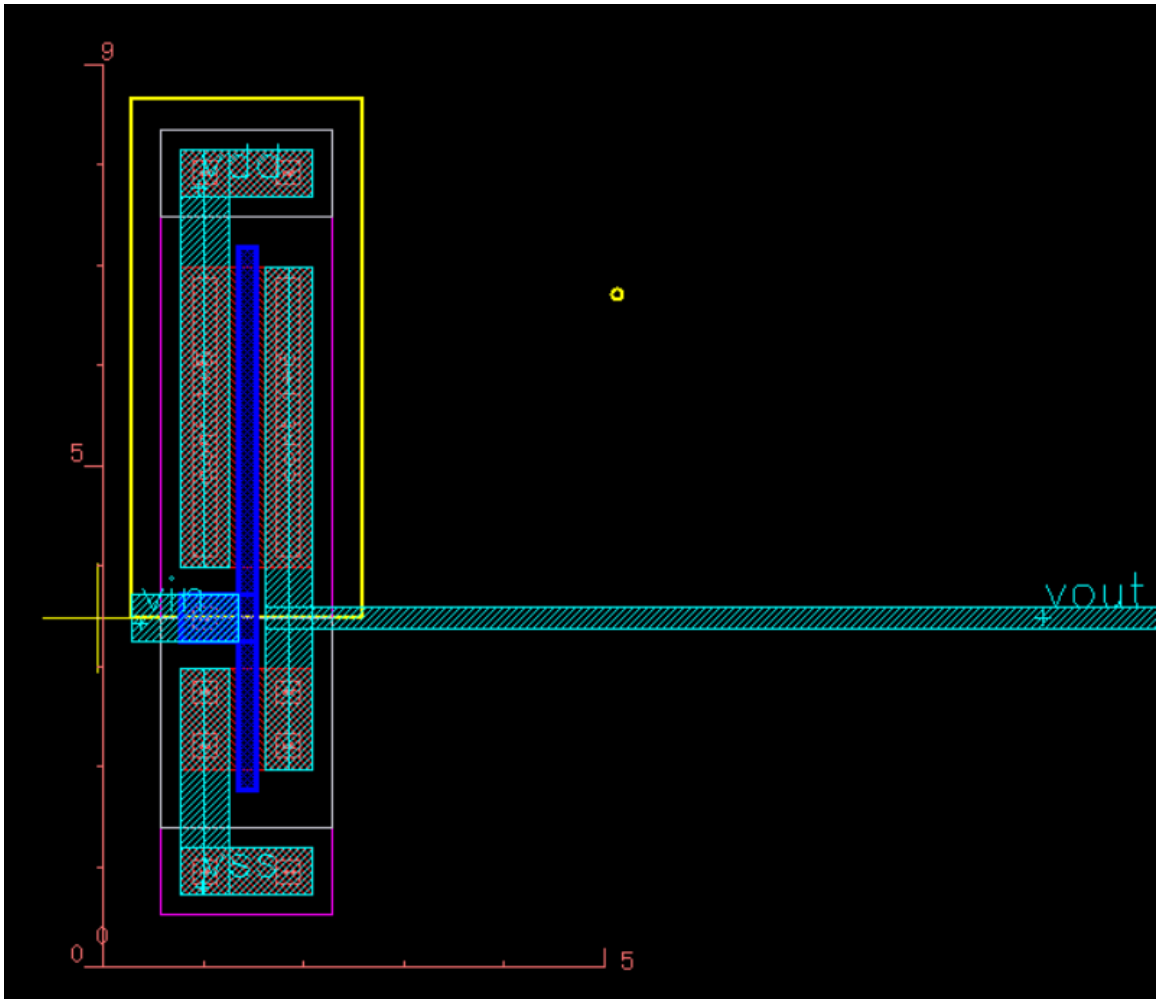
$C_w = 381.57$ fF, $R_w = 1526.68\,\Omega$] by doing a wire layout only and add the R and C in pex file of Vout node

$P_{inv} = 1$ assumed

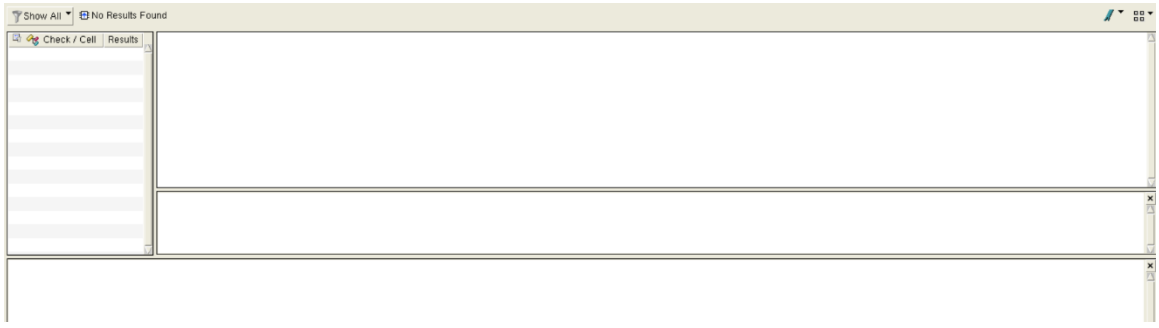
→ delay ≅ 1.27463 ns

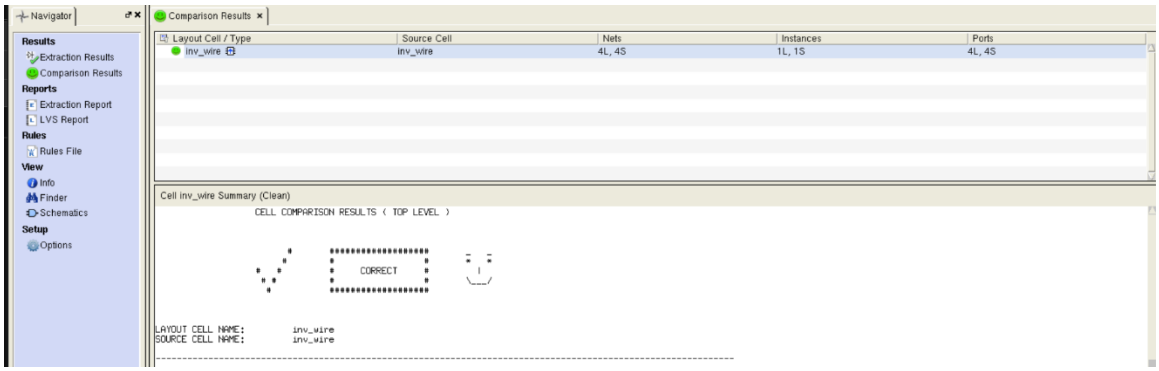
→ power ≅ 6.6320×10^{-5} W

   2) Complete the layout (driver-wire-load). Snapshot the screens that show DRC and LVS clean. Show a snapshot of the layout (with rulers that show x and y dimensions) in your report. Report the area. Furthermore, explain your layout considerations.

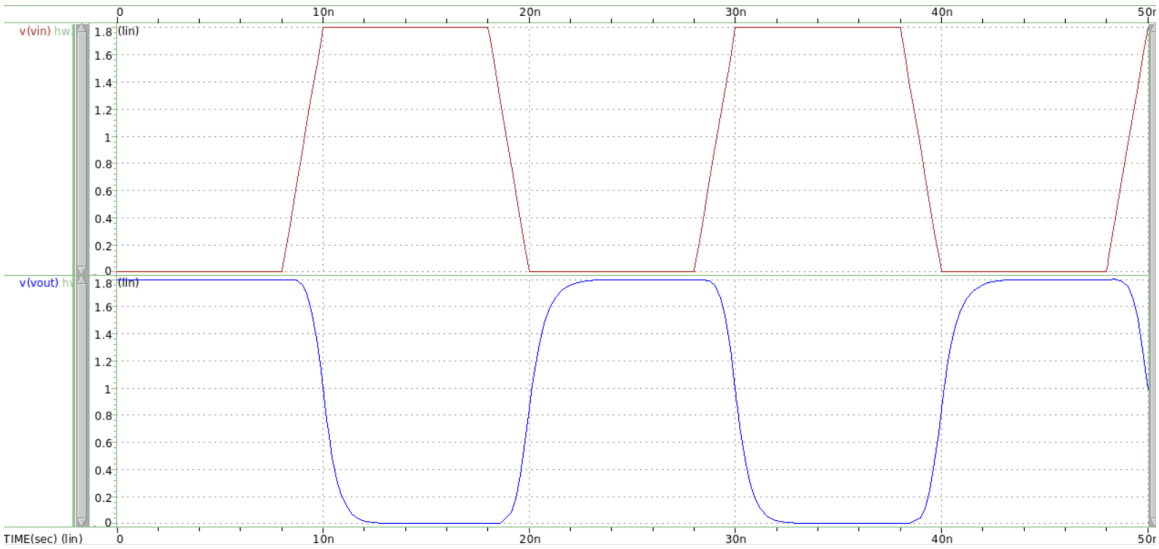


Layout considerations: try to use minimum distance to pass DRC, so the speed can be faster and area could be smaller.





3) Run post-layout simulation (R-C-CC extraction) and plot the waveforms for each node, including the input, for 50 ns. Measure the propagation delays for both the rising and falling inputs as well as the power consumption. What is the difference between the simulation result and the hand calculations? Explain why they are different with reasons as clearly as possible. (Don't just say something like 'layout causes additional parasitic'.)



Waveform

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '** 110061217 hw3 q3a testbench'
 power              tpr               tpd               temper
 alter#
  6.919e-05         1.043e-09         1.074e-09          25.0000
```

Measure of power and delay

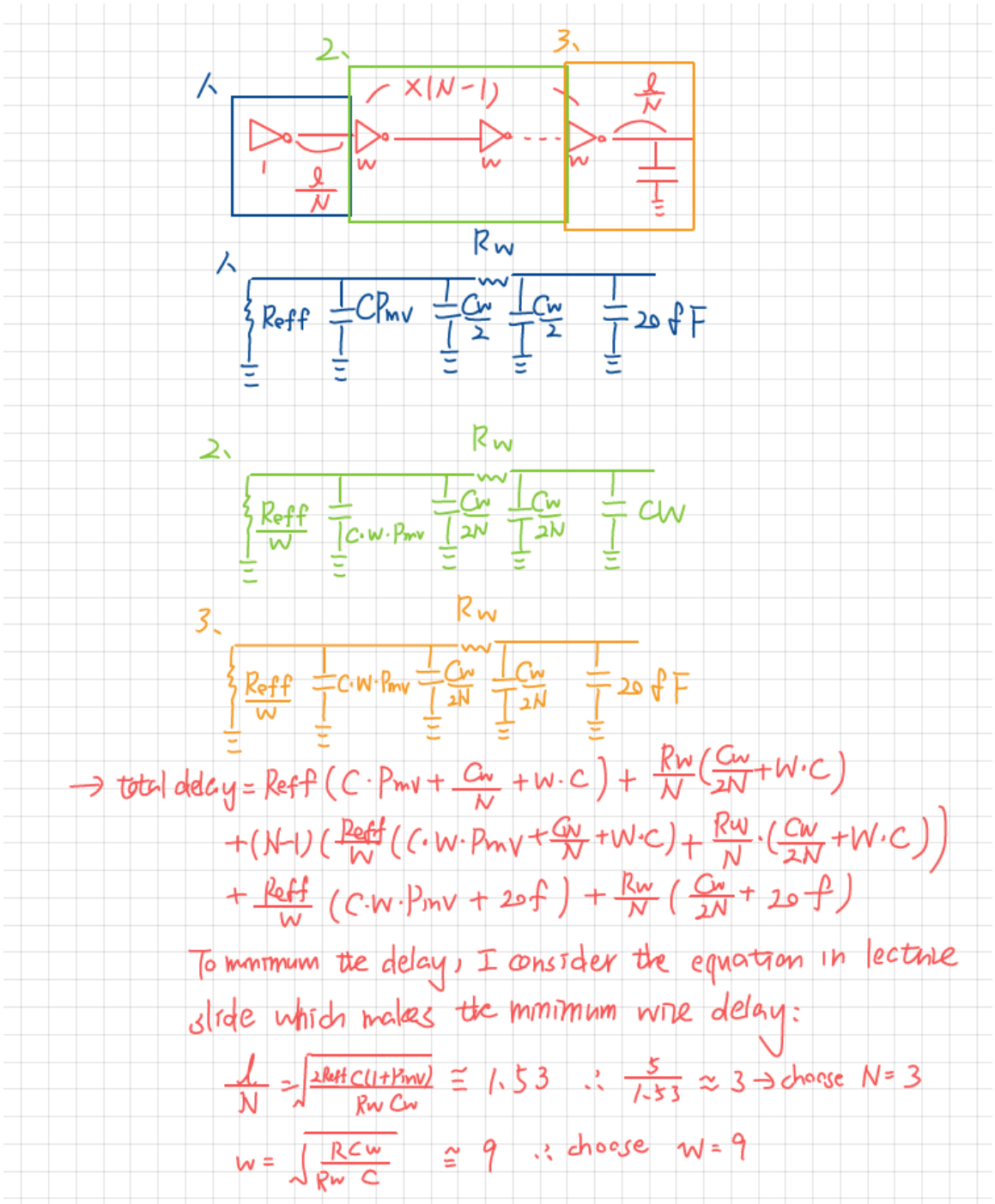
$$\text{delay} = \frac{1.043*10^{-9}+1.074*10^{-9}}{2} = 1.0585 * 10^{-9}$$

$$\text{Error of delay: } \frac{1.2746-1.0585}{1.0585} = 20.41\%$$

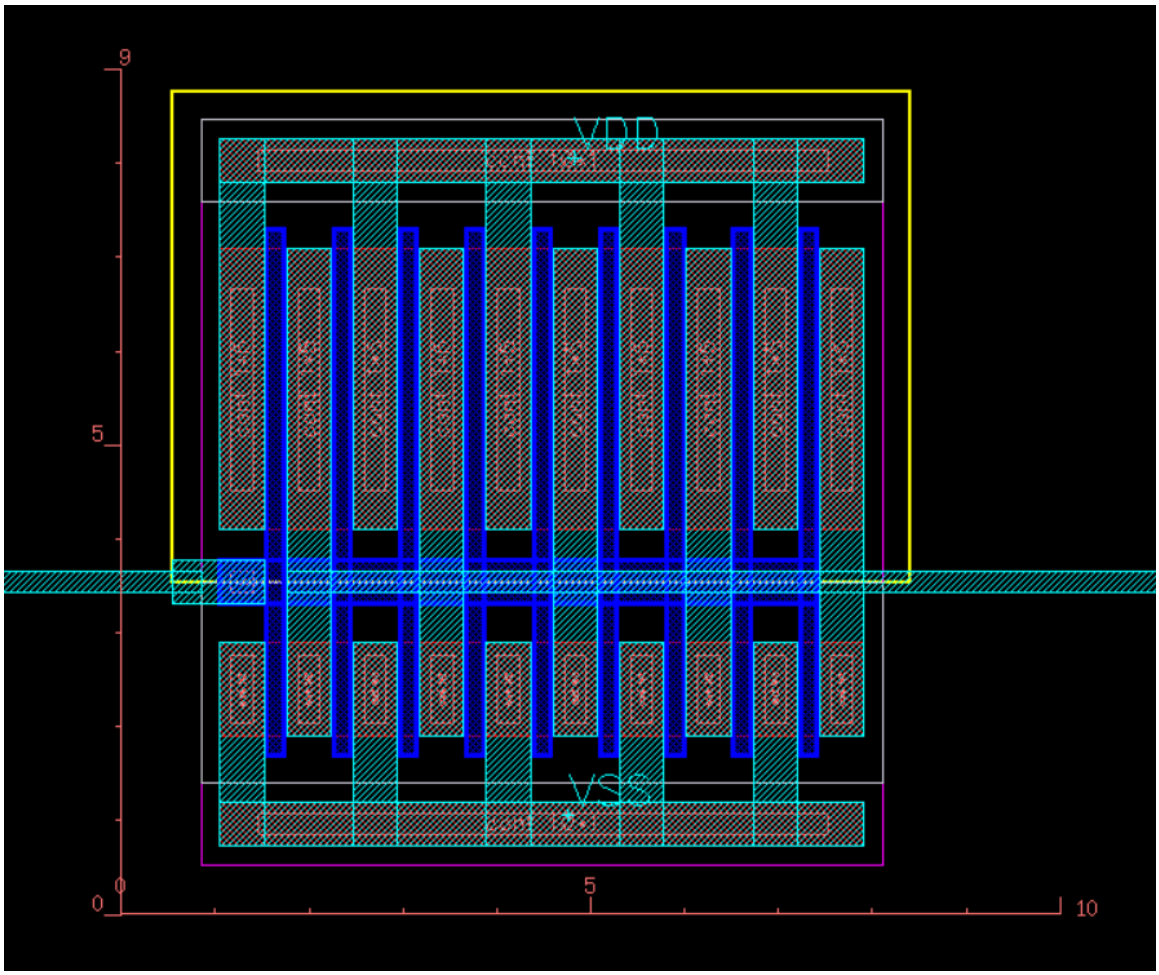
Discussion: I think it is because pi module is not accurate enough.

$$\text{Error of power: } \frac{6.632-6.919}{6.919} = 4.14\%$$

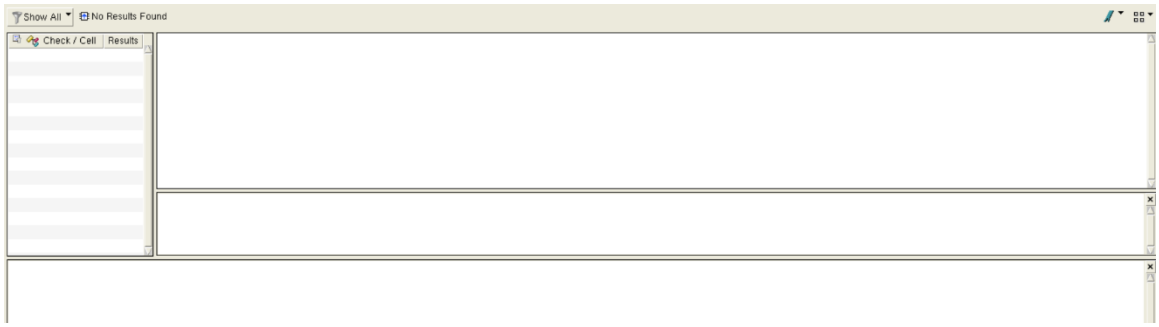
b. Inverter with repeaters that achieve the minimum delay.
    1) Design repeaters using inverters (with either even or odd numbers of inverters) to achieve the minimum delay (from input to the driver to input of the load). Hand-calculate the signal delay (from input to the driver to input of the load) and power consumption. The driver and the load are fixed, while you may freely choose the size of inverters/repeaters. explain the assumptions and details of your analysis clearly.

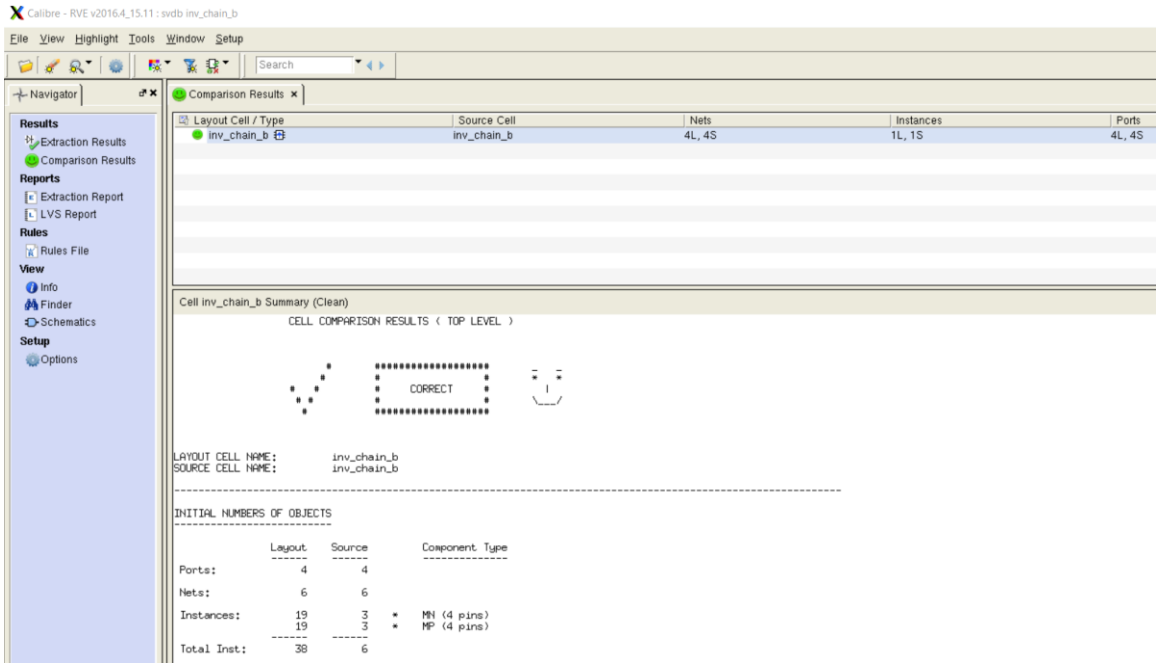


2) Complete the layout. Snapshot the screens that show DRC and LVS clean. Show a snapshot of the layout (with rulers that show x and y dimensions) in your report. Report the area. Furthermore, explain your layout considerations.

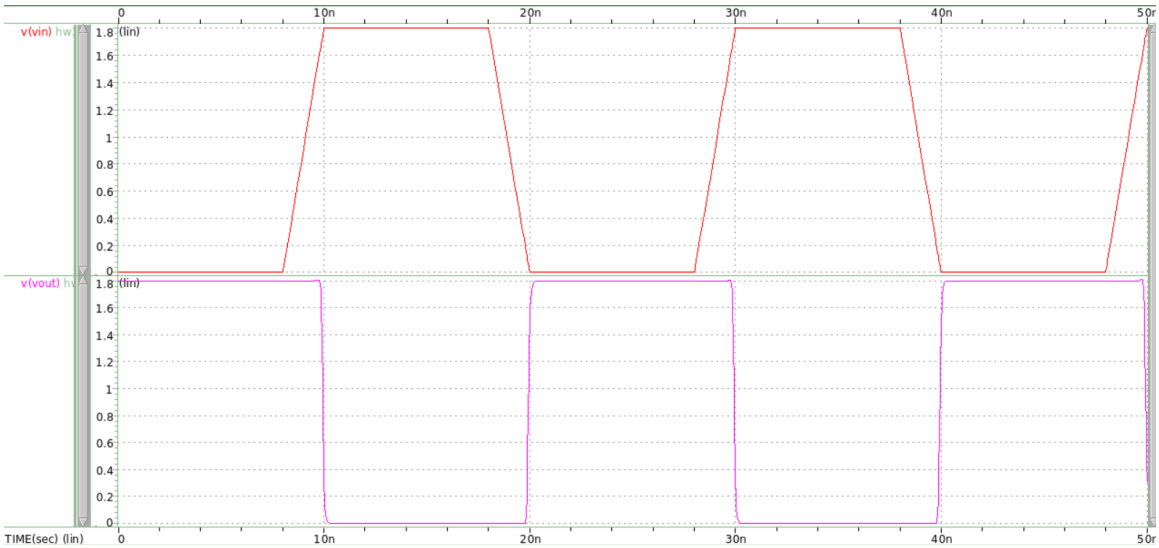


Layout considerations: use finger to draw the repeater(w=9).

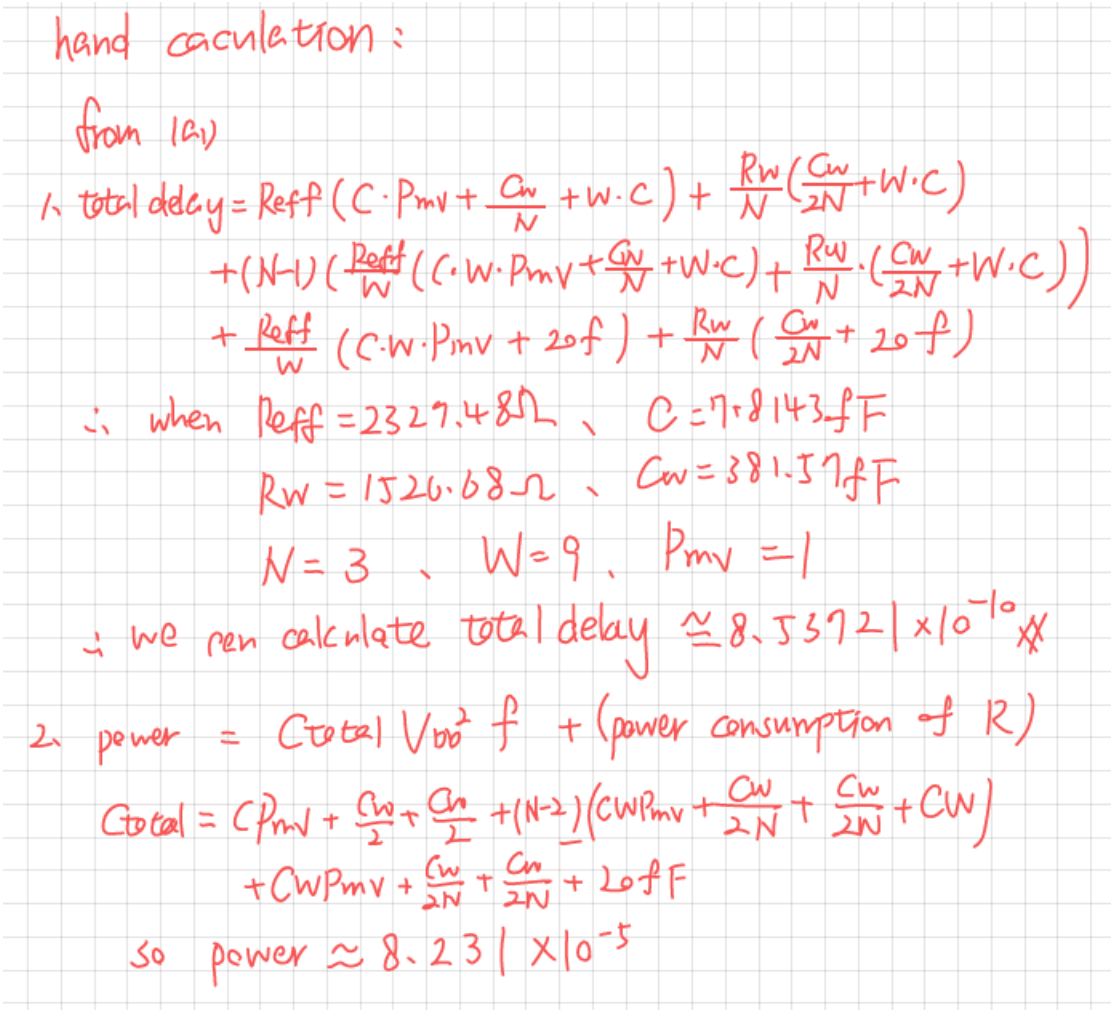




3) Run post-layout simulation (R-C-CC extraction) and plot the waveforms for each node, including the input, for 50 ns. Measure the propagation delays for both the rising and falling inputs as well as the power consumption. What is the difference between the simulation result and the hand calculations? Explain why they are different with reasons as clearly as possible. (Don't just say something like 'layout causes additional parasitic'.)




```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '** 110061217 hw3 q3b testbench'
 power            tpr              tpd              temper
 alter#
  1.595e-04        9.351e-10        9.418e-10         25.0000
```



$$\text{delay} = \frac{9.351*10^{-10}+9.418*10^{-10}}{2} = 9.3845 * 10^{-10}$$

$$\text{Error of delay: } \frac{8.5372-9.3845}{9.3845} = -9.028\%$$

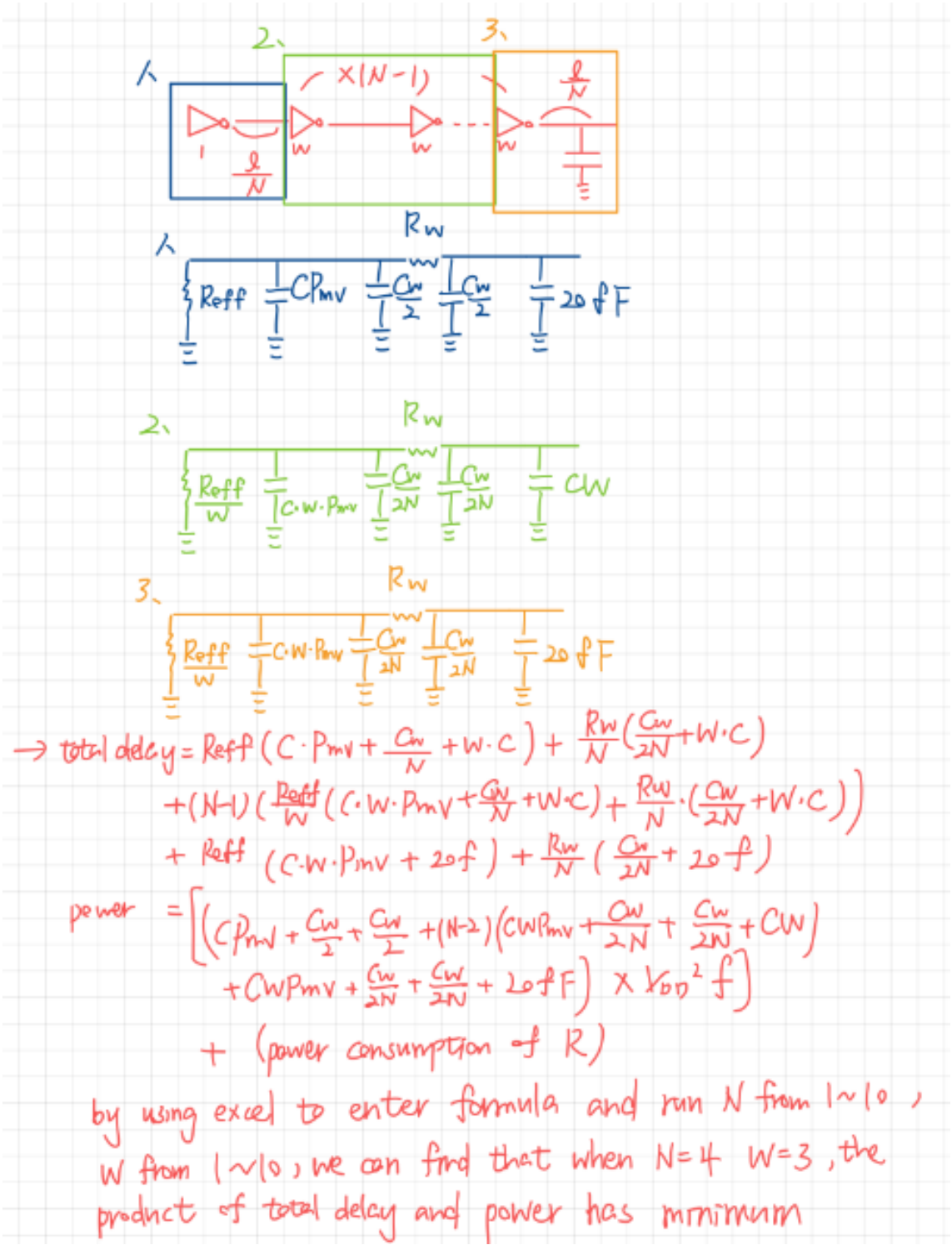
$$\text{Error of power: } \frac{8.231*10^{-5}-1.595*10^{-4}}{1.595*10^{-4}} = -48.39\%$$

Discussion: I didn't consider the power consumption consumed by resistance, so the error is large.

c. Inverter with repeaters that achieve the minimum power-delay product.

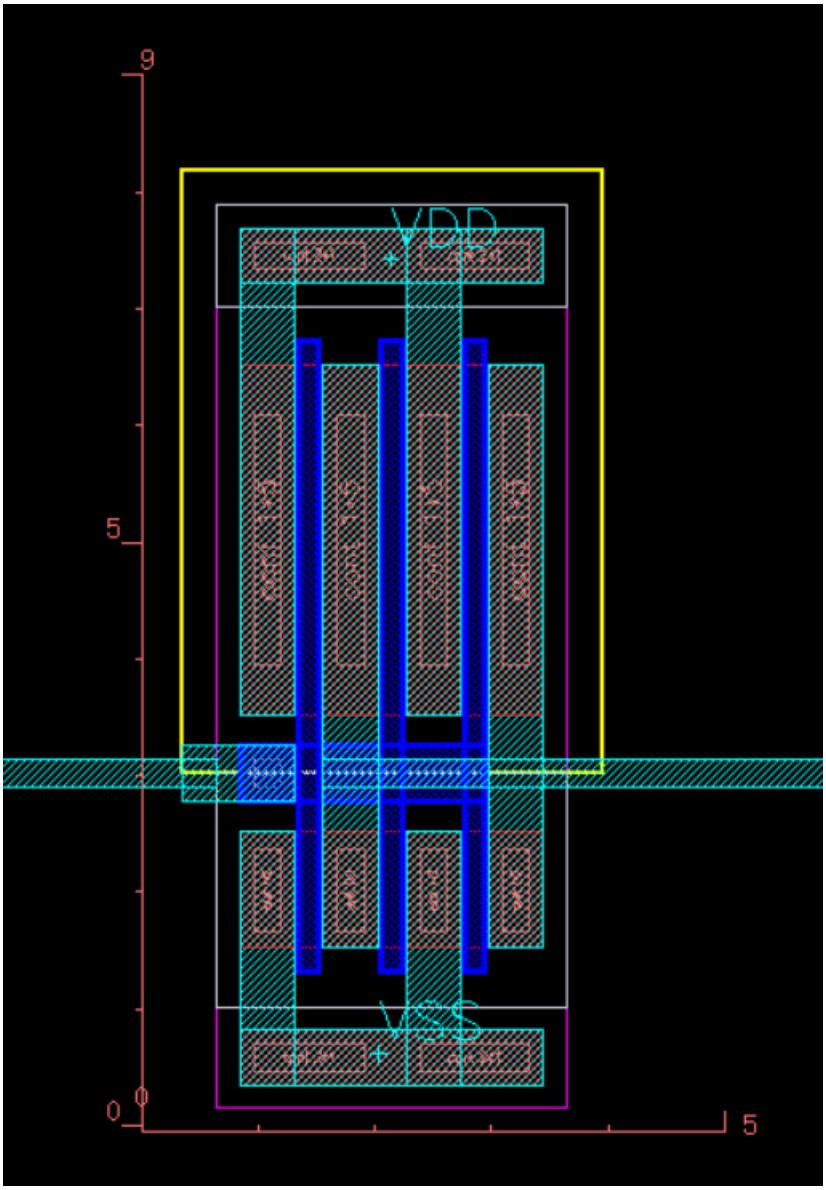
1) Design repeaters using inverters (with either even or odd numbers of inverters) to achieve the minimum power-delay product (excluding the load inverter). Hand-calculate the signal delay (from input to the driver to input of the load) and power consumption. The driver and the load

are fixed, while you may freely choose the size of inverters/repeaters. Explain the details (assumptions) of your analysis clearly.

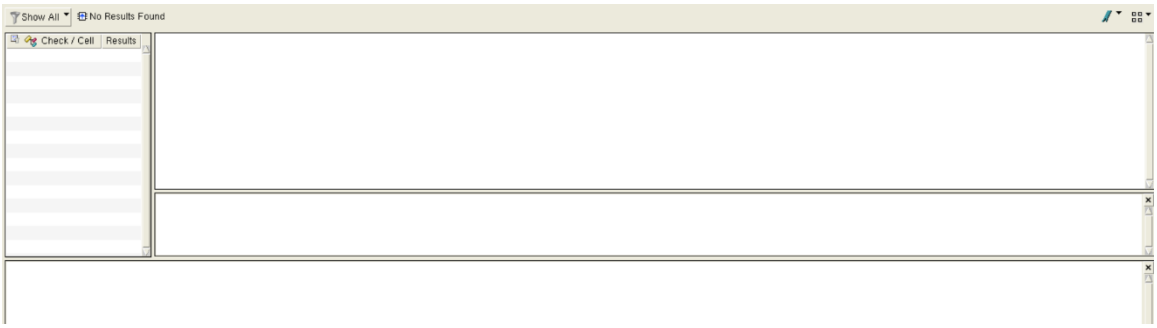


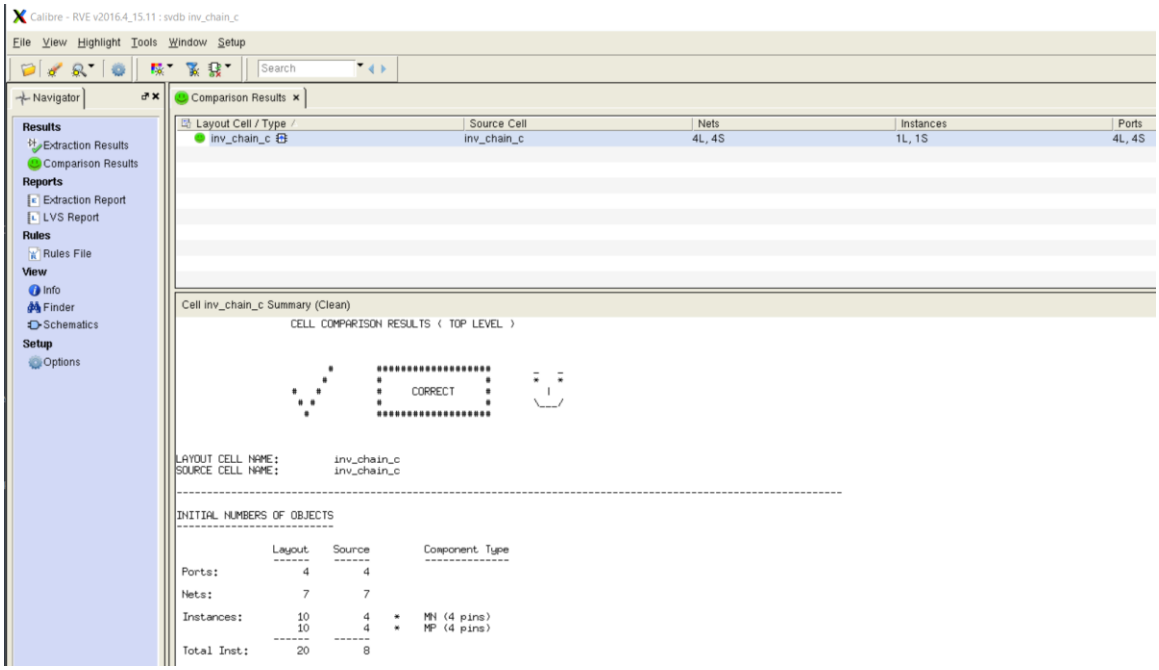
2) Complete the layout. Snapshot the screens that show DRC and LVS clean. Show a snapshot of the layout (with rulers that show x and y

dimensions) in your report. Report the area. Furthermore, explain your layout considerations.

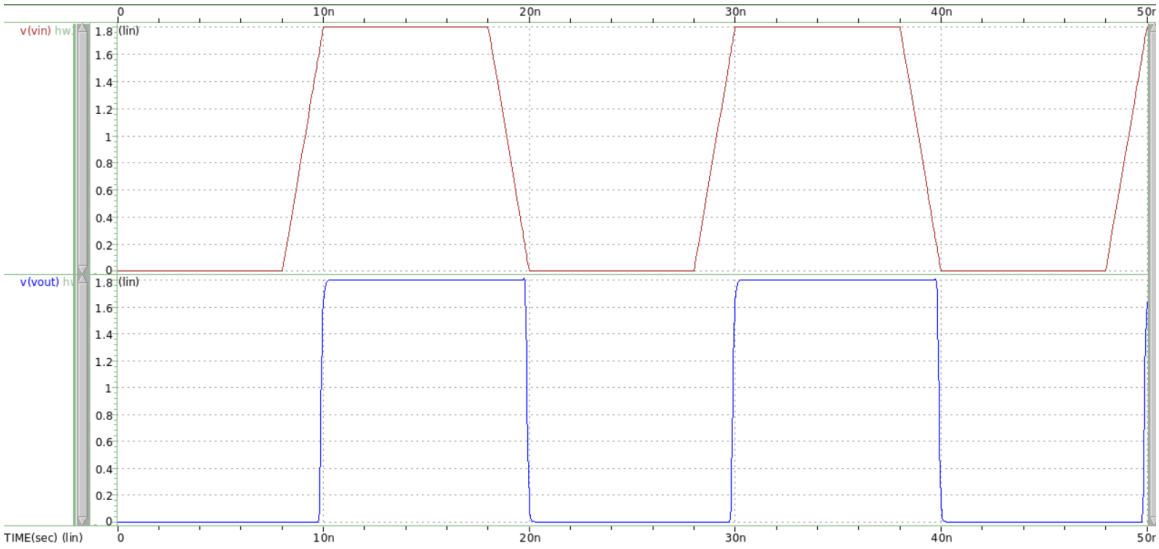


Layout considerations: use finger to draw the repeater(w=3).

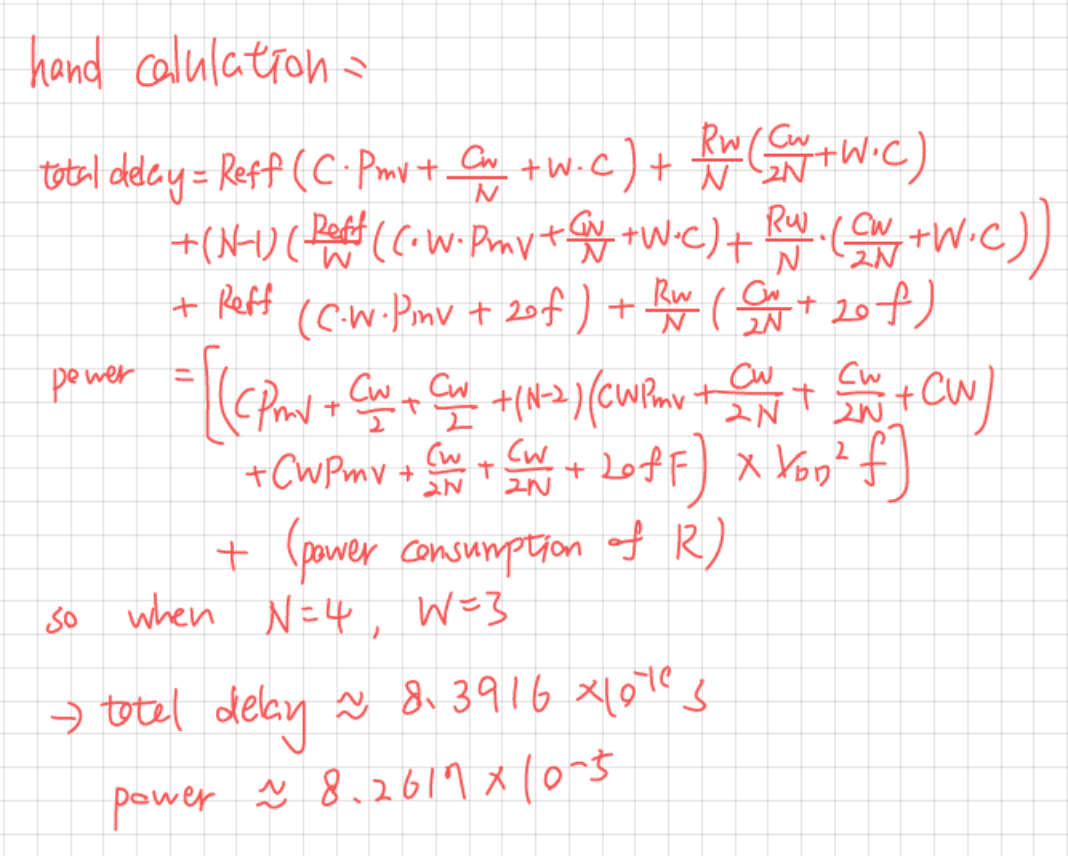




3) Run post-layout simulation (R-C-CC extraction) and plot the waveforms for each node, including the input, for 50 ns. Measure the propagation delays for both the rising and falling inputs as well as the power consumption. What is the difference between the simulation result and the hand calculations? Explain why they are different with reasons as clearly as possible. (Don't just say something like 'layout causes additional parasitic'.)




```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='R-2020.12-SP2 linux64' PARAM_COUNT=0
.TITLE '** 110061217 hw3 q3c testbench'
 power            tpr              tpd              temper
 alter#
  1.028e-04        8.860e-10        8.991e-10         25.0000
```



$$\text{delay} = \frac{8.860*10^{-10}+8.991*10^{-10}}{2} = 8.9255 * 10^{-10}$$

$$\text{Error of delay: } \frac{8.9255-8.3916}{8.3916} = 6.362\%$$

$$\text{Error of power: } \frac{8.2647*10^{-5}-1.028*10^{-4}}{1.028*10^{-4}} = -19.60\%$$

Discussion: I didn't consider the power consumption consumed by resistance, so there has some error.