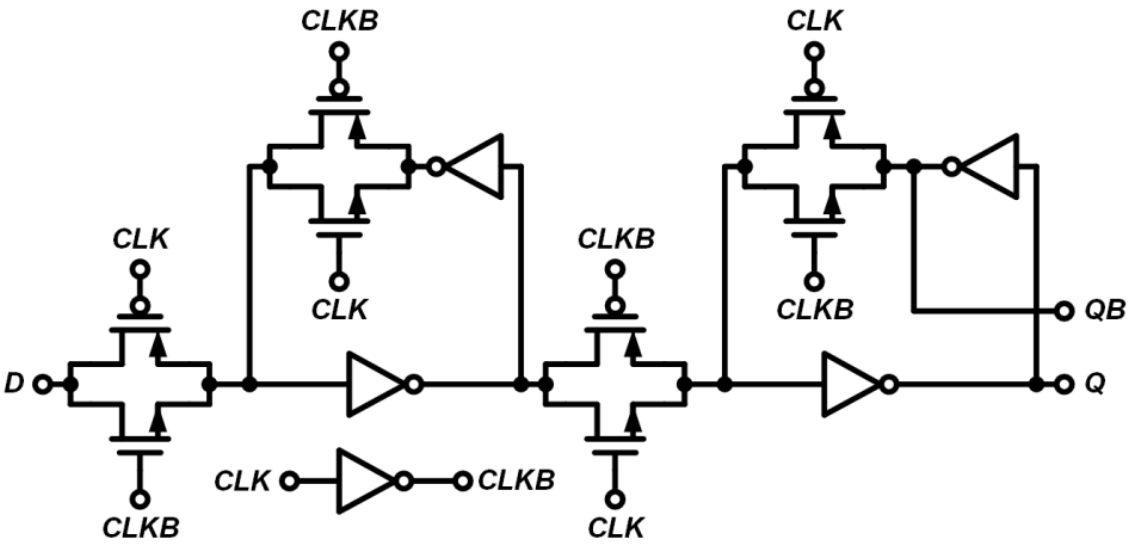
EE3230 VLSI Design (2023 Spring) HW #4

Due date: 2023/12/18 (Monday) 10am

No plagiarism is allowed!!

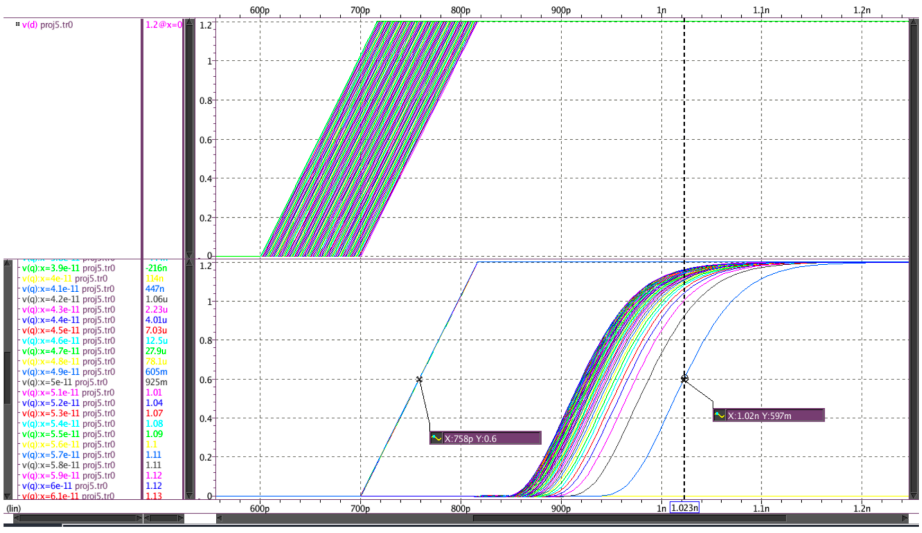
Perform the simulation with tt corner at 25℃

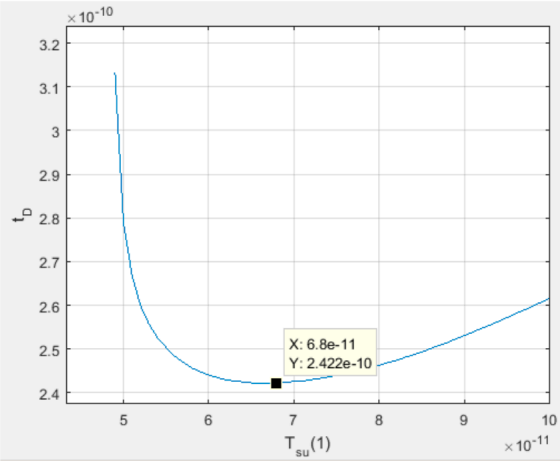
1. Please design a master-slave flip-flop with the following schematics.
   - V_{DD}=1.8 V, and the input clock CLK runs at 50MHz.
   - **There are ONLY 2 inputs to this module**, D and CLK.
     In your simulations, **EACH INPUT** sees two unit inverters in series (for proper slope shaping) with the following specified size: $(W/L)_N$=0.5μ/0.18μ and $(W/L)_P$=1.5μ/0.18μ.
   - You'll need to generate the signal CLKB so that the circuit can work properly.
   - The output (Q) drives a capacitor load of 50*f*F.
   - The rise and fall times of input signals are 0.2ns.
   - You are allowed to insert inverters wherever you like to improve the performance. In this case, please provide an updated schematic and explain you design considerations. However, remember to keep the polarity of Q correct. (In other words, Q should follow the polarity of D.)
   - You can decide all the transistor sizes by yourself except the two unit inverters that inputs see.
   - TA will provide a testbench file for your convenience later.



A. (30%) Please characterize the flilp-flop's setup time, hold time, and propagation delays, for both rising and falling input transitions. Also, with an input signal D that transitions once every clock cycle, please measure the power consumption.

- The measurement accuracy should be better than 1ps. That is to say, when sweeping the relative delay between D and clk, change it with a step smaller than 1ps, so that you can clearly see how t_{C2Q} increases as you decrease t_{D2C}.
- In the report, please provide the timing waveforms of D, clk, and Q for all the characteristics you measure. The following shows one example that I found on Internet of setup time for rising input. Please put all delay cases into **ONE** figure.
- Please also plot t_{D2Q} vs. t_{D2C} for all the characteristics that you measure. Label the curve and show how you measure the setup time like the following example that I found on Internet.





B. (10%) Explain what you have done to improve the performance (i.e., to speed up the operation and/or to reduce the power consumption). If you ever modify the schematics, provide the updated version in your report.

C. (20%) Complete the layout. Snapshot the screens that show DRC and LVS clean. Show a snapshot of the layout (with rulers that show x and y dimensions) in your report. Report the area. Furthermore, explain your layout considerations.

D. (20%) Run post-layout simulation (R-C-CC extraction) and measure the power consumption, setup time, hold time, and propagation delays, for both rising and falling input transitions again. Complete the following table and show it in your report.

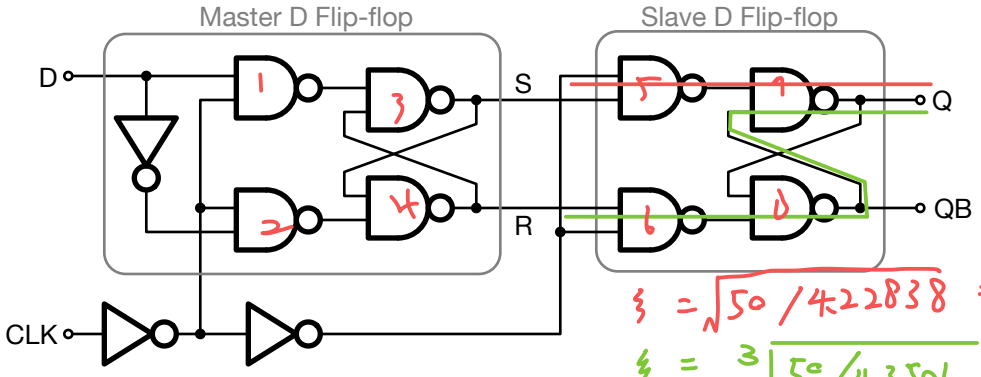
	Pre-layout simulation		Post-layout simulation	
	Rising	Falling	Rising	Falling
t_{SU}	89	92	95	82
t_H	88.6	42.7	115	47
minimum t_{D2Q}				
minimum t_{CK2Q}				
Power consumption (μW)				
Layout area (μm²)	10.195 x 21.96 um²			

81 124 107 65

56.1 108 28.5 84.5

$10.91 \times 34.86\ um^2$

2. With the following master-slave flip-flop, repeat the characterization in the previous question (Q1A to Q1D). Explain what and why the differences are in details.

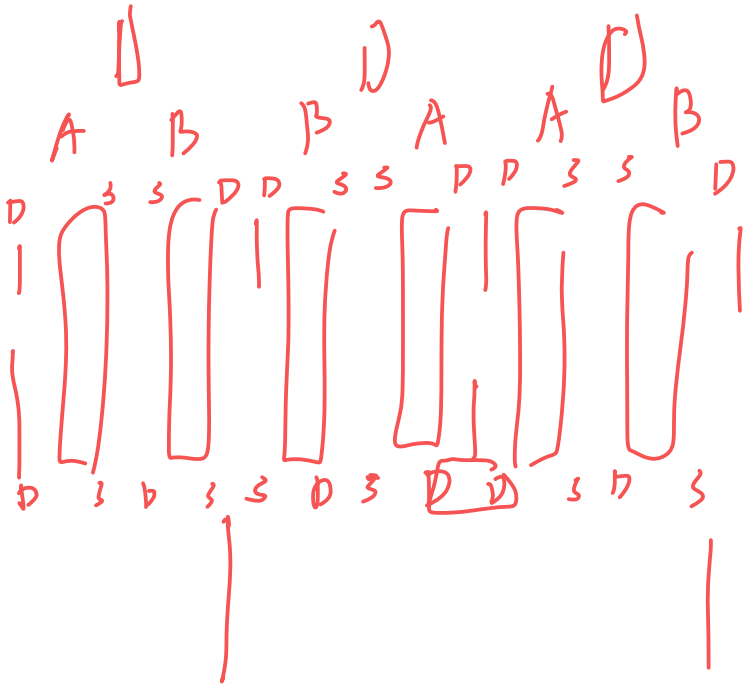


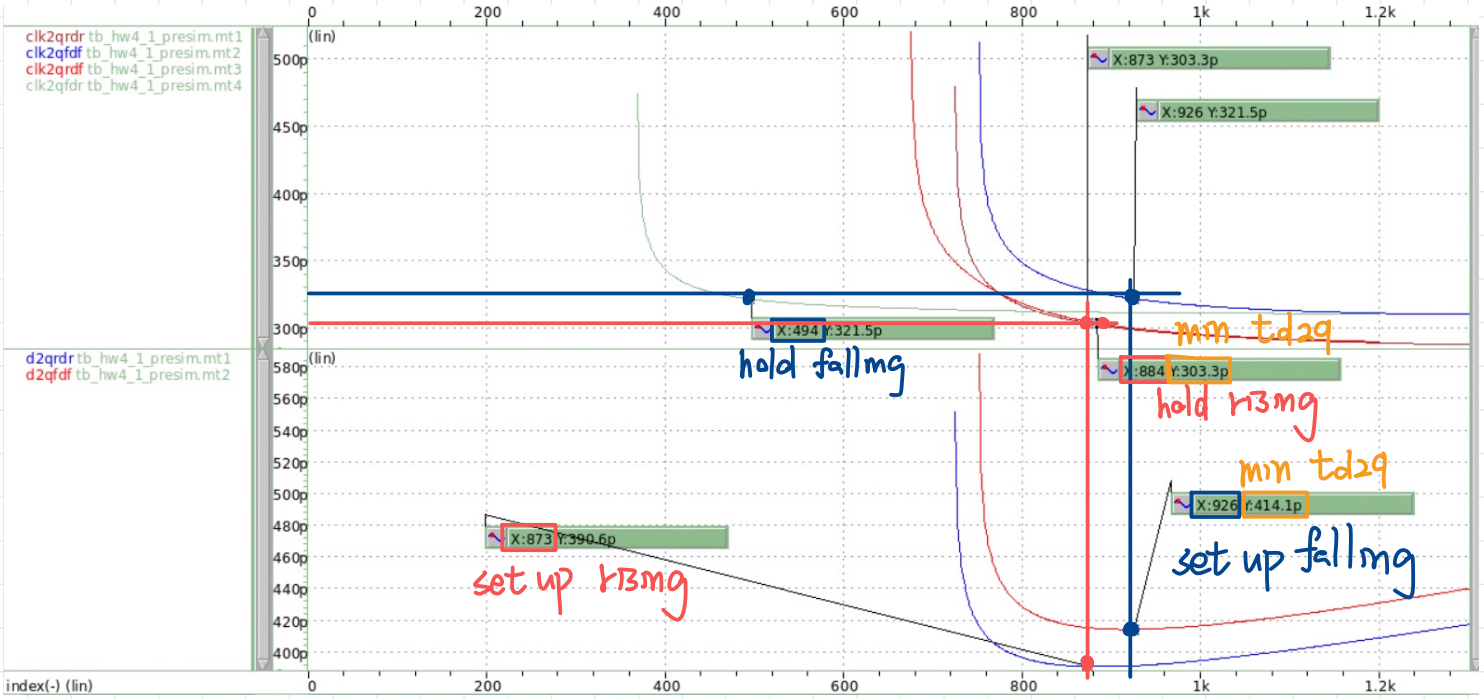
$\S = \sqrt{50/4.22838} = 3.14387$

$\S = \sqrt[3]{50/4.3506} = 2.25669$

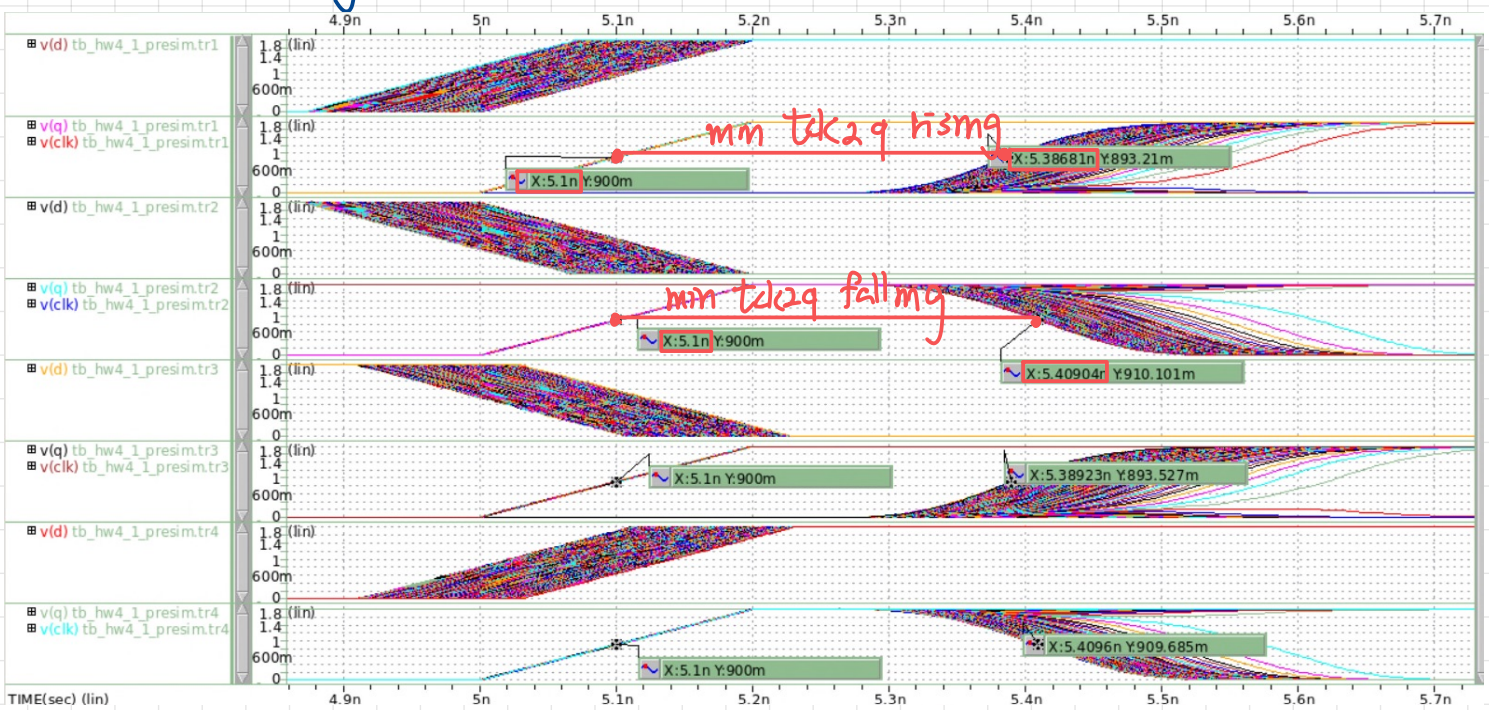
$\therefore \frac{3.14387 + 2.25669}{2} \approx 2.8476$

$\therefore$ 取 3





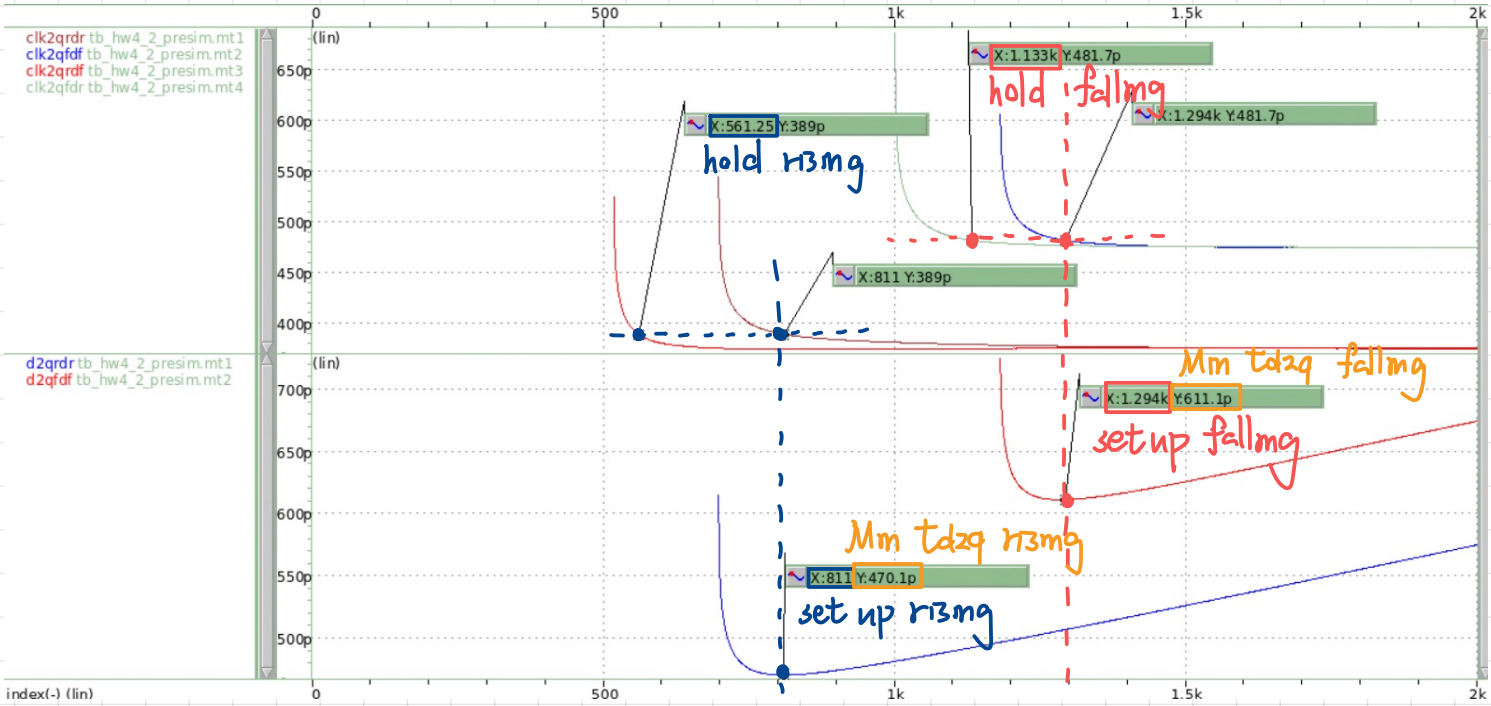
hold time : since in testbench we sweep t-hold from -90p to 30p but x-axis in graph is from 0p to 120p, so the real hold time should be
- rismg : 88.4ps − 90ps = −1.6ps
- fallmg : 49.4ps − 90ps = −40.6ps



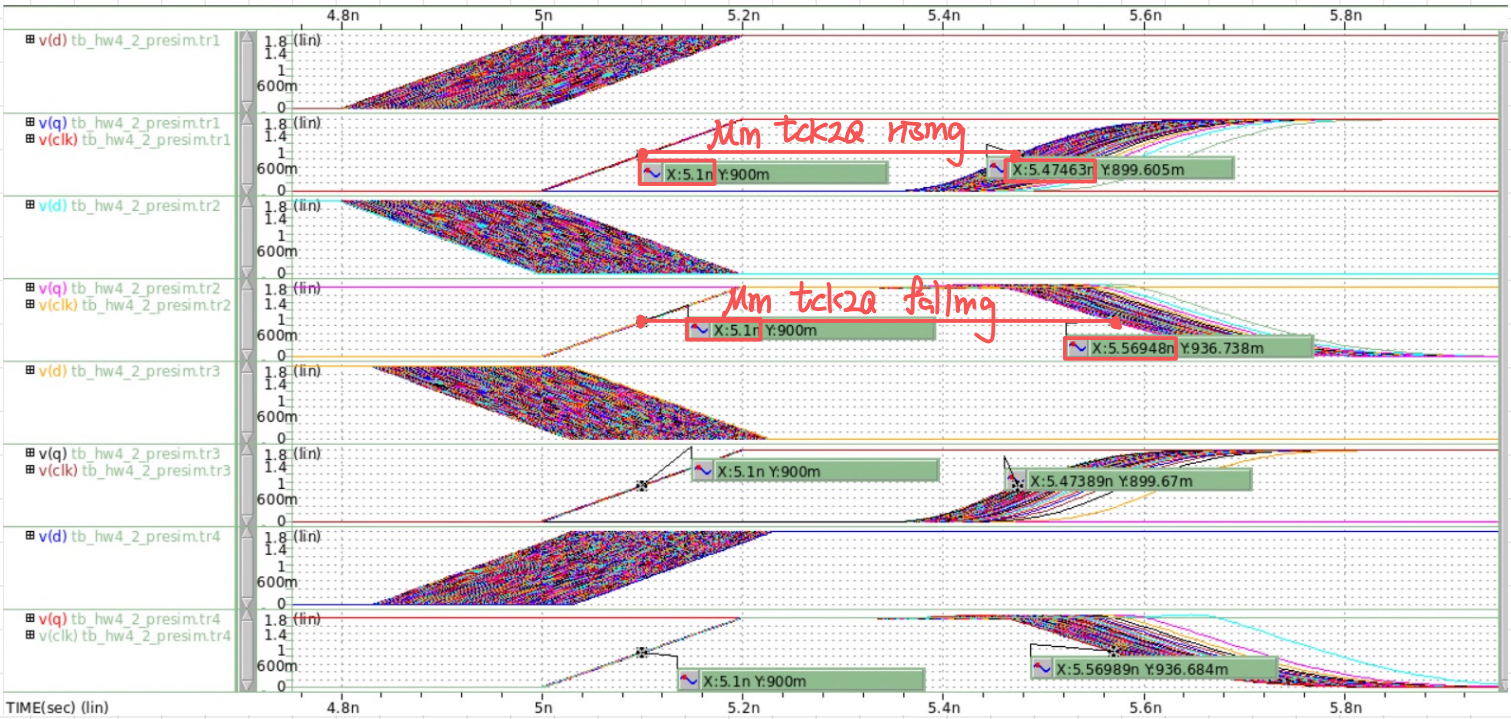
mm tclk2q rismg : 5386.81ps − 5100ps = 286.81ps

mm tclk2q fallmg : 5409.04ps − 5100ps = 309.04ps

* Use the same method to measure Tsu, Th, Min tc2q, Mm tclk2q in part1 post-layout simulation and unit size flip flop simulation.



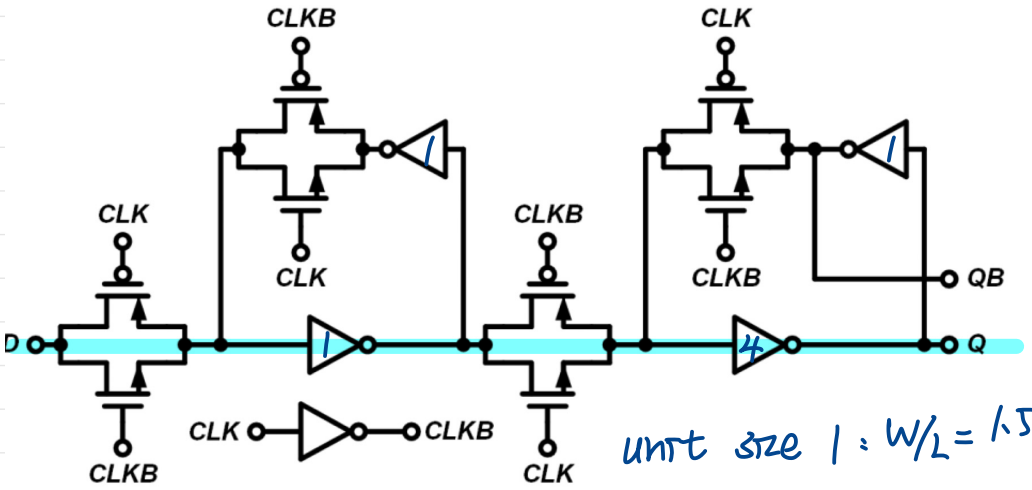
hold time : since in testbench we sweep t-hold from -170p to 30p but x-axis in graph is from 0p to 200p (sweep every 0.1ps), so the real hold time should be
- rismg : 56.1ps - 170ps = -113.9ps
- fallmg : 113.3ps - 170ps = -56.6ops



mm tck2q rismg : 5474.63 ps - 5100 ps = 374.63 ps

mm tck2q fallmg : 5569.48 ps - 5100 ps = 469.48 ps

* Use the same method to measure Tsu, Th, Mm tq2q, Mm tck2q in part2 post-layout simulation and unit size flip flop simulation.



unit size 1 : W/L = 1.5um/0.5um

critical path : D → Q

$C_m = 3.7803fF$

$C_{ont} = 50fF$

measuring C_{in} of unit inverter by ADS:

$C_m = 2.8502fF + 0.9301fF = 3.7803fF$

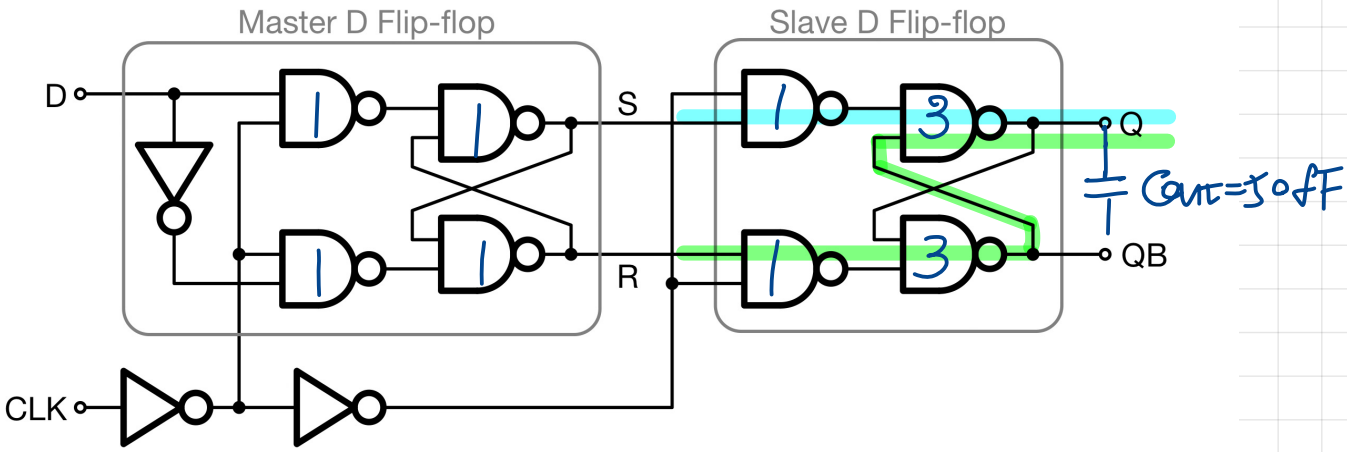
$\therefore F = GBH = 1 \times 1 \times \frac{50fF}{3.7803fF} = 13.2264$

$\therefore f_i = 3.636 \rightarrow$ choose less inverter size : 4

$\therefore$ D → 1 → 4 → Q

$C_m = 3.7803fF$

$C_{ont} = 50fF$



measuring C_{in} of unit inverter by ADS:

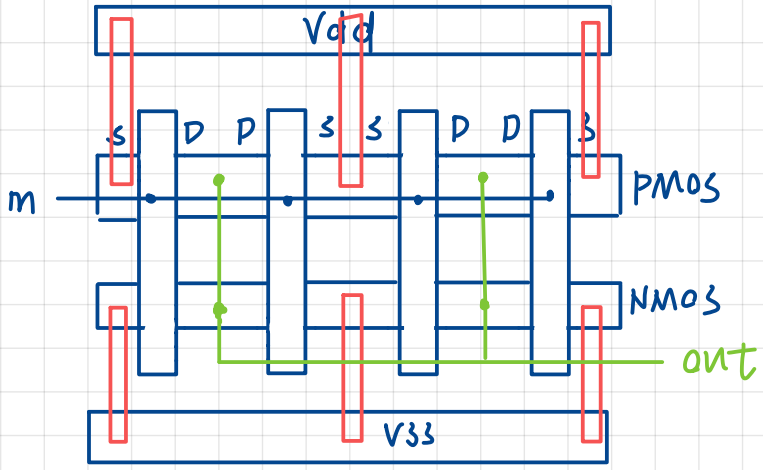
$$C_{in} = 3.3054\ fF + \frac{a9229 + 1.0452}{2}\ fF \cong 4.2895\ fF$$

considering 2 path:

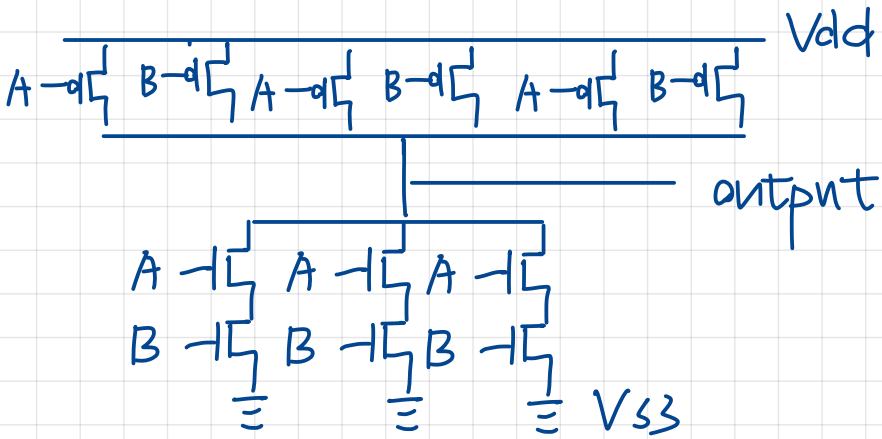
1. : $f_i = \sqrt[2]{F} = \sqrt[2]{\frac{50}{4.2895}} = 3.4141$

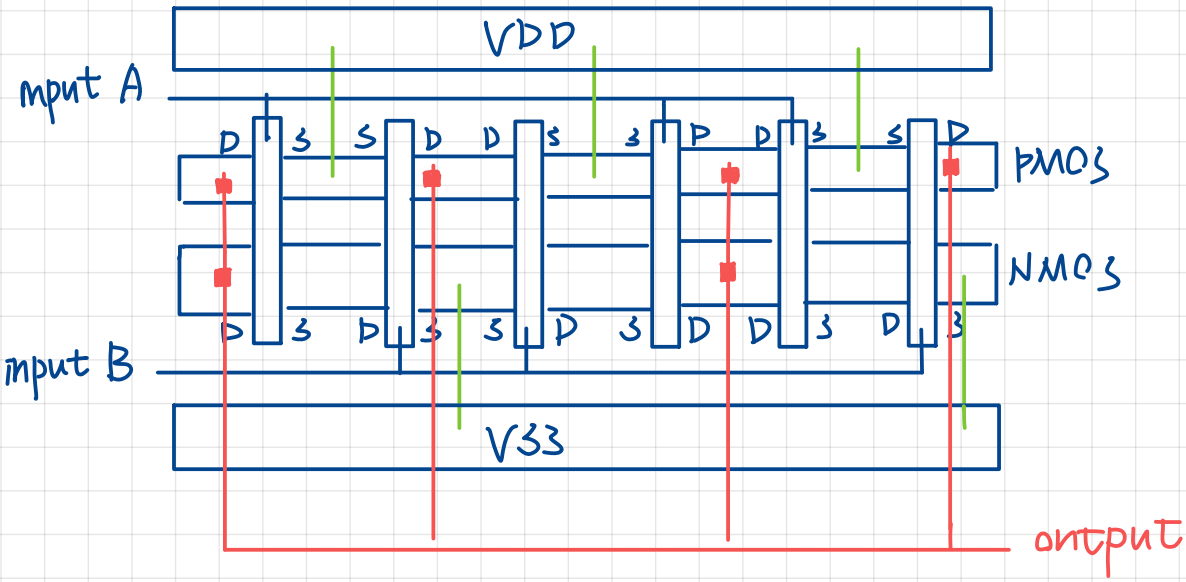
2. : $f_i = \sqrt[3]{F} = \sqrt[3]{\frac{50}{4.2895}} = 2.2673$

∴ In average, I think $n=3$ can improve the performance the most. ⟶ choose $n=3$

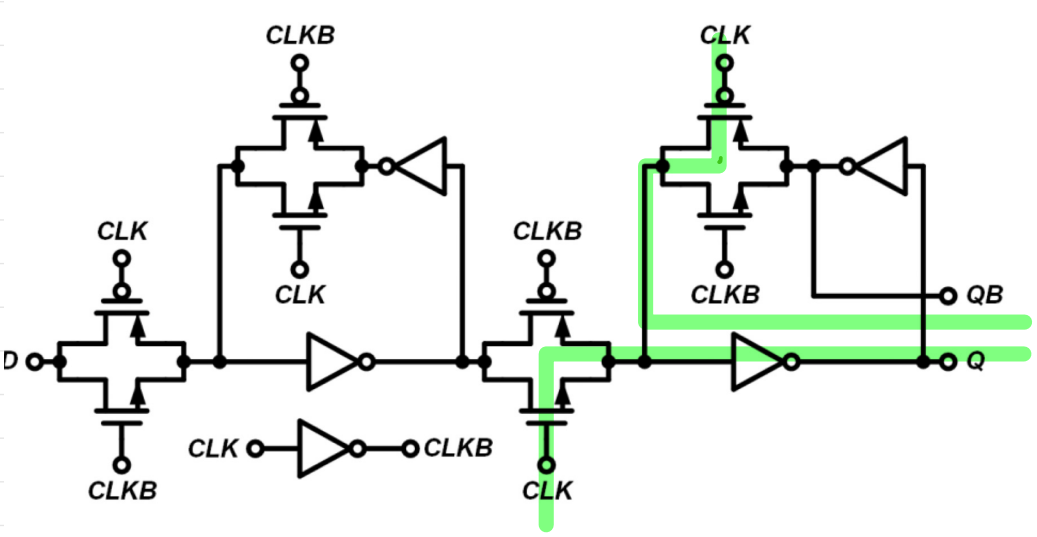


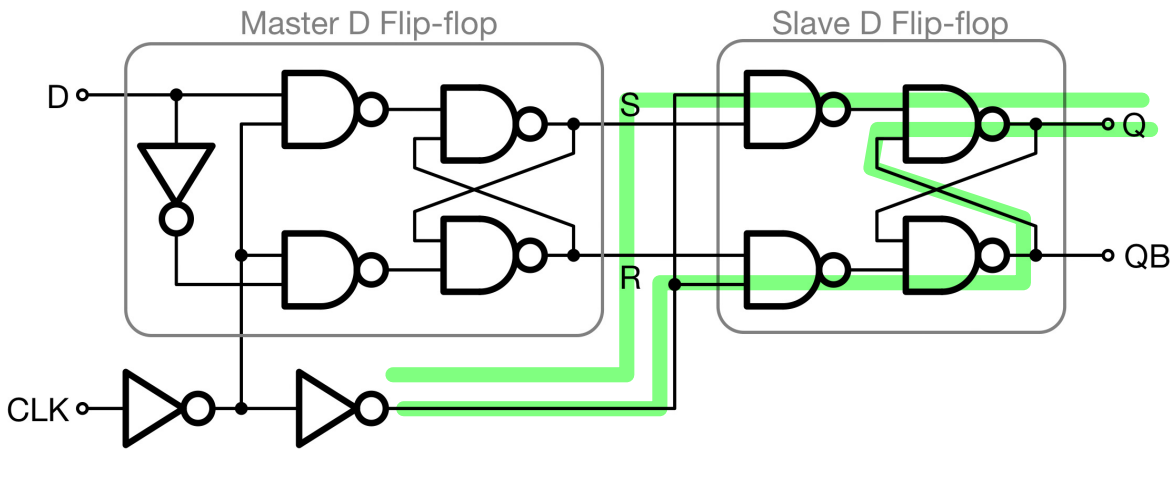
- shared dram and source
- mput gates are connected together
- output drains are connected together





- shared D and S
- 3 gate for an input (m = 3)


CLKB
CLK
CLK
CLKB
CLKB
QB
D
Q
CLK
CLKB
CLKB
CLK


Master D Flip-flop
Slave D Flip-flop
D
S
Q
QB
R
CLK