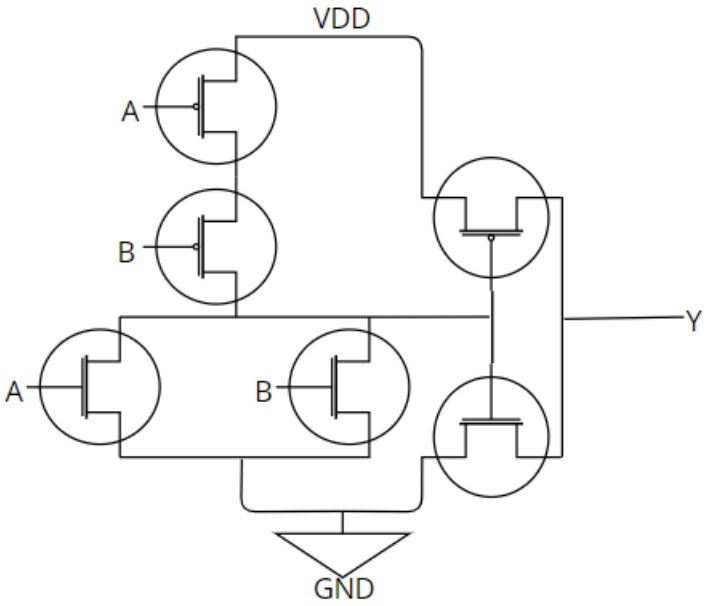
EE3230 VLSI Design (2023 Fall) HW #1

110061217 王彥智

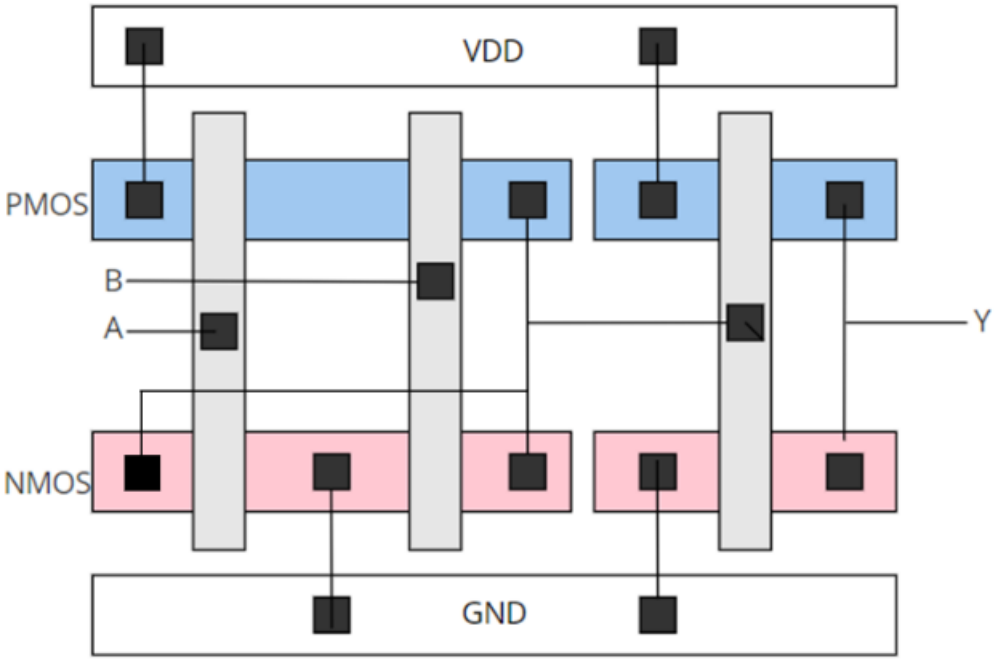
1. Use a combination of CMOS gates with no more than 2 inputs (i.e., NAND2, NOR2, and INV) to generate the schematics in gate-level symbols for the following functions from inputs A, B, and C. Then complete the stick diagrams for each of the following functions according to the schematics you draw.
   a. $Y = \left(\left(\overline{A+B}\right) + \bar{A}\right)B + \ A \rightarrow Y = A + B$=*not (A nor B)*

A	B	$\overline{A+B}$	$\bar{A}$	Y
0	0	1	1	0
0	1	0	1	1
1	0	0	0	1
1	1	0	0	1

Truth table



Gate schematic

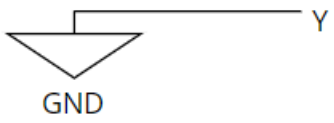


Stick diagrams

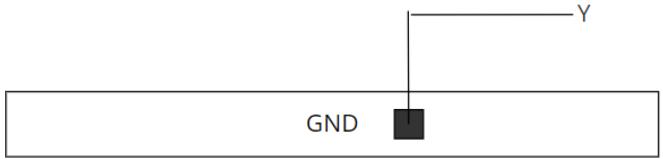
b. $Y = (A + BC)\overline{(A + B)} \rightarrow Y = 0$

A	B	C	A+BC	$\overline{A + B}$	Y
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	0	0
1	1	0	1	0	0
1	1	1	1	0	0

Truth table



Gate schematic



Stick diagrams

c. $Y = (\bar{A}B + A)((\bar{A})(\bar{B}) + C)\overline{(\bar{B} + AC)} \rightarrow Y = \bar{A}BC$

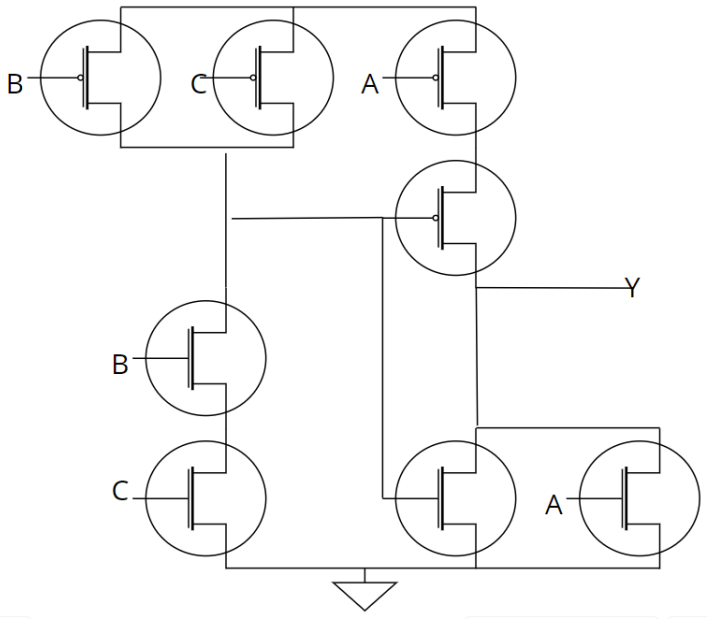
= (notA) and (notB nor notC)

= A nor not(notB nor notC)

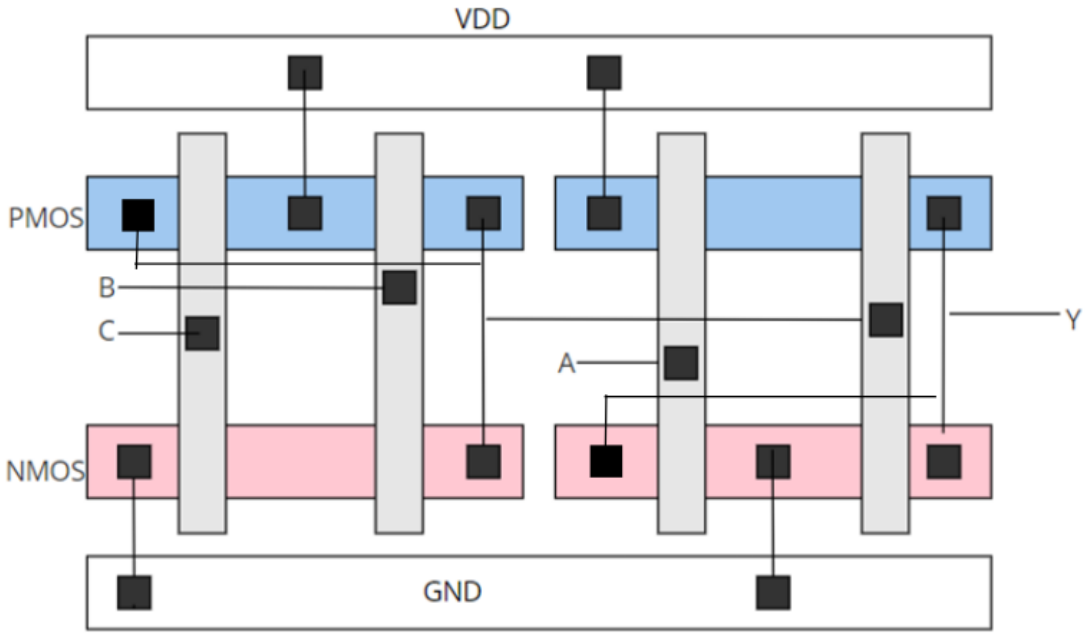
= A nor (B nand C)

A	B	C	$\bar{A}B + A$	$\bar{A}\bar{B} + C$	$\overline{\bar{B} + AC}$	Y
0	0	0	0	1	0	0
0	0	1	0	1	0	0
0	1	0	1	0	1	0
0	1	1	1	1	1	1
1	0	0	1	0	0	0
1	0	1	1	1	0	0
1	1	0	1	0	1	0
1	1	1	1	1	0	0

truth table

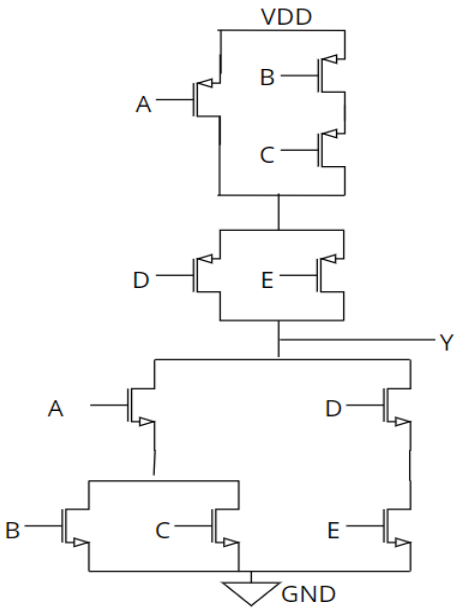


Gate schematic

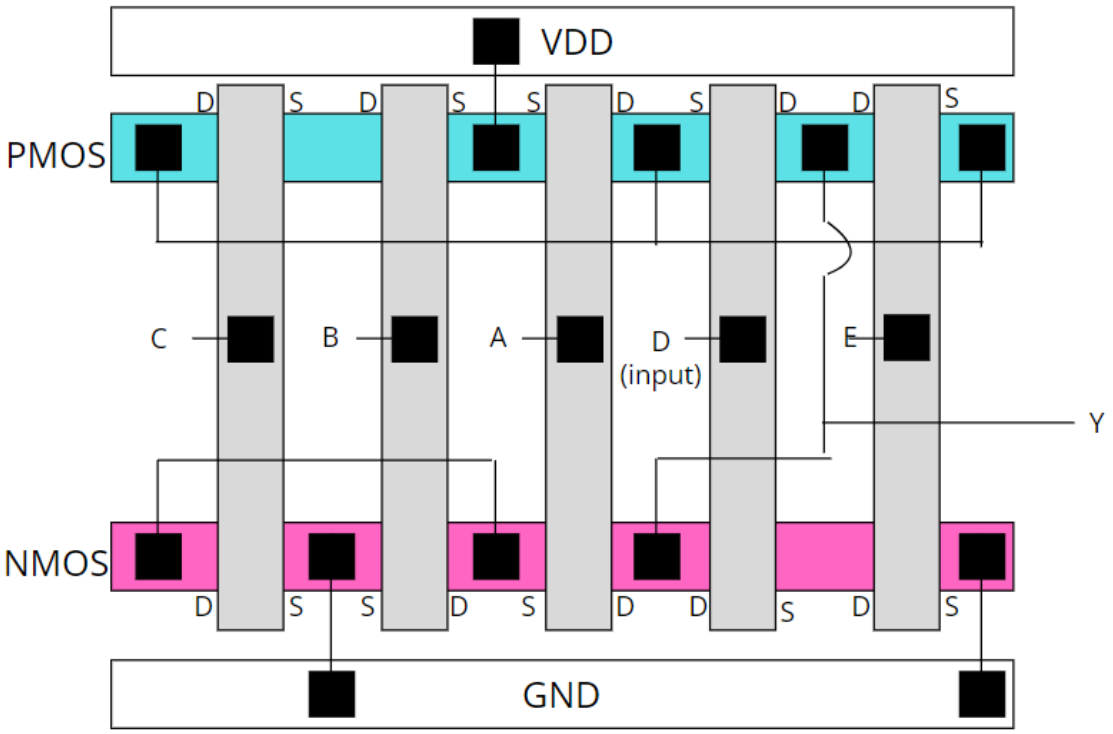


Stick diagrams

2. For the Boolean function of the function$Y = \overline{A(B + C) + DE}$ implement the logic using ONE single complex gate with 5 inputs A, B, C, D, and E. Then complete the stick diagram using only one P+ and one N+ diffusion (without breaks).
   $Y = \overline{A(B + C) + DE} = (\bar{A} + \bar{B}\bar{C})(\bar{D} + \bar{E})$

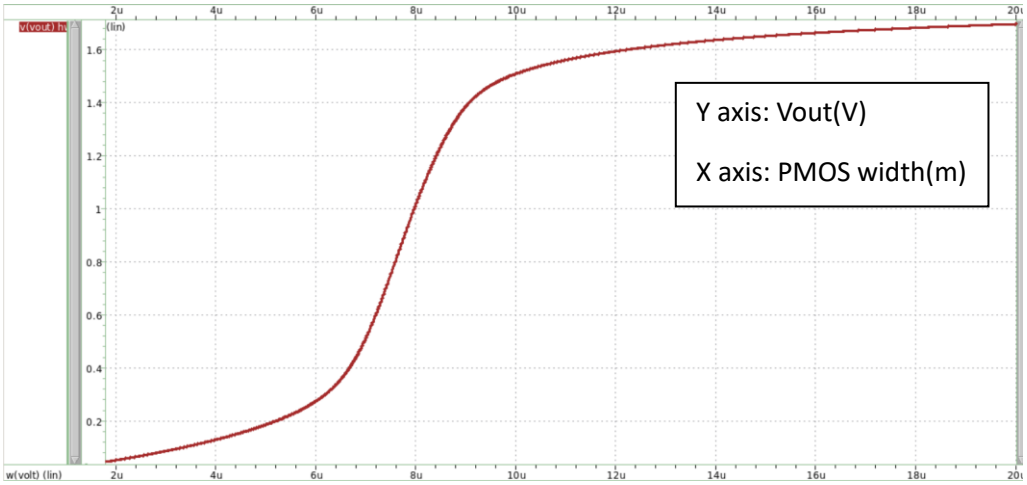


Gate schematic

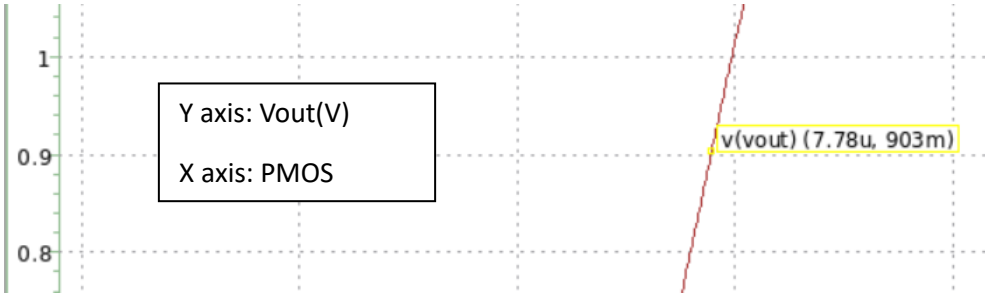


Stick diagrams

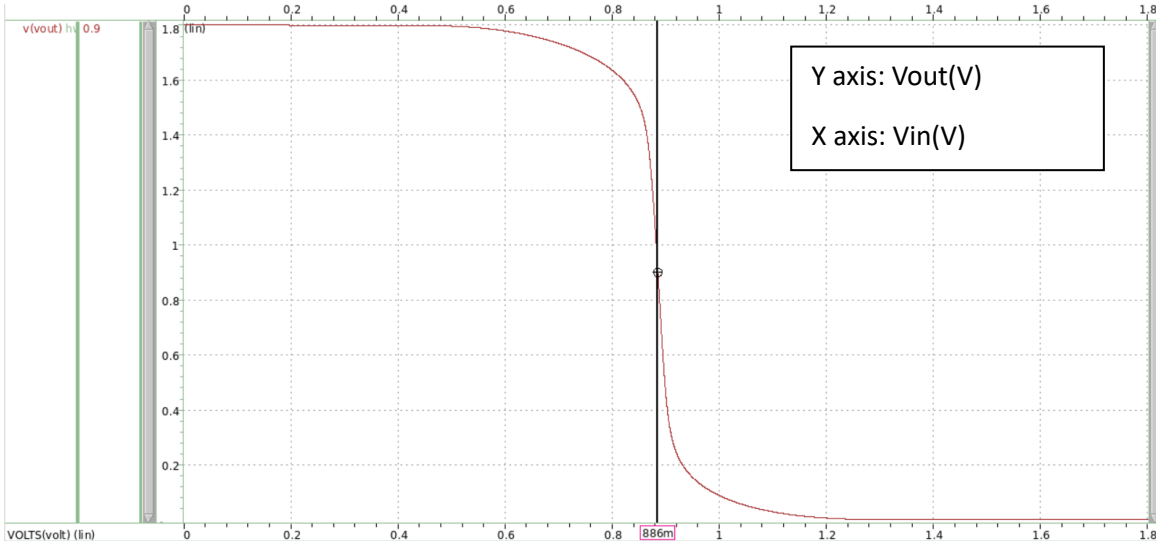
3. Please simulate and analysis a CMOS inverter according to the following conditions using the model provided by TA (CIC018.l).
   * Set the supply voltage to 1.8 V.
   * Set the output load of this inverter to 0.1 pF.
   * Use the channel length of 0.3µm for both NMOS and PMOS.
   * Use the channel width of 1.8µm for NMOS. 3a)
   a. Find the optimal width for PMOS for a balanced trigger point of inverter at tt corner 25°C, report the PMOS size you use, and then report the trigger inputs for the following four corners. The meaning of a trigger input is the input that sets Vout = 0.5×VDD. The meaning of a balanced trigger point is as the following. Vin = Vout = 0.5×VDD



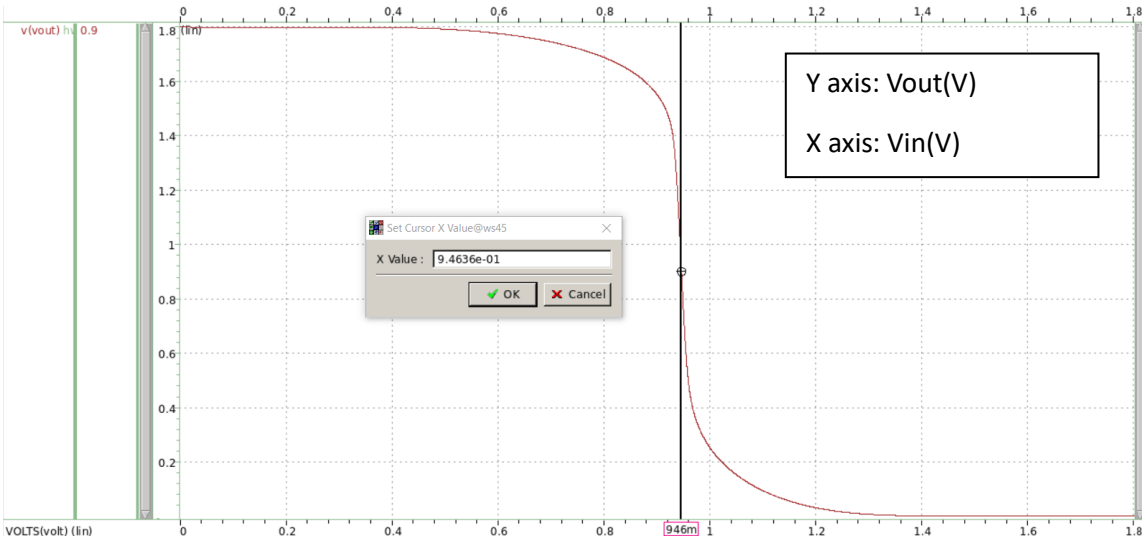
1X: Vout(volt)-PMOS width(um)



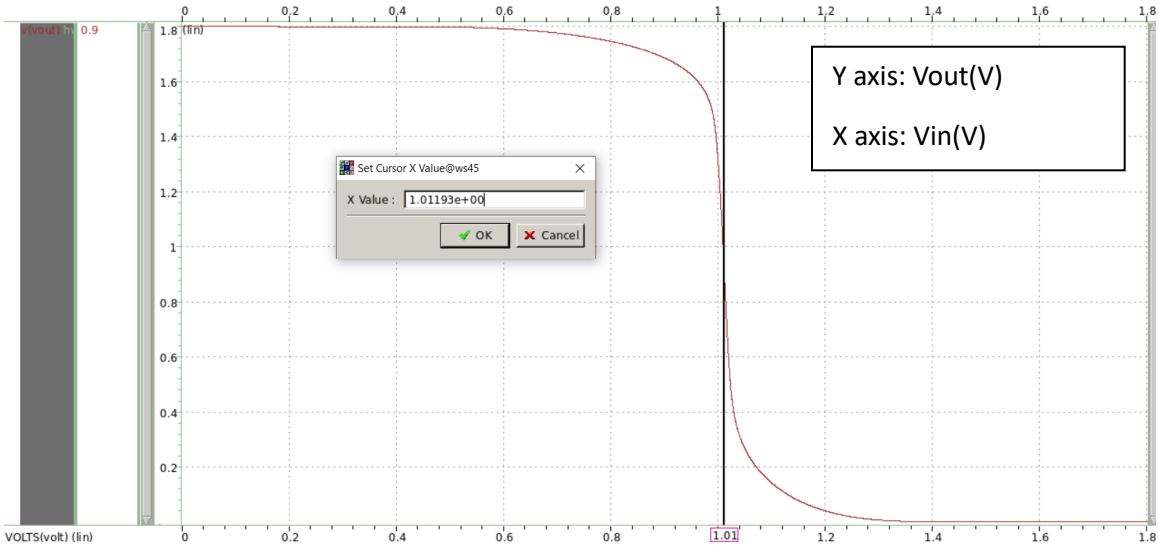
1X: Vout(volt)-PMOS width(um)



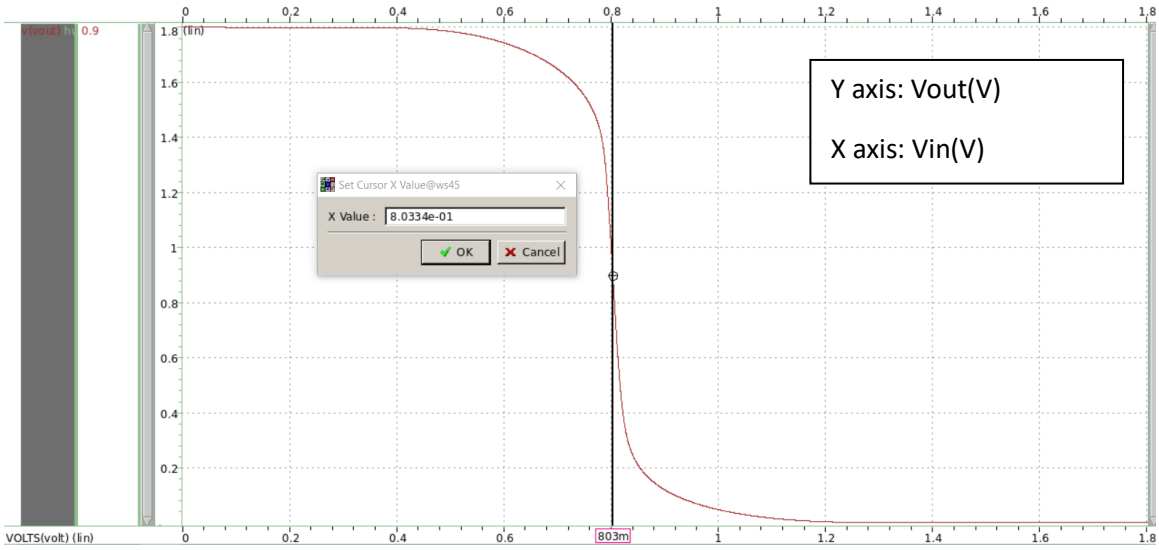
1X ff -40°C: Vout(volt)-Vin(volt)



1X ss 125°C: Vout(volt)-Vin(volt)

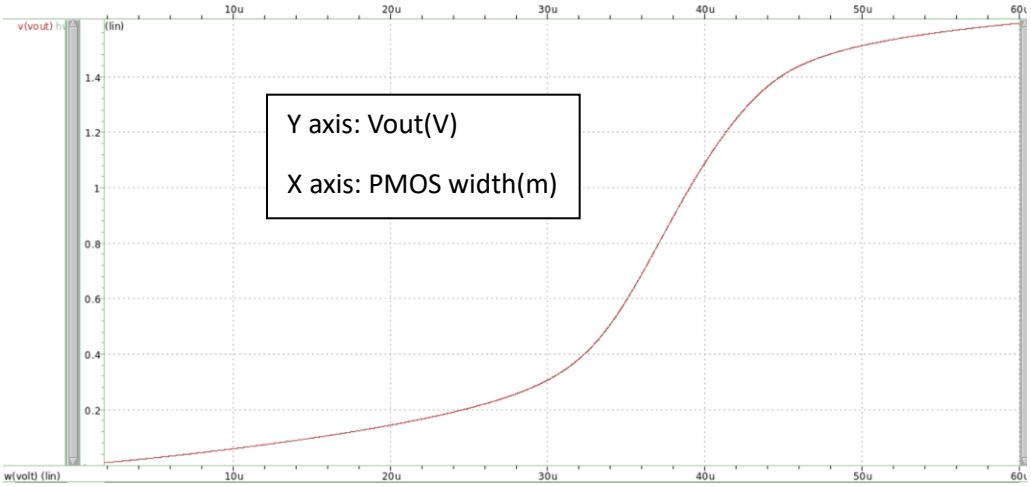


1X sf 25°C: Vout(volt)-Vin(volt)

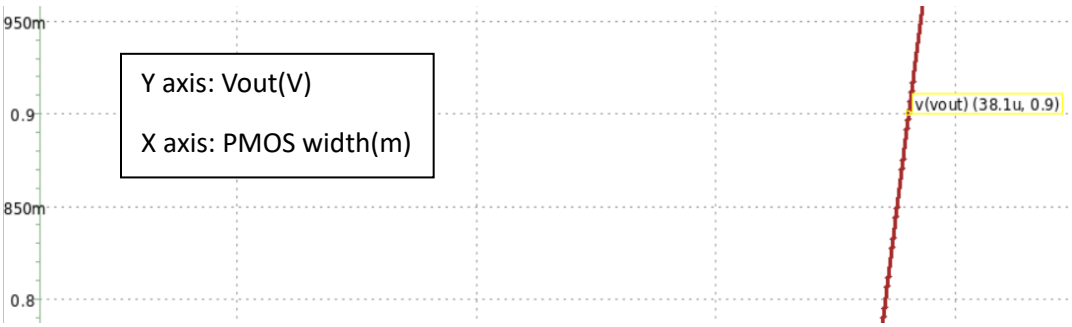


1X fs -40°C: Vout(volt)-Vin(volt)

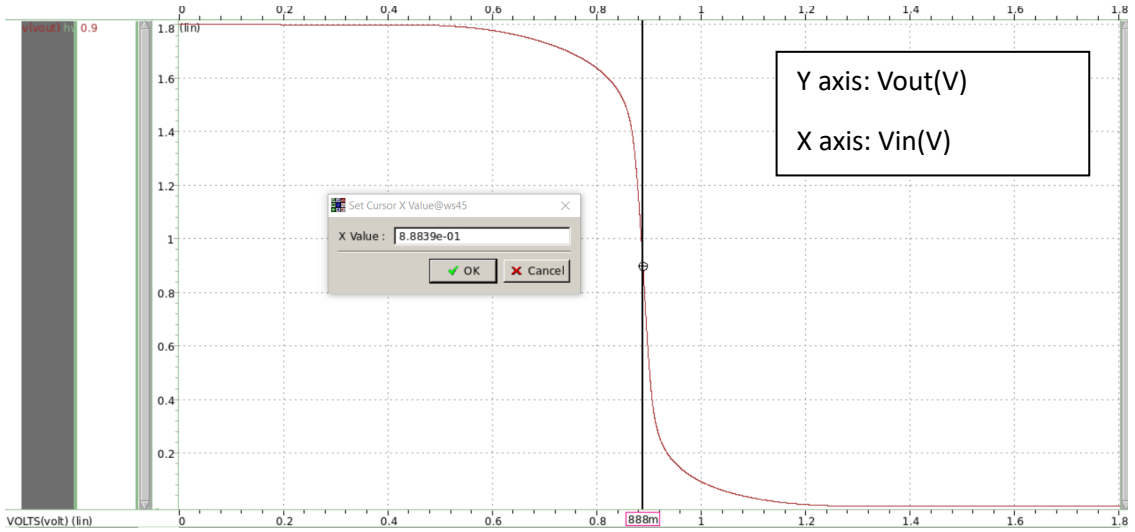
b. Repeat 3a) with 5X the NMOS channel width.



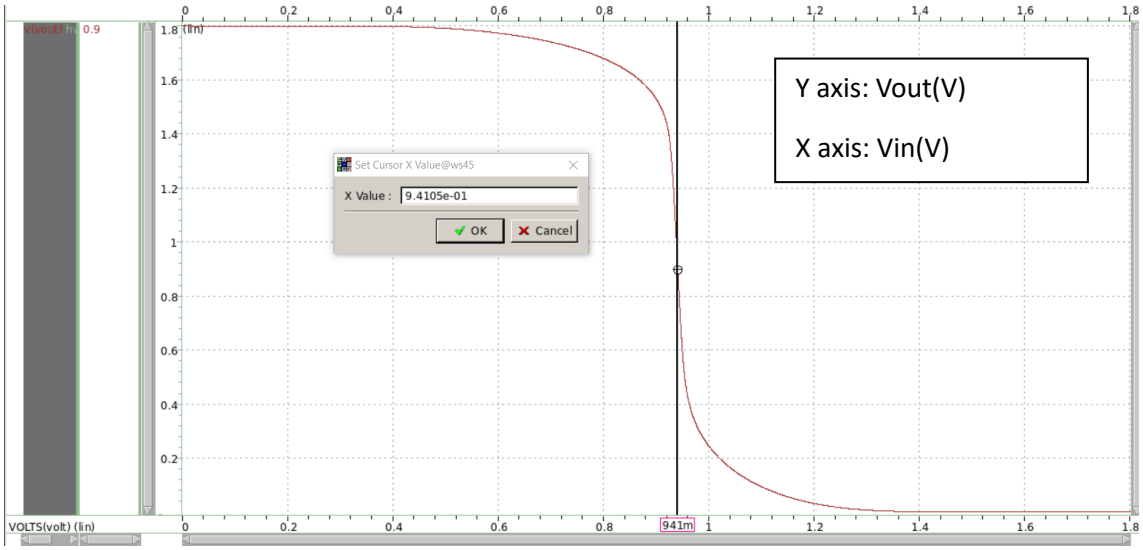
5X: Vout(volt)-PMOS width(um)



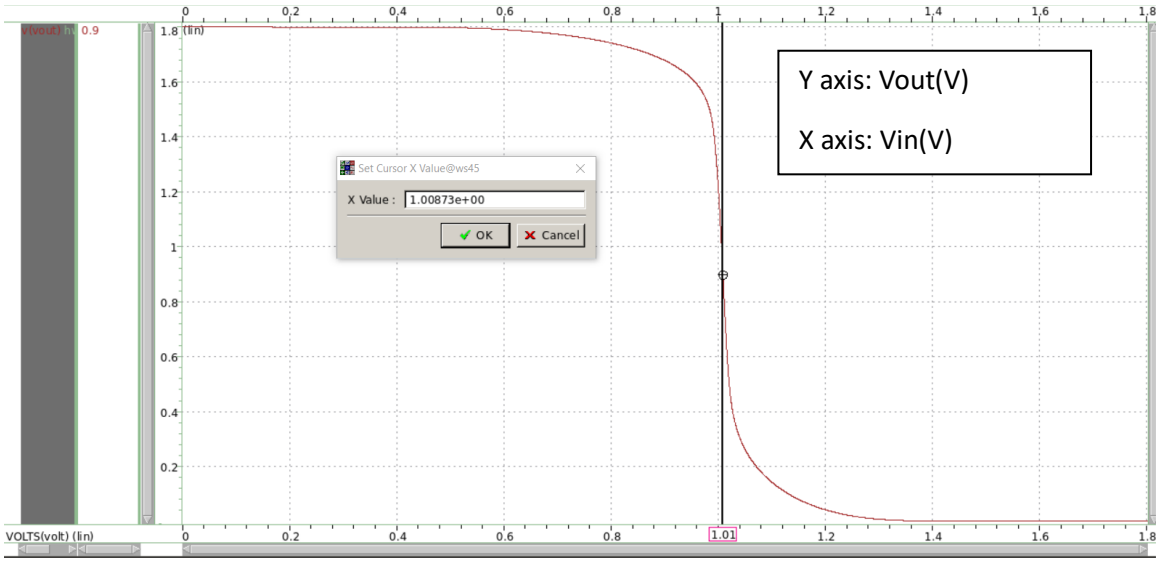
5X: Vout(volt)-PMOS width(um)



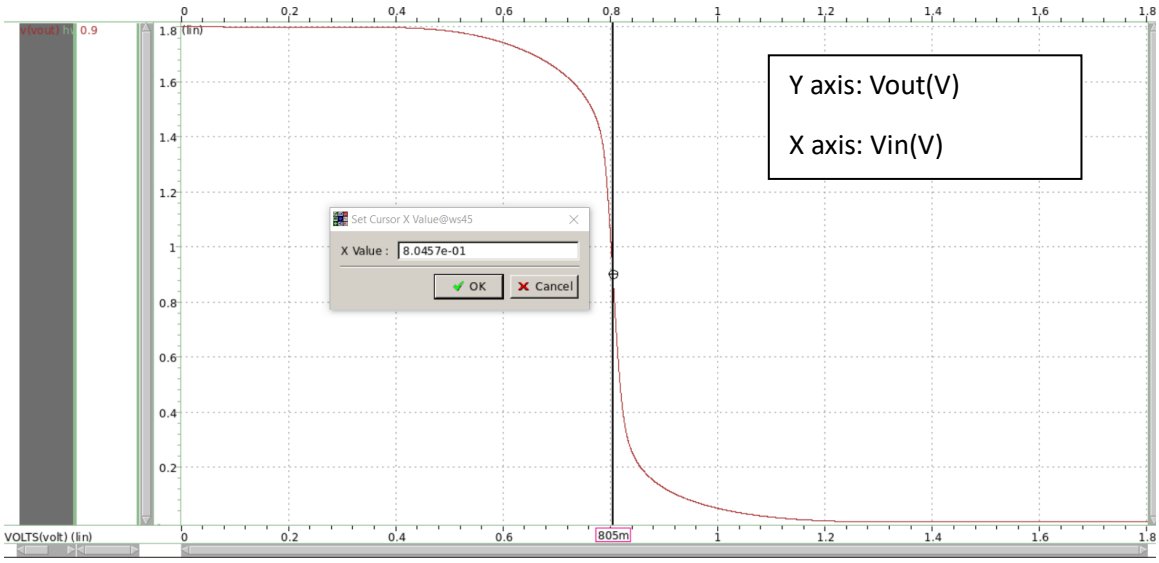
5X ff -40°C: Vout(volt)-Vin(volt)



5X ss 125°C: Vout(volt)-Vin(volt)



5X sf 25°C: Vout(volt)-Vin(volt)

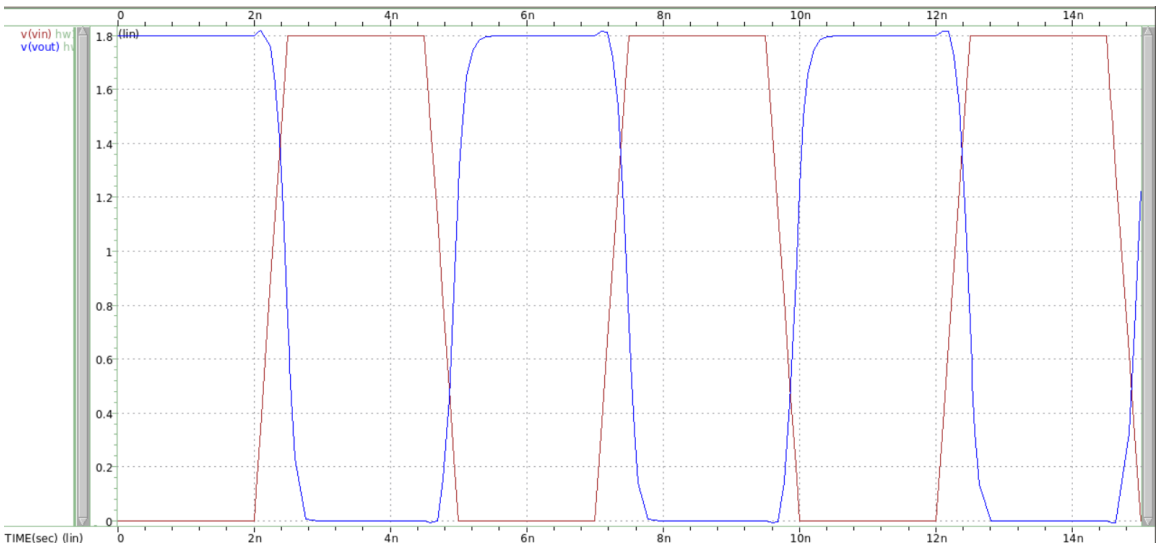


5X fs 125°C: Vout(volt)-Vin(volt)

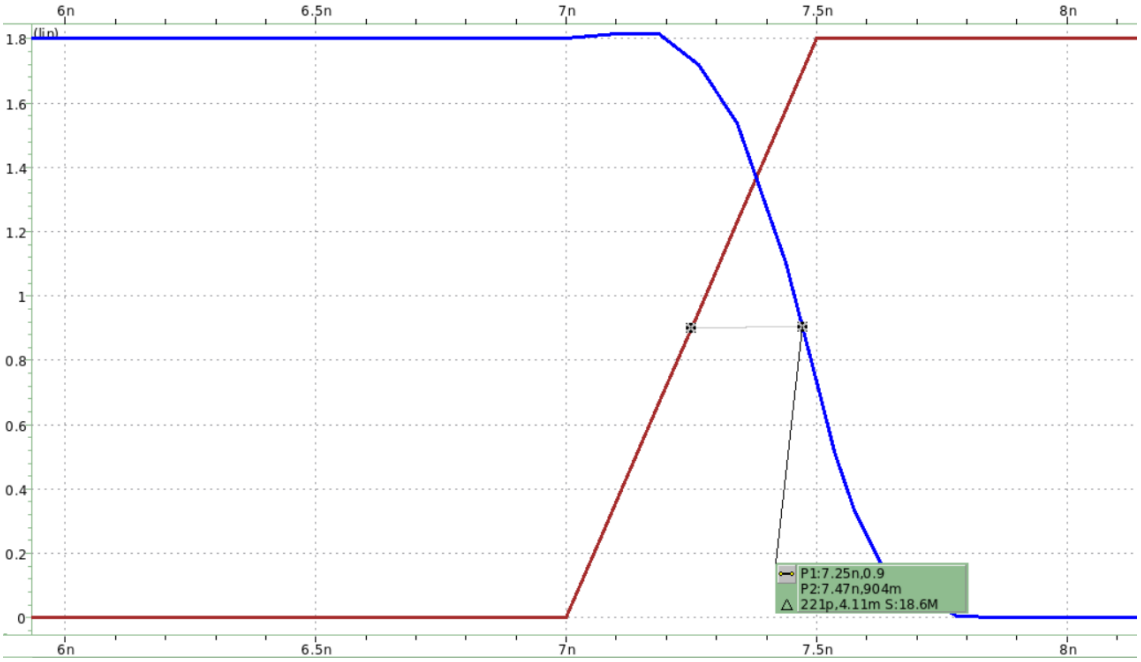
Process	Temperature	NMOS width 1x	NMOS width 5x
		PMOS width (um)	PMOS width (um)
TT	25 C°	7.8um	38.1um
		Trigger input(V)	Trigger input(V)
FF	-40 C°	0.886	0.888
SS	125 C°	0.946	0.941
SF	25 C°	1.012	1.009
FS	25 C°	0.803	0.805

4. Follow the previous question, run transient simulations for all 10 conditions and measure the input to output delay of the inverter. The input to output delay is measured from the input waveform crossing 0.5×VDD to the output waveform crossing 0.5×VDD, as shown in the following figure. In your simulations, use Vpulse for the input signal. Set the rise and fall time (tr and tf) to 500 ps, and the period to 5 ns.

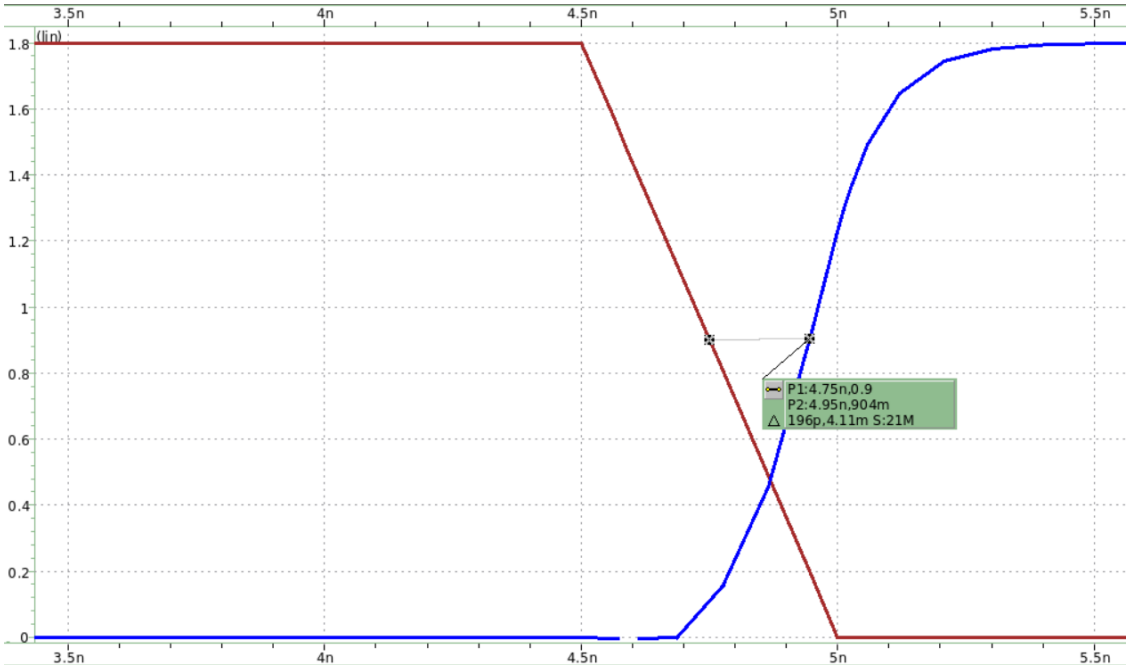
   Attach the simulated waveforms for TT 25°C (with rise and fall time labeled clearly) for both 1X NMOS and 5X NMOS.



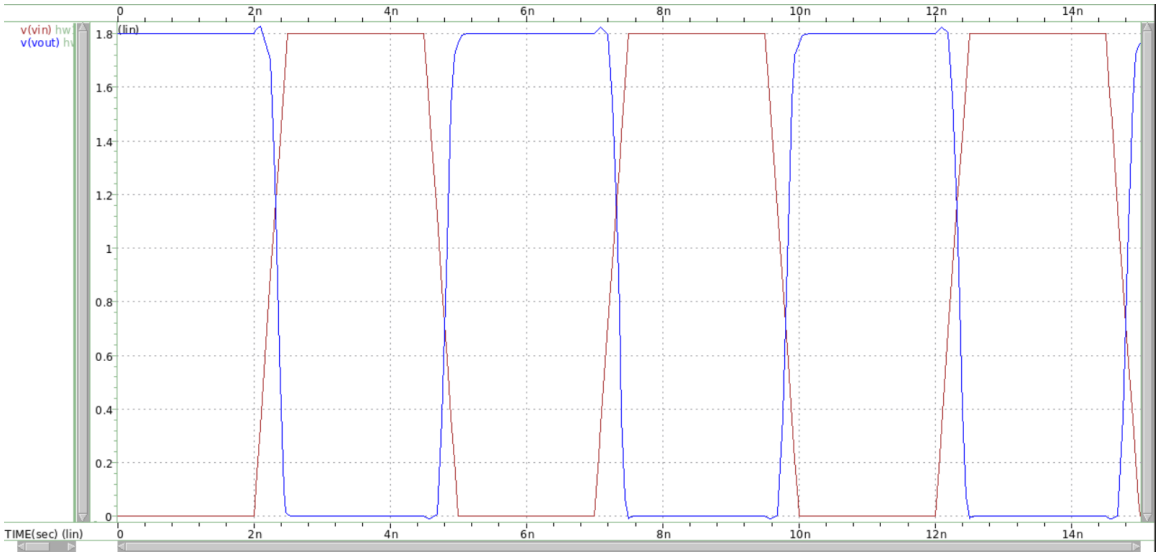
1X tt 25°C: Vin(V) and Vout(V) – time(second)



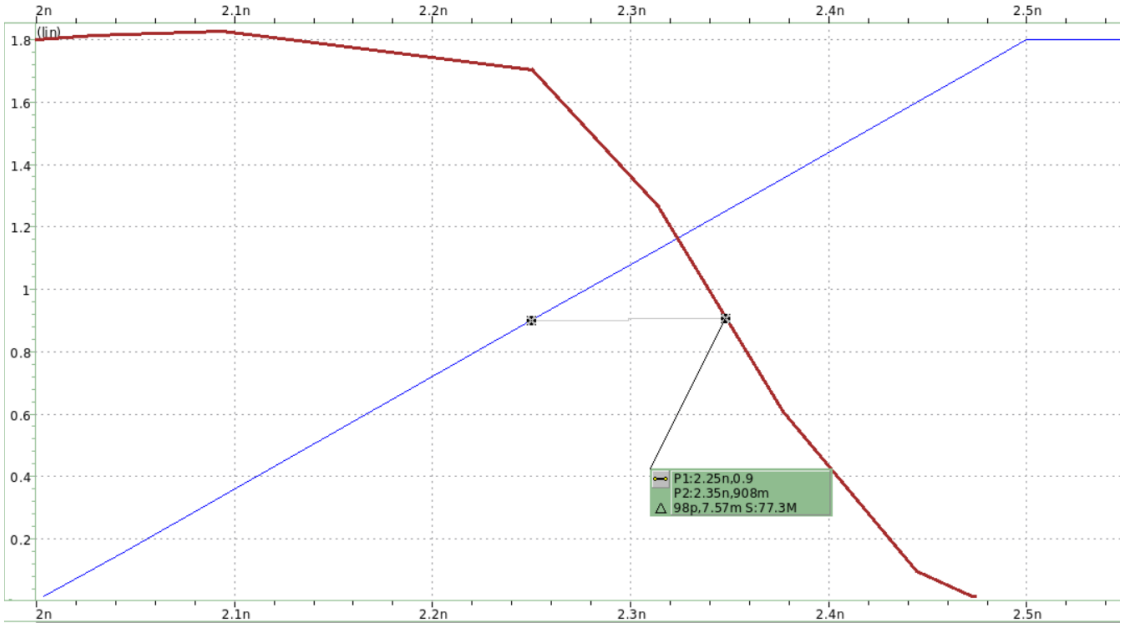
1X tt 25°C, fall delay: Vin(V) and Vout(V) – time(second)



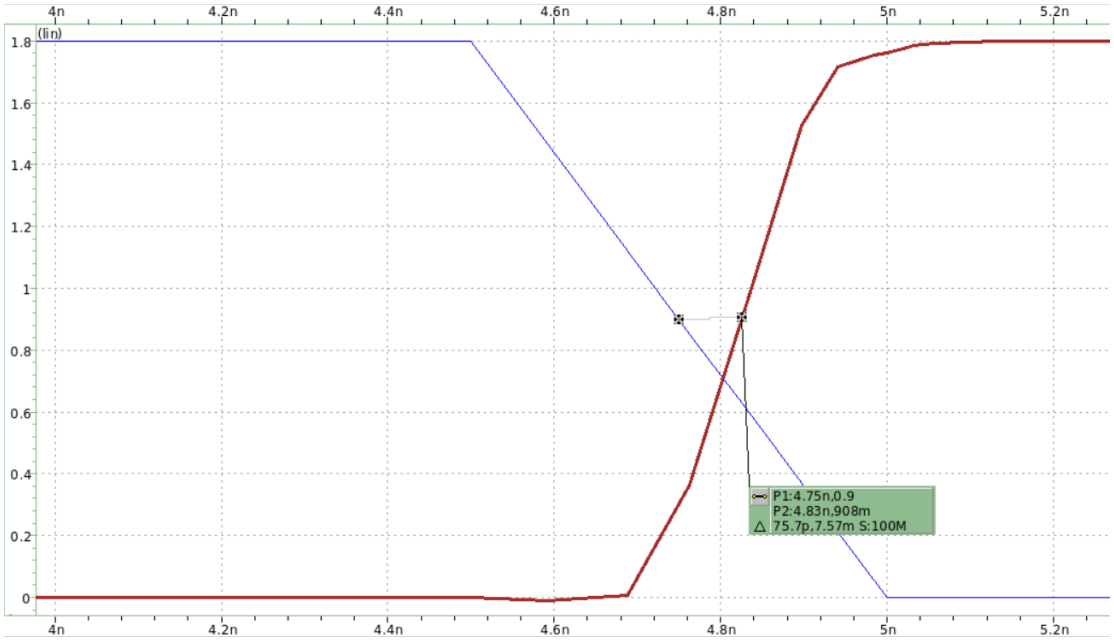
1X tt 25°C, rise delay: Vin(V) and Vout(V) – time(second)



5X tt 25°C: Vin(V) and Vout(V) – time(second)



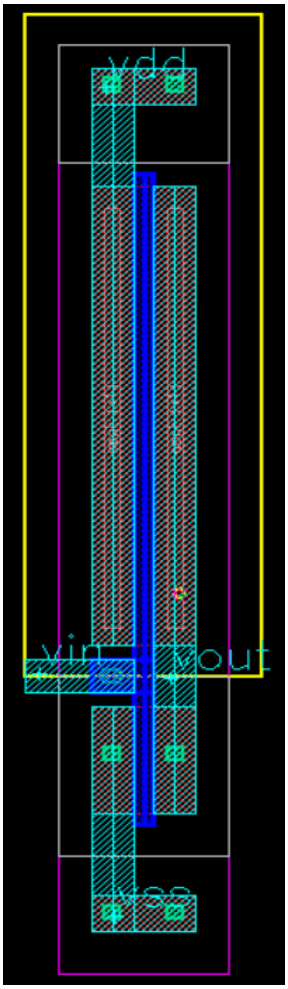
5X tt 25°C, fall edge: Vin(V) and Vout(V) – time(second)



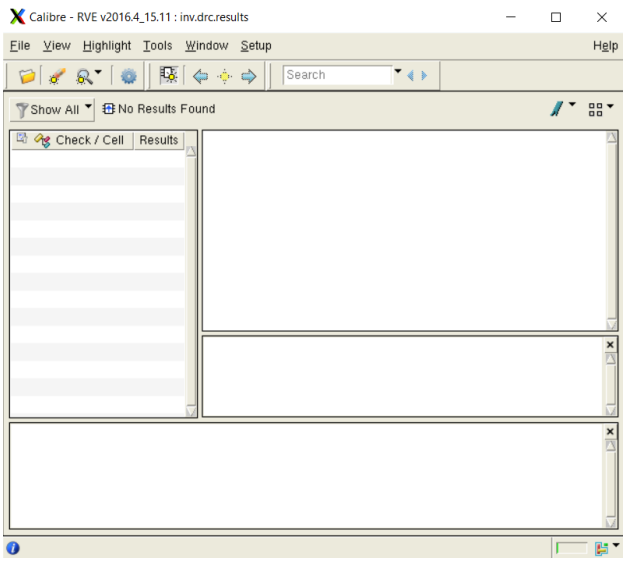
5X tt 25°C, rise edge: Vin(V) and Vout(V) – time(second)

Process	Temperature	NMOS width 1x		NMOS width 5x	
		Fall delay	Rise delay	Fall delay	Rise delay
TT	25 C°	248.4ps	194.9ps	98.75ps	74.88ps
FF	-40 C°	186.3ps	175.2ps	78.55ps	64.03ps
SS	125 C°	388.2ps	267.4ps	192.9ps	134ps
SF	25 C°	313.3ps	180.4ps	152.7ps	69.01ps
FS	25 C°	203.4ps	251.7ps	85.02ps	111ps

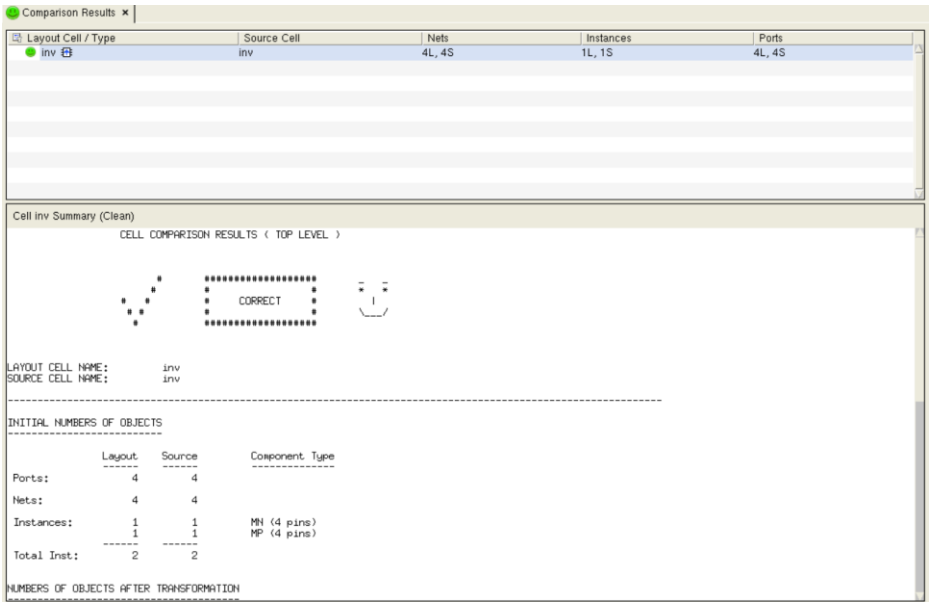
5. Complete the layout, DRC, LVS, and R+C+CC PEX of the inverter in Q3a (with the channel width of 1.8µm). Repeat Q4.



Layout



DRC



LVS

Process	Temperature	NMOS width 1x	
		Fall delay	Rise delay
TT	25 C°	235.1ps	210.8ps
FF	-40 C°	195.6ps	186.7ps
SS	125 C°	397.1ps	286.7ps
SF	25 C°	329.6ps	191.5ps
FS	25 C°	213.2ps	274.0ps