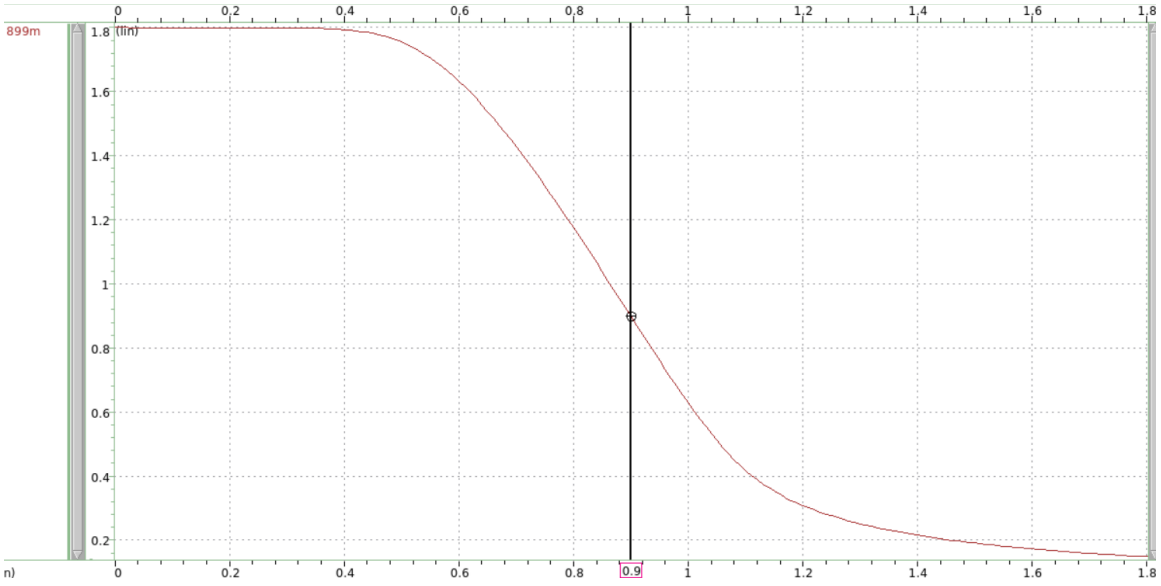
EE3230 VLSI Design HW #2

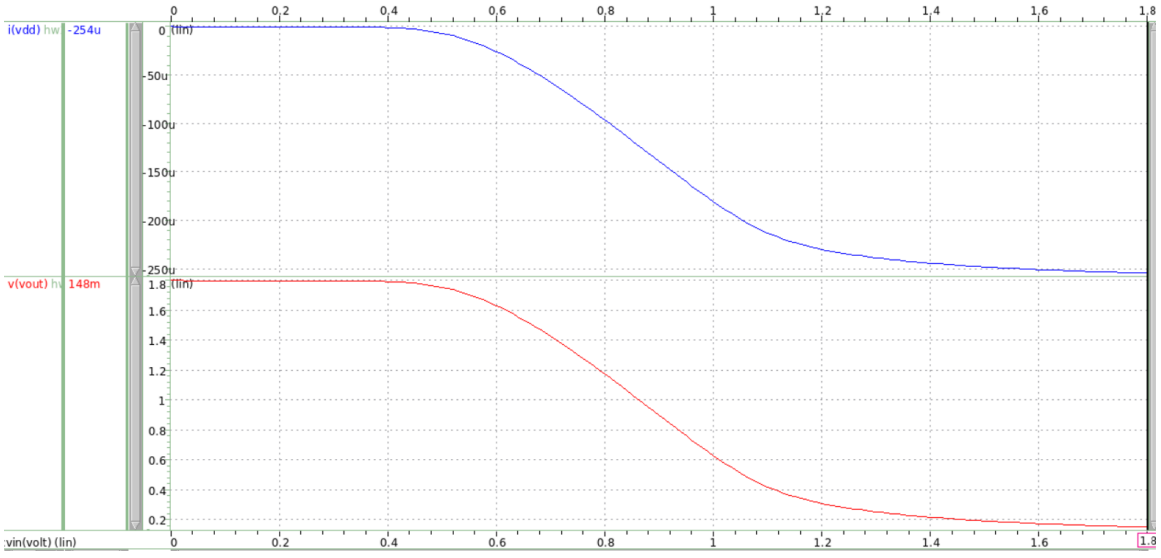
110061217 王彥智

1. Please design an inverter using a NMOS and a resister.
   a. 4680.25Ω, when Vin is 900mv, Vout is 900.00mv.



X axis: Vin(v)-Y axis: Vout(v)

   b. Vout = 148.12mv, I = 254uA and NMOS is operating in triode region.

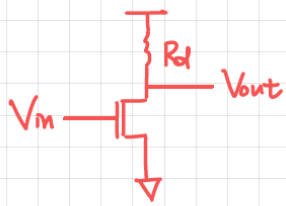


Blue line: X axis: Vin(v)-Y axis: current flow through inverter(I)

Red line: X axis: Vin(v)-Y axis: Vout(v)

   c. Shift left, why?

c.



if $V_{in} = 0.9$

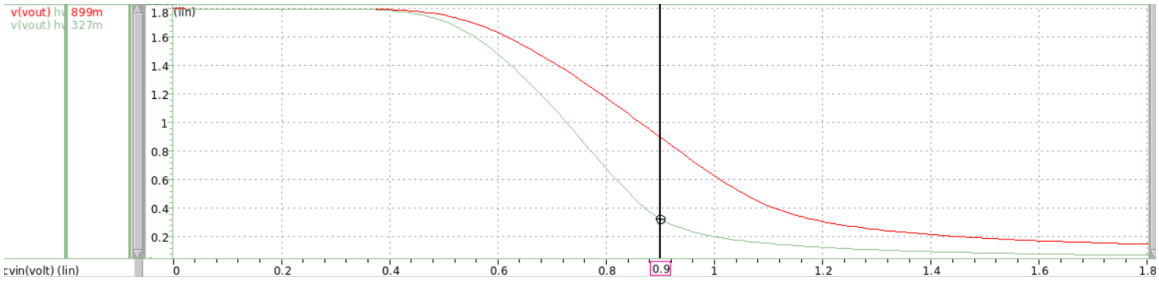
$\rightarrow V_{out} = 1.8 - R_d\left(\frac{1}{2} \times \mu_n C_{ox} \frac{W}{L}(0.9 - V_{th})^2\right)$

when Rd is larger, and other variable are fixed

V_{out} ↓, when Rd ↑

⇒ Vin on transition point ↓, when Rd ↑

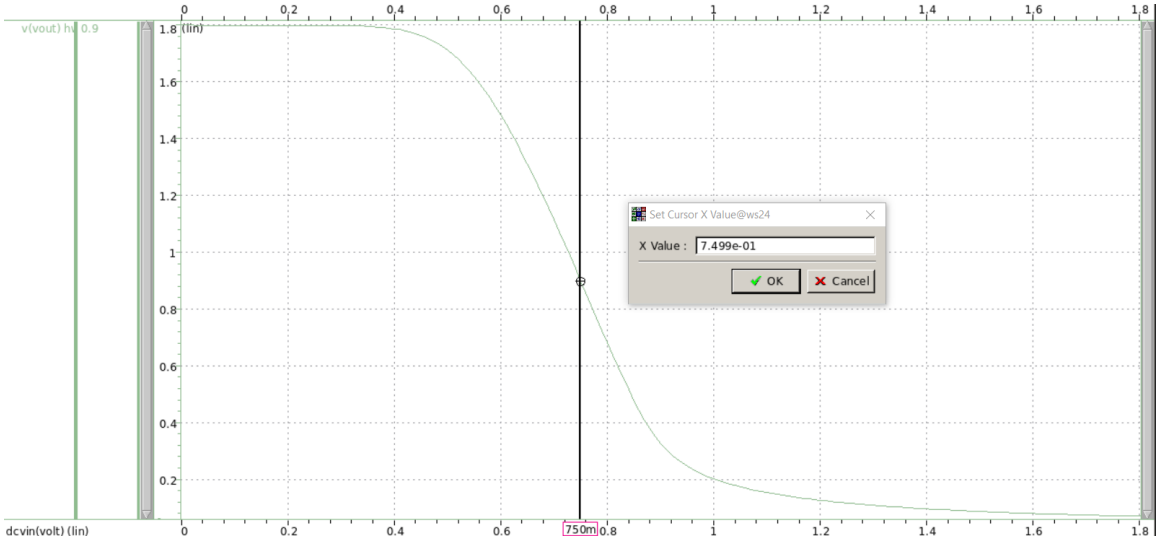
so the transition point shift left when Rd is larger.



X axis: Vin(v)-Y axis: Vout(v)

Red line when r=6480.25; Green line: when r = 2*6480.25

d. Vin0 = 749.91mV



X axis: Vin(v)-Y axis: Vout(v)

e. Find Vil, Voh, Vih and Vol

R(Ω)	Vil(mV)	Voh(mV)	Vih(mV)	Vol(mV)
6480.25	532.13	1726.43	1163.57	339.92
12960.50	478.21	1739.25	966.44	229.56

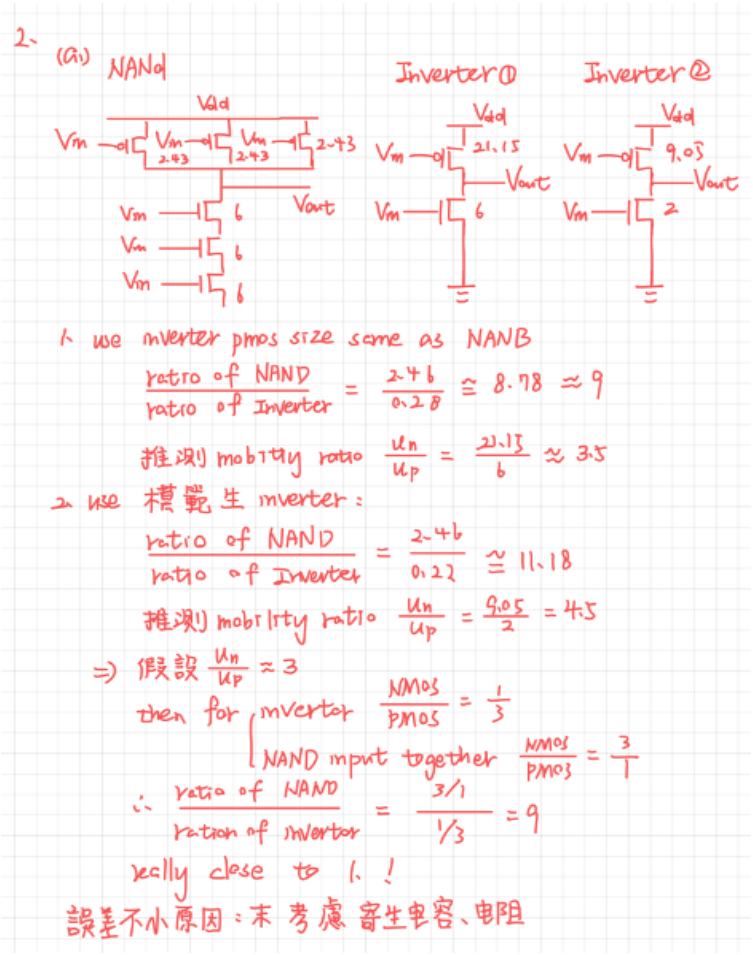
f. Noise margin

R(Ω)	NML(mV)	NMH(mV)
6480.25	192.21	562.86
12960.50	248.65	772.81

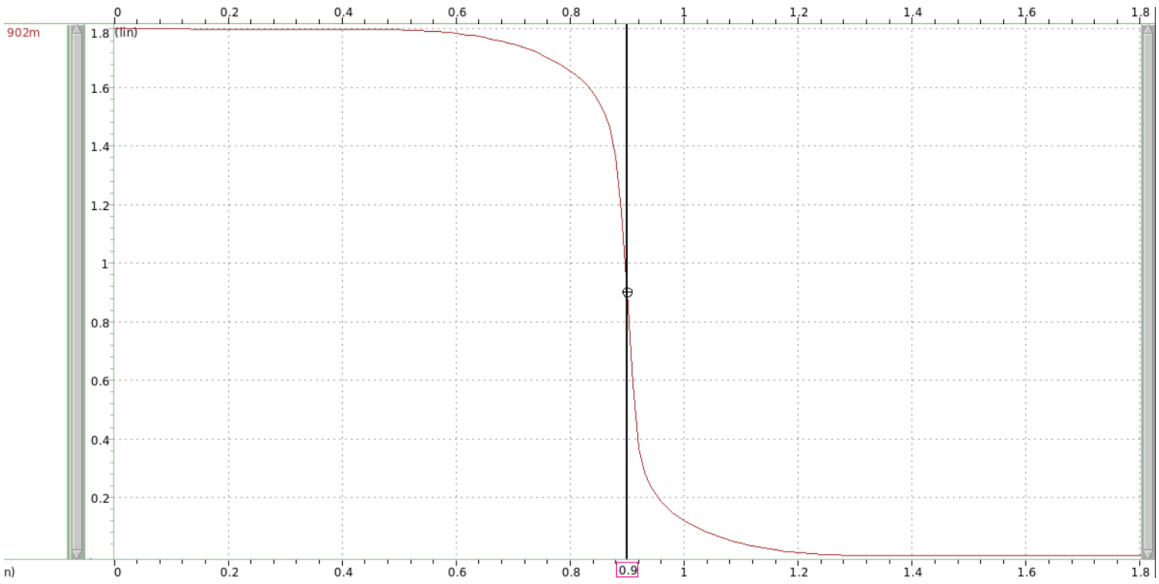
2. CMOS 3-input NAND gate

a. Ratio

Gate	NMOS(W/L)	PMOS(W/L)	NMOS/PMOS
NAND	1.2u/0.2u = 6.00	0.486u/0.2u = 2.43	6/2.43 = 2.46
Inverter	1.2u/0.2u = 6.00	4.23u/0.2u = 21.15	6/21.15 = 0.28
Inverter(模範生)	0.4u/0.2u = 2.00	1.81u/0.2u = 9.05	2/9.05 = 0.22



b. DC voltage transfer



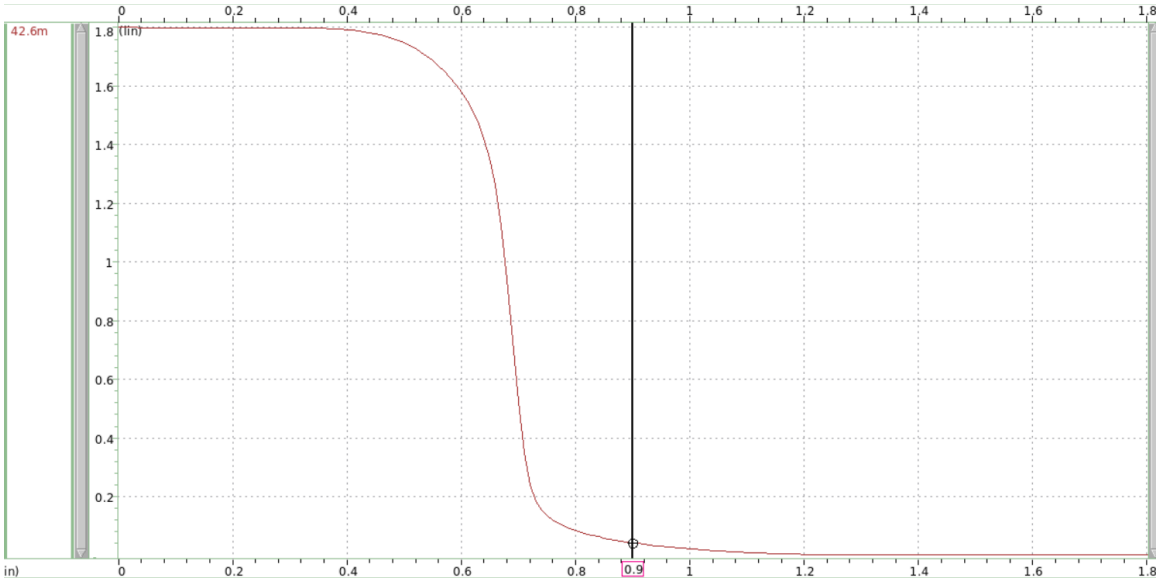
X axis: Vin(v)-Y axis: Vout(v)

c. Find Vil, Voh, Vih and Vol

NAND	Vil(mV)	Voh(mV)	Vih(mV)	Vol(mV)
Three input	771.05	1692.63	1023.15	96.52

NAND	NML(mv)	NMH(mV)
Three input	674.53	669.48

d. DC voltage transfer



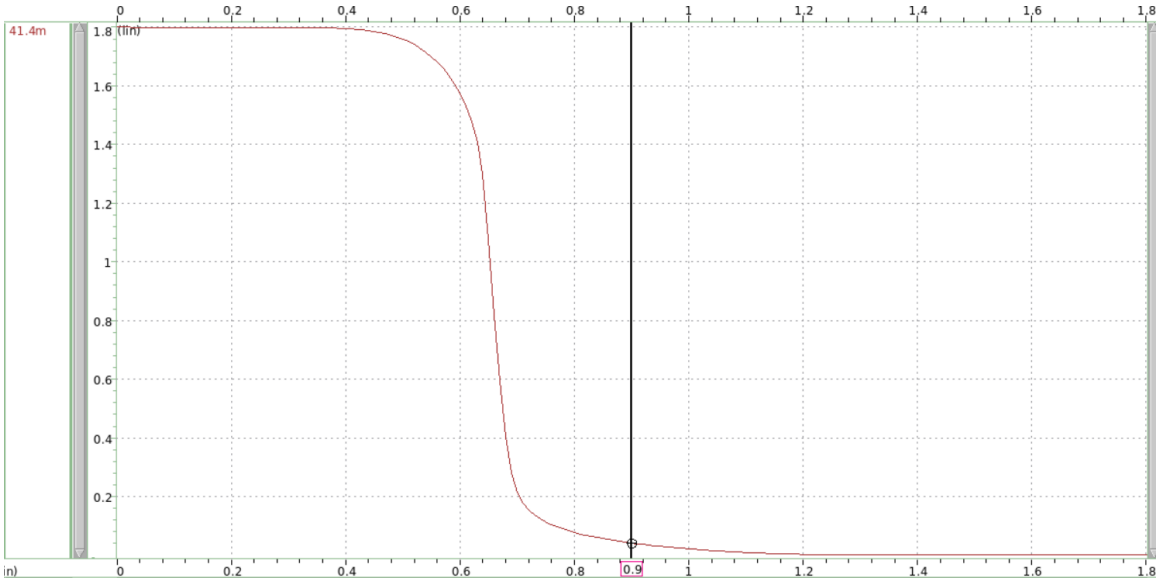
X axis: Vin(v)-Y axis: Vout(v)

e. Find Vil, Voh, Vih and Vol

NAND	Vil(mV)	Voh(mV)	Vih(mV)	Vol(mV)
VinC	515.23	1733.41	778.30	101.46

NAND	NML(mv)	NMH(mV)
VinC	413.77	955.11

f. DC voltage transfer



X axis: Vin(v)-Y axis: Vout(v)

g. Find Vil, Voh, Vih and Vol

NAND	Vil(mV)	Voh(mV)	Vih(mV)	Vol(mV)
VinA	520.81	1740.62	754.87	109.12

NAND	NML(mv)	NMH(mV)
VinA	411.69	985.75

h. Explain

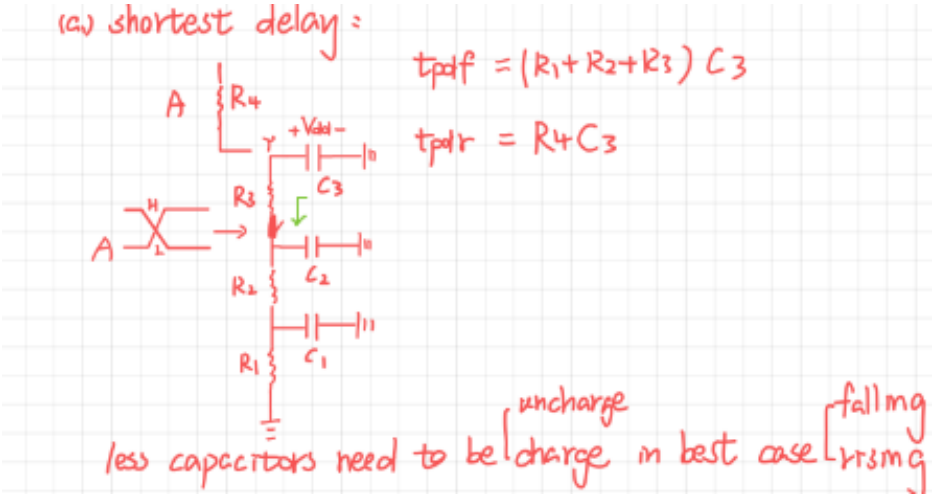
NAND	Vil(mV)	Voh(mV)	Vih(mV)	Vol(mV)
Three input	771.05	1692.63	1023.15	96.52
VinC	515.23	1733.41	778.30	101.46
VinA	520.81	1740.62	754.87	109.12

NAND	NML(mv)	NMH(mV)
Three input	674.53	669.48
VinC	413.77	955.11
VinA	411.69	985.75

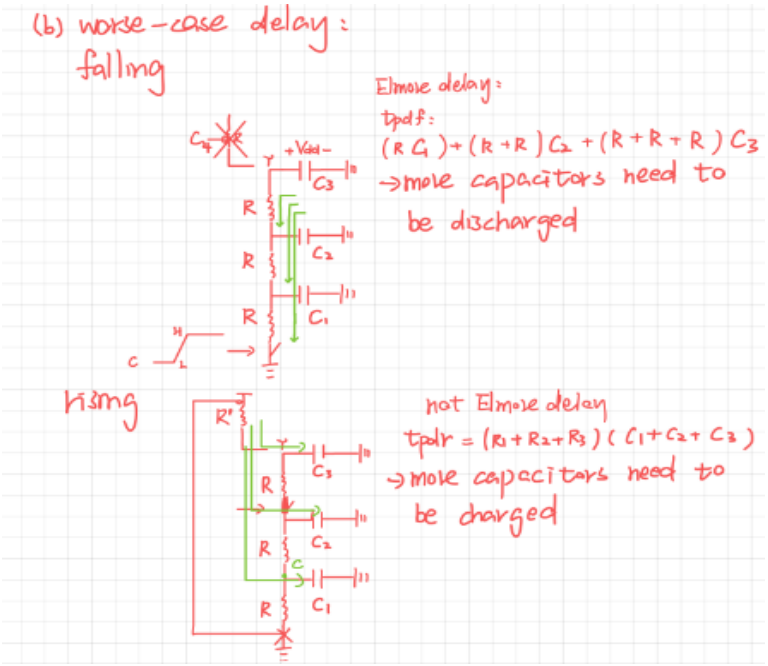
Effective beta ratio of tree different operation: Three input > VinC ≥ VinA

When the effective beta ratio of the NAND3 gate will be lower, Vout will falls earlier, transition point will shift left, NML will decrease and NMH will increase.

3. Simulate NAND gate with C_{load} of 20fF
   a. Explain shortest delay
      Rising: switch C from 1 to 0, hold A and B at 1
      Falling: switch C from 0 to 1, hold A and B at 1



   b. Explain worse case propagation delays
      Rising: switch A from 1 to 0, hold B and C at 1
      Falling: switch A from 0 to 1, hold B and C at 1

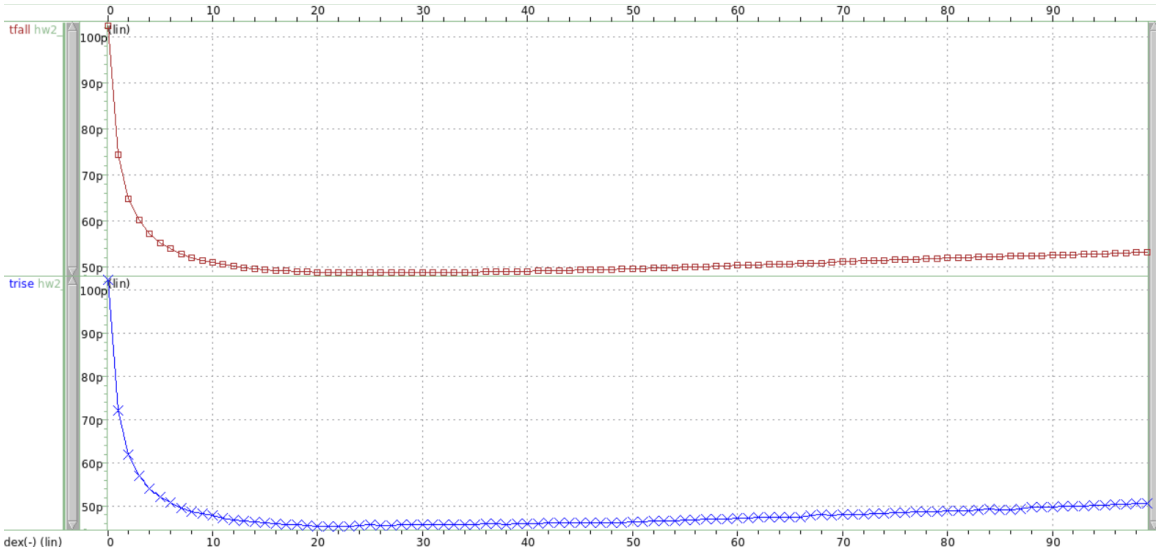


c. 5corner
d. sp netlist

Process	Temperature	tcdr(ps)	tcdf(ps)	tpdr(ps)	tpdf(ps)
TT	25	241.81	80.93	326.21	100.31
FF	-40	192.82	61.08	255.82	72.49
SS	125	517.73	209.90	751.85	283.71
SF	25	214.01	161.21	299.36	213.20
FS	25	441.82	69.26	603.81	84.11

4. M factors of NAND gate
   a. Propagation delay
      tpdf: 102.21ps
      tpdr: 102.35ps
      tpd = (102.21 + 102.35) / 2 = 102.28ps

   b. m value
      When m < 25: Increasing the size of all transistors, which will let NAND3 gate is able to drive the load capacitance more easily, and the gate capacitance doesn't increase a lot at this point, so the delay is shorter.
      When m > 25: The gate capacitance will be too large as we increase m. Although driving capability increases, the parasitic delay which is affected by the gate capacitance overweighs the increase of driving capability.



Redline: X axis: m value-Y axis: tpdf(s)

Blueline: X axis: m value-Y axis: tpdr(r)