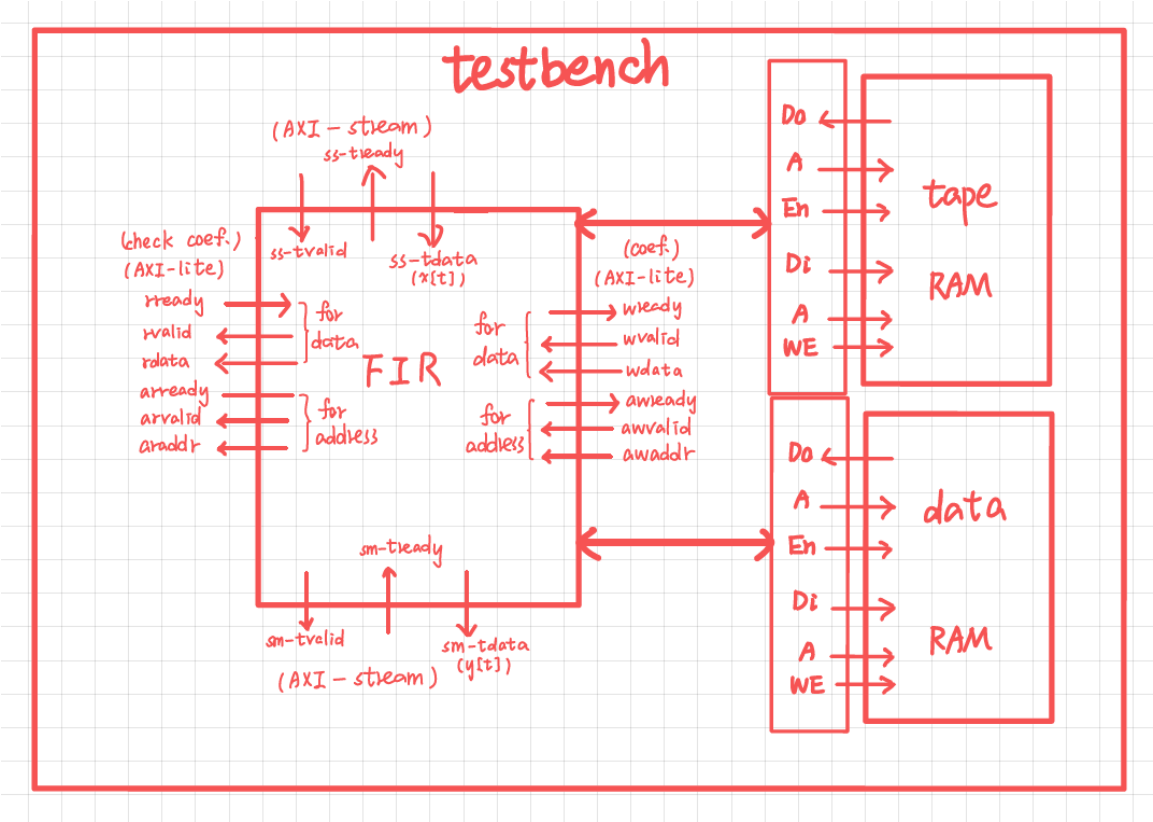
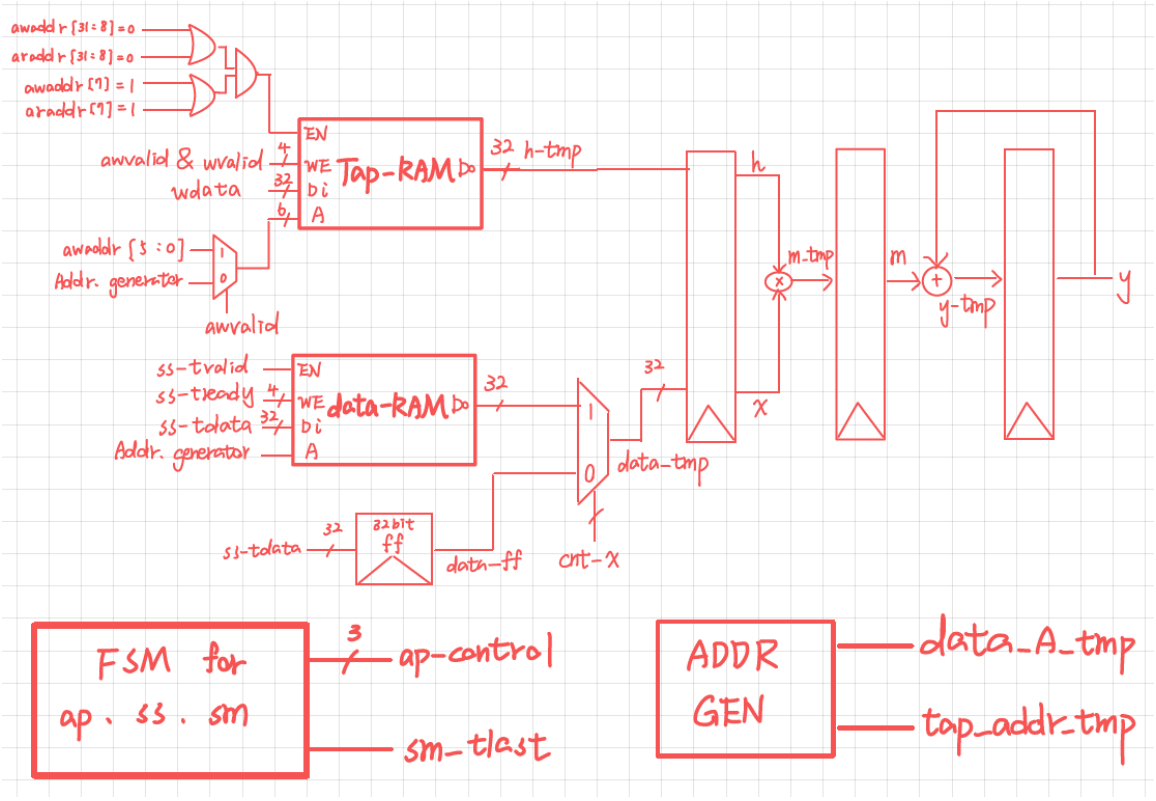
Lab3 report

- Introduction about the overall system
  - What is FIR
    The term FIR abbreviation is “Finite Impulse Response” and it is one of two main types of digital filters used in DSP applications. This is its formula:
    $$y[t]= \sum(h[i]*x[i-t])$$
  - Overall design
    - Block diagram

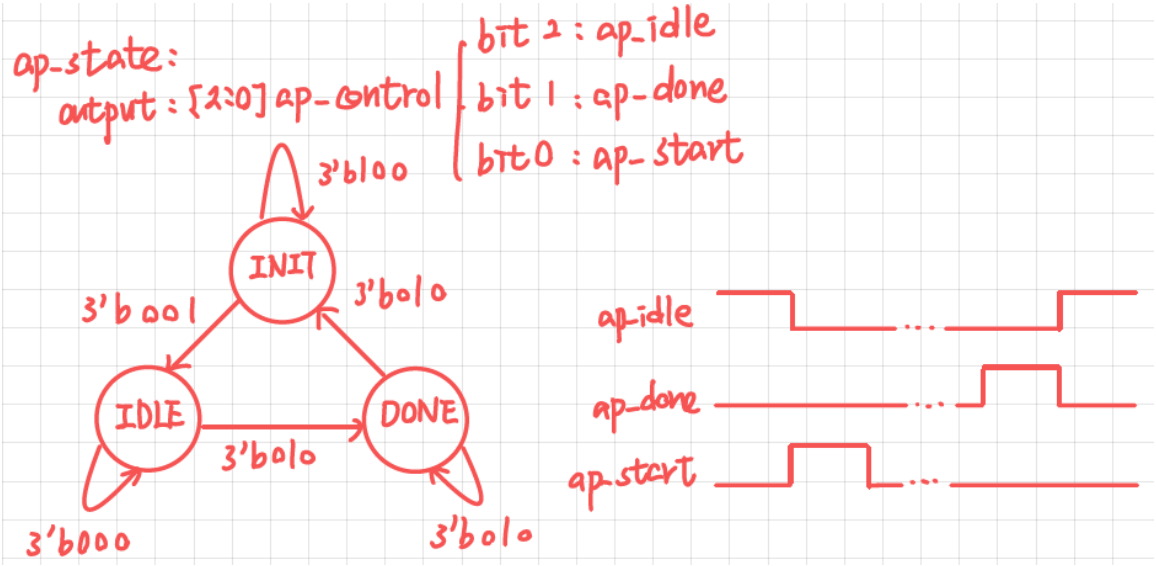


Overall view

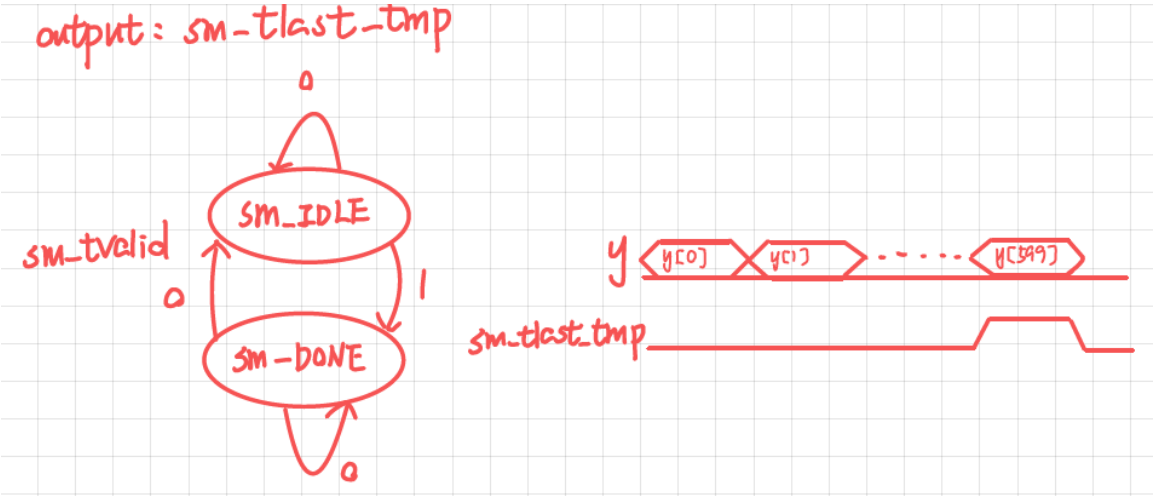


Block design in FIR

- Finite state machine

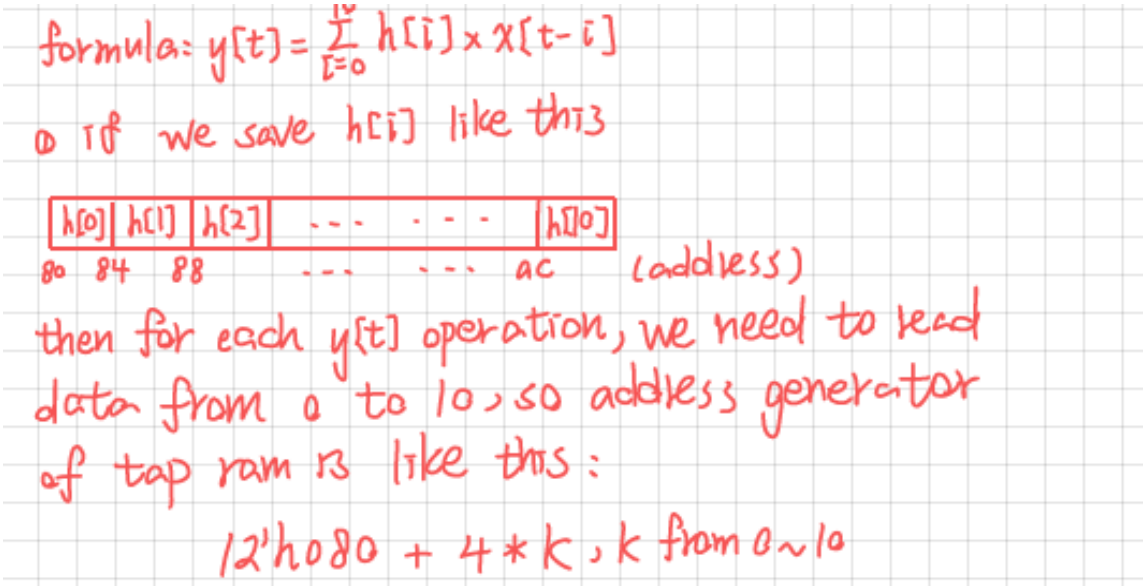


ap_control

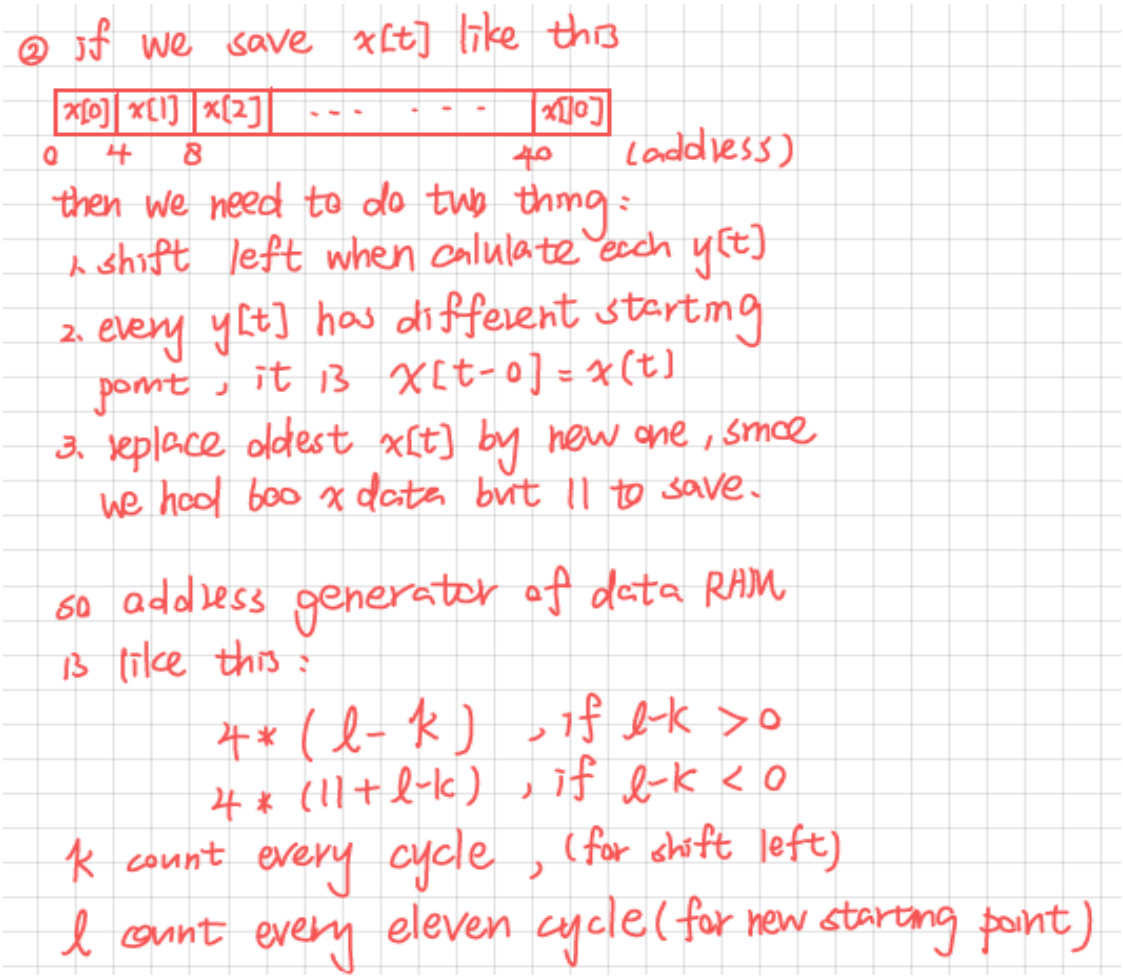


sm_state

- Address generator

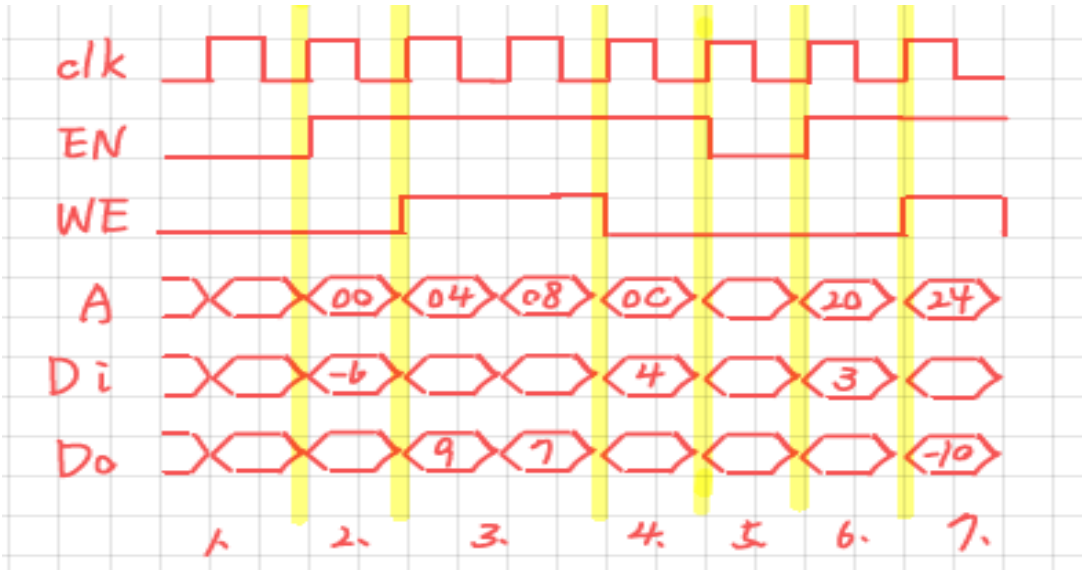


Address generator for tap RAM



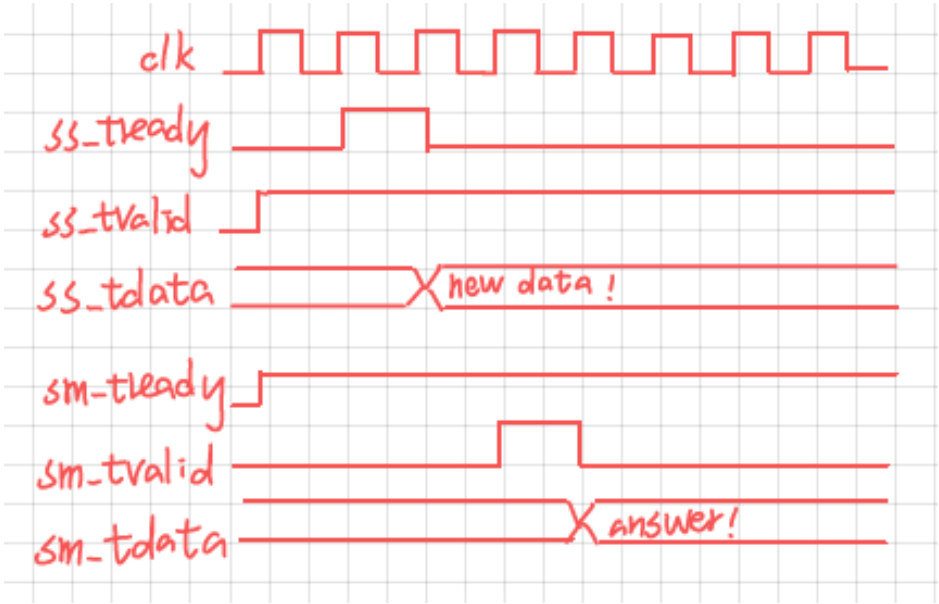
Address generator for data RAM

- How do data and tap RAM read and write data?
  If EN is 1 and WE is 1, then we can write the data to RAM(stage 3 and 7 in waveform below). If EN is 1 and WE is 0, then we can read the data in RAM(stage 2, 4 and 6 in waveform below). If EN is 0, we can't read and write the data in RAM.



Waveform

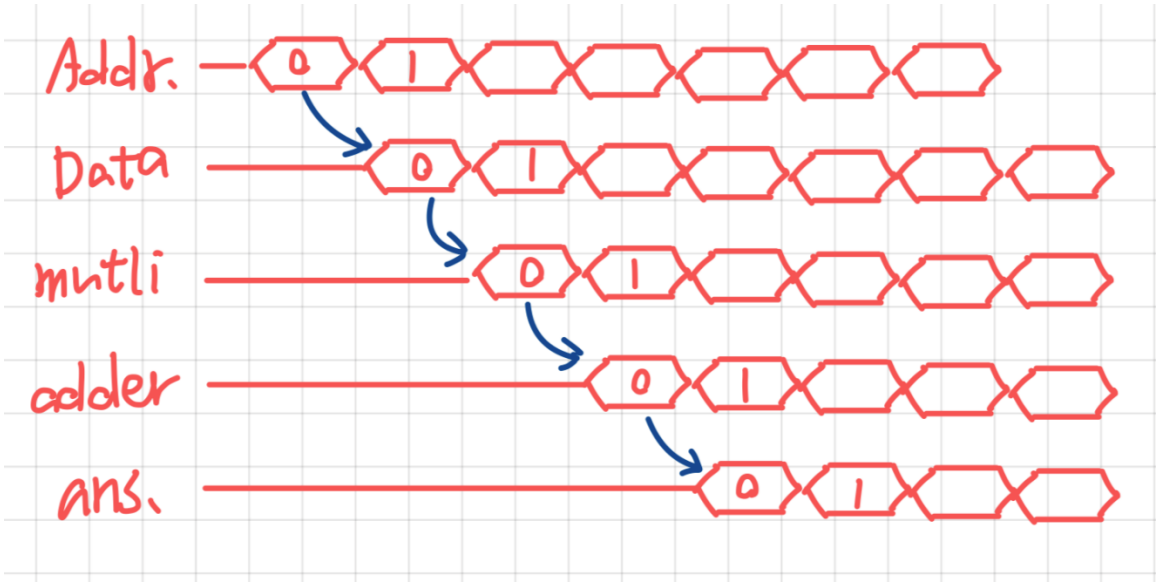
- How to input data and receive the answer?
  To receive the data in testbench, we set the ss_tvalid to 1, so when ss_tready is trigger, data will pass to our design in next cycle. To pass back the answer to testbench to check answer correct or not, we set sm_tready to 1, so when ss_tvalid is trigger, data will pass to testbench in next cycle.



AXI_stream design

- How does the pipeline operation processing?

Look in the design of RAM, we can receive data in next cycle after the address input. And we use a flipflop to save data output, multiplication result(m[i] = h[i] * x[t-i]), sigma result (y[t] =$\sum m[i]$), and then finally output answer.



Pipeline operation

- Screen dump
  - Resources usage

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	175	0	0	53200	0.33
LUT as Logic	175	0	0	53200	0.33
LUT as Memory	0	0	0	17400	0.00
Slice Registers	201	0	0	106400	0.19
Register as Flip Flop	201	0	0	106400	0.19
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

  - Timing report

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| Design Timing Summary
| ---------------------
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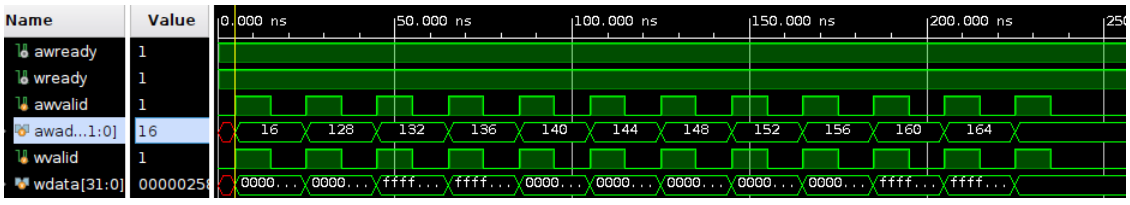
WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)
0.168	0.000	0	473	0.142	0.000

Timing summary

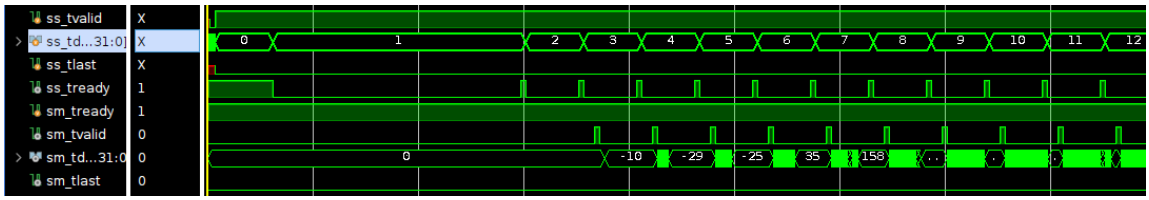
Location	Delay type	Incr(ns)	Path(ns)		Netlist Resource(s)
	(clock FIR_clk rise edge)	0.000	0.000	r	
		0.000	0.000	r	axis_clk (IN)
	net (fo=0)	0.000	0.000		axis_clk
	IBUF (Prop_ibuf_I_O)	0.972	0.972	r	axis_clk_IBUF_inst/O
	net (fo=1, unplaced)	0.800	1.771		axis_clk_IBUF
	BUFG (Prop_bufg_I_O)	0.101	1.872	r	axis_clk_IBUF_BUFG_inst/O
	net (fo=201, unplaced)	0.584	2.456		axis_clk_IBUF_BUFG
	FDPE			r	cnt_y_reg[0]/C
	FDPE (Prop_fdpe_C_Q)	0.478	2.934	f	cnt_y_reg[0]/Q
	net (fo=8, unplaced)	0.844	3.778		cnt_y[0]
	LUT5 (Prop_lut5_I0_O)	0.295	4.073	r	sm_tvalid_OBUF_inst_i_1/O
	net (fo=74, unplaced)	0.541	4.614		sm_tvalid_OBUF
	LUT6 (Prop_lut6_I2_O)	0.124	4.738	r	tlast_cnt[9]_i_2/O
	net (fo=5, unplaced)	0.477	5.215		tlast_cnt[9]_i_2_n_0
	LUT6 (Prop_lut6_I3_O)	0.124	5.339	r	rdata_OBUF[1]_inst_i_8/O
	net (fo=1, unplaced)	0.449	5.788		rdata_OBUF[1]_inst_i_8_n_0
	LUT6 (Prop_lut6_I5_O)	0.124	5.912	r	rdata_OBUF[1]_inst_i_4/O
	net (fo=1, unplaced)	0.000	5.912		rdata_OBUF[1]_inst_i_4_n_0
	CARRY4 (Prop_carry4_S[2]_CO[3])	0.380	6.292	r	rdata_OBUF[1]_inst_i_2/CO[3]
	net (fo=5, unplaced)	0.946	7.238		rdata_OBUF[1]_inst_i_2_n_0
	LUT6 (Prop_lut6_I0_O)	0.124	7.362	r	rdata_OBUF[1]_inst_i_1/O
	net (fo=1, unplaced)	0.800	8.162		rdata_OBUF[1]
	OBUF (Prop_obuf_I_O)	2.634	10.797	r	rdata_OBUF[1]_inst/O
	net (fo=0)	0.000	10.797		rdata[1]
				r	rdata[1] (OUT)
	(clock FIR_clk rise edge)	10.000	10.000	r	
	clock pessimism	0.000	10.000		
	clock uncertainty	-0.035	9.965		
	output delay	1.000	10.965		
	required time		10.965		
	arrival time		-10.797		
	slack		0.168		

Slack

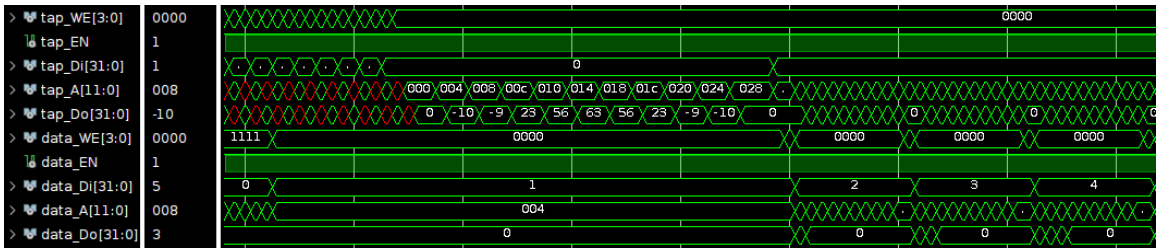
- Simulation waveform



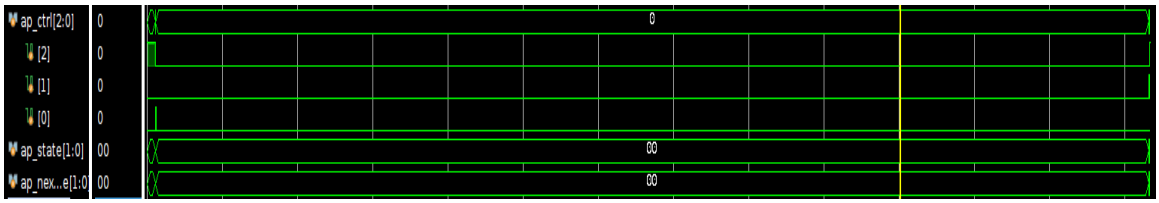
Coefficient read back



Data in stream in and data out stream out



RAM access control



FSM

Clock cycles from ap_start to ap_done:

$$\frac{done\ timing - start\ timing}{clock\ period} = \frac{66625ns - 595ns}{10ns} = 6603cycls$$

- 遲交原因：自己的時間管理不當，加上清大停電導致工作站無法使用，影響其他科目像是類比設計與分析與積體電路設計導論的進度，進而影響 SOC 的進度。還有即將完成時，電腦當機送修一個禮拜，由於檔案上外上傳，於是借了朋友的電腦重做了一次，導致無法預期完成，相當抱歉。