ECE375
Remotely communicated Rock Paper Scissors

TA:

School of Electrical Engineering and Computer Science

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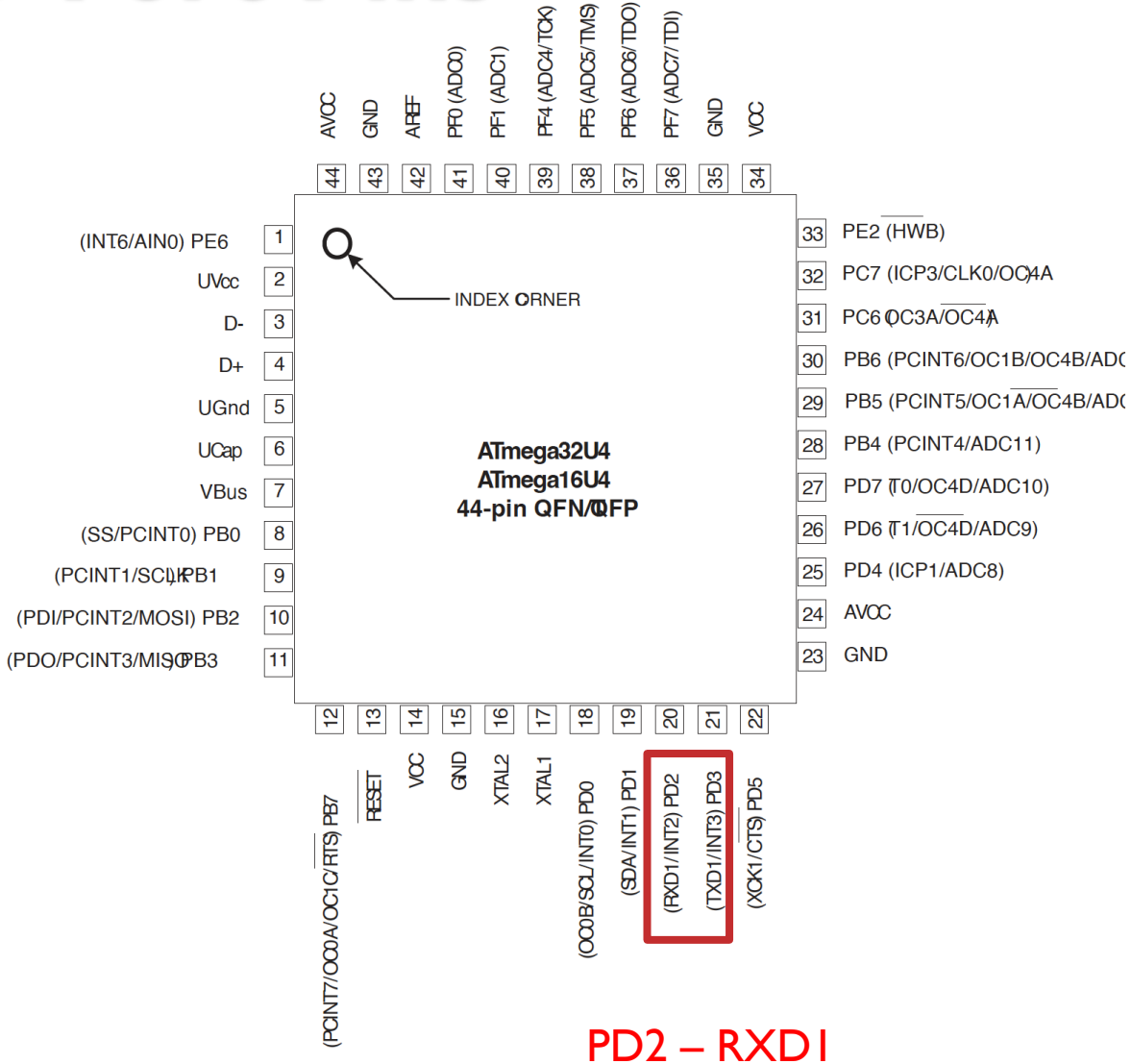
Goal of this Lab

- Learn how to use the Universal Synchronous/Asynchronous Receiver/Transmitter (USART) module.
- Correctly configure USART-related registers.
- Make two AVR boards communicate with each other.
- Learn how to configure and use the 16-bit Timer/Counter module to generate a delay

Play Rock Paper Scissors between Two Boards

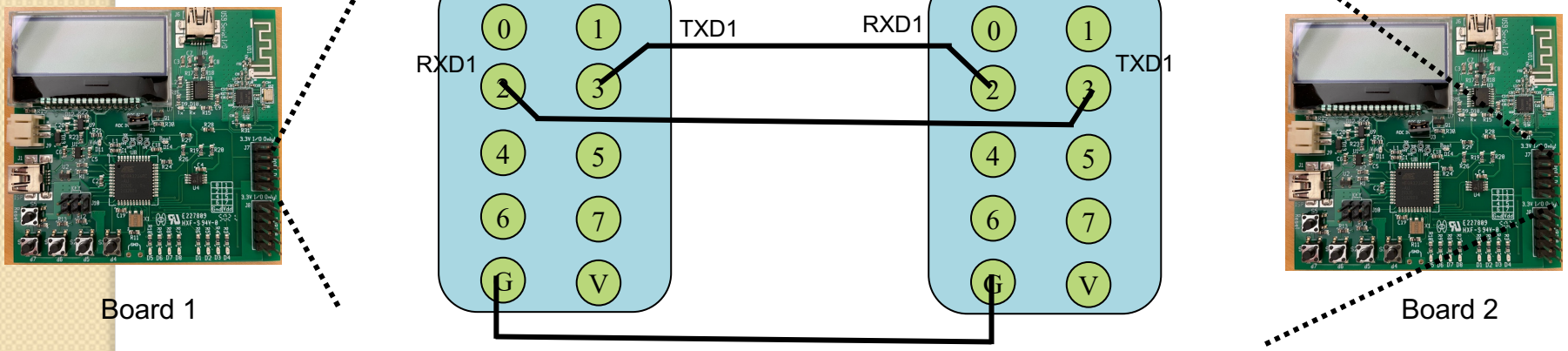
- Communicate through the USART1 modules
- LCD display to print messages.
- Buttons
  - PD7 – Start/Ready
  - PD4 – Change the current gesture and iterate through the three gestures in order
    - Rock → Paper → Scissor → Rock → Paper → …
- 4 LEDs
  - PB7:4 – Count down indicator
    - 4 × 1.5-sec delay
    - Timer/Counter1 Normal mode
  - PB3:0 – Leave for LCDDriver

I/O Port Pins



PD2 – RXD1
PD3 – TXD1

Tekbot Bumper Switch Connection



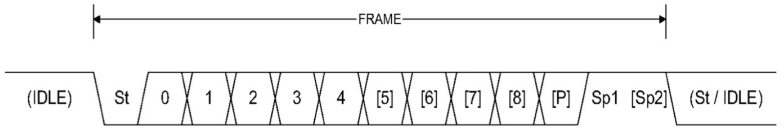
Board 1 Board 2

PD2 <=> PD3
PD3 <=> PD2
GND <=> GND

Initialization

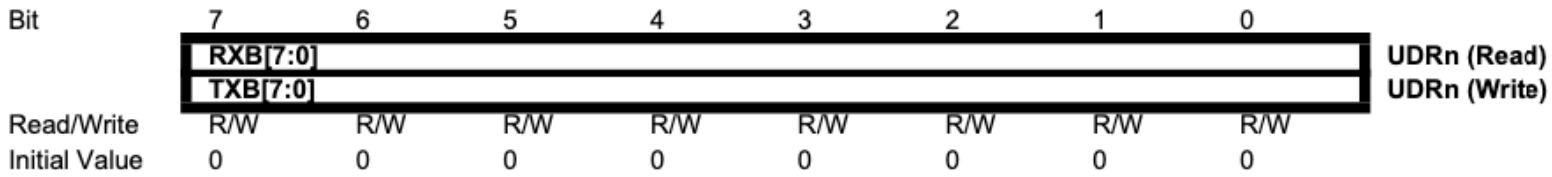
- Frame Format
  - Data Frame : 8-bit data
  - Stop bit : 2 stop bits
  - Parity bit : disable
  - Asynchronous Operation
- Baud Rate
  - 2400 bits per second
- Control Register
  - Frame Format
    - UCSR1A
    - UCSR1B
    - UCSR1C
  - Baud Rate
    - UBRR1H
    - UBRR1L
- Data Register
  - UDR1

Serial Data Frame Format



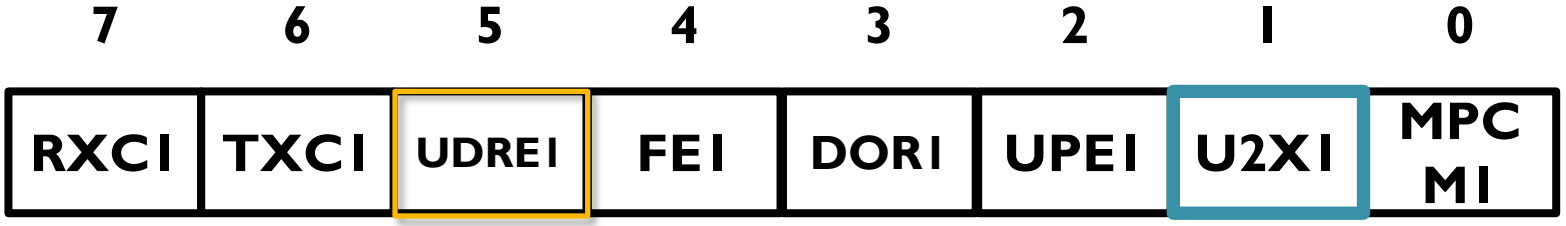
St	Start bit, always low.
(n)	Data bits (0 to 8).
P	Parity bit. Can be odd or even.
Sp	Stop bit, always high.
IDLE	No transfers on the communication line (RxD or TxD). An IDLE line must be high.

USART I/O Data Register



- Transmit
  - STS UDR1, mpr
- Receive
  - LDS mpr, UDR1

USART Control and Status Register



UCSR1A

Bit 7 – RXCn: USART Receive Complete

Bit 6 – TXCn: USART Transmit Complete

Bit 5 – UDREn: USART Data Register Empty

Bit 4 – FEn: Frame Error

Bit 3 – DORn: Data OverRun

Bit 2 – UPEn: Parity Error

Bit 1 – U2Xn: Double the USART Transmission Speed

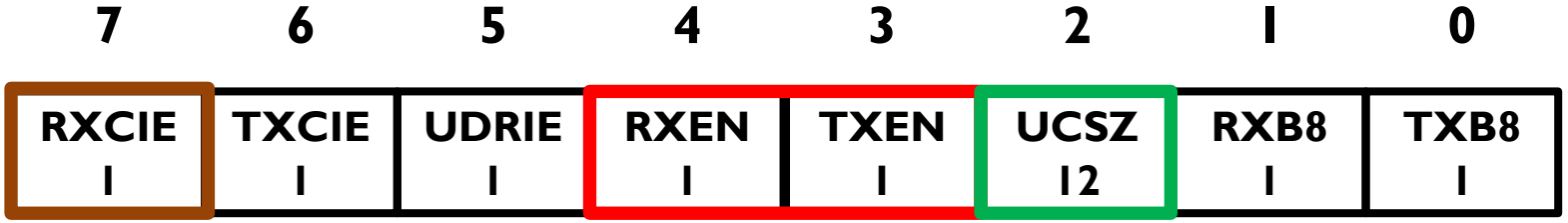
Bit 0 – MPCMn: Multi-Processor Communication Mode

- **Bit 5 – UDREn: USART Data Register Empty**

The UDREn flag indicates if the transmit buffer (UDRn) is ready to receive new data. If UDREn is one, the buffer is empty, and therefore ready to be written. The UDREn flag can generate a Data Register Empty interrupt (see description of the UDRIEn bit).

UDREn is set after a reset to indicate that the Transmitter is ready.

USART Control and Status Register



UCSR1B

Bit 7 – RXCIEn: RX Complete Interrupt Enable

Bit 6 – TXCIEn: TX Complete Interrupt Enable

Bit 5 – UDRIEn: USART Data Register Empty Interrupt Enable

Bit 4 – RXENn: Receiver Enable

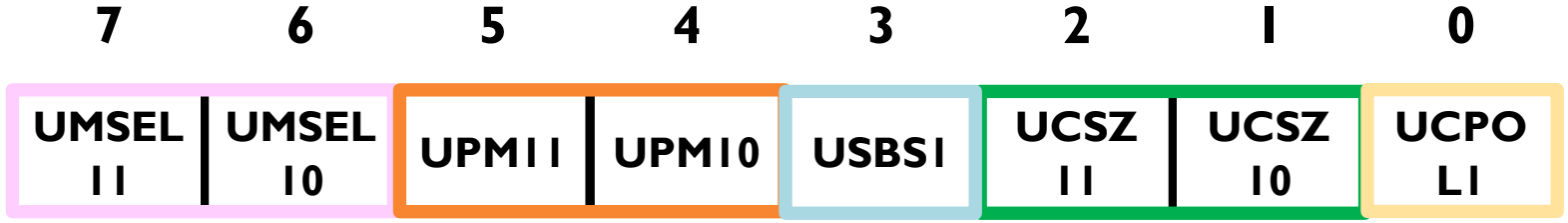
Bit 3 – TXENn: Transmitter Enable

Bit 2 – UCSZn2: Character Size

Bit 1 – RXB8n: Receive Data Bit 8

Bit 0 – TXB8n: Transmit Data Bit 8

USART Control and Status Register



UCSR1C

Bit 7:6 – UMSELn1: USART Mode Select

Bit 5:4 – UPMn1:0: Parity Mode

Bit 3 – USBSn: Stop Bit Select

Bit 2:1 – UCSZn1:0: Character Size

Bit 0 – UCPOLn: Clock Polarity

UMSELI / UPMI

Table 18-7. UMSELn Bit Settings

UMSELn1	UMSELn0	Mode
0	0	Asynchronous USART
0	1	Synchronous USART
1	0	(Reserved)
1	1	Master SPI (MSPIM)[1]

Table 18-8. UPMn Bit Settings

UPMn1	UPMn0	Parity Mode
0	0	Disabled
0	1	Reserved
1	0	Enabled, Even Parity
1	1	Enabled, Odd Parity

USBS1 / UCPOL1

Table 18-9. USBS Bit Settings

USBSn	Stop Bit(s)
0	1-bit
1	2-bit

Table 18-11. UCPOLn Bit Settings

UCPOLn	Transmitted Data Changed (Output of TxDn Pin)	Received Data Sampled (Input on RxDn Pin)
0	Rising XCKn Edge	Falling XCKn Edge
1	Falling XCKn Edge	Rising XCKn Edge

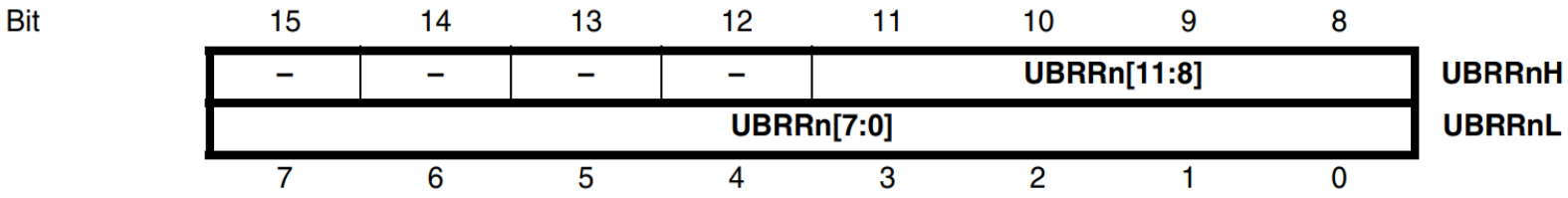
This bit is used for synchronous mode only. Write this bit to zero when asynchronous mode is used. The UCPOLn bit sets the relationship between data output change and data input sample, and the synchronous clock (XCKn).

UCSZ1

Table 80. UCSZn Bits Settings

UCSZn2	UCSZn1	UCSZn0	Character Size
0	0	0	5-bit
0	0	1	6-bit
0	1	0	7-bit
0	1	1	8-bit
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	9-bit

USART Baud Rate Registers



Bit 15:12 – Reserved Bits

Bit 11:0 – UBRRn11:0: USARTn Baud Rate Register

UBRR1H

UBRR1L

Table 18-1. Equations for Calculating Baud Rate Register Setting

Operating Mode	Equation for Calculating Baud Rate[1]	Equation for Calculating UBRR Value
Asynchronous Normal mode (U2Xn = 0)	$BAUD = \frac{f_{OSC}}{16(UBRRn+1)}$	$UBRRn = \frac{f_{OSC}}{16BAUD} - 1$
Asynchronous Double Speed mode (U2Xn = 1)	$BAUD = \frac{f_{OSC}}{8(UBRRn+1)}$	$UBRRn = \frac{f_{OSC}}{8BAUD} - 1$

Grading Criteria

- Implementation – 60 pts
  - 10 pts for Correct USART1 configuration
  - 15 pts for PD7 Functionality
    - (5pt) Game Ready/Start
    - (10pt) USART1 communication
  - 15 pts for PD4 Functionality
    - (5pt) Select Gestures and iterate correctly
    - (10pt) USART1 communication
  - 10 pts for PB7-4 Functionality
    - 4 × 1.5-sec delay using T/C1 Normal
  - 5 pts for the Correct result (Win, Loose, or Draw)
  - 5 pts for LCD does not show any garbage data

Announcements

- 2 weeks are given to finish this lab.
- There will be
  - no office hours during Thanksgiving week.
  - no office hours during the final week (11/30 and 12/2).
  - Instead, we will hold OHs on 11/28 (Mon) – 29 (Tue)
- You need to write a single code for two AVR boards to interact with each other.
- Follow the Frame formats and Baud rate provided in the slides.
- Read Atmega32U4 Datasheet
  - 188p – 213p

Questions?