ECE 375 PRELAB 7

Lab Time: Wednesday 10-11:50 am

Kenneth Tang

QUESTIONS

1. In this lab, you will be utilizing Timer/Counter1, which can make use of several 16-bit timer registers. The datasheet describes a particular manner in which these registers must be manipulated. To illustrate the process, write a snippet of assembly code that configures OCR1A with a value of 0x1234. For the sake of simplicity, you may assume that no interrupts are triggered during your code's operation.

    a. To write a value like $1234 to OCR1A we should use the write high then low method. Although the manual says that the OCRnA/B/C 16-bit registers do not involve using the temporary register, it is best to stay consistent.

    ```
    ldi     mpr, $12
    sts     OCR1AH, mpr
    ldi     mpr, $34
    sts     OCR1AL, mpr
    ```

2. Each ATmega32U4 USART module has two flags used to indicate its current transmitter state: the Data Register Empty (UDRE) flag and Transmit Complete (TXC) flag. What is the difference between these two flags, and which one always gets set first as the transmitter runs? You will probably need to read about the Data Transmission process in the datasheet (including looking at any relevant USART diagrams) to answer this question.

    a. The UDRE flag is set when the transmit buffer is ready to receive new input data and the transmit buffer is empty. The TXC flag is set when the entire frame of the transmit shift register has been shifted out and there is no new data in the transmit buffer. The UDRE flag will always be set before the TXC flag because the CPU needs to determine if new data is in the buffer or not which means we must wait for any data potentially there to be loaded in. After waiting and no data was moved in then we can say the transmit is complete.

3. Each ATmega32U4 USART module has one flag used to indicate its current receiver state (not including the error flags). For USART1 specifically, what is the name of this flag, and what is the interrupt vector address for the interrupt associated with this flag? This time, you will probably need to read about Data Reception in the datasheet to answer this question.

    a. The receive state can be determined by looking at the Receive enable bit RXENn in UCSR1B. The Receive complete interrupt can be located at $0032 and is called USART1 Rx Complete

REFERENCE

ATmega32U4 datasheet