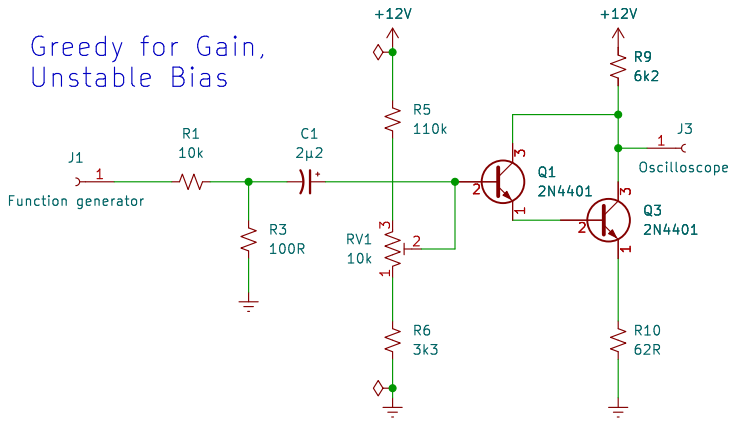


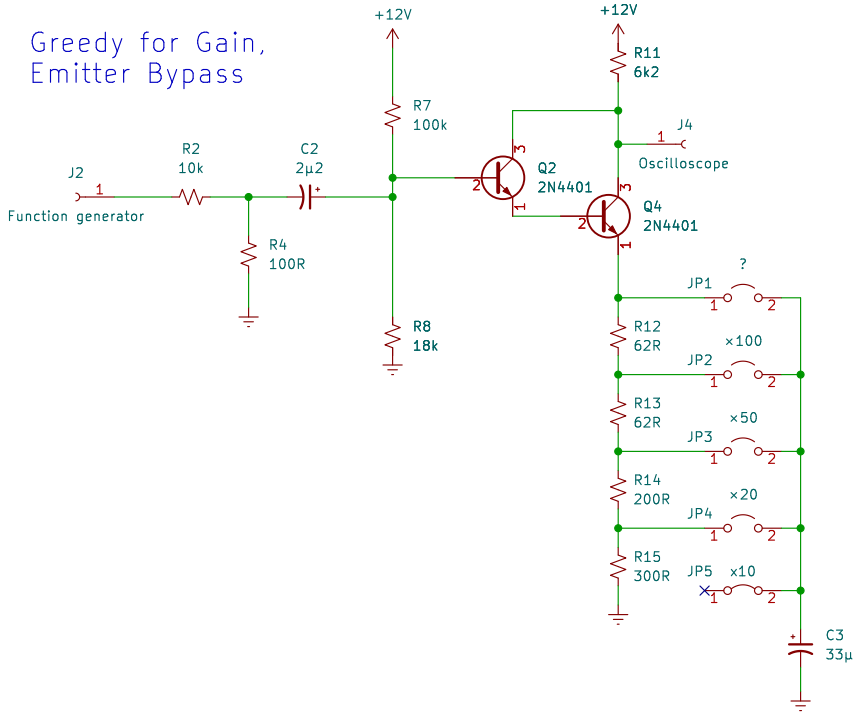
First, attempt to build bias divider wuth standard 5% resistor values (13k/110k), which doesn't work (offset too high).

Replace 13k with RV1/R7.
Trim to 1.2V at the wiper of RV1, then trim to 6V at J2.
Two-step process is necessary because tuning range of RV1 can drive J2 to the rails.

Drive J1 with 10 Vpp sine wave.
Show sine(ish) wave at J2 (albeit with gain less than predicted.)

Apply minimal heat from heat gun to Q3/Q4, or apply a minimal amount of freeze spray. Note instability of bias and clipping of signal.

Stable DC bias at G=100 appears infeasible! (Segue to greed for signal gain...)



Observe that without bypass cap, circuit gain is a little under 10×, as predicted.

With bypass cap at the 20×, 50×, 100× positions, observe fall in gain (20–15, 50–>33, 100–>50)

With bypass cap at the top position, labelled [?] because we couldn't predict the behaviour, observe that negative peaks clip at saturation voltage (~2 diode drops), positive peaks round off peculiarly at about +9V.

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Kludges from Kevin's Cave
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