Kenny Na

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Education

University of Waterloo - BASc, Systems Design Engineering — Sep 2023 – Present

Experience

Electrical Engineering Intern – Etched – San Jose, CA — May 2025 – Aug 2025

- Designed schematic and layout in Cadence Allegro for a 16-layer HDI PCB with an STM32 and high-speed signal breakouts (Ethernet, PLL clocks, PCIe 5.0) to perform S-parameter tests and emulate rudimentary ASIC functionality.
- Researched reliability requirements with physical design engineers to prevent negative effects of high DC current draw (~1.2V 450A+) from an ASIC over the product life cycle (0-5+ years), including electron migration and thermal runaway due to current crowding around fine-pitch BGA balls under computationally dense regions of the ASIC, leading to ballmap pattern design changes to reduce IR drop over 39% within the substrate and interposer.
- Designed three 12-layer HDI test interposer PCBs to sink up to 1500A with vendor-specific load slammers, while optimizing BGA fanout by using PTH/BB/microvias and researching optimal via sizing, plating, and surface finish.

Electrical Engineering Intern – Waterloo Aerial Robotics Group – Waterloo, ON — Sep 2024 – Dec 2024

- Designed a mixed-signal PCB integrating a 12-5V buck converter, LDO, ESP32, and impedance-matched RF transceiver in Altium Designer for an ExpressLRS-based RC plane, supporting up to 6 PWM outputs for servo and ESC control.
- Simulated input filtering on a buck converter with and without high-ESR capacitors using LTspice to prevent transient voltage spikes from source impedance of LiPo batteries and resonance from the use of many MLCC capacitors.
- Performed power delivery network simulation to verify stackup capabilities and address current crowding concerns.
- Designed a USB-C source to arbitrate up to 20V 5A for stationary drone debugging, complying with USB-PD & 3.2 spec.
- Assembled and reworked PCBAs using stencils and hotplate while validating with DMM, oscilloscope, and e-load.

IT Infrastructure & Operations Intern – Grand & Toy – Vaughan, ON — Jan 2024 – Apr 2024

- Managed 250+ computer users through Active Directory, Group Policies, and Microsoft Management Console.
- Led deployment for 100+ custom-imaged employee PCs using Microsoft Deployment Toolkit and Windows 10 Server.

Student Teams

Team Lead – Waterloo Reality Labs – Waterloo, ON — Jan 2024 – Aug 2025

- Created the world's first collegiate engineering design team developing open-source, hackable VR and AR headsets.
- Built an open-source 3-DoF VR headset with compatible eye-tracking that interfaces with SteamVR.
- Architected Varifocal, a custom HMD aimed to solve the vergence-accommodation conflict in VR headsets with eye tracking to approximate focal distance and using voice coils to move lenses for real-time focal length adjustment.
- Designed a VR headset with 140+ degree horizontal FOV by using custom-cut wide fresnel lenses and canted displays.
- Implemented a camera-based eye tracker with an ESP32, OmniVision camera, IR LEDs, and FOSS tracking software.

Electrical Lead – Waterloo Aerial Robotics Group – Waterloo, ON — Mar 2025 – Present

- Leading the electrical team in the design, build, and testing of sUAS/UAV systems for the AEAC national competition.
- Architected and designed a custom STM32-based flight controller with CAN, SPI, I2C, barometer and redundant IMUs.
- Designed a compact 3-phase motor driver board with an STSPIN32 MCU to control BLDCs on drones with 3S batteries.
- Optimized H-bridge MOSFET selection with calculations for conducting/switching power loss and max temperature.
- Reselected modem model on carrier PCB to cover more NA LTE bands and prioritize lower frequencies for better range.

Skills

- **Hardware:** Power Electronics, Analog/Digital Design, PCB Layout, Schematic Capture, Simulation & Validation
- **Applications & Tools:** Cadence Allegro, Altium Designer, LTSpice, SOLIDWORKS, Arduino, Git, Linux
- **Languages & Protocols:** C, C++, Python, HTML, CSS, JavaScript, MATLAB, I2C, SPI, UART, USB-PD, USB 3.2