# ABSTRACT

This project topic is the design and construction of an Intelligent Transistor Analyzer (ITA).

The ITA utilizes the phase shift properties of the Common-Emitter (CE) and Common Collector (or Emitter Follower) configurations of Bipolar Junction Transistors (BJT) to identify the leads of any BJT transistor and also deduce if the transistor is an NPN or PNP transistor. The results of the analysis are displayed on a 3-digit seven segment displays.

The Intel 8051 microcontroller was used along with other sequential logic I.Cs to input the test conditions, read the response, make the appropriate deductions and finally output the results on the display.

# CHAPTER 1

## 1.0 INTRODUCTION

The transistor could be said to be one of man's greatest inventions. It is an essential ingredient of every electronic circuit from the simplest amplifier or oscillator to the most elaborate digital computer. It is also used in power devices to switch on relays and power drives. There is hardly any electronic circuit without one or more transistor existing in it either as discrete transistors or embedded as integrated circuits (I.C). For this reason an electronic Engineer, technician, electronic hobbyist and electronic circuit designers find it to be an indispensable component in the art of electronics.

In as much as the transistor is a vital element in the electronic world, it has a big snag, which is the difficulty in identifying which pin is which (i.e. emitter, base and collector) by mere looking at it. There is no common standard adopted by manufacturers for arranging the pins or leads. The only known method of identifying the leads is the "Resistance Test" using an analog or digital multimeters. The resistance measured between the Base and Emitter leads is higher than that measured between the Base and Collector leads. But it takes a well-trained hand to be able to distinguish the pins using the multimeter without making wrong deductions. This is done by stages of elimination tests guided by easily forgotten rules. This process is usually

time consuming and is un-reliable because of errors or faults that may be on the test equipment.

This snag has always been a problem to students learning practical electronics because of the confusing trial and error tests. For the skilled hands in electronics, the process is usually time-consuming thus decreasing productivity.

For this reasons, it was necessary to design a device that will be used to identify the leads of a BJT without having to go through the excruciating pains of trial and error associated with the Resistance Method. The device should be easy to use by anyone and no need to memorize any rules or guidelines and also take at most 30 seconds to analyze a transistor.

The “Intelligent Transistor Analyzer, (ITA)” is a project that was designed and constructed to meet the above stated requirements and specifications. The ITA has three probes (labeled A, B and C) with crocodile clips at the ends for easy connection to the leads of a transistor. It is capable of identifying which pin is connected to any of its probes no irrespective of the order. The results are displayed on a seven-segment display. Since the ITA is microprocessor controlled, it takes the analyzer less than a minute to identify the leads of a transistor and tell is if it is an NPN or PNP transistor.

## 1.1 LITERATURE REVIEW

Man has always been known to be a very inquisitive creature. He is always on a quest to know the reason for the occurrence of some existing natural phenomena and eventually finds a means of quantifying these phenomena. He does this by creating or inventing instruments he uses to measure (or analyze) not only the existing natural phenomena but also the efficiency or performance of his own creations. With this inquisitive nature of man, he has succeeded in creating a technologically advanced world.

Therefore, the scientific and technological progress of any nation or community depends on its ability to measure, calculate and finally estimate the unknown. Also, the success of an Engineer or technician is judged by his ability to analyze, measure precisely and correctly interpret a circuit or component performance.

There are three ways of making such measurements or analysis.

(i) By mechanical means-like measuring atmospheric pressure –Using aneroid barometer

(ii) By electrical means- like measuring potential difference with an electrical voltmeter

(iii) By electronic means- which is a very sensitive way of detecting the measured (or analyzed) quantity because of amplification provided by the active electron device(s).

The electronic instruments generally have higher sensitivity, faster and greater flexibility than mechanical or electrical instruments in indicating, analyzing, recording, and where required, in controlling the measured quantity or component.

In this project, the transistor is the concerned quantity (or component). Ever since the invention of the transistor, some instruments have been designed to measure the efficiency (amplification factor) of the transistor, while some have been designed simply to test if a transistor is good or bad. In either case, the pin/lead of the transistor arrangement MUST be known before connecting it to such instrument. And this has limited the use of such instruments by novices in electronics.

The ITA is a new addition or invention to the family of instruments associated with BJTs.

## 1.2 THE BIPOLAR JUNCTION TRANSISTOR (BJT).

### OVERVIEW

The first junction transistor was invented in 1954 by a team of scientists led by William Shockley at the Bell Laboratories in America. The term "transistor" is derive from the words "transfer resistor" namely a device for the transfer of current form low resistance circuit to approximately the same current in a high resistance circuit.

The bipolar junction transistor is a three terminal device consisting of two junction diodes and consist of either a thin layer of P-type semiconductor as in Figure1.0 (a), and referred to as an NPN transistor, or a thin layer N-type semiconductor sandwiched between two P-type semiconductor, as in figure 1.0(b) and referred to as PNP transistor.

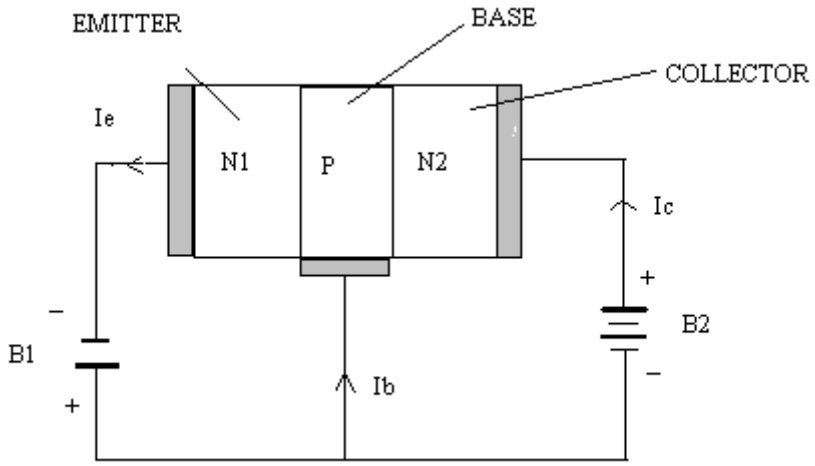



**FIGURE 1** (a) NPN TRANSISTOR

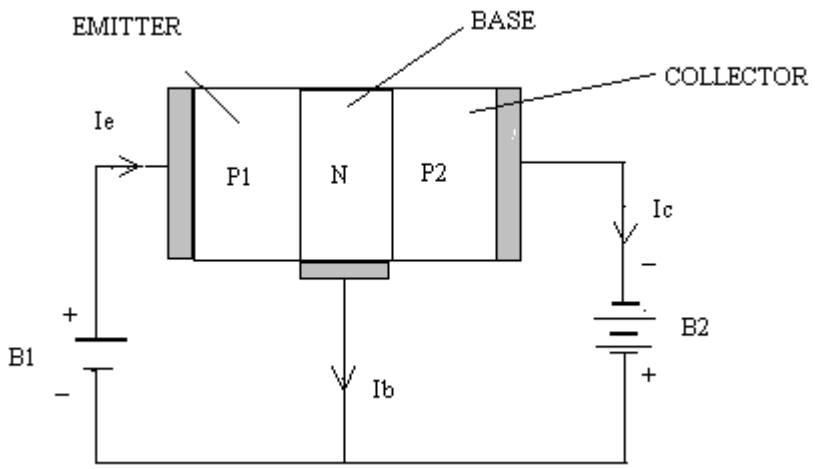



**FIGURE 1(b)** PNP TRANSISTOR

**FIGURE 1.0** ARRANGEMENT OF A JUNCTION TRANSISTOR

The thickness of the central layer, known as the base is of the order of 0.001 inch (or 0.025mm). The junction diode formed by $N_1$p in Figure 1.0(a) is biased in the forward direction by battery $B_1$ so that free electrons are urged from $N_1$ towards P. Hence $N_1$ termed emitter. On the other hand, the junction diode formed by $N_2$ P in Figure 1.0(a) biased in the reversed direction by battery $B_2$ so that if battery $B_1$ were disconnected, i.e. with zero emitter current, no current would flow between $N_2$ and P apart from that due to thermally generated minority carriers. However, with $B_1$ connected as in Figure 1.0(a) the electrons from emitter $N_1$ enter P and diffuse through the base until they come within the influence of $N_2$, which is connected, to the positive terminal of battery, $B_2$. Consequently, the electrons that reach are

collected but the metal electrode attached to $N_2$, hence $N_2$ is termed "collector".

Some of the electrons, in passing through the base, combine with holes; others reach the base terminal. The electrons which do not reach the collector $N_2$ are responsible for the current at the base terminal, and the distribution of electron flow in an NPN transistor can be represented diagrammatically as in Figure 1.1 below.

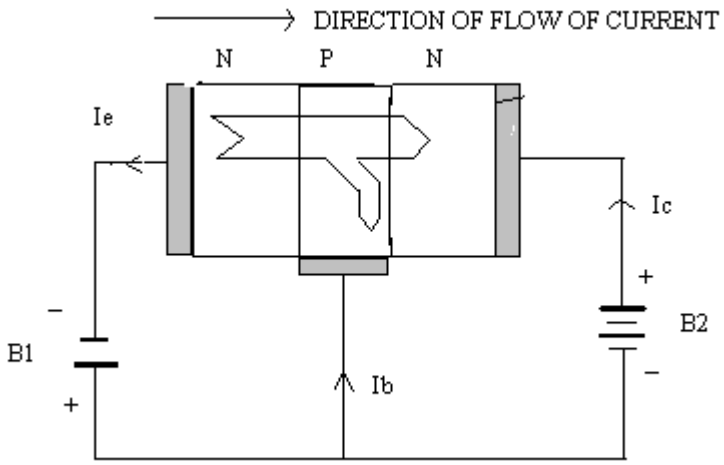



**FIGURE 1.1** ELECTRON FLOW IN AN NPN TRANSISTOR.

The conventional directions of the currents are indicated by the arrows marked $I_E$, $I_B$, and $I_C$ .By making the thickness of the base very small and the impurity concentration in the base much less than in the emitter and collector, the free electrons emerging from the emitter and collector have

little opportunity of combining with holes in the base, with the result that about 98% of these electrons reach the collector.

By Kirchoff's first law, which states that the total current flowing towards a junction is equal to the total current flowing away from that junction, i.e. $I_E = I_B + I_C$, so that $I_c = 0.98I_E$, then $I_B = 0.20IE$; thus when IE=1mA. Ic=0.98mA and $I_B$=0.02mA as in Figure 1.2 below.

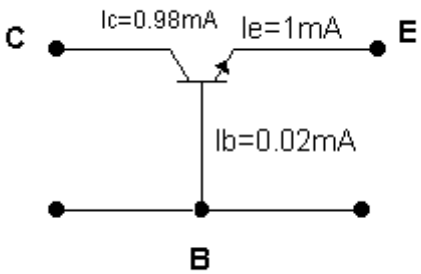



**FIGURE 1.2** CURRENTS IN THE EMITTER, COLLECTOR AND BASE CIRCUITS OF AN NPN TRANSISTOR.

In the above explanation, the NPN transistor has been discussed, but exactly the same explanation applies to the PNP transistor of Figure 1.0(b) except that the movement electrons are replaced by the movement of holes.

## 1.3 CONSTRUCTION OF A TRANSISTOR.

The first step is to purify the germanium or silicon so that any impurity does not exceed about 1 part in $10^{10}$ . Various methods have been developed for attaining this exceptional degree of purity and intensive research is still being carried out to develop new methods of purifying and doping germanium and silicon. In one form of construction of PNP transistor, the purified material is grown as a single crystal, and while the material is in a molten state, an N-type impurity (e.g. antimony in the case of germanium and phosphorus in the case of silicon) is added in the proportion of about 1 part in $10^8$. The solidified crystal is then sawn into slices about 0.1mm thick. Each slice is used to form the base region of a transistor; thus in the case of N-type germanium a pellet of P-type impurity such as indium is placed on each side of the slice, the one which is to form the collector being about three times the size of that forming the emitter. One reason for the larger size of the collector bead is that the current carriers from the emitter spread outwards as they pass through the base, and the larger area of the collector enables the latter to collect carriers more effectively. Another reason is that the larger area assists in dissipating the greater power loss at the collector-base junction.

The assembly is heated in a hydrogen atmosphere until the pellets melt and dissolve some of the germanium from the slice, as shown in Figure 1.3. Leads for the emitter and collector are soldered to the surplus material in the

pellet to make non-rectifying contacts, and a nickel tab is soldered to make connection to the base. The assembly is hermitically sealed in a protective (moisture and light tight) enclosure, which could be made of metal, glass or epoxy.

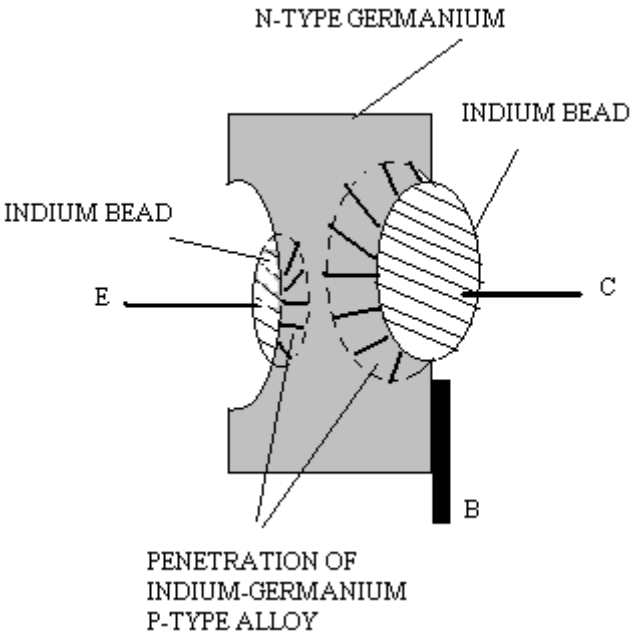



**FIGURE 1.3.** CONSTRUCTION OF PNP GERMANIUM TRANSISTOR.

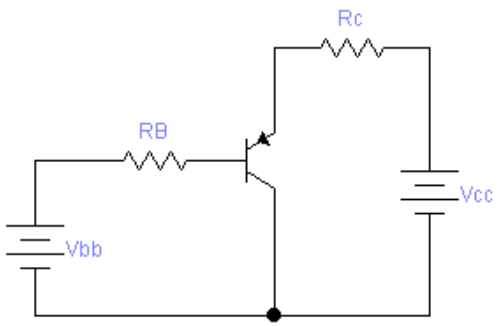
There are three useful ways to connect a transistor, which are

(1) Common Emitter (CE) (2) Common Collector (CC)[The CC is sometimes called an emitter follower.] (3) Common Base.

The CE and CC configurations were discussed only because of their relevance to this project.

## 1.4 COMMON-EMITTER CONFIGURATION

The most frequently encountered transistor configuration is shown in Figure 1.4 below for the PNP and NPN transistors. It is called the CE configuration since the emitter is common or reference to both the input and output terminals (in the case common to both the base and collector terminals).



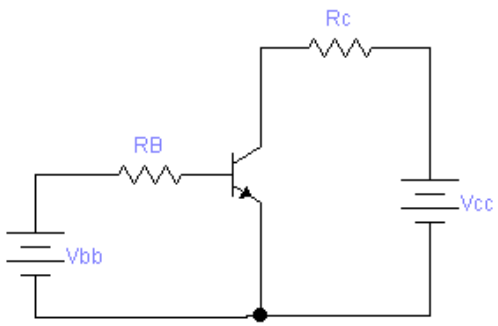




Fig 1.4 (a) Using a PNP transistor

Fig.1.4 (b) Using an NPN transistor

**FIGURE 1.4** COMMON-EMITTER CONFIGURATIONS USING NPN AND PNP TRANSISTORS

For the common emitter configuration, the current relation, $I_E = I_B + I_C$ still holds. The circuit shown in fig. 1.4 has two loops. The left loop is the base loop, and the right loop is the collector loop.

In the base loop, the $V_{BB}$ source forward biases the emitter diode with $R_B$ as current limiting resistor. By changing $V_B$ or $R_B$, we can change the

collector current. In other words, the base current controls the collector current. It means that a small base current controls a large current (collector).

In the collector, a source voltage $V_{CC}$ reverse biases the collector diode through $R_C$. The supply voltage $V_{CC}$ must reverse bias the collector diode as shown or else the transistor won't work properly. In other words, the collector must be positive in fig. 1.4 to collect most of the free electrons injected into the base.

Applying Ohm's law to the base resistor, gives

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

Where VBE = 0.7V (for Silicon transistors)

= 0.2 (for Germanium transistors)

The output is taken from the collector.

## 1.5 COMMON – COLLECTOR (EMITTER FOLLOWER)

The common collector configuration for PNP and NPN transistors are shown in fig. 1.5 (a) and (b) respectively.

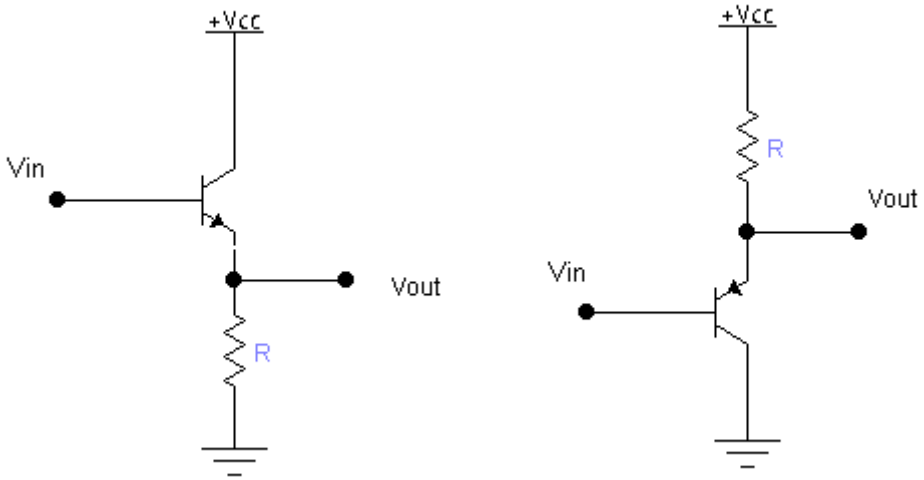



**FIGURE. 1.5** COMMON-COLLECTOR CONFIGURATION FOR NPN AND PNP TRANSISTORS.

The common collector configuration is also called emitter follower. This is because the output terminal is the emitter, which follows the input (the base), less one diode, that is, the output is a replica of the input, but 0.6 – 0.7V less positive. An emitter follower has no collector resistor. The common collector configuration is used primarily for impedance matching purposes since it has a high input impedance and low output impedance, opposite to that of common emitter and common base configurations. This means that it has higher power gain than other configurations.

Table 1.0 below shows the circuit configurations using an NPN transistor and summarises their characteristics. (Typical values are shown in brackets)

| **PARAMETER** | **COMMON EMITTER** | **COMMON COLLECTOR** |
|---|---|---|
| *VOLTAGE GAIN* | MEDIUM/HIGH(50) | UNITY(1) |
| *CURRENT GAIN* | HIGH (200) | HIGH(200) |
| *POWER GAIN* | VERY HIGH(10,000) | HIGH(200) |
| *INPUT RESISTANCE* | MEDIUM (2.5KΩ) | HIGH(100KΩ) |
| *OUTPUT RESISTANCE* | MEDIUM/HIGH (20KΩ) | LOW(100Ω) |
| *PHASE SHIFT* | $180^0$ | $0^0$ |

**TABLE 1.0** CHARACTERISTICS OF CE AND CC CONFIGURATIONS.

## USES OF TRANSISTORS

(i) For signal amplification.

(ii) As switches; a small current at the base can be used to drive or control large loads.

(iii) Used in d.c voltage regulators.

(iv) Used in oscillators.

## 1.6 THE INTELLIGENT TRANSISTOR ANALYZER

### -PRINCIPLE OF OPERATION.

When an NPN transistor is connected in CE configuration and a pulse is applied at the base, the output is always $180^{o}$ out of phase with the input. But when a PNP transistor is connected as an emitter follower, the output is in phase with the input, i.e. the logic level is the same as that at the input.

The intelligent transistor analyzer utilizes the phase-shift characteristics of the common emitter and common collector configurations to determine the leads of a transistor connected to it.

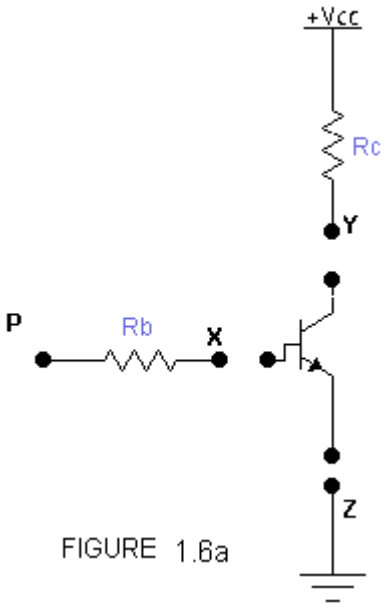



FIGURE 1.6a

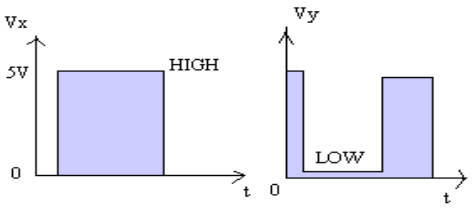



FIGURE 1.6b(i)

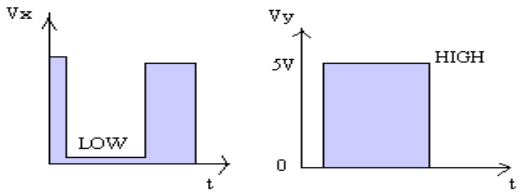



FIGURE 1.6b(ii)

**FIGURE 1.6**: ILLUSTRATING THE PRINCIPLE OF OPERATION OF THE ITA WITH AN NPN TRANSISTOR.

Supposed in the above circuit of figure 1.6(a), an NPN transistor, $Q_1$ is connected in the order shown, that is, the base connected to point X, the emitter to point Z, and the collector to point Y(in this order, the transistor

would be in CE configuration). When a positive pulse (or logic 1) is applied at point P (which is connected to the base through a resistor) then a similar pulse would appear on Y, but $180^o$ out of phase with that at X(or P). figure 1.6(b) shows the output waveforms for both HIGH and LOW logic inputs at X. Actual voltage levels measured at point 'Y' when an NPN transistor (D400) was connected in all possible lead permutations of a transistor when $V_X$(Input voltage)=5V and $V_X$=0V respectively are shown in Table 1.1

| **Z** | **Y** | **X** | **Vx**= 5V(HIGH) | **Vx**= 0V(LOW) |
|---|---|---|---|---|
| **B** | **C** | **E** | 4.89V(HIGH) | 4.97V(LOW) |
| **C** | **B** | **E** | 0.69V(LOW) | 0.69V(LOW) |
| **B** | **E** | **C** | 4.51V(HIGH) | 4.57V(HIGH) |
| **E** | **B** | **C** | 0.7V(LOW) | 0.70V(LOW) |
| **C** | **E** | **B** | 3.63V(HIGH) | 5.00V(HIGH) |
| **E** | **C** | **B** | 0.06V(LOW) | 4.89V(HIGH) |

**TABLE 1.1**: VOLTAGES MEASURED AT POINT Y WHEN AN NPN TRANSITOR WAS CONNECTED TO POINTS Z, Y, AND Y IN ALL SIX POSSIBLE PERMUTATIONS.

From the table, it was observed that point Y gave the opposite state to that at the input, only when the emitter was connected to Z (ground), collector to Y

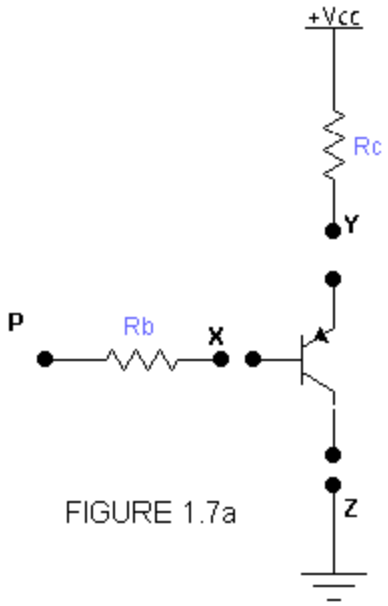



FIGURE 1.7a

and base to X.

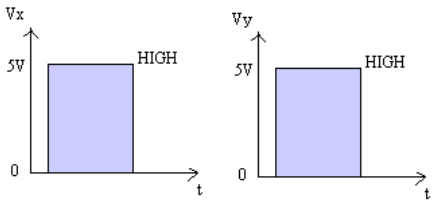



FIGURE 1.7b(i)

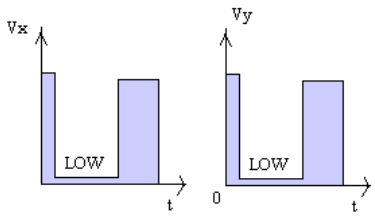



FIGURE 1.7b(ii)

**FIGURE 1.7** ILLUSTRATING THE PRINCIPLE OF OPERATION WITH A PNP TRANSISTOR

Similarly, if a PNP transistor was connected to points X,Y and Z as shown in figure 1.7(a), in this case with the base on X, emitter on Y and the collector on Z, the exact opposite situation as above would arise. The transistor would be behaving as an emitter follower and point Y would always have the same state with the input.

Table 1.2 shows the actual voltage levels at point Y when a PNP transistor (C9012) was connected in all six possible permutations for both HIGH and LOW input states.

| **Z** | **Y** | **X** | **Vx**= 5V(HIGH) | **Vx**= 0V(LOW) |
|---|---|---|---|---|
| **B** | **C** | **E** | 4.991V(HIGH) | 4.687V(HIGH) |
| **C** | **B** | **E** | 4.991V(HIGH) | 4.687V(HIGH) |
| **B** | **E** | **C** | 4.991V(HIGH) | 0.94V(LOW) |
| **E** | **B** | **C** | 4.991V(HIGH) | 4.996V(LOW) |
| **C** | **E** | **B** | 0.813V(LOW) | 0.813V(LOW) |
| **E** | **C** | **B** | 0.794V(LOW) | 0.794V(LOW) |

**TABLE 1.2**: VOLTAGES MEASURED AT POINT Y WHEN A PNP TRANSITOR WAS CONNECTED TO POINTS Z, Y, AND Y IN ALL SIX POSSIBLE PERMUTATIONS.

Similarly, the table shows that point Y would always have the same state with the input if and only when the base , emitter and collector are connected to Z,Y and X respectively.

With the support of solid – state matrix switches, the leads are automatically swapped in sequence for all possible permutations to points X,Y and Z. Hence, by noting the logic level at point Y in relation to that applied at point X(input), the leads of a transistor and the type of transistor could be deduced.

The results are displayed on a 3-digit seven-segment display.

A microcontroller is used to control the electronic switch matrix, the display, input the test pulses and read the logic states of point Y. The figure below shows the arrangement of the ITA.

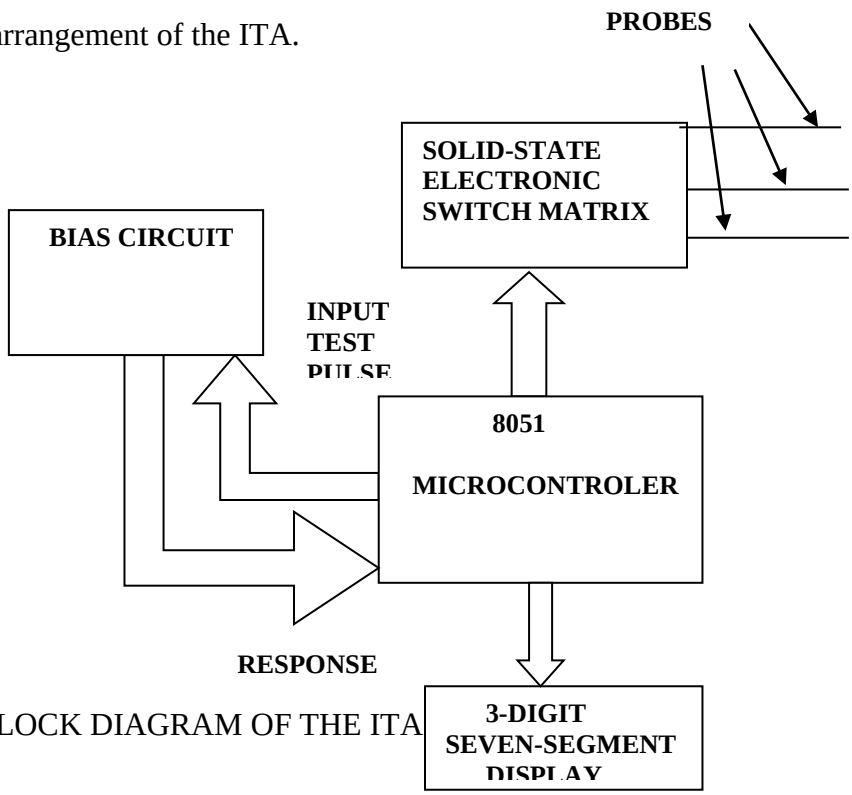



**FIGURE 1.8**: BLOCK DIAGRAM OF THE ITA

# CHAPTER 2

## 2.0 COMPONENTS DESCRIPTION

### 2.10 INTRODUCTION

This chapter aims at describing the major components of the ITA. The components making up each building block of the ITA were described.

## 2.2O THE ELECTRONIC SWITCH ARRAY MATRIX

### 2.21 THE 4066 QUAD BILATERAL ANALOG SWITCHES.

This device is a CMOS (Complementary Metal Oxide Semiconductor). It contains four bilateral analog switches, which acts essentially as a single-pole, single throw switch controlled but an input logic level. This device will pass signals in both directions and is useful for digital and analog applications. Figure 2.0 shows the basic arrangement for one of the four switches contained in the package. It consists of a P-MOSFET and N-MOSFET in parallel so that both polarities of input voltage can be switched. The CONTROL and its inverse are used to turn the switch ON (closed) and OFF (open). When the CONTROL is HIGH, both MOSFETS are turned ON and the switch is closed. When CONTROL IS low, both MOSFETS are turned OFF and the switch is open. Ideally, this circuit operates like an

electromechanical relay. In practice, when the switch is closed, the switch resistance $R_{ON}$ is typically 200Ω. In the open state, the switch resistance is very high, typically $10^{12}$Ω, which for most purposes is an open circuit.

**CONTROL**

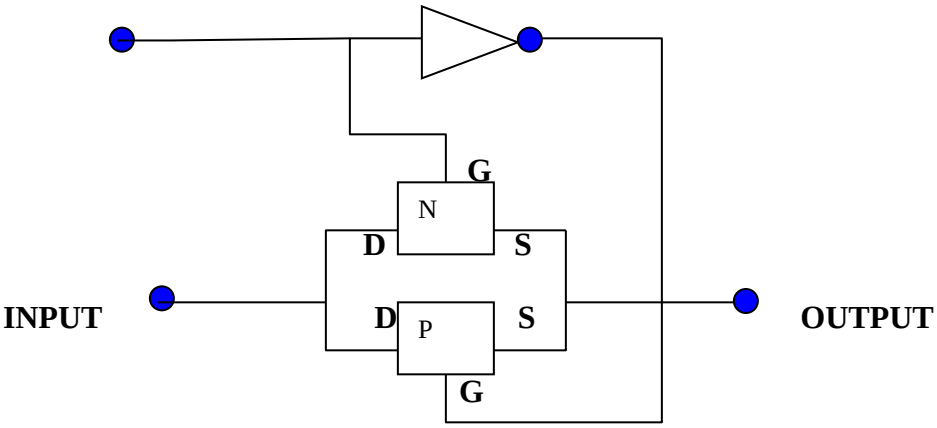
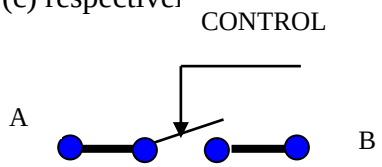
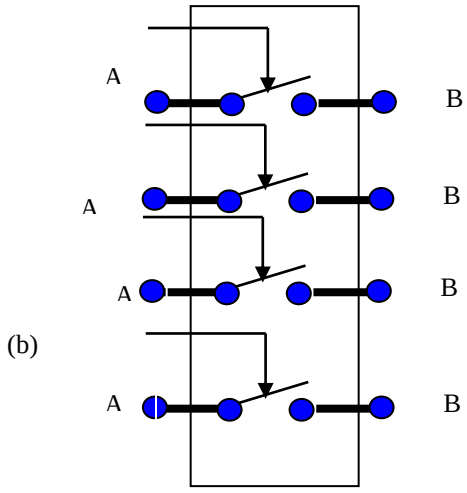



**FIGURE 2.0:** BASIC ARRANGEMENT OF BILATERAL SWITCH

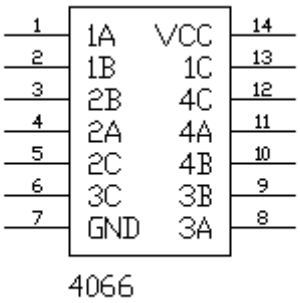
Each of the four switches is independently controlled by its own control input. The symbol, innards and pin-out are shown in Figure 2.1(a), (b) and (c) respectivel--




(a)




(b)




(c)

**FIGURE 2.1** THE 4066 BILATERAL SWITCH (a) BILATERAL SWITCH SYMBOL (b) TRADITIONAL LOGIC SYMBOL (c) PIN CONFIGURATION.

The I.C comes in a 14-pin DIL package and the power supply ranges from 3V to 15V DC. CMOS devices are susceptible to damage by electrostatic charges, so care is always taken when handling them.

## 2.22 THE CMOS HEF 40106 HEX SCHMITT INVERTER.

An inverter is a logic circuit that has only a single input, and its output logic level is always opposite to the logic level of this input. It is sometimes called

a NOT gate. Figure 2.2 shows the truth table, symbol and sample waveforms of the inverter.

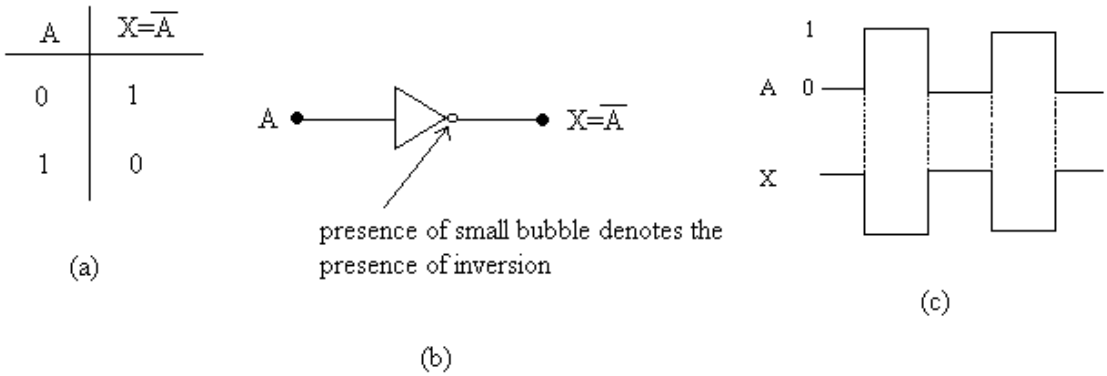



**FIGURE 2.2** THE NOT GATE (a) TRUTH TABLE (b) SYMBOL FOR THE INVERTER (c) SAMPLE WAVEFORMS.

The HEF40106 HEX SCHMITT INVERTER is a 14-pin DIL I.C manufactured by Philips Semiconductors, though other manufacturers are also producing the same device. This I.C contains six independent Schmitt inverters (indicated by the word “HEX”) and it is also a CMOS device.

A device with Schmitt trigger-type of inputs is designed to accept slow changing signals and produce an output that has oscillation-free transistors. Logic gates or deices with Schmitt-type inputs have a double “S” like symbol, “∫∫”, drawn on it. Standard devices without Schmitt type of inputs are susceptible to produce oscillations when driven by inputs with relatively

slow transitions times. These oscillations can produce erratic triggering of flip-flops and other devices connected to it.

## 2.23 THE ZENER DIODE

A diode is a two terminal semiconductor device consisting of a P-N junction formed either with germanium or silicon crystals. Its circuit symbol (of Zener diode) is shown in figure 2.3 below. The P- and N- type regions are referred to as anode and cathode respectively.

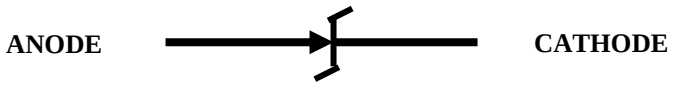



**FIGURE 2.3:** A ZENER DIODE CIRCUIT SYMBOL

A Zener diode is a reverse-biased heavily doped silicon (germanium) P-N junction diode that is operated in the breakdown voltage where current limited by both external resistance and power dissipation of the diode.

For proper working of a Zener diode in any circuit, it is essential that it must

(i) be reversed- biased

(ii) have voltage across it greater than $V_Z$ ( which is Zener breakdown voltage)

(iii) be in a circuit where current is less that $I_{ZMAX}$ (maximum zener current limited by maximum power dissipation).

## 2.231 USES OF ZENER DIODES

(i) As voltage regulators.

(ii) As fixed reference voltage in a network for biasing and comparison purposes and for calibrating voltmeters.

(iii) For meter/ instrument protection against damage from accidental application of excessive voltage and electrostatic discharges. It is for protection purpose that a zener diode was used in the ITA.

## 2.24 THE 74138 DECODER.

A decoder is a logic circuit that accepts a set of inputs that represents a binary number and activates only the output that corresponds to that input number. In other words, a decoder circuit looks at its input, determine which binary number is present there, and activates the one output that corresponds to that number; all other outputs remain inactive. The diagram for a general decoder is shown in figure 2.4 with N inputs and M outputs. Since each of the N inputs can be 0 or 1, there are $2^N$ possible input conditions or codes. For each of these input conditions only one of the M outputs will be active (HIGH); all other outputs are LOW. Many decoders are designed to produce active-Low outputs like the 74138 decoder.

Figure 2.4 shows the pin-outs for the 74138 decoder. The 74138 has three inputs and $2^3$, i.e. 8 outputs. This decoder is referred to in several ways. It can be called 3-line-to-8-line-decoder, because it has three input lines and 8

output lines. It could also be called a binary-to –octal decoder because it takes a 3-bit binary input code and activates the one of the eight (octal) outputs corresponding to that code. It is also referred to as 1-of-8- decoder because only 1 of the 8 outputs is activated at one time.

Table 2.0 shows the Truth Table

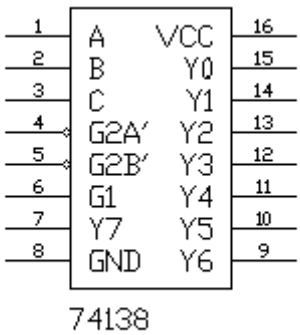



**FIGURE 2.4** PIN ARRANGEMENT OF THE 74138 DECODER.

| C | B | A | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ | $Q_6$ | $Q_7$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**TABLE 2.0** TRUTH TABLE OF THE 74138 LINE DECODER

## 2.25 TEST LEADS.

The test leads all have crocodile clips at their ends for easy connection to the leads of the transistor. The leads are labeled A, B and C and each correspond to a digit of the display.

## 2.30 THE DISPLAY

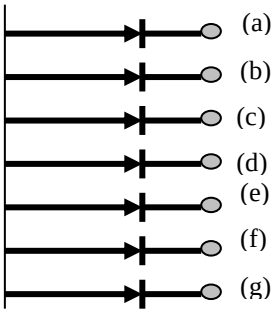
### 2.31 SEVEN SEGMENT DISPLAY.

A seven segment display consist of seven rectangular LEDS which can form the digits 0-9 and some alphabets such as e, b, c, d, e, f, y, e.t.c.

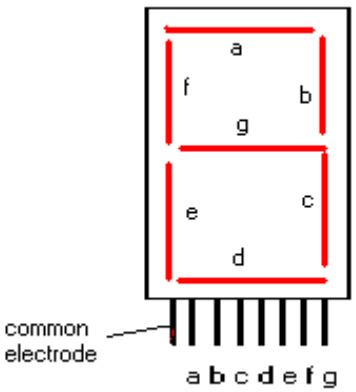
The seven LEDS segments are labeled ‘a’ to ‘g’. Each of the segments is controlled through one of the display LEDS. Seven segment displays come in two types; Common anode and Common cathode types.

In the Common anode type, all the anodes of the diodes are tied together as shown in Figure 2.5. This makes it possible to light any segment by forward biasing that particular LED. For example, to light the letter ‘e’, segments a, b, d, e, f and g must be forward biased. Since the anodes are tied together to $V_{CC}$ (5 V), only a ground is to be applied to the cathodes of these segments.

The common cathode seven segment display has all its cathodes tied together to ground and 5V is used to light the individual segment. The common anode type was used for the intelligent transistor analyzer.




(a)




(b)

**FIGURE 2.5** SEVEN-SEGMENT DISPLAY (a) COMMON ANODE SEVEN SEGEMNT ARRANGEMENT (b) DISPLAY MODULE.

## 2.32 RESISTORS.

A resistor is a device, which provides resistance in any electrical circuit. The resistance of a resistor is said to be linear if the current through the resistor is proportional to the potential difference across its terminals. If the resistance were to vary with the magnitude of either the voltage or the current, the resistance is said to be non-linear. Resistors made from semiconductor materials are examples of non-linear resistors.

All resistors have power ratings, which is the maximum power that can be dissipated without the temperature rise being such that damage occurs to the resistor. Thus a 1-watt resistor with a resistance of 100 ohm can pass a current of 100mA; whereas a ¼ watt resistor with the same resistance could

only handle a current of 50mA. In electronic circuits, the common standard ratings are ¼, ½, 1 and 2 watts. This is mainly proportional to size with bigger resistor having a higher power rating.

Resistors are made in a variety of ways but they all fall into the following categories:

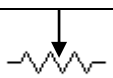
| **SYMBOL** | **REPRESENTATION** |
|---|---|
|  | Fixed resistor |
|  | Variable resistor |
|  | |
|  | Potentiometer |

**TABLE 2.1** TYPES OF RESISTORS

Resistors are made with different ratings and the rating is written on the body or represented by coloured rings (bands) around its body. There are normally four bands around a colour-coded resistor. The first two bands (closer to the resistor's end) represents the first two digits of its resistance. The third band represents the number of 'zeroes' to be added to this two digits and the last one represents the tolerance of the resistor.

The value of each colour is shown in Table2.1a below and tolerance in Table 2.1b.

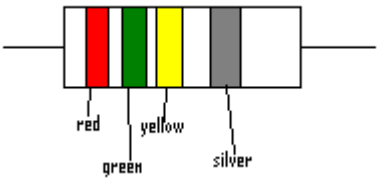
| Digit | Colour |
|---|---|
| 0 | Black |
| 1 | Brown |
| 2 | Red |
| 3 | Orange |
| 4 | Yellow |
| 5 | Green |
| 6 | Blue |
| 7 | Violet |
| 8 | Gray |
| 9 | White |

**TABLE 2.1 (a)**: DIGIT REPRESENTED BY EACH COLOUR IN A RESISTOR

| **Tolerance** | **Colour** |
|---|---|
| 1% | Brown |
| 5% | Gold |
| 10% | Silver |
| 20% | No colour Band |

**TABLE 2.1(b)**: TOLERANCE REPRESENTED BY A COLOUR IN A RESISTOR

Example:




(Rating is 250000 ± 25000)

**FIGURE 2.6**: ILLUSTRATING RESISTOR COLOUR CODING

## 2.40 THE CONTROL CIRCUIT.

The control circuit or section controls all the processes of the sequencer, matrix switching and display circuits. The control circuit provides the test signals for the sequencer circuit and reads the logic levels at the test points A and B, hence making deduction on the type of transistor. At the same time, it sends signals to the matrix switching circuit to automatically swap (or routes) the probes to the different permutations.

The control section also provides the necessary codes used by the display.

The control section is simply made up of one component, which is the Intel's 8051 microcontroller.

## 2.41 THE INTEL'S 8051 MICROCONTROLLER.

A microcontroller is a microcomputer specially designed for dedicated control applications.

The 8051 microcontroller is an 8-bit controller first manufactured in 1980 by Intel. The microcontroller is widely used in many applications because of its ease to use and program. It is a 40-pin I.C available in a variety of packages. Figure 2.7 below shows the pin-outs of the 8051 in a 40-pin DIL package.

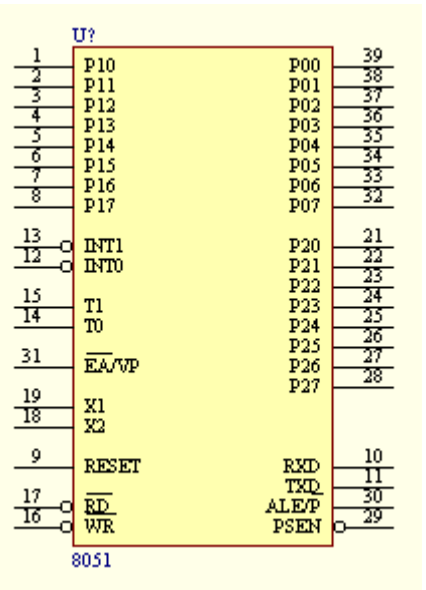



**FIGURE 2.7** LOGIC SYMBOL OF THE 8051 MICROCONTROLLER.

## 2.411 ELEMENTS OF THE 8051.

### 2.4111 THE CPU.

The CPU, or Central Processing Unit, executes program instructions. Types of instructions include, arithmetic (addition, subtraction), logic (AND,

OR, NOT), data transfer (MOVE), and program branching (Jump) operations. An external crystal (12MHZ) provides a timing reference for clocking the CPU.

### 2.4112 THE ROM

ROM (Read-Only-Memory) is the read only memory that is programmed into the chip in the manufacturing process. The 8051 has 4KB of on- chip ROM.

### 2.4113 THE RAM

RAM (Random- Access-Memory) is where programs store information for temporary use. Unlike the ROM, the CPU can write to the RAM as well as read it. Any information stored in the RAM is lost when power is removed form the chip. The 8051 has 128 Bytes of RAM.

### 2.4114 I/O PORTS.

I/O (Input/output) ports enable the 8051 to read and write to external memory and other components. The 8051 has four 8-bit I/O ports (labeled Ports 0-3). As the name suggests, the port s can act as inputs (to be read) or output (to be written to). Many of the port's bits have optional, alternate functions relating to accessing external memory, using the on-chip

timer/counters, detecting external interrupts and handling serial communications.

## 2.4115 EXTERNAL MEMORY.

Although the 8051 is a single-chip computer, a complete 8051 system requires additional components. It must have an EPROM, EEPROM, or battery-backed RAM for permanent storage programs. EPROMS are widely used in most applications.

## 2.4116 THE EPROM

The user can program an EPROM, and it can also be erased and re-programmed a often as desired. Once programmed, the EPROM is a non-volatile memory that would hold its stored data indefinitely. The process for programming an EPROM involves the application of special voltage levels (typically 10V-25V range) to the appropriate chip inputs for a specified amount of time (typically 50ms per address location). A special programming circuit that is separate from the circuit in which the EPROM will eventually be working usually performs the programming process. The programming circuit or device is called an EPROM programmer.

An EPROM is erased by exposing it to ultraviolet light applied through a quartz window on the chip package.

EPROMs are available in a wide range of capacities, e.g. 32K X 8, 64K X 8, e.t.c . The numbers ‘32’ and ‘64’ indicates the memory size and ‘8’ indicates the word size, i.e. it is an 8-bit EPROM.

The figure 2.7 below shows the logic symbol of a 4K X8 EPROM.

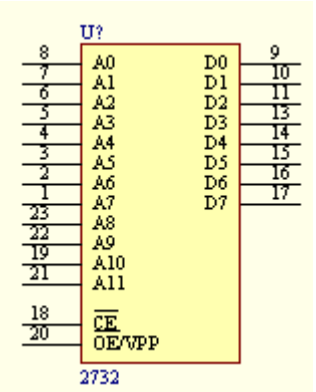



**FIGURE 2.7** AN EPROM (a) TRADITIONAL LOGIC SYMBOL.

Accessing this external memory(-ies) uses all of ports 0 and 2, plus bit 6 and 7 of port3 of the 8051, to hold data, addresses, and control signals, for reading or writing to external memory. Data here refers to a byte or word to be written or read.

## 2.4117 RESET

The RESET input pin resets the chip and cause it to begin executing the program from the start of memory. A logic HIGH on the RESET input will reset the 8051.

## 2.4118 CONTROL SIGNALS

a. PSEN (Program Store Enable): This is an external control signal. The 8051 strobes, or pulses PSEN whenever it accesses external code memory. Accesses to internal code memory do not use PSEN or any external control signals.
b. RD/WR (READ/WRITE): Instructions that read data from memory strobes the RD line while those that write to RAM strobe WR.

## 2.4119 POWER SUPPLY CONNECTIONS.

The 8051 has two pins for connecting to a 5V D.C power supply ($V_{CC}$) and ground ($V_{SS}$). The pin numbers are pin 40 and pin20 respectively.

## 2.50 POWER SUPPLY

### 2.51 THE 7805 POSITIVE VOLTAGE REGULATOR.

"Voltage regulators otherwise known as voltage stabilizers are employed to produce a regulated 5V D.C supply to the microcontroller board, display and bias circuits.

The 7805 comes in a T220 plastic package. The prefix "78" denotes positive input and output voltages, and the suffix "05" denotes the voltage output form the regulator. The regulator is rated for a maximum load current of 1A. Worst-case unregulated D.C input voltage should normally be at least 3V greater than the nominal regulated output voltage. If this is not observed, there would be problem of poor regulation and unacceptable level of residual mains hum present at the output.

Also, the worst unregulated D.C input voltage should not be allowed to exceed the nominal output voltage by more than 15V otherwise the regulator heat dissipation will be excessive. This leads to premature thermal shutdown.

| SPECIFICATIONS FOR 7805 REGULATOR | |
|---|---|
| TYPE | POSITIVE |
| INPUT VOLTAGE(VOLTS) | 7-25 |
| LOAD REGULATION (%) | 0.2 |
| TIME REGULATIION (%) | 0.2 |
| RIPPLE REJECTION (%) | 71 |
| OUTPUT RESISTANCE (MΩ) | 30 |
| OUTPUT NOISE VOLTAGE (10Hz TO 100KHz) | 40 |
| SHORT-CIRCUIT(mA) | 750 |

**TABLE 2.2** SPECIFICATIONS FOR THE 7805 POSITIVE VOLTAGE REGULATOR

# CHAPTER 3

## 3.0 DESIGN OF THE INTELLIGENT TRANSISTOR ANALYZER.

### 3.1 INTRODUCTION.

The Intelligent Transistor Analyzer (ITA) on its own is a dedicated mini-computer. This is because a microcontroller is embedded into it for the purpose of control.

A microcontroller project is composed of two parts:-

(i) The hardware and (ii) The software or program.

The hardware is basically the components used in the circuit, while the software refers to the program stored in the EPROM, which the computer executes. The program is written in assembly language. Assembly language is a low-level language that is one-step above machine language. It is used for real time applications such as the ITA. Assembly language is made up of abbreviations called mnemonics (memory aids) used instead of the actual machine language oriented codes.

This chapter is aimed at describing the design and working of both the hardware and software components of the ITA. A flow chart was used to explain the program flow.

## 3.2 THE HARDWARE

The hardware consists of three parts.

(i) The bias circuit

(ii) The display circuit

(iii) The controller circuit.

## 3.21 DESIGN OF THE BIAS CIRCUIT.

The core circuit of the ITA is the bias circuit shown in Fig. 3.0

The points X, Y and Z are also connected to the solid- state switch matrix. Point Y is an output to the matrix and to the microcontroller, so that when a transistor is well biased, the microcontroller would take the appropriate action. Point X is an input from the microcontroller.

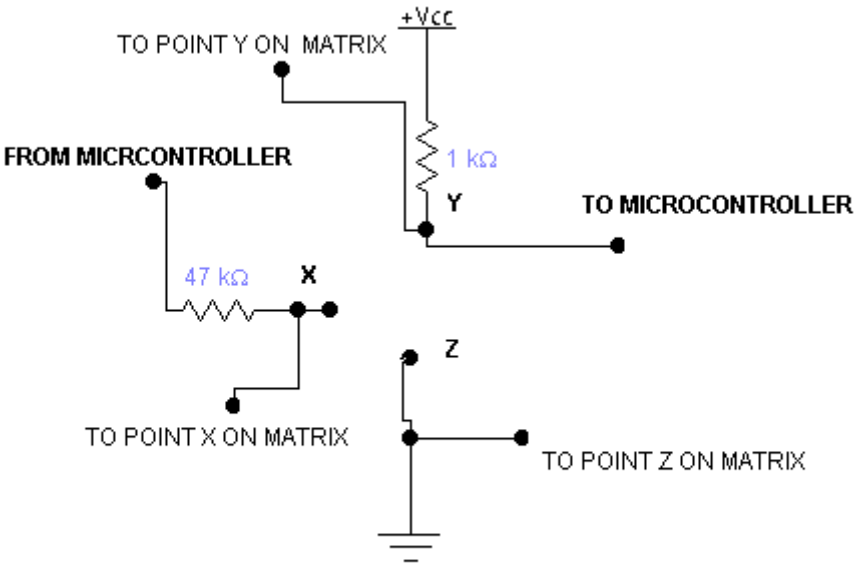



**FIGURE 3.0**: THE BIAS CIRCUIT

## CALCULATIONS

The bias circuit gives the correct logic only when it is biased as a common emitter configuration or common collector (emitter follower). In either configuration, the transistor is driven into saturation.

Using the common emitter configuration shown in figure 3.1

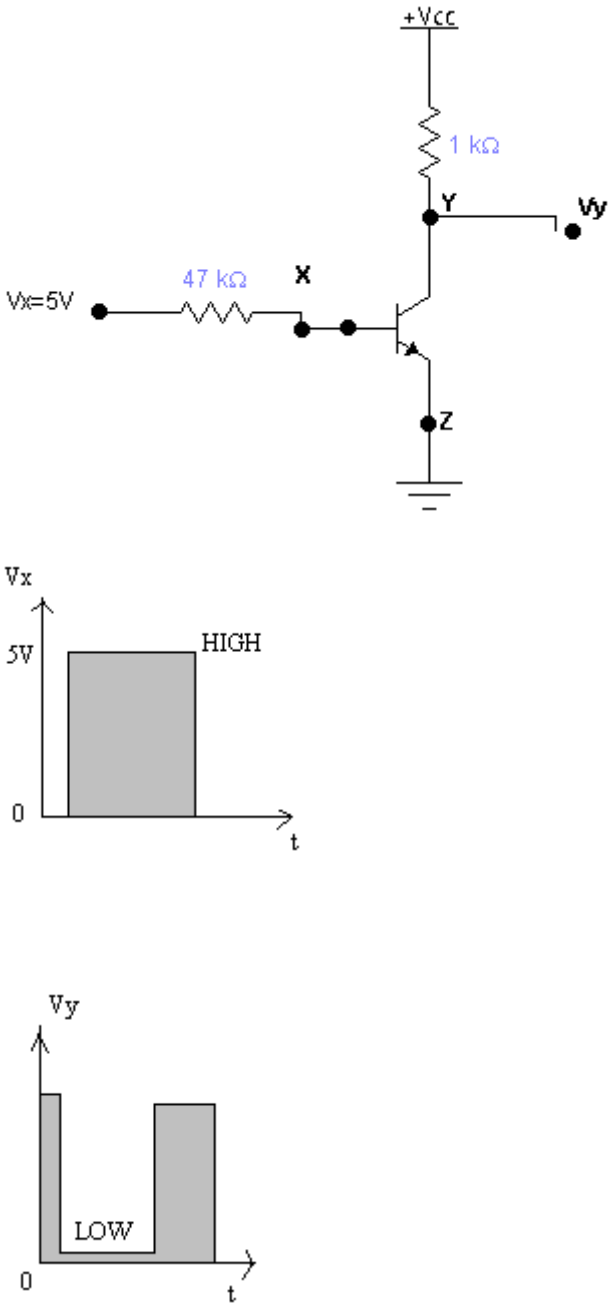



**FIGURE 3.1** A SATURATED COMMON EMITTER NPN TRANSISTOR

$I_{CSAT}=\frac{V_{CC}}{R_C} = 5/R_C$

$R_C$

Choosing Icsat=5mA which is within the limits of most transistors.

By Ohm's law

Rc=5V/5mA=1000Ω = 1KΩ

A typical value of β for transistors is 50. The level of $I_B$ in the active region just before saturation is given as

$I_B= I_{cSAT}/\beta_{dc}$

Therefore, $I_B$=5mA/50=100μA

The value of $R_B$ is given by

$I_B= V_i\text{-}0.7/R_B$

Where $V_i$ is the base input voltage=5V

Therefore, $R_B$=5-0.7/100μ=43KΩ

A preferred value is 47KΩ/10% tolerance.

For practical purposes, the output characteristics of a common collector are the same for a CE configuration. Hence, the same values of $R_c$ and $R_B$ applies for the CC using a PNP transistor.

## 3.22 DESIGN OF THE ELECTRONIC SWITCHING ARRAY MATRIX.

The full-circuit diagram for the electronic switch array matrix is shown in figure 3.2

The solid-state matrix was required to provide an automatic way of swapping the transistor leads around in all six possible permutations. It is made up of 18 bilateral electronic switches.

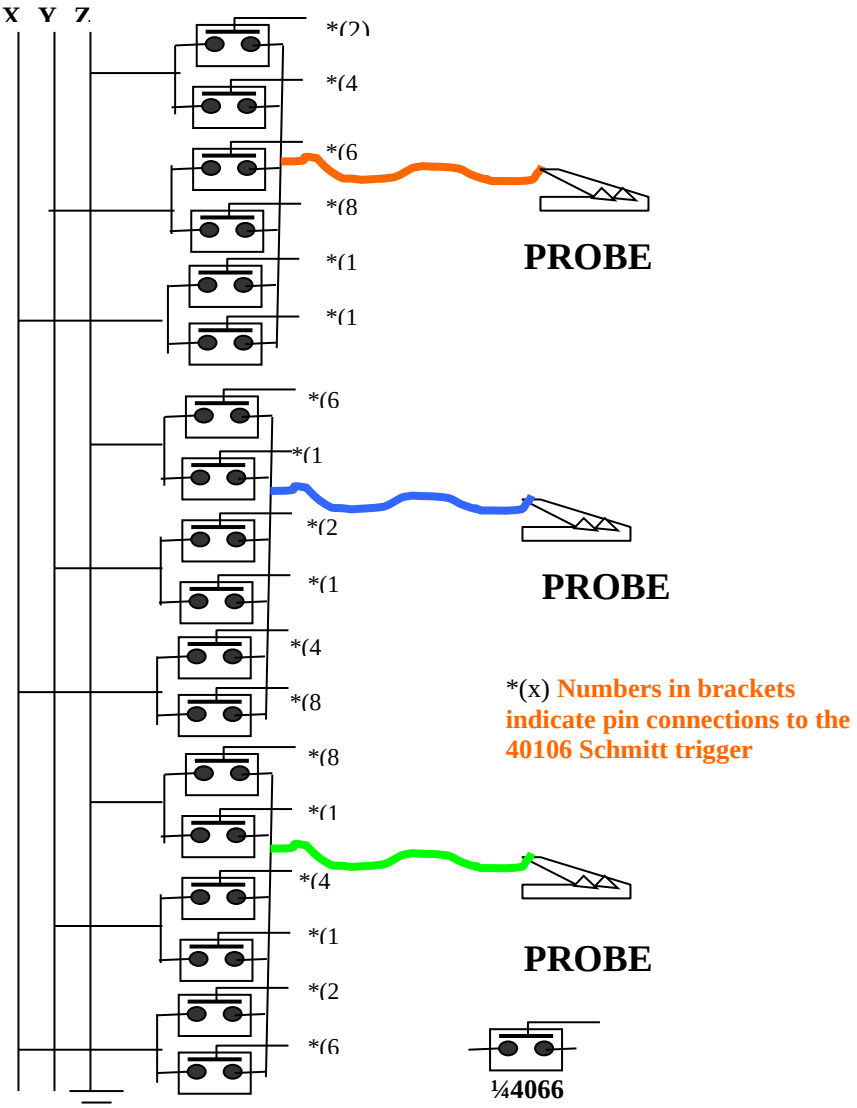



**FIGURE 3.2** CIRCUIT DIAGRAM OF THE ELECTRONIC SWITCH MATRIX ARRAY

The matrix was designed to route the leads of the transistor under test to the bias circuit in a particular order until the bias circuit responds to the permutation that gives the required logic conditions. When this happens, the

microcontroller takes note of the permutation. The matrix switches swaps the leads of the transistor points Z, Y and X respectively when a signal is applied to the appropriate control input used to close the electronic switches.

The six signals used to drive the control inputs of the electronic switches were derived from inverted outputs of the 74138, which is a line decoder. Zener diodes, $D_1$ to $D_3$ are present to protect the circuit from static charges that may come in contact with the test leads. Under normal circumstances, the Zener diode would not conduct and therefore doesn't interfere with the normal circuit operation. A 7V Zener diode was used for circuit.

## 3.23 DESIGN OF THE 3-DIGIT SEVEN SEGMENT DISPLAY.

The display is made up of 3-digit seven segment displays. It was designed based on the principle of demultiplexing. Demultiplexing is a process of using a single input source of data and distribute it over several outputs. Figure 3.3 shows the functional diagram for a digital multiplexer.

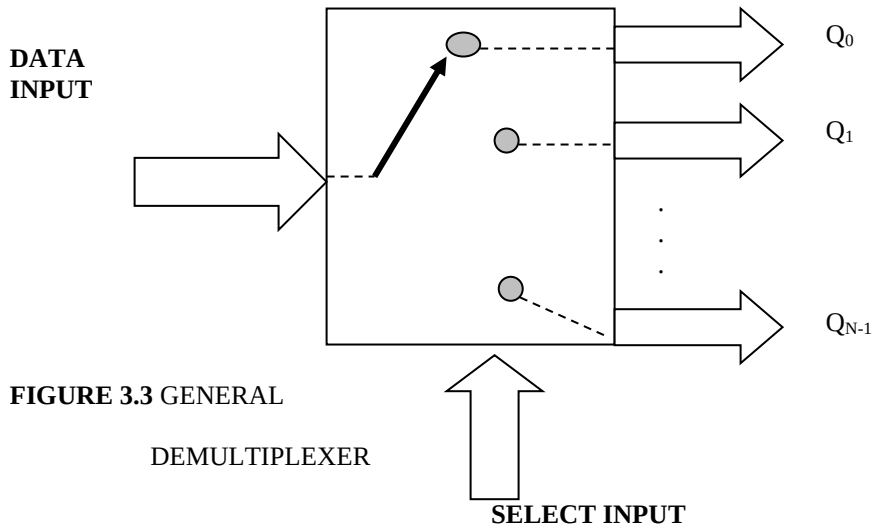



**FIGURE 3.3** GENERAL DEMULTIPLEXER

The large arrow for inputs and outputs each represent one or more lines. The SELECT input code determines to which output the DATA input will be transmitted. In other words, a demultiplexer takes one input DATA source and selectively distributes it to 1-to-N output channels just like a multi-position switch.

In the display, all the corresponding segments were tied together. The microcontroller emulates a demultiplexer in the sense that the different display codes to the segments for all the digits is input from the seven lines of port1(of the microcontroller) and selectively distributed to the digits of the display. Only the digit that its common anode is activated will display the DATA input at that particular time.

The demultiplexing action is done at a very high speed with different input codes from the controller being input to selected digits. This tends to create an illusion that all the digits are lit simultaneously.

Figure 3.4 shows the diagram of the display. All the corresponding segments of each digit were tied together to form a common connection.

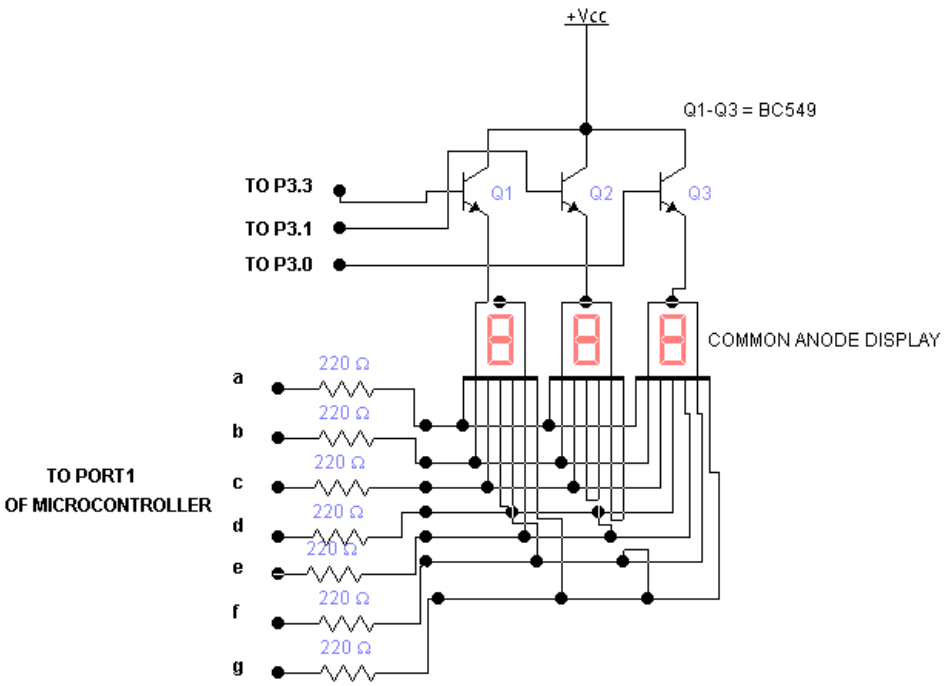



**FIGURE 3.4** THE 3-DIGIT MULTIPLEXED DISPLAY

## CALCULATIONS

### --CURRENT LIMITING RESISTORS.

Each segment of the seven-segment LED display is rated to operate at 10mA at 2.7v for normal brightness.

In order to limit the forward current to the appropriate value, a fixed resistor was connected in series with each LED segment as shown in figure 3.4.

The value of resistors were calculated from

$R= V-V_F/I$

Where $V_F$ is the forward voltage drop produced by the LED and V is the supply voltage which is +5V. $V_F$ is usually 2.7V

Therefore, R=5-2.7/10 X 10-3 =230Ω

The nearest preferred value is 220Ω.

The transistors are intended to provide enough current to drive the LEDS.

## 3.24 DESIGN OF THE POWER SUPPLY.

The ITA requires a 5V operation. This was gotten by stepping down, rectifying and smoothening of the mains supply voltage from the power company (NEPA). The supply was enhanced by regulating it with voltage regulator ICs to prevent voltage drops when load is added and any 100Hz ripple left over by the smoothing capacitors.

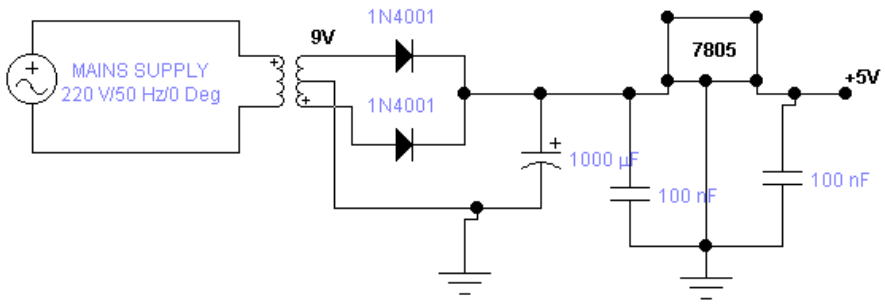



**FIGURE 3.5** A REGULATED 5 VOLTS POWER SUPPLY

## THE TRANSFORMER.

The transformer rating that was used was determined by the required voltage inputs to the ITA circuits. All the various circuits of the ITA was designed to be operated on a 5V supply. The voltage regulators require at least 2-3v above its regulated output (5V).

So, a 9V-0-9V center tap transformer was used to give an output of 9V measured from either end terminals to the center terminal. A transformer steps down the 240v rms nominal line voltage 9V rms voltage. This voltage has the same frequency of 50 Hz with the input voltage. The voltage transformation is done by the ratio of turns of the coils at the primary to the turns of the coil at the secondary path of the transformer,

$$E_1/N_1 = E_2/N_2$$

where $E_1$ and $E_2$ are the input voltage and output voltage respectively, and $N_1$ and $N_2$ the turns-ratio of the input and output coils respectively.

The 9V rms gives a peak to peak secondary voltage of

$$V_p = 9V/ 0.707 = 12.86V$$

## THE RECTIFIER.

Two rectifier diodes were used to rectify the AC output from the transformer. The 9V and -9V outputs from the transformer were connected to the rectifiers' anodes and the centre-tap connected to ground. The pulsating DC output was from the cathodes of the rectifier diodes connected together. The DC load voltage from the rectifier is given by

$$V_{DC} = 2V_p/\pi = (2 \times 12.86)/ \pi = 8.19V$$

And the output frequency = 2 x input frequency= 2 x 50 = 100Hz

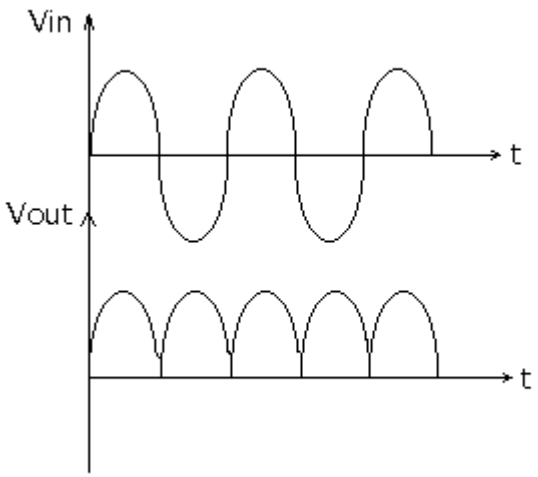



**FIGURE 3.6** VOLTAGE WAVEFORM OF A BRIDGE RECTIFIER

For each half-cycle, only one diode conducts, i.e there is a 0.7V drop in the output voltage.

Therefore, $V_{p\,(out)} = V_{p\,(in)} - 0.7V$

$V_{p(out)} = 8.19 - 0.7V = 7.49V$

## CAPACITORS.

The required power in the circuit is a steady DC supply so a capacitor was used to smooth the wave form from the full-wave rectifier. A capacitor placed across the pulsating output holds the voltage steady by charging and discharging with a ramp waveform so in calculating its value there is no need for a time constant or exponential.

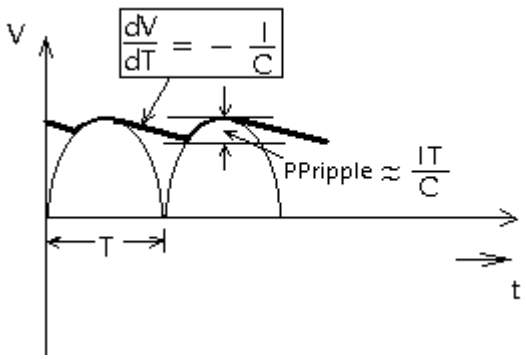



**FIGURE 3.7** THE EXPONENTIAL DISCHARGE OF A CAPACITOR

The circuit requires a 5 volt supply and can draw a maximum current of about 300mA from a regulated supply. Already chosen is the 9V-0V-9V

transformer which can give a peak voltage of 7.49V after rectification. The input to the regulator is required to be kept to about 2 volts peak-peak pp or less.

$$Ppripple = T\ (\Delta V/\Delta T) = T\ I/C$$

Where I= load current=300mA

$$T\ (period) = 1/f = 1/\ (2 \times 50) = 0.01s$$

$$So,\ \ 2 = 0.01\ (300\ X\ 10^{-3})\ /\ C$$

$$Therefore,\ C = 0.00003/2 = 0.0015 = 1500\mu F$$

The preferred value would be a 1000μF electrolytic capacitor.

## VOLTAGE REGULATOR.

This fairly constant voltage was kept constant using a 7805 positive voltage regulator.

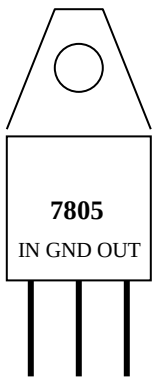



**FIGURE 3.8** A 5V FIXED VOLTAGE REGULATOR

The capacitor across the output improves the transient response and keeps the impedance low at high frequencies

## 3.3 THE SOFTWARE

The software directs the microcontroller on what action(s) it should take, how it should be taken, and when to take such actions(s).

The software for the ITA simply refers to the program written in assembly language. The program was stored in an EPROM.

### 3.21 SOFTWARE OPERATIONAL PRINCIPLE.

The program (or software) causes (or directs) the microcontroller to input a logic 1 at the point X of the biasing circuit and simultaneously closing a set of the bilateral switches of the matrix array, thereby routing the leads of the transistor under test to the biasing circuit. The transistor is tested for the first possible permutation. The program will then instruct the microcontroller to read the logic states at point Y and compares the phase shift with the input (point X). if it corresponds to the condition for NPN-Common Emitter or PNP-Common Collector configurations described earlier, the microcontroller sends the codes to display the configuration on the seven segment display, otherwise, the microcontroller advances to test for the next possible permutation.

The flow chart for program is shown in Appendix A.

# CHAPTER 4

## 4.0 CONSTRUCTION, EPROM PROGRAMMING AND PACKAGING OF THE ITA.

### 4.1 CONSTRUCTION OF THE ITA.

All the individual circuits making up the ITA were constructed on Veroboards. The I.C sockets for the semiconductors were first soldered to the Veroboards, followed by the crystal, resistors, capacitor, regulator, diodes, push buttons and the seven segment displays. Interconnections on the board were done with 26 S.W.G wires.

Care was taken during soldering to make sure that perfect and solid joints were made; otherwise the circuit may work intermittently.

### 4.11 CONSTRUCTION OF THE CASING.

The casing of the ITA was constructed with Perspex. Perspex was chosen because it is light, cheap and easy to work on and lastly, it gives a fine finishing.

The top side of the casing was made with red-coloured Perspex while the other sides were constructed with transparent Perspex. The top side was constructed with red-coloured Perspex because it enhances the display.

The Perspex was cut into shapes using a hack-saw, and “superglue” was then used to join the pieces together to form a cuboid-like enclosure.

Holes were drilled using a 10mm drill to bore holes for the mounting screws, test probes

Push buttons and power supply inlet.

Figure 4.0 shows the finished casing for the ITA.

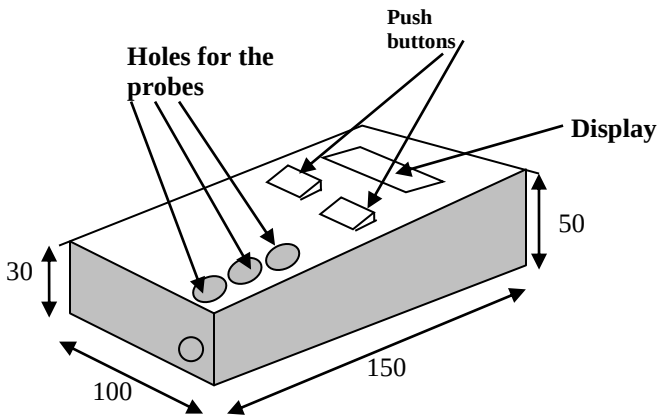



**FIGURE 4.0** PERSPEX CASING FOR THE ITA

## 4.2 PROGRAMMING THE EPROM.

The program for the ITA is stored in the EPROM. The EPROM was programmed using an equipment known are “EPROM PROGRAMMER” or “EPROM BURNER”. The program that is burned in the EPROM remain there even when power is removed from the circuit. The programmme is erased when it is exposed to ultraviolet light.

After the EPROM was programmed, it was removed from the programmer and inserted in its D.I.L socket on the microcontroller board.

## 4.30 PACKAGING OF THE ITA.

The dimensions of the casing were just enough to accommodate the microcontroller board, transformer, matrix switch array and display circuits. The display was mounted beneath the top red-coloured Perspex with screws. In this way, the display can be viewed at a wide angle. The other circuits were firmly screwed to the case.

Next, the test probes, the push-buttons, power switch were secured in their positions.

Lastly, the probes and display were labeled using ink.

# CHAPTER 5

# 5.0 TESTING, LIMITATIONS, CONCLUSION AND RECOMMENDATION

## 5.10 INTRODUCTION.

This chapter describes the testing of the ITA and how the ITA is used to analyze BJTs. The limitations of the ITA were stated and conclusion and recommendation given.

## 5.20 TESTING AND THE USE OF THE ITA.

First, the power cord of the ITA was inserted into a 220V 50Hz mains supply outlet and switched on. The display showed a message “USE ITA TO TEST BJT” repeatedly. This shows that the ITA was working and ready to be used.

Next, a 2N2222 transistor whose lead arrangement is known was connected to the probes using the crocodile clips at their ends. The emitter (e) was connected to probe ‘A’, the base (b) on probe ‘B’ and the collector(c) on probe ‘C’. Then, the “TEST” button was depressed and within seconds the display showed ‘EBC’/ NPN on segments A,B and C respectively. Probes ‘A’ and ‘B’ were interchanged after the ‘CLEAR’ button was depressed and the ‘TEST’ button depressed again, the ITA took note of the change on displayed ‘BEC”/NPN. Similar results were obtained using a PNP transistor.

When a bad transistor or any other three-terminal semiconductor was connected, the ITA displayed “BAD” or “ERR” (meaning Error) alternately on its display.

## 5.30 LIMITATIONS OF THE ITA

(i) The ITA was not designed for testing or analyzing transistors other than BJTs.

Though when used to test FETS, it gave the BJT’s Leads equivalents.

(ii) The ITA is not able to test transistors that are in-circuit and must NEVER be connected to nay powered devices as damage could result to both the ITA and the equipment under test.

## 5.40 CONCLUSION

It is no exaggeration to say that the microprocessor and the microcontroller have revolutionized the electronics industry and have had a remarkable impact on many aspects of our lives. The development of extremely high-density I.Cs has so sharply reduced the size and cost of microcomputer that designers routinely consider using their power and versatility in a wide variety of products and applications. One of such applications includes the ITA described here in this work. The use of microcontrollers as basis of

design has the following advantage over sequential logic I.Cs or discrete components:

***(I)COMPATIBILTY***: Complex circuits designed with microcontrollers require lesser components to implement hence making them to be small in size.

***(II) COST***: Though some microcontrollers are quite expensive, but their processing power is a price worth paying. It costs less (in terms of time and perhaps money) to accomplish a complex task with a microcontroller than using sequential logic I.Cs to perform the same task.

(III) ***SPEED:*** Circuits designed with microcontrollers are far much faster and efficient than those built with logic I.Cs.

(IV) Improvements or modification could easily be done by just re-programming the EPROM and little or no change on the hardware.

Therefore, the microcontroller is a better choice when a complex task is to be accomplished. With a microcontroller, the designer has the sky as his starting point.

# RECOMMENDATIONS

The design work is recommended for use

(i) In all electrical/electronic laboratories of Universities, Polytechnics and technical colleges for experiments relating to bipolar transistors.

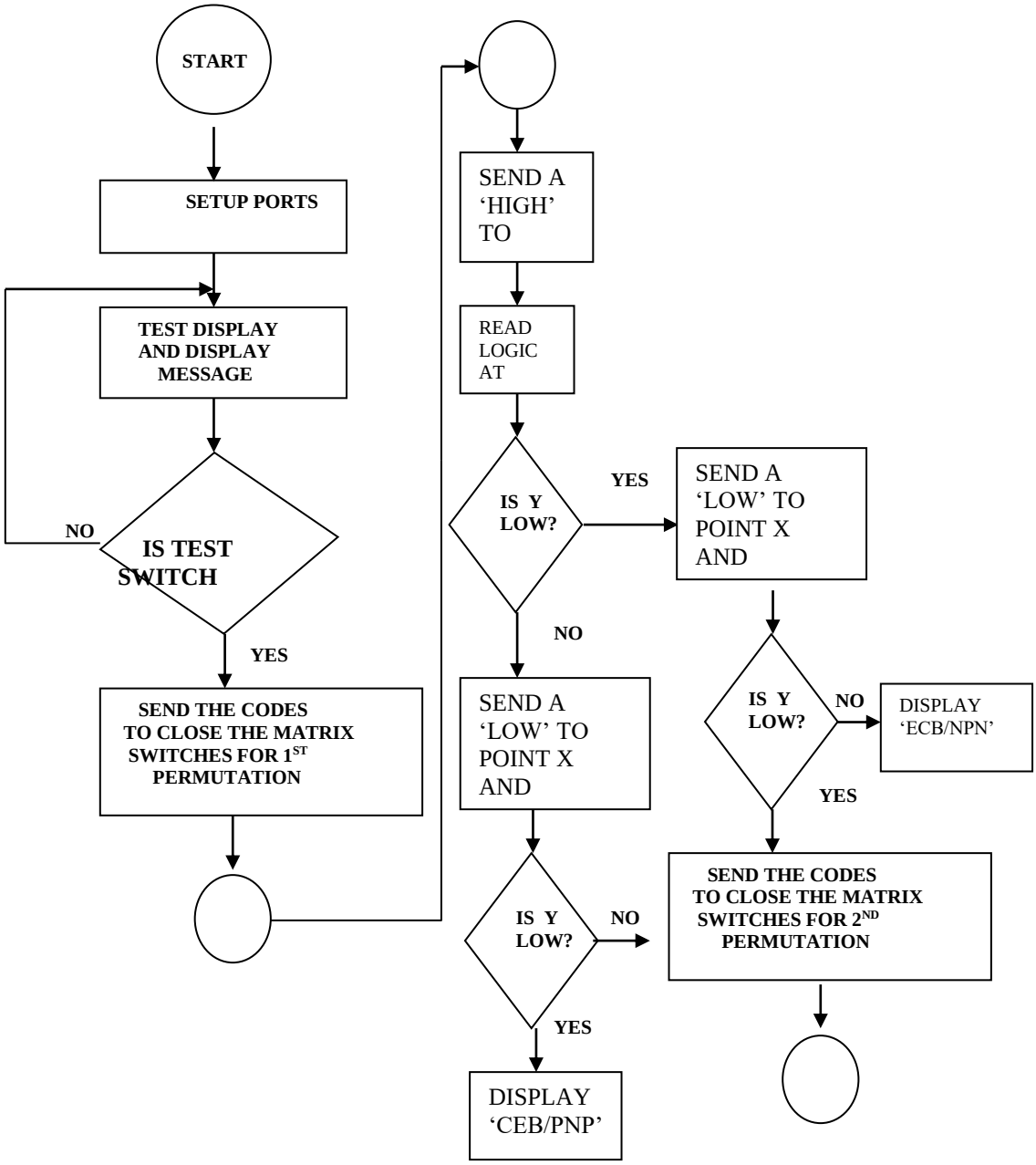
(ii) In small scale production workshops.

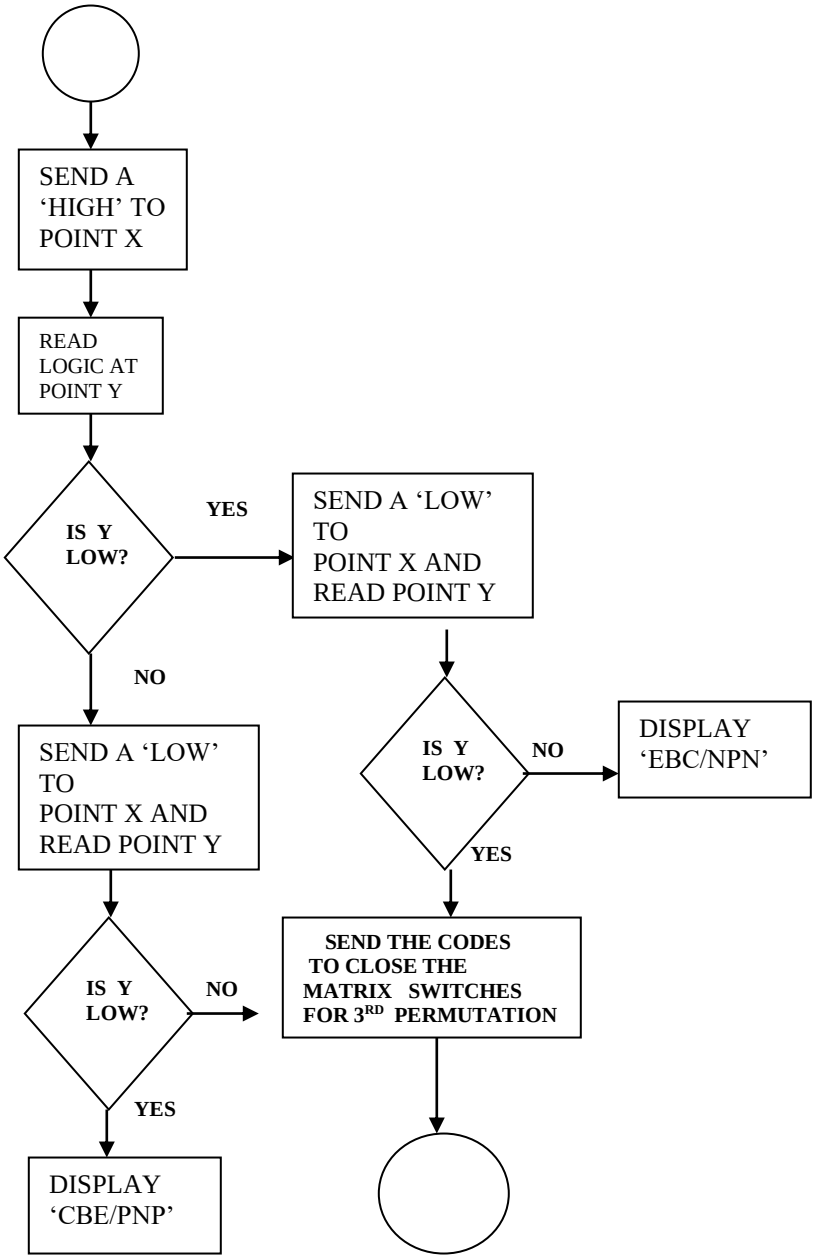
(iii) By technicians and road-side consumer electronics maintenance personnel.

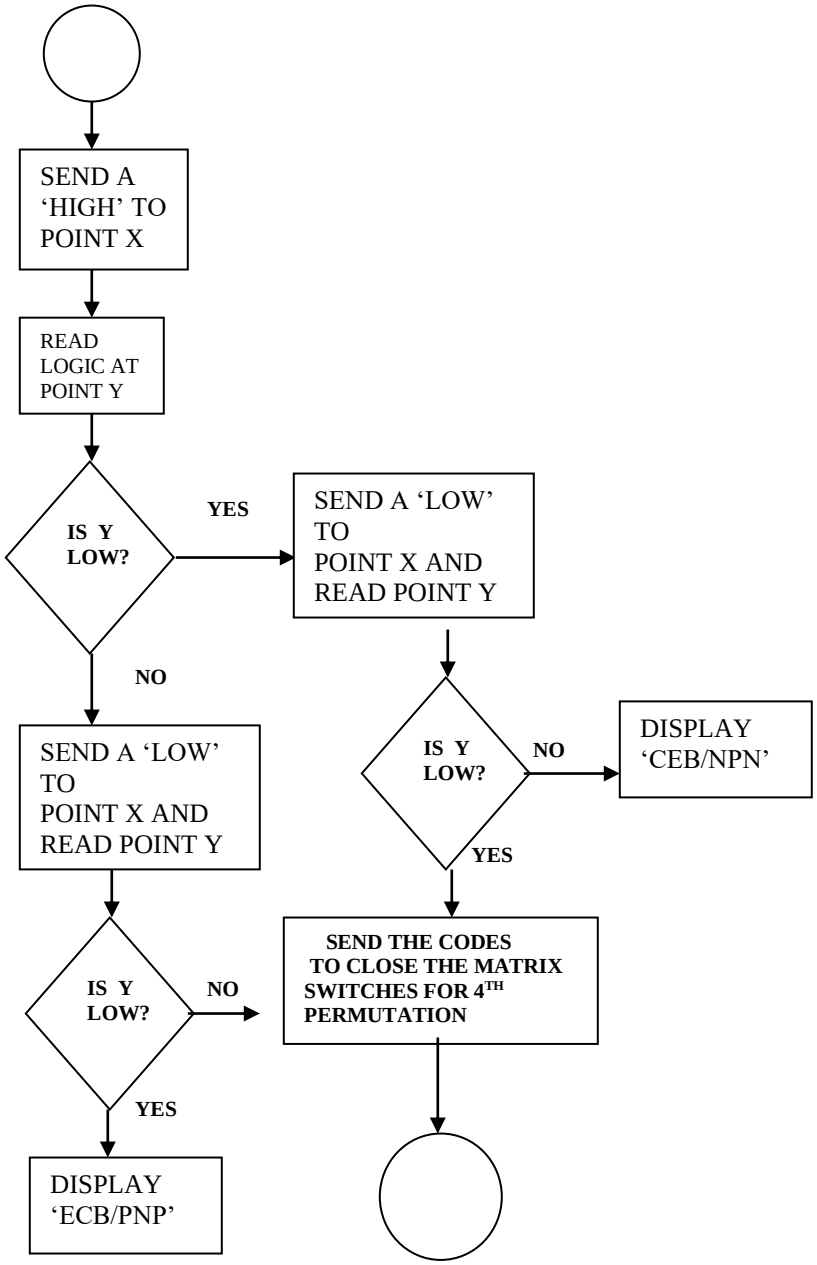
(iv) By any electronic hobbyist.

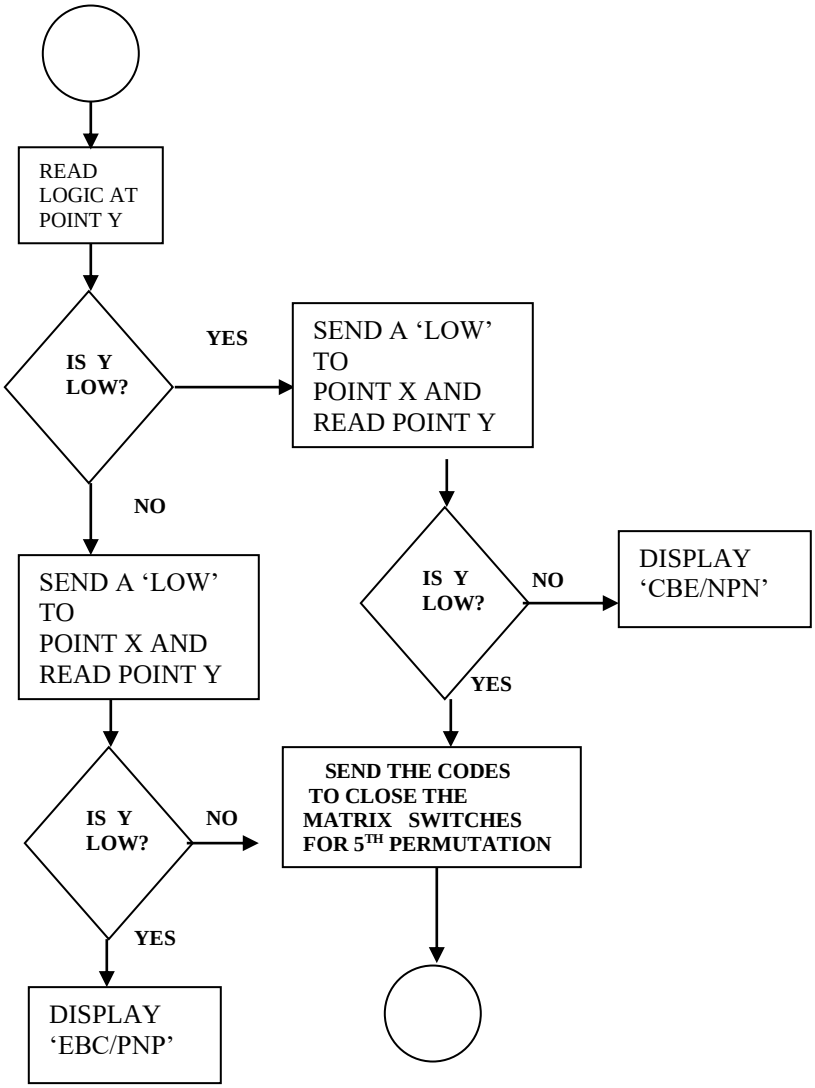
I also recommend that the department should introduce practical courses on computer engineering to include the use of microcontrollers and assembly language to enable students to be capable of designing and building microcontroller based projects used in accomplishing complex tasks. Computer systems equipped with EPROM burners should be provided in the laboratory made to be at the students' disposal.

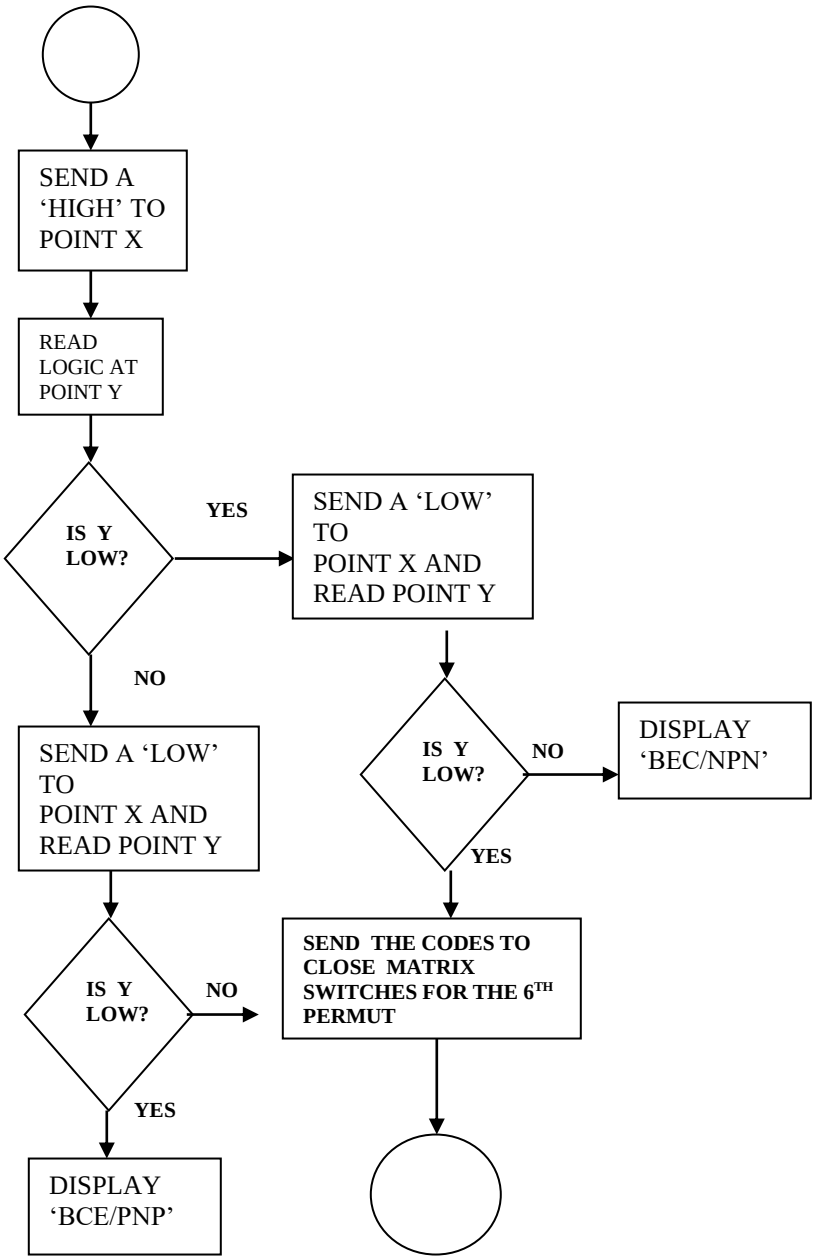
## APPENDIX A PROGRAM FLOW CHART FOR THE INTELLIGENT TRANSISTOR ANALYZER

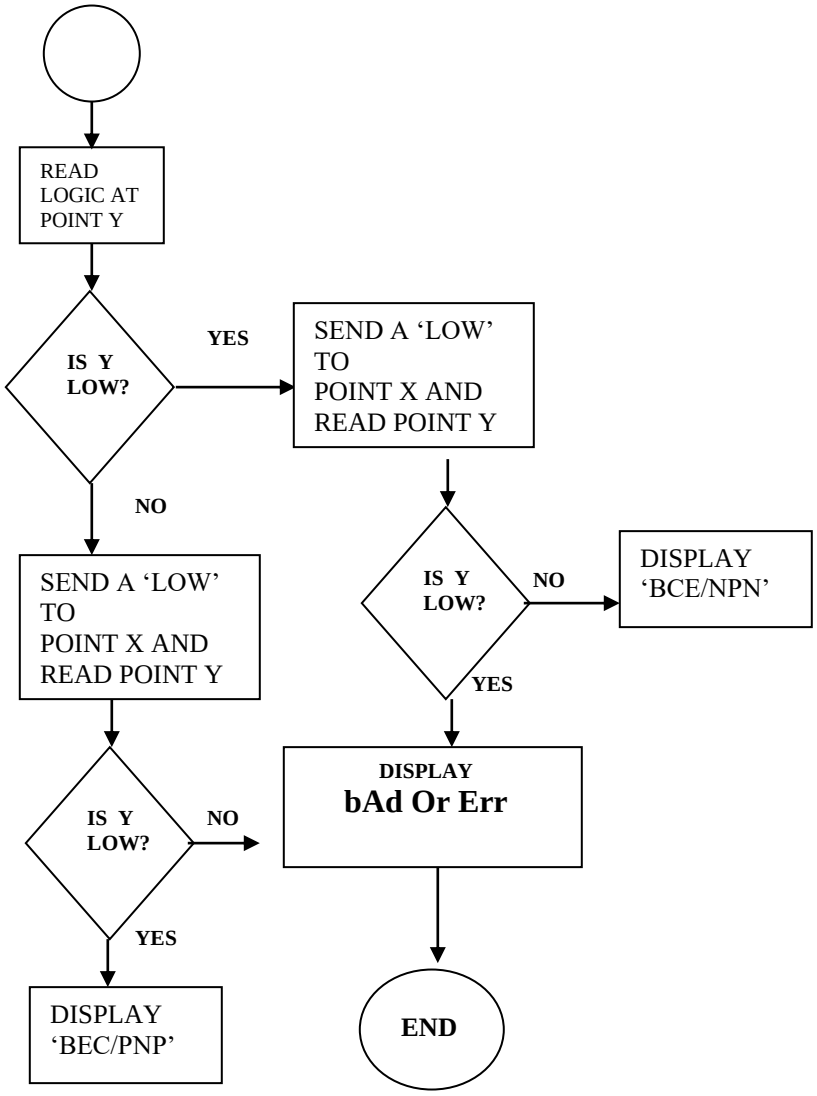



SEND A 'HIGH' TO POINT X
READ LOGIC AT POINT Y
IS Y LOW?
YES
SEND A 'LOW' TO POINT X AND READ POINT Y
NO
SEND A 'LOW' TO POINT X AND READ POINT Y
IS Y LOW?
NO
DISPLAY 'EBC/NPN'
YES
SEND THE CODES TO CLOSE THE MATRIX SWITCHES FOR 3RD PERMUTATION
IS Y LOW?
NO
YES
DISPLAY 'CBE/PNP'


SEND A 'HIGH' TO POINT X
READ LOGIC AT POINT Y
IS Y LOW?
YES
SEND A 'LOW' TO POINT X AND READ POINT Y
IS Y LOW?
NO
DISPLAY 'CEB/NPN'
YES
SEND THE CODES TO CLOSE THE MATRIX SWITCHES FOR 4TH PERMUTATION
NO
SEND A 'LOW' TO POINT X AND READ POINT Y
IS Y LOW?
NO
YES
DISPLAY 'ECB/PNP'


READ LOGIC AT POINT Y
IS Y LOW?
YES
SEND A 'LOW' TO POINT X AND READ POINT Y
NO
IS Y LOW?
NO
DISPLAY 'CBE/NPN'
YES
SEND A 'LOW' TO POINT X AND READ POINT Y
IS Y LOW?
NO
SEND THE CODES TO CLOSE THE MATRIX SWITCHES FOR 5TH PERMUTATION
YES
DISPLAY 'EBC/PNP'


SEND A 'HIGH' TO POINT X
READ LOGIC AT POINT Y
IS Y LOW?
YES
SEND A 'LOW' TO POINT X AND READ POINT Y
NO
SEND A 'LOW' TO POINT X AND READ POINT Y
IS Y LOW?
NO
DISPLAY 'BEC/NPN'
YES
IS Y LOW?
NO
SEND THE CODES TO CLOSE MATRIX SWITCHES FOR THE 6TH PERMUT
YES
DISPLAY 'BCE/PNP'


READ
LOGIC AT
POINT Y
IS Y
LOW?
YES
SEND A 'LOW'
TO
POINT X AND
READ POINT Y
NO
SEND A 'LOW'
TO
POINT X AND
READ POINT Y
IS Y
LOW?
NO
DISPLAY
'BCE/NPN'
YES
IS Y
LOW?
NO
DISPLAY
bAd Or Err
YES
DISPLAY
'BEC/PNP'
END

# **APPENDIX B** PROGRAM FOR THE ITA WRITTEN IN ASSEMBLY LANGUAGE.

```
org 00h
Ao equ p3.5
Bo equ p3.6
Co equ p3.7
ex equ p3.4
wy equ p3.3
test equ p1.7
setb wy
start:      call message
            jnb test, stage1
            jmp start
stage1:     call switch1
            setb Ex
            call delay
            jnb wy, clrex
            clr ex
            call delay

            jmp stage2
            call delay
            jnb wy, clrex2
            clr ex
            call delay



            call busy
            setb Ex
            call delay
            jnb wy, clrex3
            clr ex
            call delay
            jnb wy, rcebnpn
            jmp stage4
clrex3:     clr ex
            call delay
            jnb wy, stage4
recbpnp:    ljmp ecbpnp
rcebnpn:    ljmp cebnpn
clrex:      clr ex
            call delay
            jnb wy, stage2
rcebpnp:    ljmp cebpnp
recbnpn     :ljmp ecbnpn

stage2:     call switch2
            call busy
            setb Ex
            jnb wy,stage3
rcbepnp:    ljmp cbepnp
rebcnpn:    ljmp ebcnpn

clrex2:     clr ex
            call delay
            jnb wy, rebcnpn
            jmp stage3

stage4:  call switch4
         call busy
         setb Ex
         call delay
         jnb wy, clrex4
         clr ex



            call delay
            jnb wy, rcbenpn
            jmp stage5
clrex4:     clr ex
            call delay
            jnb wy,stage5
```

```
                rebcpnp:ljmp
ebcpnp
                rcbenpn:ljmp
          cbenpn

                call delay
                jnb wy, clrex5
                clr ex
                call delay
                jnb wy, rbecnpn
                jmp stage6
  clrex5:       clr ex
                call delay
                jnb wy,stage6
  rbcepnp:      ljmp bcepnp
rbecnpn:        ljmp becnpn

stage6:         call switch6
                call busy
                setb Ex
                call delay
                jnb wy, clrex6
                clr ex
                 call delay
                jmp error
  clrex6:       clr ex
                call delay
                 jnb wy,  error

 rbecpnp:       call becpnp
rbcenpn:        ljmp  bcenpn
                ret


error:          call smb
                call shift
                call capa
                call shift
                call smd
                call shift
                call delay

stage5:         call switch5
                call busy
                setb Ex
                call moveout
                call delay
                call capo
                call shift
                call smr
                call shift
                call delay
                call moveout
                call cape
                call shift
                call smr
                call shift
                call smr
                call shift
                call delay
                call moveout
                ljmp error
stage12:        ljmp stage1
message:        call capu
                call shift
                call caps
                jnb test, stage12
                call shift
                call sme
                call shift
                call delay
                jnb test, stage12
                call delay
                call moveout
                jnb test, stage12
                call delay

                call capl
                call shift
                call smt
                call shift
```

```
            call capa
            jnb test, stage12
            call shift
            call delay
             jnb test,
stage12
             call delay
             call moveout
             call delay
              jnb test,
stage12
              call smt
             jnb test,
stage12
              call shift
              call capo
               jnb test,
stage12
              call SHIFT
              call  GAP
              jnb test,
stage12
              call delay
              call delay
              jnb test,
stage12
              call moveout
               jnb test,
stage12
              call delay
               jnb test,
stage12
              call smt
              call shift
                jnb test,
stage13
              call sme
              call shift
               jnb test,
stage13
              call caps
                call shift
                call smt
               jnb test, stage13
               call shift
               call delay
               jnb test, stage13
               call moveout
               call smb
               jnb test, stage13
               call shift
               jnb test, stage13
               call smj
               call shift
               call smt
               call shift
               call delay
                jnb test, stage13
               call moveout
               call delay
                ret

stage13: ljmp stage1
ecbnpn: call cape
            call shift
            call capc
            call shift
            call smb
            call shift
            call delay
            call moveout

            call delay
            call delay
           call smn
            call shift
           call capp
           call shift
           call smn
           call shift
           call delay
           call moveout
```

```
jmp ecbnpn

ecbpnp: call cape
        call shift
        call capc
        call shift
         call smb
        call shift
        call delay
        call moveout

        call delay
        call delay
       call capp
        call shift
       call smn
       call shift
       call capp
       call shift
       call delay
       call moveout
jmp ecbpnp

ebcnpn: call cape
        call shift
        call smb
        call shift
         call capc
        call shift
         call gap
        call delay
        call moveout

        call delay
        call delay
       call smn
        call shift
       call capp
       call shift
       call smn
       call shift
        call delay
        call moveout
jmp ebcnpn


ebcpnp: call cape
        call shift
        call smb
        call shift
         call capc
        call shift
         call gap
        call delay
        call moveout

        call delay
        call delay
       call capp
        call shift
       call smn
       call shift
       call capp
       call shift
       call delay
       call moveout
jmp ebcpnp

cebnpn: call capc
        call shift
        call sme
        call shift
        call smb
        call shift
        call gap
        call delay
        call moveout
       call delay
        call delay
        call smn
        call shift
        call capp
```

```
            call shift
            call smn
            call shift

            call delay
            call moveout
          jmp cebnpn
        cebpnp: call capc
              call shift
             call sme
             call shift
              call smb
             call shift
              call gap
             call delay
             call moveout
            call capp
             call shift
            call smn
            call shift
            call capp
            call shift
            call delay
            call moveout
             jmp cebpnp
    cbenpn: call capc
            call shift
            call smb
            call shift
            call sme
            call shift
            call gap
            call delay
            call moveout
            call smn
            call shift
            call capp
            call shift
            call smn
            call shift
            call delay
                call moveout
    jmp cbenpn
          cbepnp: call capc
                call shift
                call smb
                call shift
                 call sme
                call shift
                 call gap
                call delay
                call moveout
               call capp
                call shift
               call smn
               call shift
               call capp
               call shift
               call delay
               call moveout
    jmp cbepnp
    becpnp: call smb
                call shift
                call sme
                call shift
                 call capc
                call shift
                 call gap
                call delay
                call moveout
               call capp
                call shift
               call smn
               call shift
               call capp
               call shift
               call delay
               call moveout
    jmp becpnp
    becnpn: call smb
                call shift
                call sme
```

```
            call shift
             call capc
            call shift
             call gap
            call delay
            call moveout
           call smn
            call shift
           call capp
           call shift
           call smn
           call shift
           call delay
           call moveout
jmp becnpn
bcenpn: call smb
            call shift
            call capc
            call shift
             call sme
            call shift
             call gap
            call delay
            call moveout

            call delay
            call delay
           call smn
            call shift
           call capp
           call shift
           call smn
           call shift
           call delay
           call moveout
jmp bcenpn
bcepnp: call smb
            call shift
            call capc
            call shift
             call sme
            call shift
             call gap
            call delay
            call moveout
            call delay
            call delay
           call capp
            call shift
           call smn
           call shift
           call capp
           call shift
           call delay
           call moveout
jmp bcepnp

switch1:clr Co
            clr Bo
            clr Ao
  ret
switch2:clr Co
            clr Bo
            setb Ao
  ret
switch3:clr Co
            setb Bo
            clr Ao
  ret
switch4:clr Co
            setb Bo
            setb Ao
  ret
switch5:setb Co
            clr Bo
            clr Ao
  ret
switch6: setb Co
            clr Bo
            setb Ao
  ret
```

```
shift:
        mov a,r4
        mov r3,a
        mov a,r5
       mov r4,a
      mov r5,30h
call shiftdelay
ret
moveout:    call gap
            call shift
            call shift
            call shift
            call shift
            ret

gap:mov 30h,#0ffh
        ret
capa:         mov 30h,#88h
        ret
smb:mov 30h,#83h
        ret
capc:         mov 30h,#0c6h
        ret
smd:mov 30h,#0A1h
        ret
sme:        mov 30h,#84h
        ret
cape:         mov 30h,#86h
        ret
capf:mov 30h,#8eh
        ret
smg:mov 30h,#90h
        ret
smh:mov 30h,#8bh
        ret
caph:         mov 30h,#8bh
        ret
capi:mov 30h,#0f9h
        ret
smj:  mov 30h,#61h
        ret
capl:mov 30h,#0c7h
        ret
sml:          mov 30h,#0c7h
        ret
smn:mov 30h,#0c8h
        ret
capo:         mov  30h,#0c0h
        ret
capp:         mov  30h,#8ch
        ret
smq:mov  30h,#98h
        ret
smr: mov  30h,#0ceh
        ret
caps:         mov 30h,#92h
        ret
smt: mov 30h,#87h
        ret

capt:       mov 30h,#78h
        ret
smu:mov  30h,#0c1h
        ret
capu:         mov  30h,#0c1h
        ret
capy:         mov  30h,#91h
        ret
smy:mov  30h,#91h
        ret
capz:         mov  30h,#0a4h
        ret
```

```
nine:mov  30h,#98h
       ret
eight:         mov  30h,#80h
       ret
seven:        mov  30h,#0f8h
       ret
six:  mov  30h,#82h
       ret
five: mov  30h,#92h
       ret
four: mov  30h,#99h
       ret
three:         mov  30h,#0b0h
       ret
two:  mov  30h,#0a4h
       ret
one: mov  30h, #0f9h
       ret
zero:mov  30h,#0c0h
       ret
screen:
          mov p1,r3
           call cleardgt
          setb p3.2
          call screendelay
         mov p1,r4
        call cleardgt
          setb p3.1
           call screendelay
          mov p1,r5
       call cleardgt
          setb p3.0
          call screendelay
         ret
```

```
shiftdelay:mov r0, #01h
shdelay1:    mov r1, #0fh
shdelay2:    call screen
       djnz r1, shdelay2
       djnz r0, shdelay1
ret
Delay:       mov r0, #04h
delaya:      mov r1, #0fh
delayb:      call screen
       djnz r1, delayb
       djnz r0, delaya
ret

Delay1:      mov r0, #01h
delayc:      mov r1, #0fh
delayd:      call screen
       djnz r1, delayd
       djnz r0, delayc
ret
screendelay:mov r6, #06h
sdelay1:mov r7, #0ffh
sdelay2:nop
       djnz r7, sdelay2
       djnz r6, sdelay1
ret
cleardgt:
       clr p3.1
       clr p3.2

       ret


dgt3:
    mov r3, 30h

       ret


dgt2:
  mov r4, 30h
```

```
        ret


dgt1:
  mov r5, 30h

        ret

busy:call gap
     call shift
     call gap
call shift
call gap
shift
call gap
call shift
 call smb
  call shift
  call  capu
          call shift
           call caps
           call shift
           call delay
           call smy
           call shift
            call delay
           call moveout
ret




end
```

# REFERENCES

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