

Lab 1 - Intro to Vivado

CECS 341 - Computer Architecture & Organization

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Goal/Objective:

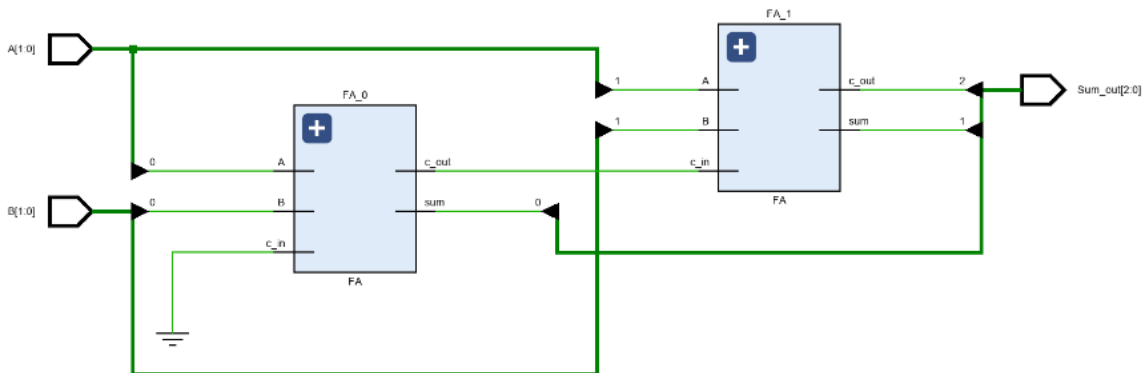
This lab aims to learn how to create Verilog modules, instantiate the top module in a test bench, and simulate it.

Technical Description/Steps:

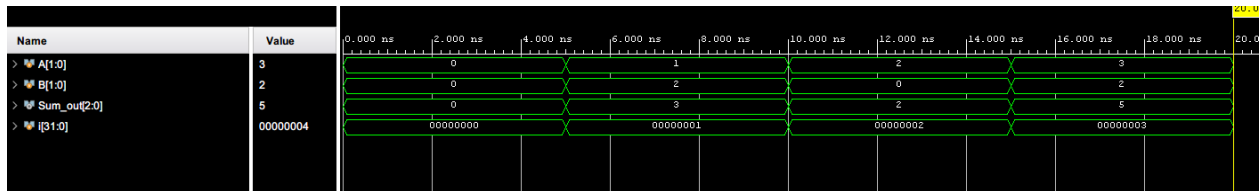
I used Xilinx Vivado software in this lab. First, I created the project named “lab_1”, and then I did two design modules which are “FA.v” and “adder_2bit.v”. The “FA.v” is a full adder module that will be used in the “adder_2bit.v” file. I defined the identifiers and created the internal wire declarations to connect the inputs, outputs, and full adder. In the end, I used the test bench provided by my lab instructor to run the simulation.

Results:

I generated a schematic based on the design source code of “adder_2bit”. The schematic visually presented the internal wiring of the inputs to the full adder and from the full adder to the output.



After that, I simulated with the test bench to show me the waveform, which shows the value change for each input and output.



Conclusion:

I learned a couple of skills in Vivado, including creating projects, creating modules, wiring variables, running simulations, and creating visual presentations of the program. I ran into some difficulties while I tried to set the test bench as the simulation source, but after couple tweaking, I was able to run the simulation and generate the waveform for this lab.