

Lab 5 - MIPS Datapath for R-type and I-Type Instructions

CECS 341 - Computer Architecture & Organization

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Goal/Objective:

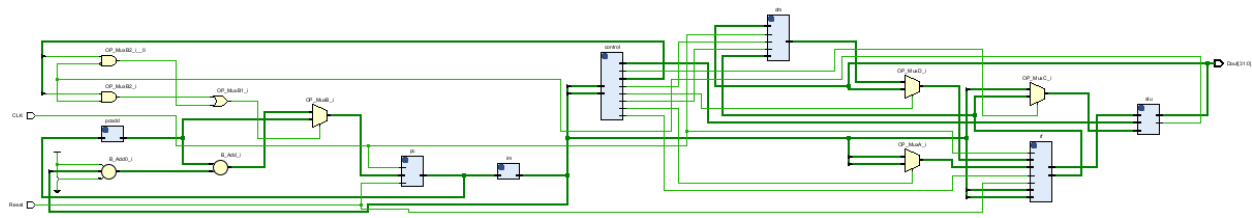
The goal of this lab is to modify the existing MIPS datapath for R-type instruction from lab 4 to support and implement I-type instructions.

Technical Description/Steps:

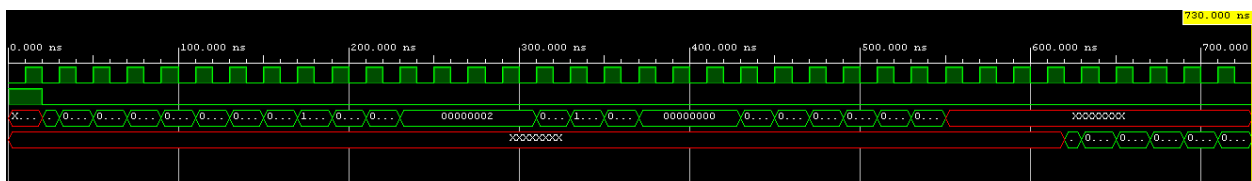
The first step of the project is to modify the control module of the MIPS datapath, we added several extra variables to determine the behavior and add a switch statement for the I-type instructions.

The second step of the project is to modify the datapath module of the MIPS datapath, we added several variables and wires in the module to connect the new variables added in the control module. We also added a few multiplexers to determine the data that we want to input to the ALU.

The third step of the project is to modify the testbench and import the new data files provided by the instructor. After that, we ran the testbench and compared it to our handwritten calculation.

Results:

The image above is the schematic of the datapath module, it shows that our modules are connected together with the new multiplexers we added. In addition, the “DataMem.v” file provided by the instructor is also connected in the schematic.



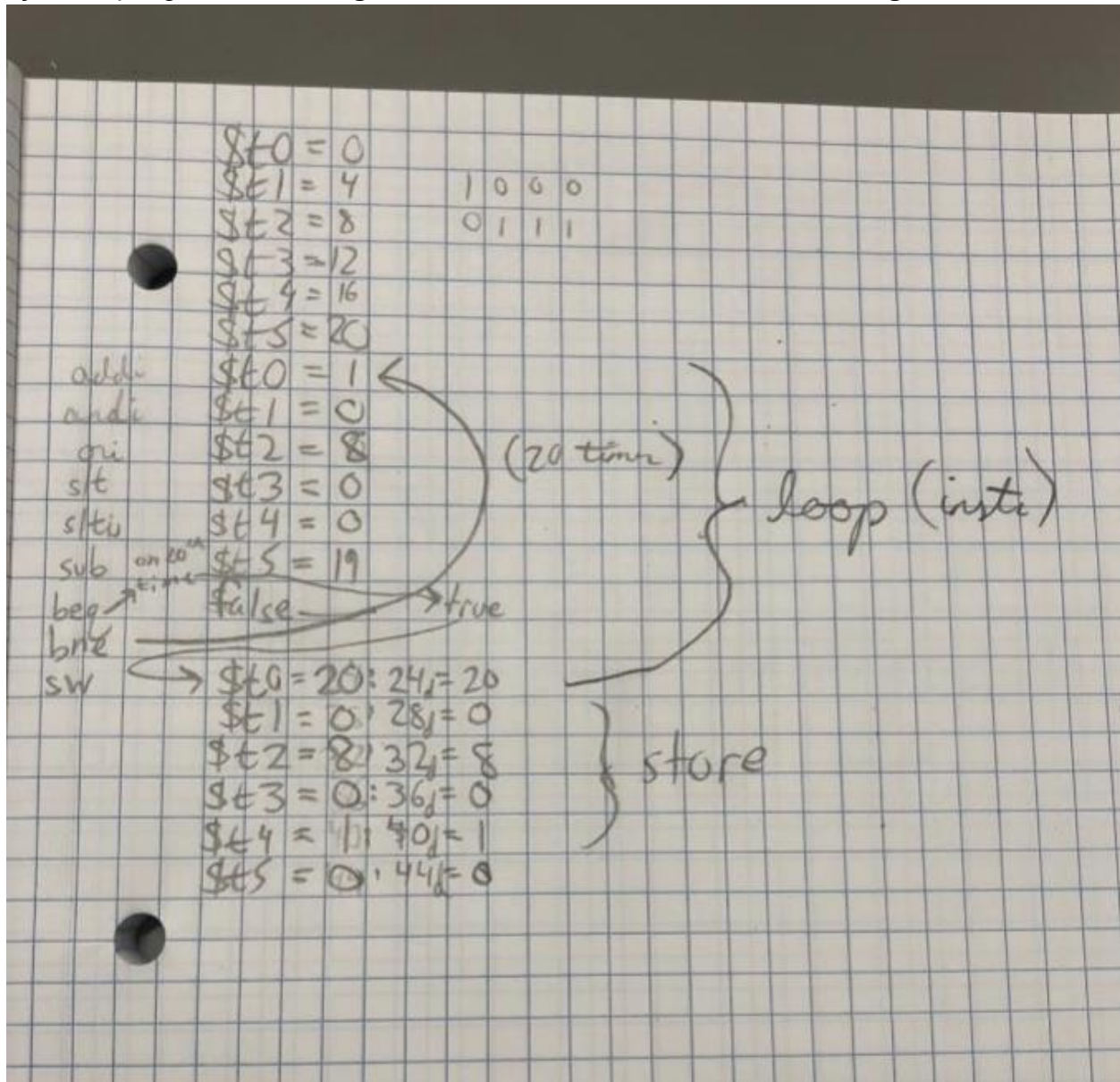
The image above is the waveform of the simulation of the MIPS datapath. The waveform shows the program began running after the reset turns to 0. After that, the program is fetched and decoded the

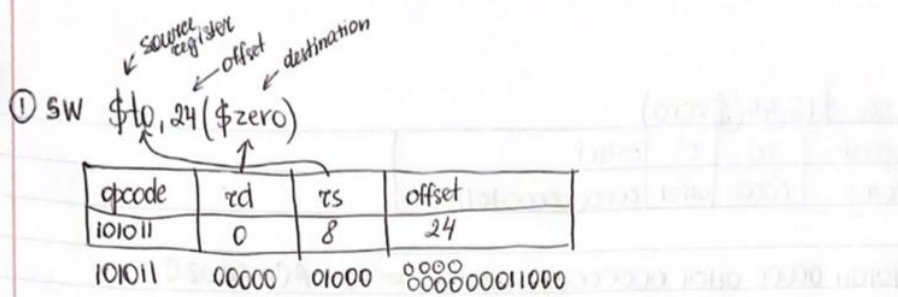
instruction from the “DataMem.dat” and the “imem - Copy.dat” files. The program fetched the data from the register files, performed calculations, then stored the results back to the register files. The output of the ALU became “XXXXXX” in the waveform because there’s no output for store word instructions.

```
# run 1000ns
t= 630.0ns dm[24] 00000002
t= 650.0ns dm[28] 00000000
t= 670.0ns dm[32] 1234567f
t= 690.0ns dm[36] 00000001
t= 710.0ns dm[40] 00000000
t= 730.0ns dm[44] 00000000
```

The image above is the console output of the program, it displays the result of the instructions that were stored in the specified registers. Our handwritten calculation matches the operation performed

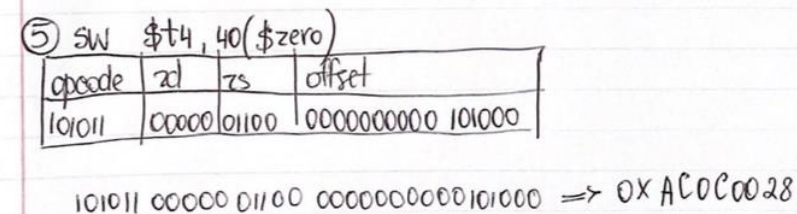
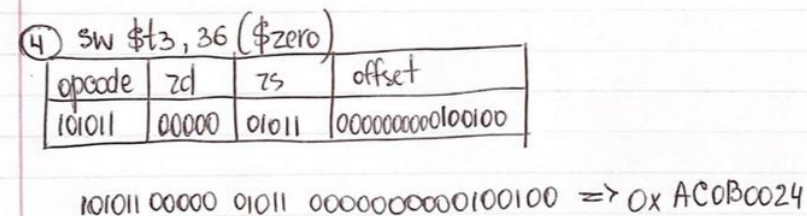
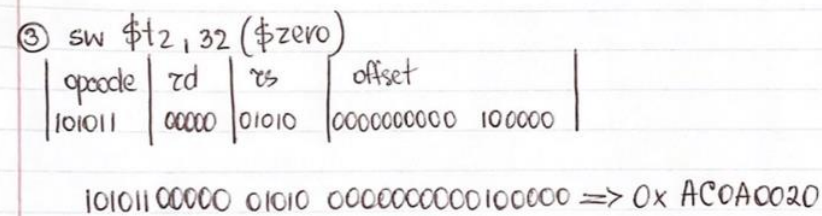
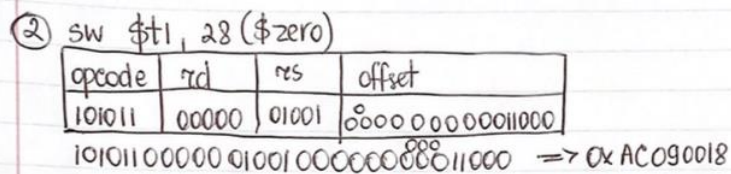
by the project, meaning that our module codes are working as intended.





101011 00000 01000 00000000011000 \Rightarrow 0x AC080018

SW \$zero \$t0 offset



10. $\text{slti } \$t3, \$t3, 9: 295B0009$

$\begin{array}{cccccccccccccccccccccccc}
0 & 0 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 \\
\text{op} & & & & & & & & & & \text{rt} & & & & & & \text{rs} & & & & & & & & & & & & & & \\
2 & & & & & & & & & & 5 & & & & & & 8 & & & & & & & & & & & & & & & & \\
\end{array}$

$rs = B_{16}, imm = 9_{16}, B < 9, \therefore rt = 00000001_{16} \text{ (true)}$

11. $\text{slti } \$t4, \$t4, 0: 2D8C0000$

$\begin{array}{cccccccccccccccccccccccc}
0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\text{op} & & & & & & & & & & \text{rt} & & & & & & \text{rs} & & & & & & & & & & & & & & \\
2 & & & & & & & & & & 8 & & & & & & C & & & & & & & & & & & & & & & & \\
\end{array}$

$rs = C_{16}, imm = 0_{16}, C \nless 0, \therefore rt = 0_{16} \text{ (false)}$

(R-type) 12. $\text{sub } \$t5, \$t5, \$t0: 01685822$

$\begin{array}{cccccccccccccccccccccccc}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 \\
\text{op} & & & & & & & & & & \text{rs} & & & & & & \text{rt} & & & & & & & & & & \text{rd} & & & & & \\
0 & & & & & & & & & & 1 & & & & & & 6 & & & & & & & & & & 5 & & & & & & \\
\end{array}$

$rs: \$t5 = 0$
 $rt: \$t0 = -8_{16} \therefore rd: \$t5 = 5_{16} = 00000005$

13. $\text{beg } \$t5, \$zero, store$

10=A
 11=B
 12=C
 13=D
 14=E
 15=F

8C080000
 1. lw \$t0, 0(\$zero): 10001100000000000100000000000000
 \$t0 = 0
 8C090004
 2. lw \$t1, 4(\$zero): 10001100000000000100000000000100
 8C0A0008
 3. lw \$t2, 8(\$zero): 10001100000000000100000000000100
 8C0B000C
 4. lw \$t3, 12(\$zero): 10001100000000000100000000000100
 8C0C0010
 5. lw \$t4, 16(\$zero): 10001100000000000100000000000100
 8C0D0014
 6. lw \$t5, 20(\$zero): 10001100000000000100000000000100
 21080001
 7. addi \$t0, \$t0, 1: 00100001000000000100000000000001
 31290000
 8. andi \$t1, \$t1, 0: 00110001000000000100000000000000
 rs: \$t1: 00000000000000000000000000000000
 imm: 0: 00000000000000000000000000000000
 rt: \$t1 = 00000000000000000000000000000000
 398A0007
 9. ori \$t2, \$t2, 7: 00110001000000000100000000000111
 rt: \$t2 = 00000000000000000000000000000111

⑥ `sw $t5, 44($zero)`

opcode	rd	rs	offset
101011	00000	01101	0000000000101100

101011 00000 01101 0000000000101100 $\Rightarrow 0xA0B002C$

Conclusion:

In this lab, we learned how to modify the project from the last lab to support I-type instructions in the datapath. We also learned how to use the syntax for multiplexers to determine the input data that we want. Over the project, we encountered two challenges that slowed our progress.

First, our console output wasn't displaying any numbers even when the waveform shows the program is running as intended. We realized that we were supposed to delay the display statement until when the store word instructions were completed. Moving the display statement under the time statement fixed the problem immediately.

Second, the result of the "slti" instructions does not match our handwritten calculation. After examining the behavior of "slti" instruction, we changed our codes in ALU and it began to output correct results.