True random number generator based on metastability in FPGA

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Introduction

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a versatile reprogrammable circuit

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reprogrammable logic

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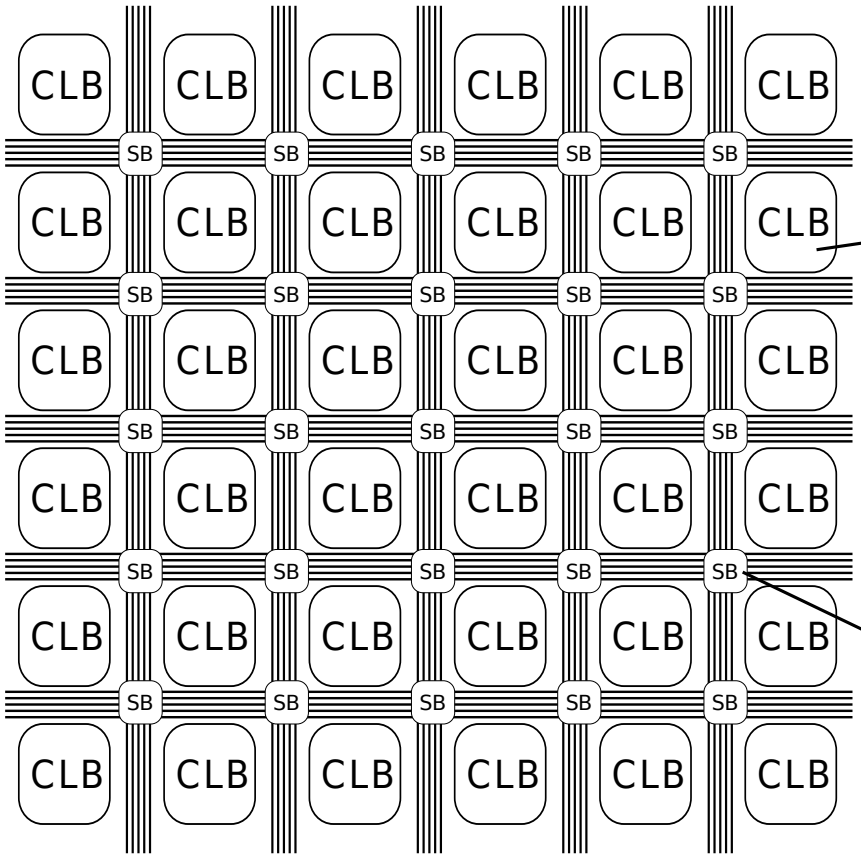
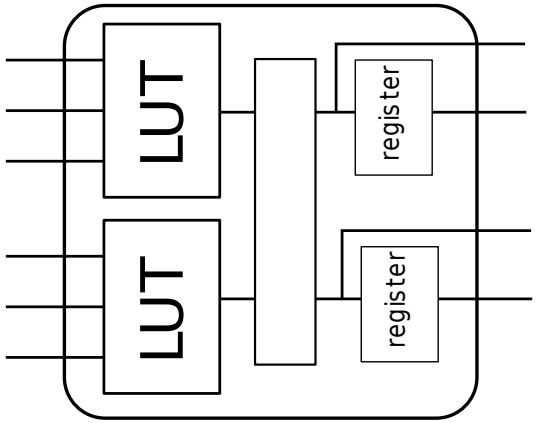
- embed is own CPU (hardcore or softcore)
- communicate at high speed typically >6Gbs (PCIe, SATA, USB 3.0, ethernet,...)

FPGA architecture

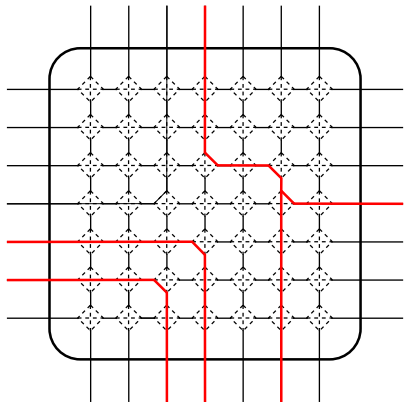
made of thousand of CLB (logic)
interconnected by SB (routing)



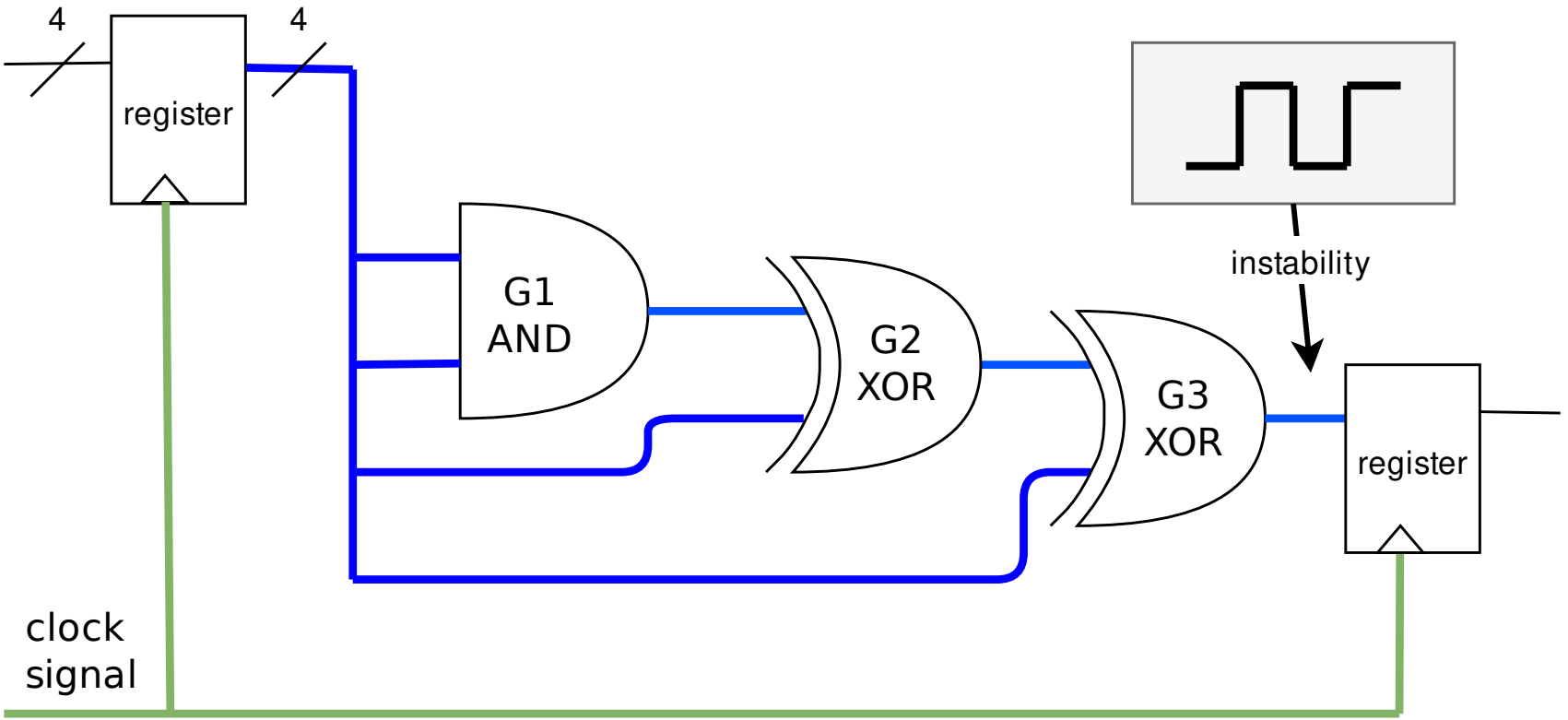
Configurable Logic Block



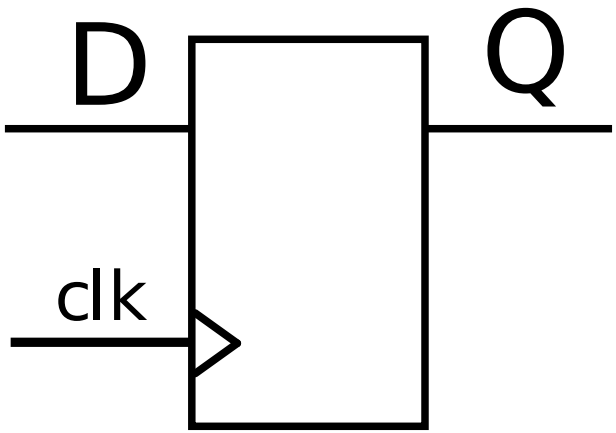
Switch Block

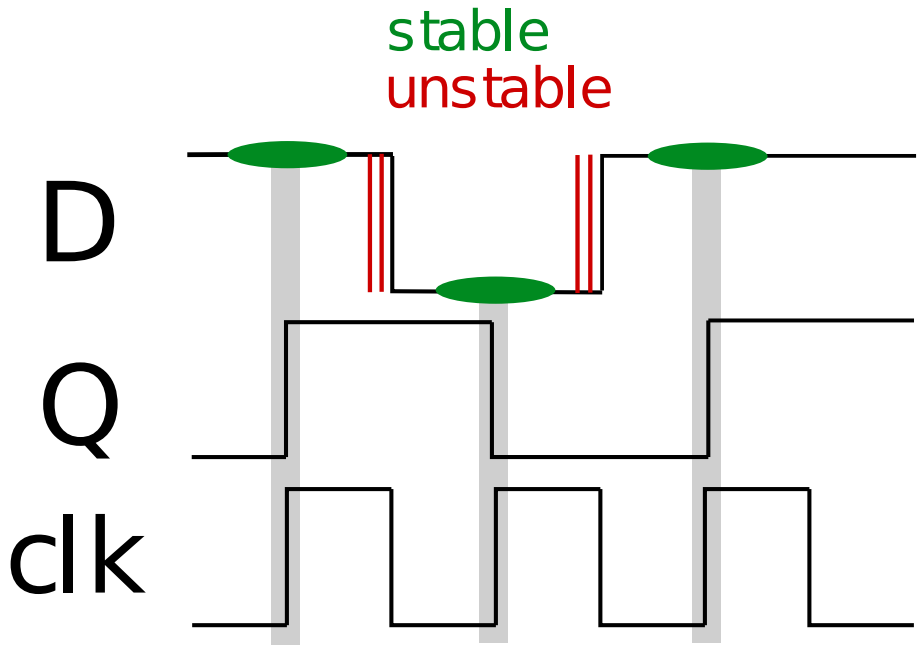


Signal propagation and instability

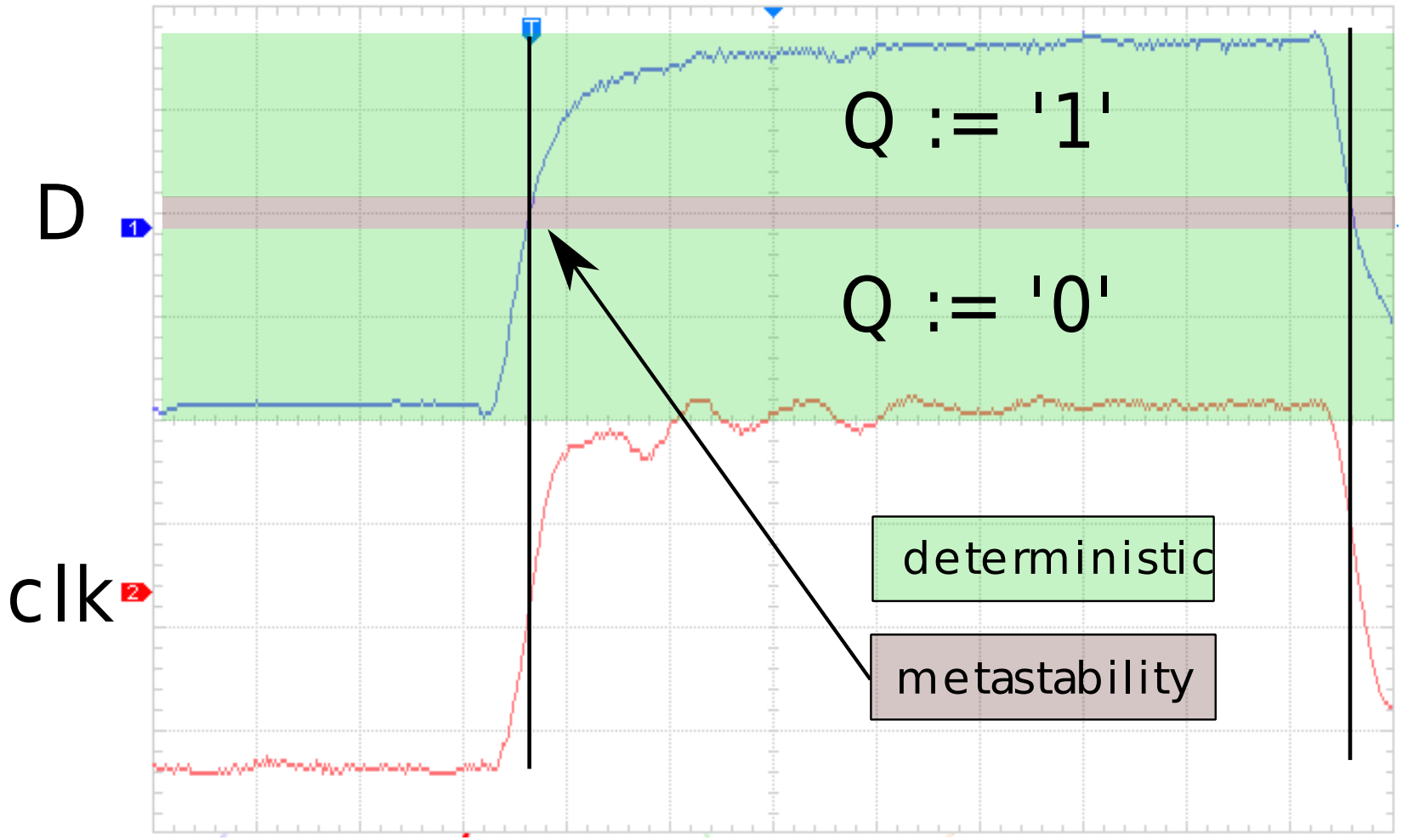


Reminder about registers





Metastability as source of randomness



NIST Statistical Test Suite for Random and Pseudorandom Number Generators

NIST test
monobits frequency test (distribution of 0s and 1s)
block frequency test (periodicity)
spectral (DFT) test

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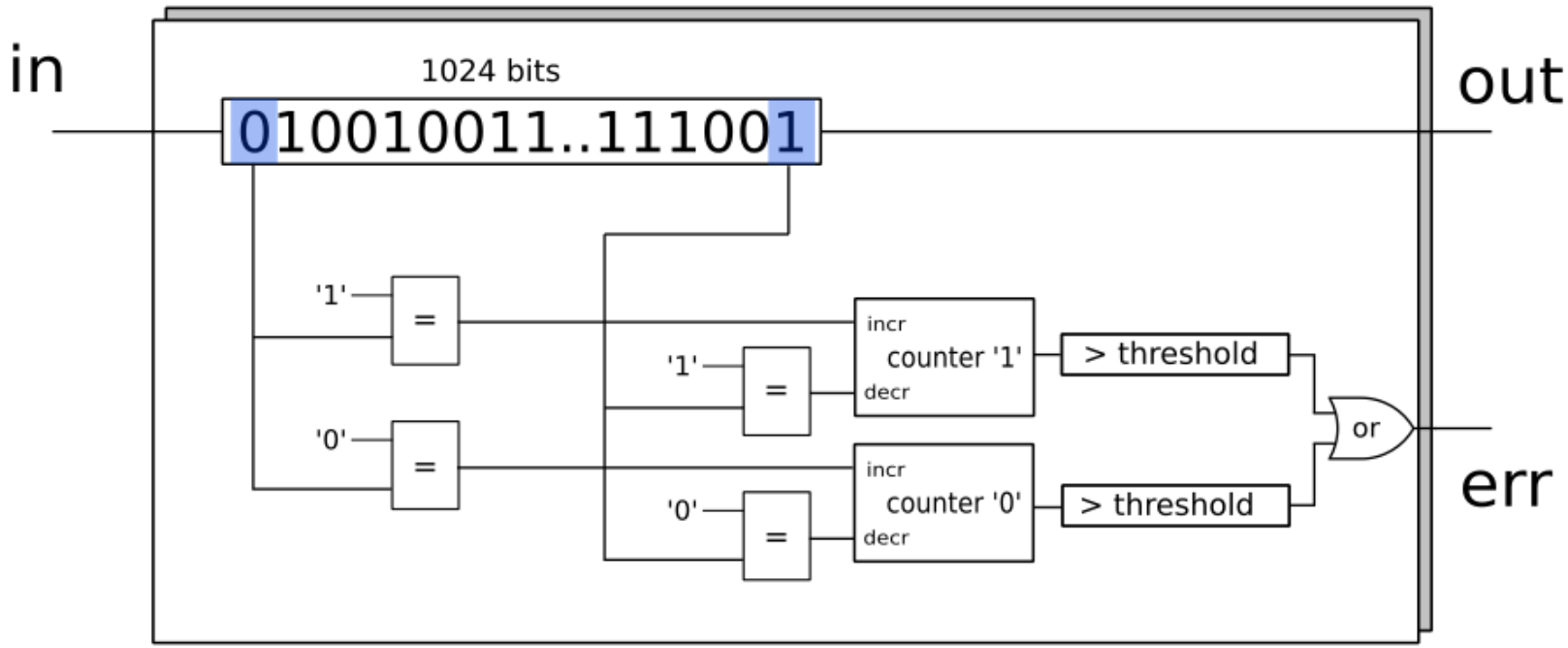
FPGA fails test so a correction is needed

Adaptive Proportion Test (Von Neumann algorithm)
Cryptographic hash function as randomness extractor (keccak)

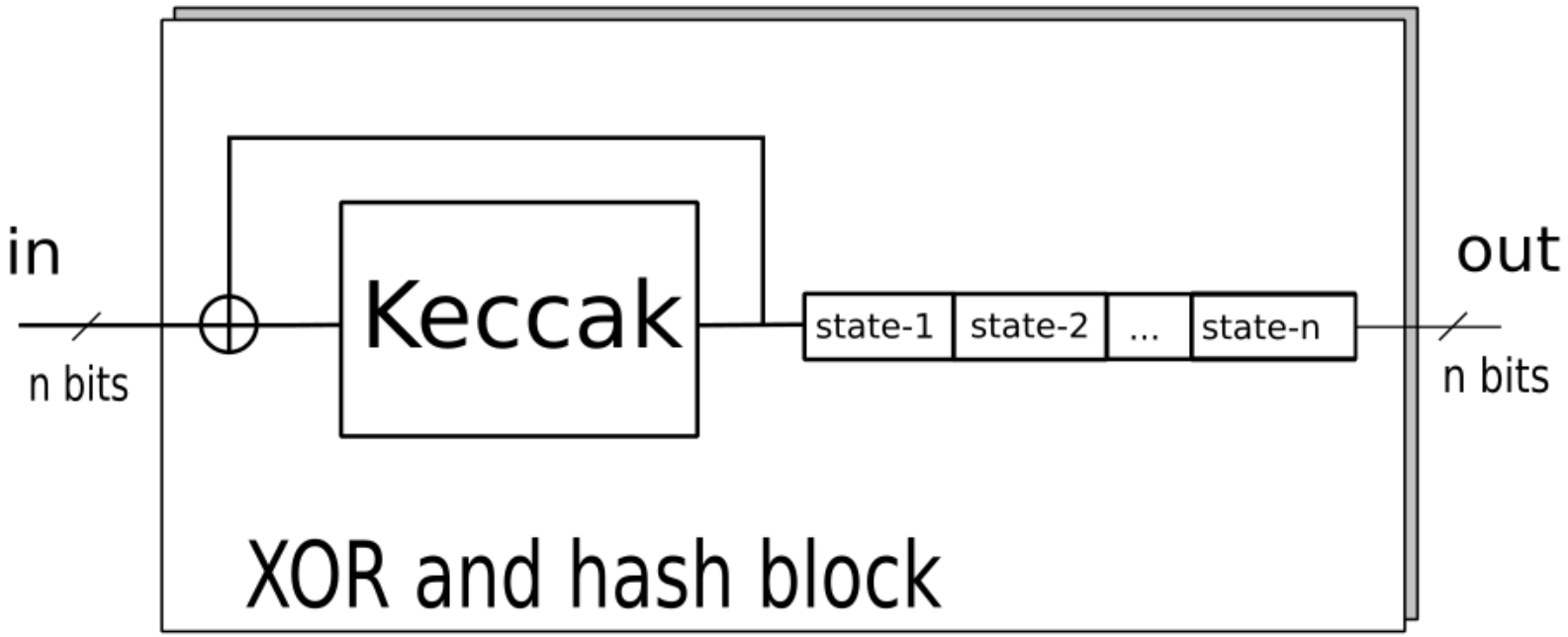
Adaptive Proportion Test

Accept output only if fairly balanced (bit level)



keccak extractor

XOR hash(state) with previous state (block level)



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- can be coupled with more complex cryptography algorithm

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Problems and security risk

- hard to implement (hardware specific)
- thermal attack
- power supply attack

Questions ?

links

- Génération de vrais nombres aléatoires en FPGA
  https://sitehepia.hesge.ch/diplome/ITI/2019/Perez-467
- FPGA pour la générationde de vrais nombres aléatoires
  https://sitehepia.hesge.ch/diplome/ITI/2017/Damien-59
- Provably Robust Sponge-Based PRNGs and KDFs
  https://dl.acm.org/citation.cfm?id=3081774
- Quantum Random Number GeneratorsMiguel
  https://arxiv.org/pdf/1604.03304.pdf
- NIST test suite (one of many)
  https://github.com/ycmjason/nist-randomness-test-suite