

Hw4-soln .pdf

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Course

ENG COMS3827

Subject

Computer Science

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Pages

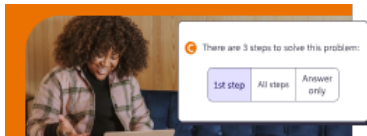
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HW #4 Solutions

CSEE W3827 - Fundamentals of Computer Systems Spring 2023

Topics: flip-flops, state design, sequential circuit design

Note that this homework has 3 HARDER problems and is 9 pages long.

Warmup Problems

1. Build

- (a) a T flip-flop out of a D flip-flop and combinational circuitry.

Answer: Let's build this circuit such that the output of the D flip-flop is the same as the output of the T flip-flop we are attempting to build. First, let's design the state table, where the rows represent the current value stored in the D flip-flop, and the columns represent the current value of the input In and the desired value of the T flip-flop.

In	$D(t)$	$D(t+1)$
0	0	0
0	1	1
1	0	1
1	1	0

Since the value fed into the D flip-flop at time t will equal its output at time $t+1$, the value fed into the D flip-flop is the right-most column of our state table. Note that the value fed into the T flip-flop, and existing states, is simply $In \oplus D(t)$.

- (b) a D flip-flop out of a T flip-flop and combinational circuitry.

Answer: Using a similar approach as above, we consider the input and current value of the T flip-flop, and determine the next value we need the T flip-flop to hold in order to match the behavior of a D flip-flop. Note $T(t+1)$ should just match the input to produce the desired output.

flop. Our state table must contain one additional column that shows the value that must be put into the T flip-flop at time t such that it goes from its value (at time t) to the value it must hold at time $t + 1$.

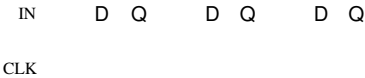
In	$T(t)$	$T(t + 1)$	T_{In}
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

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2. Build a sequential circuit that returns 1 whenever the last 3 inputs (INCLUDING the current input) have been 1. (Note: This is a different problem than the one in the previous question.)
- Answer:



3. Build a sequential circuit that returns 1 whenever the last 3 inputs (PRIOR to the current input) have been 1. (Note: This is a different problem than the one in the previous question.)
- Answer:



Harder Problems

1. A special flip-flop is formed from three latches, arranged in sequence. The first is a normal flip-flop: the leader latch's enable is attached to the clock, and the follower's enable is attached to the complement of the clock. The third latch, which follows the follower, is also attached to the complement of the clock. What is different about the outputs of this flip-flop?

Answer: A normal, 2-latch flip flop reads its input during the up-pulse (or changes its output on the down pulse (or up-edge). This one delays the output by half a cycle, so that the output changes at the same time the new input is "locked" in the third latch.

2. Design a circuit using JK flip-flops that takes in a binary stream $B_1 B_2 B_3 \dots$ and outputs the parity of the stream received thus far (i.e., $B_1 \oplus B_2 \oplus B_3 \oplus \dots \oplus B_t$), when read as an unsigned binary number is divisible by 3.

The following table depicts a sample input stream and what should be output.

t	0	1	2	3	4	5	6	7	8
In (t)	0	0	1	1	0	0	1	0	0
Val of input	0	0	4	12	12	12	76	76	76
val mod 3	0	0	1	0	0	0	1	1	1
output	1	1	0	1	1	1	0	0	0

Hint: The value of the new bit starts as equal to 1 which is 1 mod 3 then is 2 which

From the table of the new sequence we expect $x_i \bmod 3 = 1 \bmod 3$, then $x_i \bmod 3 = 2 \bmod 3$, then $x_i \bmod 3 = 0 \bmod 3$, then $x_i \bmod 3 = 1 \bmod 3$, etc.

- (a) Draw the state machine, numbering your states in an "obvious" manner. You must start in the right state at time $t = 0$.

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Answer:

This problem can actually be solved using only 3 states, but the explanation is more complex. It suffices to solve this problem using 6 states.

Each state tracks two pieces of information: the first is the current value mod 3 (we have to track this value since it determines the output). The second piece of information is the value to be added when the current input is a 1. An important observation is that adding 1 which adds 2^i to the overall value changes the value mod 3 by 1 when i is even and 2 when i is odd. Thus, we have to track whether the current timeslot is an even or odd clock cycle. Hence, a state will track the current value mod 3 (0, 1, or 2) and whether the current clock cycle is an even (0) or odd (1) clock cycle.

00-0			01-0			10-0		
			1/0			1/0		
1/1	0/1	0/1		0/0	0/0		0/0	
			1/1			1/0		
1/0	00-1			01-1			10-1	

Note in the above state machine, each state ABC is represented as 4 bits AB that represent the current value mod 3 (not including the current input) the value 2^C that the current input has mod 3. Note that in this state machine, the value that *includes the current input* equals 0 mod 3, i.e., we output 1

state where $AB = 00$.

Note also that the red arrows on the margins indicate where the transition page.

- (b) Give the algebraic formula (simplified as much as possible) for the J and K in also for the output.

Answer:

time t					t + 1	time t			t + 1	time t	
A	B	C	In	Out	A	J _A	K _A	B	J _B	K _B	
0	0	0	0	1	0	0	X	0	0	X	
0	0	0	1	0	0	0	X	1	1	X	
0	0	1	0	1	0	0	X	0	0	X	
0	0	1	1	0	1	1	X	0	0	X	
0	1	0	0	0	0	0	X	1	X	0	
0	1	0	1	0	1	1	X	0	X	1	
0	1	1	0	0	0	0	X	1	X	0	
0	1	1	1	1	0	0	X	0	X	1	
1	0	0	0	0	1	X	0	0	0	X	
1	0	0	1	1	0	X	1	0	0	X	
1	0	1	0	0	1	X	0	0	0	X	
1	0	1	1	0	0	X	1	1	1	X	
1	1	0	0	X	X	X	X	X	X	X	
1	1	0	1	X	X	X	X	X	X	X	
1	1	1	0	X	X	X	X	X	X	X	
1	1	1	1	X	X	X	X	X	X	X	

Answer continued on next page.

Answer: Continued from previous page

C In					C In				
AB	00	01	11	10	AB	00	01	11	10
00	0	0	1	0	00	X	X	X	X
01	0	1	0	0	01	X	X	X	X
11	X	X	X	X	11	X	X	X	X
10	X	X	X	X	10	0	1	1	1

$J_A = B\bar{C}In + \bar{B}CIn$					$K_A = In$				
C In					C In				
AB	00	01	11	10	AB	00	01	11	
00	0	1	0	0	00	X	X	X	
01	X	X	X	X	01	0	1	1	
11	X	X	X	X	11	X	X	X	
10	0	0	1	0	10	X	X	X	

$$J_B = \bar{A}\bar{C}In + ACIn \quad K_B = In$$

Obviously: $J_C = K_C = 1$.

C In				
AB	00	01	11	10
00	1	0	0	1
01	0	0	1	0
11	X	X	X	X
10	0	1	0	0

$$Out = A\bar{C}In + BCIn + \bar{A}\bar{B}In$$

3. Consider a sequential circuit that reads in an input $X(t)$ during clock cycle t . The sequence 011. Design the sequential circuit (i.e., give simplified algebraic expressions for each of the following versions:

(a) If the second 1 arrives during clock cycle t , then the circuit should output a

(d) if the second 1 arrives during clock cycle 1, then the circuit should output a 1, otherwise outputs a 0.

Answer:

To design this state machine, there needs to be a state that indicates that a 0 has been received, then a state that indicates that thusfar 01 has been received. When a 1 is received, the machine can output 1. Last, there must also be a state that indicates the sequence has not yet been initiated (i.e., a 1 has been received without a 0 preceding it or without a 01 immediately preceding it). Since 3 states are needed to be described by (at minimum) a 2-bit sequence, $A(t)B(t)$. At the not-yet-initiated state, 01 to the received-0 state, and 10 to the received-0 state

1/0	0/0	1/0
00	01	10
{}	{0}	{01}
	0/0	
	1/1	

A(t)	B(t)	In(t)	Out(t)	A(t+1)	B(t+1)
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	0	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	X	X	X
1	1	1	X	X	X

A	B	In	Out	
	00	01	11	10
0	0	0	0	0
1	0	1	X	X

$$\text{Out}(t) = A(t)\text{In}(t)$$

A	B	In	Out	
	00	01	11	10
0	0	0	1	0
1	0	0	X	X

$$A(t+1) = B(t)\text{In}(t)$$

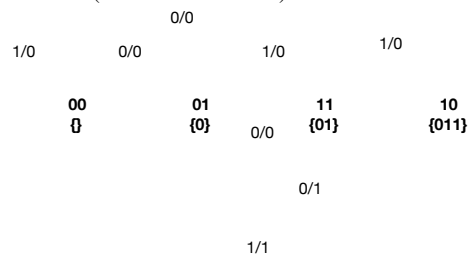
A	B	In	Out	
	00	01	11	10
0	1	0	0	1
1	1	0	X	X

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$$B(t+1) = \text{In}(t)$$

- (b) If the second 1 arrives during clock cycle t , then the circuit should output a 1 and otherwise outputs a 0.

Answer: Here, we need 4 states. One that represents the sequence not yet received (we will use state 00). Another for the 0 having been received (we will use state 01) and another for 011 received (we will use state 11) and another for 0111 received (we will use state 10).



A(t)	B(t)	In(t)	Out(t)	A(t + 1)	B(t + 1)
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	0	1	0

	B	In			
A	00	01	11	10	
0	0	0	0	0	0
1	1	1	0	0	0

$$\text{Out}(t) = A(t)B(t)$$

	B	In			
A	00	01	11	10	
0	0	0	0	1	0
1	0	0	1	0	0

$$A(t + 1) = B(t)In(t)$$

	B	In			
A	00	01	11	10	
0	0	1	0	1	1
1	1	1	0	0	1

$$B(t + 1) = I(t) + A(t)B(t)$$

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(c) Suppose the sequence is 111 instead of 011. If at time t , the current and two then a 1 should be output during clock cycle t , and otherwise a 0 should be consecutive outputs of 1 are possible.

Answer:

		0/0			
			1/0		
start	0	0/0	1 ₁	1/0	1 ₂
			0/0		
				0/0	

In	A	B	A'=D _A	B'=D _B	Out
0	0	0	0	0	0
1	0	0	0	1	0
0	0	1	0	0	0
1	0	1	1	0	0
0	1	0	0	0	0
1	1	0	1	1	1
0	1	1	0	0	0
1	1	1	1	1	1

B In					B In					B In				
A	00	01	11	10	A	00	01	11	10	A	00	01	11	10
0	0	0	0	1	0	0	0	1	0	0	0	0	1	0
1	0	1	1	0	1	0	1	1	0	1	0	1	1	0

$$D_A = AIn + BIn \qquad D_B = AIn + \bar{B}In$$

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Lec-34-worksheet solution



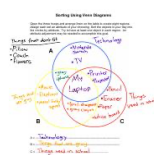
Lab9p2'



Hw7pracSP22



FAQ speed camera 2019



Sorting



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LAB4



Assign unixxxx



Revised Sln



Assignment1-hji61final



Homework 1

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