Hw4-soln .pdf

HW #4 Solutions

CSEE W3827 - Fundamentals of Computer Systems Spring 2023

Topics: flip-flops, state design, sequential circuit design

Note that this homework has 3 HARDER problems and is 9 pages long.

Warmup Problems

1. Build

   (a) a T flip-flop out of a D flip-flop and combinational circuitry.

   Answer: Let's build this circuit such that the output of the D flip-flop is t
   flip-flop we are attempting to build. First, let's design the state table, wh
   the T flip-flop, the current value stored in the D flip-flop, and the desire
   the T flip-flop).

In	$D(t)$	$D(t+1)$
0	0	0
0	1	1
1	0	1
1	1	0

   Since the value fed into the D flip-flop at time t will equal its output at ti
   to the D flip-flop is the right-most column of our state table. Note thi
   and existing states, is simply $In \oplus D(t)$.

   (b) a D flip-flop out of a T flip-flop and combinational circuitry.

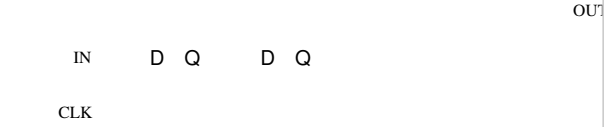
   Answer: Using a similar approach as above, we consider the input and c
   flip-flop, and determine the next value we need the T flip-flop to hold in
   behavior of a D flip-flop. Note $T(t+1)$ should just match the input to prope

flop. Our state table must contain one additional column that shows the va
into the T flip-flop at time t such that it goes from its value (at time t) to the
to hold at time $t + 1$.

In	$T(t)$	$T(t+1)$	T_{In}
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

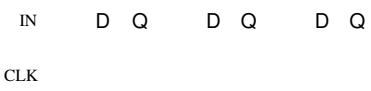
2. Build a sequential circuit that returns 1 whenever the last 3 inputs (INCLUDING the
cal.

Answer:



3. Build a sequential circuit that returns 1 whenever the last 3 inputs (PRIOR to the cu

Answer:



Harder Problems

1. A special flip-flop is formed from three latches, arranged in sequence. The first
   normal flip-flop: the leader latch's enable is attached to the clock, and the followe
   complement of the clock. The third latch, which follows the follower, is also att
   different about the outputs of this flip-flop?

   Answer: A normal, 2-latch flip flop reads its input during the up-pulse (or c
   changes its output on the down pulse (or up-edge). This one delays the
   half cycle, so that the output changes at the same time the new input is "locked" i
   latch.

2. Design a circuit using JK flip-flops that takes in a binary stream $B = B_1 B_2 B_3 \cdots$ and
   stream received thusfar (i.e., $B = B_1 \cdots B_{t-1} B_t$), when read as an unsigned binary nu
   is divisible by 3.

   The following table depicts a sample input stream and what should be output.

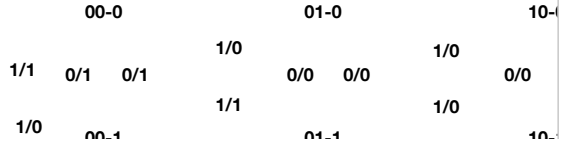
t	0	1	2	3	4	5	6	7	8
In (t)	0	0	1	1	0	0	1	0	0
Val of input	0	0	4	12	12	12	76	76	76
val mod 3	0	0	1	0	0	0	1	1	1
output	1	1	0	1	1	1	0	0	0

   Hint: The value of the new bit starts as equal to 1 which is 1 mod 3, then is 2 which

is back to 1 mod 3, etc.

(a) Draw the state machine, numbering your states in an "obvious" manner. You m
starts in the right state at time $t = 0$.

Answer:
This problem can actually be solved using only 3 states, but the explanation i
suffice it to solve this problem using 6 states.
Each state tracks two pieces of information: the first is the current value mod
have to track this value since it determines the output). The second piece o
value to be added when the current input is a 1. An important observation is
being 1 which adds 2^i to the overall value changes the value mod 3 by 1 w
2 when i is odd. Thus, we have to track whether the current timeslot is an
odd timeslot. Hence, a state will track the current value mod 2 (0,1, or 2) and
clock cycle is an even (0) or odd (1) clock cycle.



Note in the above state machine, each state ABC is represented as A
bits AB that represent the current value mod 3 (not including the current inpu
the value 2^C that the current input has mod 3. Note that in this state machine,
the value that *includes the current input* equals 0 mod 3, i.e., we output 1

state where AB = 00.
Note also that the red arrows on the margins indicate where the transitior
page.

(b) Give the algebraic formula (simplified as much as possible) for the J and K in
also for the output.

Answer:

time t					t + 1	time t		t + 1		time t
A	B	C	In	Out	A	J_A	K_A	B	J_B	K_B
0	0	0	0	1	0	0	X	0	0	X
0	0	0	1	0	0	0	X	1	1	X
0	0	1	0	1	0	0	X	0	0	X
0	0	1	1	0	1	1	X	0	0	X
0	1	0	0	0	0	0	X	1	X	0
0	1	0	1	0	1	1	X	0	X	1
0	1	1	0	0	0	0	X	1	X	0
0	1	1	1	1	0	0	X	0	X	1
1	0	0	0	0	1	X	0	0	0	X
1	0	0	1	1	0	X	1	0	0	X
1	0	1	0	0	1	X	0	0	0	X
1	0	1	1	0	0	X	1	1	1	X
1	1	0	0	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X

Answer continued on next page.

Answer: Continued from previous page

AB \ C In	00	01	11	10
00	0	0	1	0
01	0	1	0	0
11	X	X	X	X
10	X	X	X	X

AB \ C In	00	01	11
00	X	X	X
01	X	X	X
11	X	X	X
10	0	1	1

$$J_A = B\bar{C}In + \bar{B}CIn \qquad K_A = In$$

AB \ C In	00	01	11	10
00	0	1	0	0
01	X	X	X	X
11	X	X	X	X
10	0	0	1	0

AB \ C In	00	01	11
00	X	X	X
01	0	1	1
11	X	X	X
10	X	X	X

$$J_B = \bar{A}\bar{C}In + ACIn \qquad K_B = In$$

Obviously: $J_C = K_C = 1$.

AB \ C In	00	01	11	10
00	1	0	0	1
01	0	0	1	0
11	X	X	X	X
10	0	1	0	0

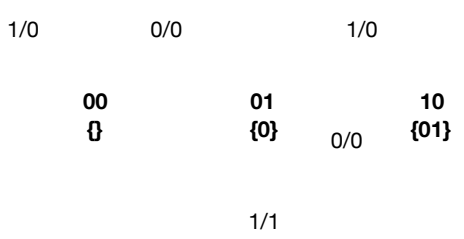
$$Out = A\bar{C}In + BCIn + \bar{A}\bar{B}In$$

3. Consider a sequential circuit that reads in an input X (t) during clock cycle t. The sequence 011. Design the sequential circuit (i.e., give simplified algebraic express each of the following versions:

(a) If the second 1 arrives during clock cycle t, then the circuit should output a

(a) If the second 1 arrives during clock cycle t, then the circuit should output a otherwise outputs a 0.

Answer:
To design this state machine, there needs to be a state that indicates that a
received, then a state that indicates that thusfar 01 has been received. Whe
if a 1 is received, the machine can output 1. Last, there must also be state
the sequence has not yet been initiated (i.e., a 1 has been received withou
preceding it or without a 01 immediately preceding it. Since 3 states
needs to be described by (at minimum) a 2-bit sequence, $A(t)B(t)$. Ar
to the not-yet-initiated state, 01 to the received-0 state, and 10 to the received



$A(t)$	$B(t)$	$In(t)$	$Out(t)$	$A(t+1)$	$B(t+1)$
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	0	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	X	X	X
1	1	1	X	X	X

A \ B In	00	01	11	10
0	0	0	0	0
1	0	1	X	X

$$Out(t) = A(t)In(t)$$

A \ B In	00	01	11	10
0	0	0	1	0
1	0	0	X	X

$$A(t+1) = B(t)In(t)$$

A \ B In	00	01	11	10
0	1	0	0	1
1	1	0	X	X

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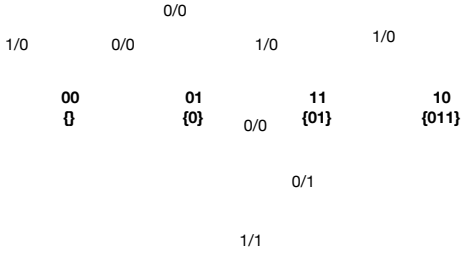
$$B(t+1) = In(t)$$

(b) If the second 1 arrives during clock cycle t , then the circuit should output a 1 d
and otherwise outputs a 0.

Answer: Here, we need 4 states. One that represents the sequence not yet r
will use state 00). Another for the 0 having been received (we will use state
received (we will use state 11) and another for 011 received (we will use state



A(t)	B(t)	In(t)	Out(t)	A(t+1)	B(t+1)
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	0	1	0

A \ B In	00	01	11	10
0	0	0	0	0
1	1	1	0	0

$$\text{Out}(t) = A(t)B(t)$$

A \ B In	00	01	11	10
0	0	0	1	0
1	0	0	1	0

$$A(t+1) = B(t)\text{In}(t)$$

A \ B In	00	01	11	10
0	1	0	1	1
1	1	0	0	1

$$B(t+1) = I(t) + A(t)B(t)$$

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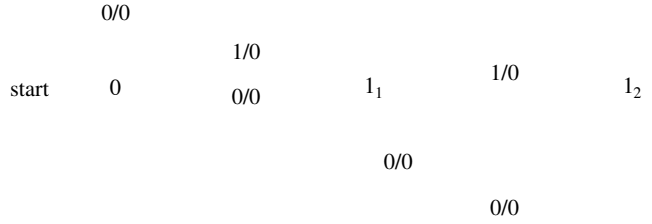
(c) Suppose the sequence is 111 instead of 011. If at time t, the current and two then a 1 should be output during clock cycle t, and otherwise a 0 should be consecutive outputs of 1 are possible.

Answer:



In	A	B	A'= D_A	B'= D_B	Out
0	0	0	0	0	0
1	0	0	0	1	0
0	0	1	0	0	0
1	0	1	1	0	0
0	1	0	0	0	0
1	1	0	1	1	1
0	1	1	0	0	0
1	1	1	1	1	1

A \ B In	00	01	11	10
0	0	0	1	0
1	0	1	1	0

$$D_A = AIn + BIn$$

A \ B In	00	01	11	10
0	0	1	0	0
1	0	1	1	0

$$D_B = AIn + \bar{B}In$$

A \ B In	
0	0
1	1

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