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Time-Based Current Source: A Highly Digital Robust Current Generator for Switched Capacitor Circuits

Kentaro YOSHIOKA†, *Nonmember*

SUMMARY The resistor variation can severely affect current reference sources, which may vary up to ±40% in scaled CMOS processes. In addition, such variations make the opamp design challenging and increase the design margin, impacting power consumption. This paper proposes a Time-Based Current Source (TBCS): a robust and process-scalable reference current source suitable for switched-capacitor (SC) circuits. We construct a delay-locked-loop (DLL) to lock the current-starved inverter with the reference clock, enabling the use of the settled current directly as a reference current. Since the load capacitors determine the delay, the generated current is decoupled from resistor values and enables a robust reference current source.

The prototype TBCS fabricated in 28nm CMOS achieved a minimal area of $1200um^2$. The current variation is suppressed to half compared to BGR based current sources, confirmed in extensive PVT variation simulations. Moreover, when used as the opamp's bias, TBCS achieves comparable opamp GBW to an ideal current source.

key words: *Current reference, Process scalable, DLL, Switched capacitor circuits.*

1. Introduction

Switched-capacitor (SC) circuits are fundamental building blocks of high-precision, high-speed ADCs (e.g. pipelined ADCs and pipeline-SAR ADCs), which are critical circuit components upon realizing 5G and beyond 5G wireless-communication circuits [1–6]. Especially for high-speed SC circuits, the opamp speed is one of the critical design parameters and is severely affected by the reference current source PVT variation effects.

There are mainly two design approaches for reference current sources: beta-multiplier and voltage-current conversion. Beta-multiplier, which generates a current in a self-bias fashion, exploits the complementary temperature characteristics of resistors and transistors to cancel the temperature dependence [7–12]. In the voltage-current conversion approach, a resistor performs voltage-current conversion utilizing a reference voltage generated by a robust bandgap reference (BGR) voltage source, which is highly robust to PVT variations [13–17]. However, for both methods, the generated currents are directly affected by the absolute resistance value. Since resistors available in scaled digital CMOS technology may vary ±40% due to manufacturing variations, the generated current can vary ±40% as well.

A common practice is to calibrate the resistance at shipping or allow the variations as a design margin. However, the former increases analog test costs, while the latter worsens the system power consumption, area, and yield due to the opamp overdesign. Prior researches focused on replacing the resistors by utilizing transistor leakage and achieved robust reference generation [18–21]. However, its current range is in the nA, pA order and insufficient for high-speed circuits, and its operation relies on analog elements with poor CMOS scaling characteristics.

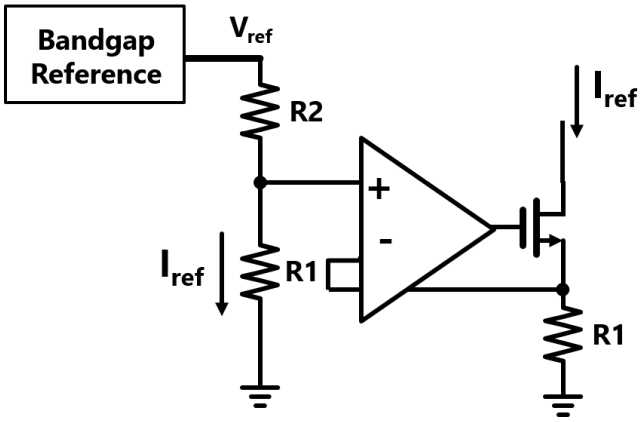

Fig. 1 Bandgap reference current source utilizing voltage-current conversion.

In this paper, we propose a time-based current source (TBCS) to realize a highly digital and low-cost current source for switched-capacitor circuits [22]. Unlike the conventional current sources, TBCS exploits the SC circuit's clock as a reference and utilizes a delay-locked-loop (DLL) to lock the current-starved delay-line (CSD) to the reference clock. Thus, we directly exploit the locked current value as the reference current. A robust current source can be constructed since the CSD delay is mainly determined by the current and load capacitance, which decouples the current from the transistor and resistor process variations. In addition, while the TBCS is sensitive to capacitor variations, TBCS automatically compensates for the opamp speed to cope with the capacitor variations. When load capacitance increases, TBCS increases the current to keep the delay constant, which helps the opamp to drive the increased load to maintain the speed. When the TBCS is used as the opamp's bias, TBCS achieves competitive opamp gain-bandwidth (GBW) to an ideal current source through exhaustive PVT variations. Lastly, the TBCS can be composed almost entirely of inverter cells and digital circuits and is highly process-scalable. The prototype circuit was fabricated with 28nm CMOS and occupied an area of only $1200um^2$.

In extension to ref. [22, 23], this paper adds extensive analysis of TBCS. Specifically, we make the following con-

†The author is with Keio University
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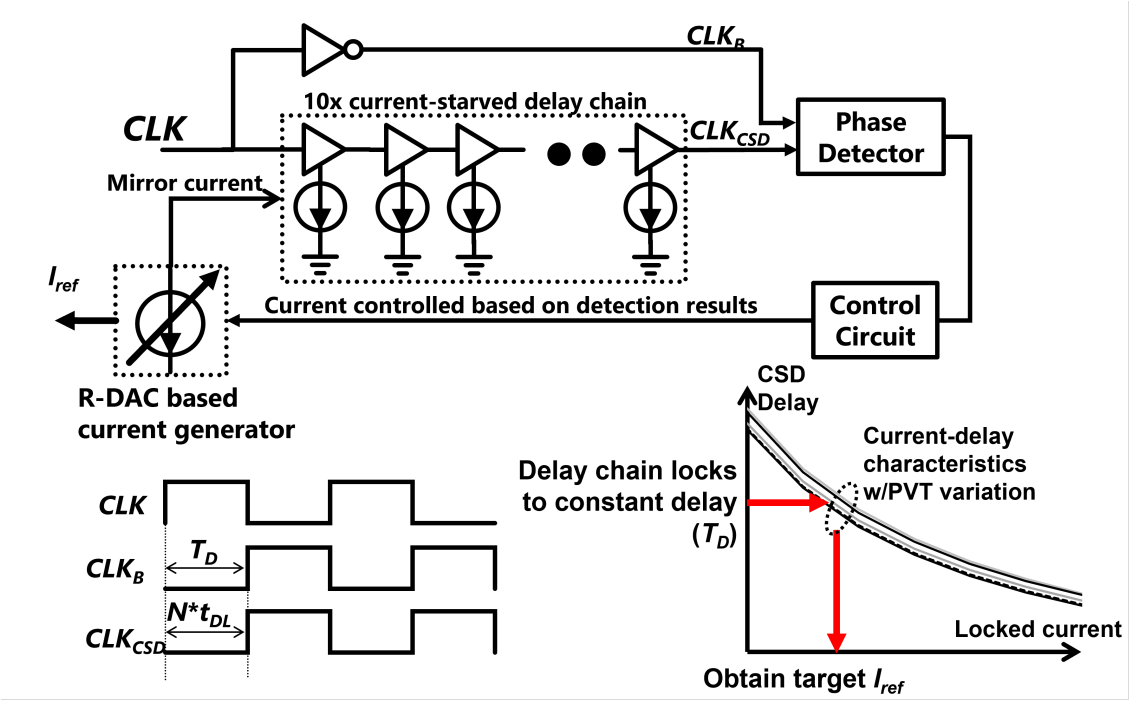


Fig. 2 Block diagram of the TBCS. The current is controlled so that the CSD delay will lock to a half cycle of the CLK. When the delay is locked, the current value will depend on the capacitive load and be decoupled from resistor values, thus realizing a PVT robust current source.

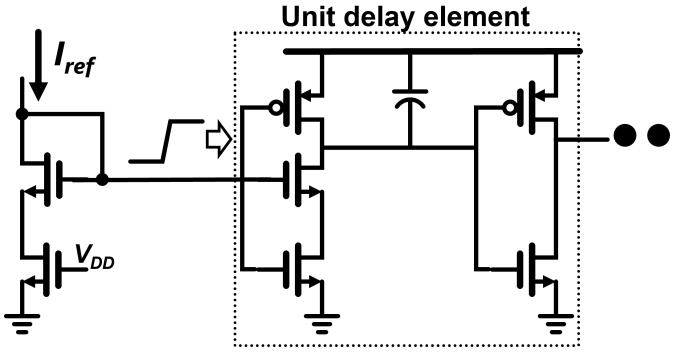


Fig. 3 Circuit diagram of the current-starved delayline (CSD).

tributions. 1) In-depth discussion of TBCS principles and circuit implications, 2) Analysis on the opamp characteristics biased with TBCS are added. This paper is organized as follows: Section 2 describes the previous studies and their challenges. Section 3 explains the principle of TBCS and Section 4 discusses the circuit implementation of TBCS. Finally, Section 5 reports the simulation results and analysis.

2. Related researches

Bandgap reference: The BGR is widely used as a current source, as shown in Fig.1. The BGR generates a robust reference voltage V_{ref} and the reference current I_{ref} is generated by voltage-current conversion as:

$$I_{ref} = \frac{V_{ref}}{R_1 + R_2} \tag{1}$$

The BGR can generate a constant voltage without environmental variations (temperature, transistor threshold, supply voltage). On the other hand, the resistance R1 and R2 suffer greatly from process variations, where the resistance values can vary by up to ±40% in the case of poly-resistors. For example, when I_{ref}=20uA is targeted, we must expect the max-min current values to be 32uA and 12uA, respectively. Such variations increase the opamp design margin and impacts system power consumption.

Switched-capacitor (SC) resistor current source: Current sources capable of resistance variations are important for analog products and much research has been undergone. Ref. [24, 25] utilizes an SC resistor, which is a pseudo-resistor realized by switching a capacitor at a constant frequency to achieve a current source that relies only on capacitance and frequencies. Although the idea and the goal of SC resistor current sources are similar to TBCS, SC resistors must repeatedly switch at high speeds, resulting in large spurious at the output current. Thus, to remove such unwanted components, a large area-consuming low-pass filter is required. On the other hand, TBCS minimizes switching noise via hysteresis-based control and realizes a PVT-robust current source using mostly-digital circuits without analog components; the overhead is much smaller.

Analog circuit calibration techniques using time information: Ref. [26] uses the time information of the ref-

erence clock to calibrate analog circuit characteristics. Precisely, the supply voltage is controlled with a DLL, and the basic idea is similar to TBCS. Additionally, ref. [27,28] uses a DLL to control the delay of an asynchronous SAR clock to optimize the DAC settling timing. However, these researches aim to calibrate the delay characteristics of the analog circuits. To the best of the author's knowledge, the proposed TBCS is the first approach to suppress the reference current source variation using delay-locking.

3. Time based current source (TBCS)

3.1 TBCS fundamentals

A simplified circuit block diagram of the TBCS is shown in Fig.2. The TBCS requires only a predetermined frequency clock (CLK), such as the sample clock of an ADC, and its components, and the operation is similar to a Delay-Locked-Loop circuit (DLL) [29–31]. The generated reference current (I_{ref}) is fed to the core circuitry (e.g. opamp) and the current-starved-delay-line (CSD). The CSD outputs CLK_{CSD}, which appends delay $N \times t_{DL}$ to CLK, where the number of stages in the CSD is N and the CSD stage delay is t_{DL}. Note that the larger I_{ref} is, the smaller t_{DL} becomes and vice versa. Then, phase comparison is performed between CLK_{CSD} and CLK_B (the inverted output of CLK). Given the comparison results, the I_{ref} is controlled so that the delay will converge to the half-cycle time of CLK (T_D). Note that frequency references can be finely generated from crystal oscillators, providing a precise reference independent of PVT variations. While loop filters [29] and digital filters [32] are utilized in DLLs to generate fine delay, TBCS does not require such filters because its primary purpose is to realize a robust current source and not provide precise delays.

By further studying the delay characteristics of the CSD, we show that the TBCS is capable of the robust current generation (Fig.2 lower-right). The circuit diagram of the CSD circuit is shown in Fig.3, consisting of a current-starved inverter(CSI) [33] driving the capacitive load C and the next-stage inverter. Based on the large-signal characteristics, the CSD unit delay t_D can be expressed as:

$$t_D = \frac{V_{th}C}{I_{ref}} + t_{inv} \tag{2}$$

where V_{th} and t_{inv} is the on-threshold and the delay of the next-stage inverter, respectively, since the signal fully propagates by the time the CSI current source enters the triode region, such effect can be neglected from the analysis. In eq.(2), if we assume that t_{inv} and V_{th} variation is sufficiently small, t_D will be determined by C and I_{ref}. Since TBCS converges t_{DL} to a predetermined value, after locking, I_{ref} will become a value corresponding to the capacitance C. In advanced CMOS processes, capacitors are significantly less invariant to environmental variations such as voltage, temperature, and mismatch than resistors and transistors.

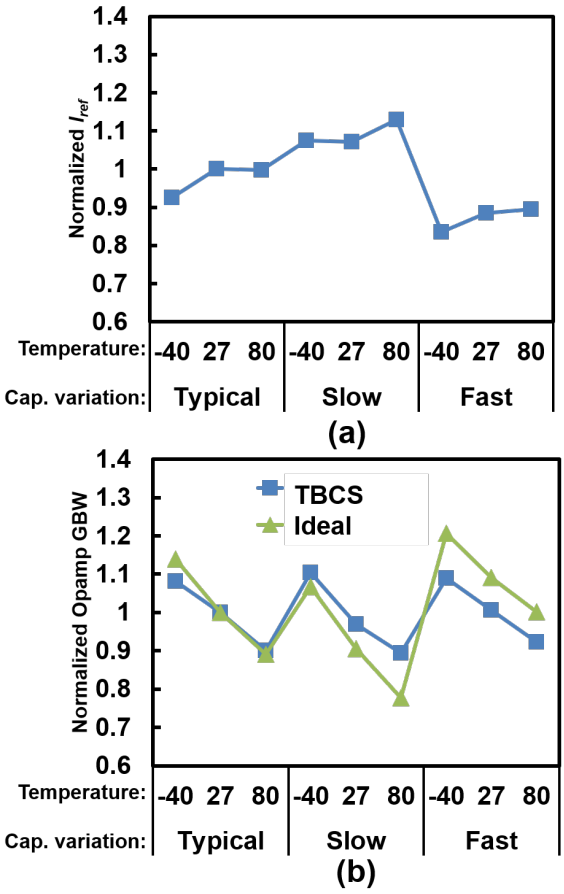


Fig. 4 (a) Simulation results of the TBCS I_{ref} under capacitor manufacturing variations. "Slow" conditions indicate variations with increased capacitance and *vice versa*. (b) Simulation results of the opamp GBW biased by TBCS and ideal current source under the same variations, respectively.

Therefore, TBCS can achieve robust current generation independent of environmental variations with delay lock-based configuration.

From eq.(2), the TBCS variation factors are 1) next-stage inverter delay 2) load capacitance variation and 3) V_{th} variation. Since the delay of the next-stage inverter is one order of magnitude smaller than the CSI delay, its effect is negligible. On the other hand, the capacitance variation must be small for TBCS to be a robust current source. While metal-insulator-metal (MIM) capacitors have small local mismatches, they are not suitable for TBCS due to their large absolute capacitance variation. On the other hand, metal-oxide-metal (MOM) capacitors have a significantly smaller absolute capacitance variation, making them suitable for TBCS. Moreover, in the next section, we will show that the current drifts due to capacitance and V_{th} variation can help to stabilize the opamp characteristics.

3.2 PVT adaptive current generation characteristics

While the TBCS decouples current generation from resistor variation, the capacitor and V_{th} variation causes current drifts since T_{DL} is determined by the capacitor charging

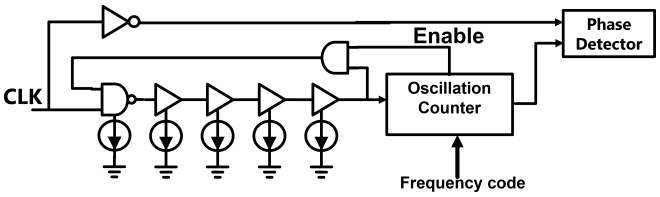


Fig. 5 Circuit diagram of TBCS supporting multiple input frequencies. The use of oscillation counter makes it possible to lock to the same I_{ref}, as long as the input frequencies are integer multiples of each other.

time. Interestingly, the current drift due to the capacitance and V_{TH} variation militates to improve the opamp PVT tolerance. From eq.(2), as C increases, I_{ref} will increase, and conversely, as C decreases, I_{ref} decreases. Such characteristic is undesirable from the viewpoint of a *constant* current source. On the other hand, it is important to note that when such capacitance variation occurs, the load capacitance of the opamp will increase/decrease as well. As the load capacitance increases, the gain-bandwidth (GBW) of the opamp degrades; however, the TBCS *adaptively* increases the current to compensate for the degraded GBW. Thus, the TBCS will help to keep the opamp GBW constant through PVT variations. Vth variation has a similar effect: under "slow" conditions where V_{th} increases, I_{ref} increases to compensate for the slowdown of the opamp.

To further analyze this effect, we perform extensive simulations, where Fig.4(a) and (b) show the generated TBCS current (I_{ref}) and opamp GBW under capacitance variation, respectively. Here, a simple two-stage differential opamp biased via TBCS was utilized. In the "slow" conditions (larger capacitance), the I_{ref} increases by about 10-15%, which compensates for the opamp GBW degraded by the increased load capacitance. Interestingly, due to the adaptive current generation, TBCS can maintain opamp GBW constant through variations than an ideal current source. Under "fast" conditions, the I_{ref} is reduced, but the effect on GBW is small because the opamp load is also reduced. Thus, TBCS reduces the power consumption while maintaining the required opamp GBW.

In general, mass-produced chips are designed to meet the critical performance (e.g. opamp GBW) even under the worst variations. Therefore, if we can suppress GBW degradation under the worst condition, the design margin can be reduced to improve the system power consumption. In Fig.4(b), the GBW under the worst condition is improved by 13% with TBCS over the ideal current source, proving that TBCS contributes to the design margin reduction.

3.3 Varying CLK input frequency

In this design, the CSD is designed to assume that the clock frequency is fixed to 80MHz. However, since we consider a wireless frontend as an application, other operating frequencies such as 20MHz and 40MHz can be considered TBCS input candidates.

Here, we will show some additional design ideas to realize TBCS with multiple input frequencies. If the candidate clock frequencies have a relationship of integral multiples (common for wireless receiver ADCs), a constant current can be generated by oscillating the CSD multiple times as Fig.5. For example, when the input clock is 1/4 of the design frequency (20MHz), the current source can be locked at a state close to 80MHz by oscillating the CSD four times using a counter to generate a constant current. Note that the input frequency state must be given to the counter for operation.

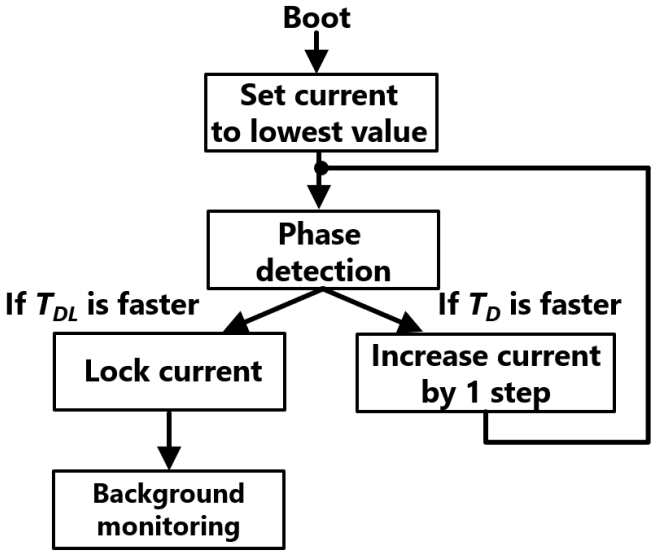


Fig. 6 TBCS control flowchart.

4. Circuit Implementations

4.1 Control circuit

Firstly, the primary control flow of TBCS is explained in detail using Fig.6. When the power is turned on, the current source is set to output the lowest I_{ref}. Then, we search the optimal current code by increasing the code step by step. Since I_{ref} is small at the beginning, T_{DL} is prolonged, and the phase detector judge that T_D arrives early and I_{ref} is increased by one step. This procedure is repeated, and once T_{DL} arrives earlier, the current is "locked", and TBCS enters the background tracking mode.

Since this control method is simple bang-bang control, a maximum of 2^N cycles are required to converge (N is the number of bits in the configurable current source). For example, if we utilize successive approximations, we can achieve faster convergence. However, it may not be possible to track the environment drifts during the locking procedure (e.g. sharp voltage drifts).

4.2 Phase detector

Next, we will discuss the implementation of the phase detector. While a 1-bit TDC is easily realized with a single flip-flop, there is a possibility of code flapping (chattering) which is illustrated in Fig.8. If I_{ref} is increased in the first

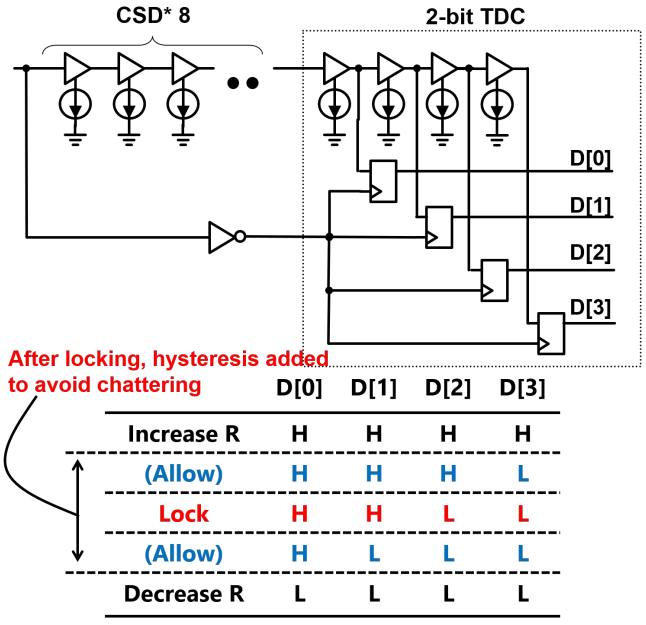


Fig. 7 Background monitoring control of TBCS utilizing a 2-bit TDC circuit.

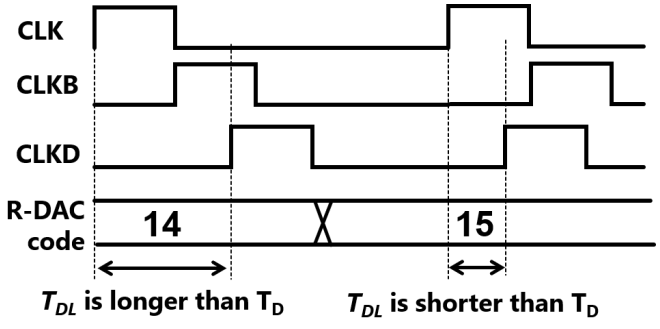


Fig. 8 Timing chart showing the chattering effects.

phase cycle (code 14 to 15), the delay becomes smaller than T_D in the next phase comparison. Then, I_{ref} will be reduced in the next cycle, reflecting the comparison result (codes 15 to 14), and such chattering may cause unwanted spurs in the SC circuit. While chattering can be prevented by fixing the control code after the current is locked, TBCS will lose the ability to track PVT drifts.

In our design, we utilize a 2-bit TDC as the phase detector to prevent chattering and provide PVT drift tracking (Fig.7). Once the current is locked, the TBCS enters the background monitoring mode to track long-term environmental variations. As shown in the table of Fig.7, the current code is not updated except when all the D[0:3] bits transition to High or Low, which prevents chattering but can respond to long-term environmental changes. Note that before locking, only bit D[1] is used for control (identical to 1-bit TDC), and after locking, the full 2-bit output D[0:3] is utilized.

4.3 R-DAC based current generator

The circuit diagram of the R-DAC, which constructs the

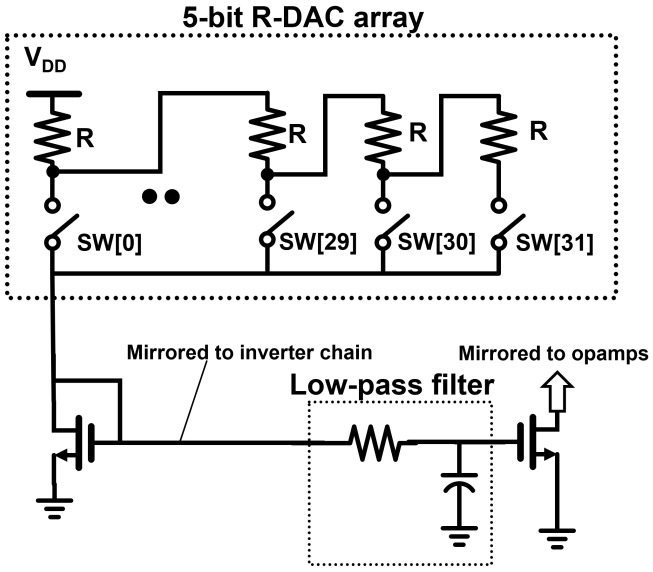


Fig. 9 Circuit diagram of 5-bit R-DAC and low-pass filter.

Table 1 Generated current resolution with 4, 5, and 6-bit R-DACs. The simulation is done with unit resistance = 4kΩ.

R-DAC resolution	4-bit	5-bit	6-bit
Current resolution [uA]	5.3	1.3	0.3

variable reference current source is shown in Fig.9. The generated current I_{ref} is decided by configuring the resistance value of the R-DAC as:

$$I_{ref} = \frac{V_{DD}}{R_{NMOS} + R_{DAC}} \tag{3}$$

R_{DAC} is controlled by a one-hot digital code (SW[0:31]): when SW[31] is high, the resistance takes the maximum value of 32R and the lowest value R at SW[0]. In TBCS, the R-DAC design is the most critical factor. Specifically, the R-DAC must be designed to satisfy the following two points: (1) whether the accuracy of the generated current is sufficient and (2) whether the current target value can be generated even under PVT variations.

First of all, the R-DAC resolution directly couples to the generated current precision as shown in eq.(3). Table 1 summarizes the simulation result of the I_{ref} resolution when the R-DAC resolution was varied from 4, 5 to 6 bits. In simulations, we adapt the current differential of the center code for simplicity. The 4-bit R-DAC had a step of 5uA, which is too large for our design. On the other hand, the 5-bit R-DAC had a step of 1.3uA, which is sufficient precision.

In addition, we need to check if the TBCS can lock to the target current even with resistance variation. The DAC code vs. I_{ref} with resistance variation is plotted in Fig. 10. It can be seen that the target I_{ref}= 30uA can be covered in all conditions. If the resistance variation is too large to cover the target I_{ref}, the R-DAC resolution should be increased

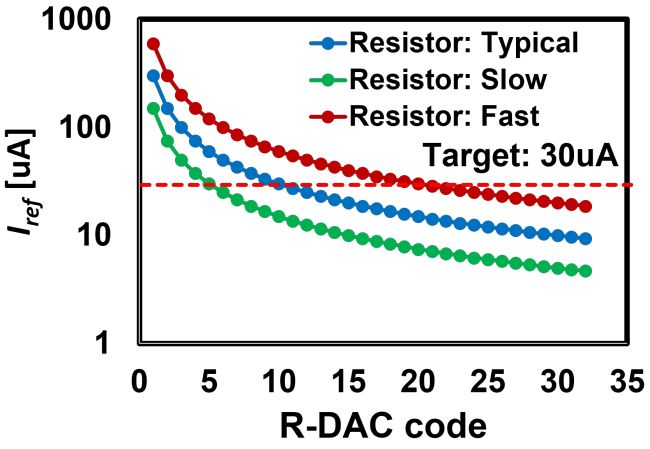


Fig. 10 Simulation results of R-DAC code versus generated current under resistance variation.

to widen the resistor range. To cancel the kickback from the CSIs, a small low-pass filter is configured (Fig.9) with passive devices to remove the switching component from the opamp bias.

4.4 Current starved delaylines (CSD)

Finally, we describe the current starved delaylines (CSD) shown in Fig.3. While resistance mismatch affects I_{ref} in conventional current sources, the effect of resistance mismatch is small in TBCS due to the delay-locking feature. However, the CSD delay time variation harms I_{ref}. If we denote the delay mismatch of the single delayer as var, the overall variation of the N-stage CSD increases to $var \times \sqrt{N}$. However, since the signal component also become N times more significant, the variation is mitigated to $\frac{1}{\sqrt{N}}$. To improve the TBCS tracking ability towards capacitance variation, it is necessary to use a same type of capacitor for both the amplifier and the CSI to ensure capacitance drifts are similar. In this design, MIM capacitors are used for both capacitors. Furthermore, to assure that the load capacitance determines the CSD delay, we design the load (16fF) to be sufficiently larger than the inverter gate capacitance (1fF). In this design, the load capacitance determines the opamp GBW, but the transistor parasitics may dominate the speed with a faster opamp design. In this case, the CSD should also be designed without load capacitance so that the parasitic capacitance will determine the speed to improve the TBCS tracking ability.

While jitter is also an important design factor in DLLs, the effect is small in TBCS. Since the jitter is sufficiently small compared to the total delay and TBCS uses hysteresis after locking, the jitter effect can be neglected.

5. Simulation and measurement results

The prototype TBCS was fabricated with 28nm CMOS, and the chip photograph is shown in Fig. 11. TBCS occupies

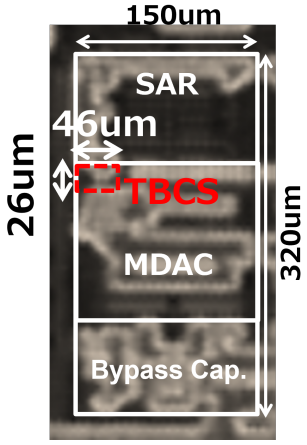


Fig. 11 Fabricated chip photograph of the TBCS, integrated into an ADC.

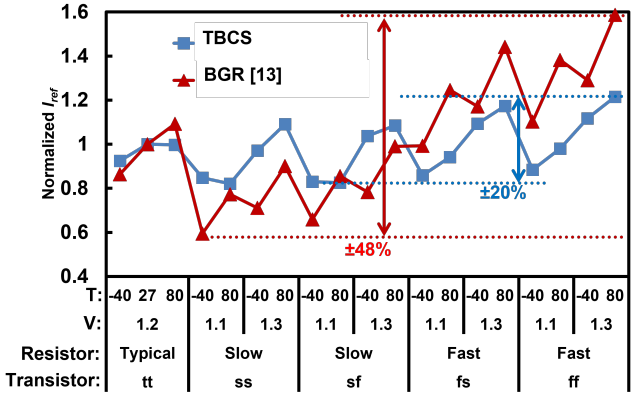


Fig. 12 Simulation result of the TBCS and BGR current source I_{ref} under PVT variations, respectively.

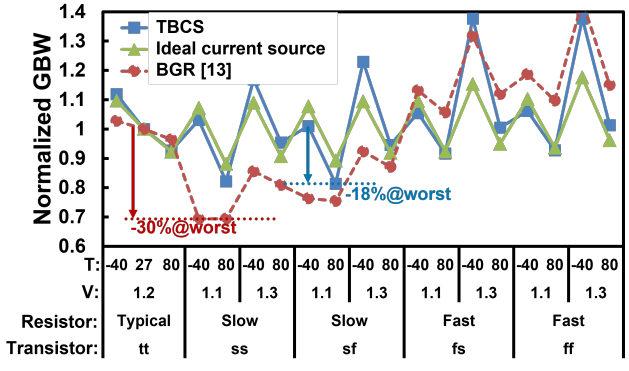


Fig. 13 Simulation result of the opamp GBW biased with TBCS, ideal and BGR current source I_{ref} under PVT variations, respectively.

a very small area of $46um \times 26um$ ($0.0012mm^2$). Unlike the BGR, TBCS does not require bipolar transistors or amplifiers and can be easily designed in advanced CMOS with low supply voltage. Since bipolar transistors and opamps have poor CMOS scaling characteristics, realizing them in scaled CMOS results in a relatively high cost. In the prototype chip, the TBCS is integrated into the ADC of ref. [22]. Since the

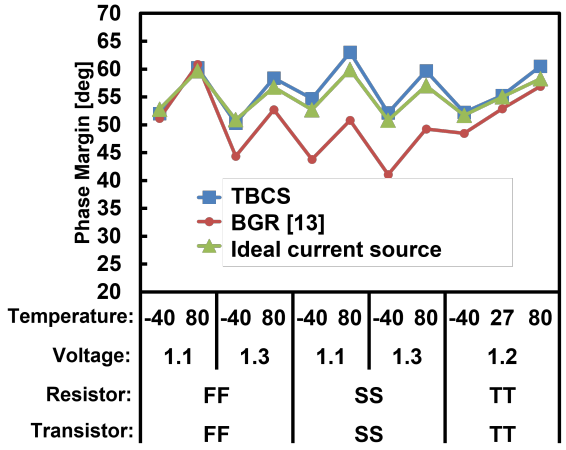


Fig. 14 Simulation result of the opamp phase margin when biased with TBCS, ideal and BGR current source I_{ref} under PVT variations, respectively.

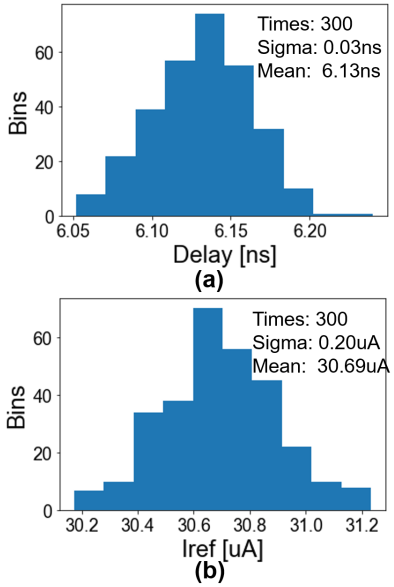


Fig. 15 (a) Monte-Carlo simulation results of the CSD delay. (b) Monte-Carlo simulation results of the TBCS I_{ref} under typical conditions.

prototype does not have an I_{ref} monitoring pin, it was not possible to directly measure the detailed characteristics of the TBCS. Thus, we mainly report simulation analysis in this paper†

Firstly, we analyze the I_{ref} of BGR current source (BGR ref) [13] as in Fig.1 and TBCS, respectively. Fig.12 shows the simulation results of both current sources under the written PVT variations. The BGR ref with poly-resistors has a large sensitivity to manufacturing variations, and the min-max current value is more than 30uA throughout the variations. The variance is substantial at SSLTLV conditions, where I_{ref} drops by 40% compared to typical conditions. Since this corner condition is where the opamp speed is most severe, it will become more challenging to satisfy the target opamp GBW.

In addition, the significant I_{ref} increase in the FF condition also poses a problem: the increase in I_{ref} requires to increase the transistor V_{gs} which may narrow down the output range of the opamp. To summarize, to make robust opamp characteristics, it is desirable that I_{ref} increases in the SS condition and decreases in the FF condition.

On the other hand, the simulated TBCS I_{ref} is reported in Fig.12. The input clock frequency is 80MHz, and the TBCS is designed to output 30uA. The main difference between TBCS and BGR ref is the min-max current divergence under PVT. In contrast to BGR, which has a min-max difference of 30uA due to resistance variation, the TBCS reduces the variation width by over half (14uA) thanks to the delay-

†For NDA reasons, all simulation results are reported based on the circuit reimplemented in 65nm CMOS. There is no significant change in the fundamental TBCS performance.

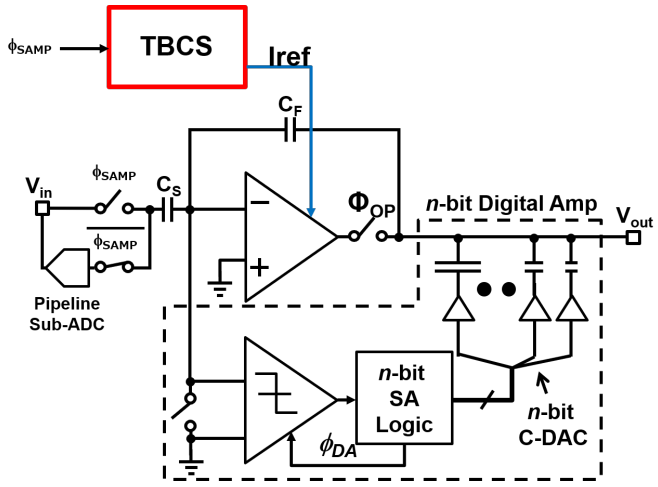


Fig. 16 Circuit diagram of the SC circuit with integrated TBCS.

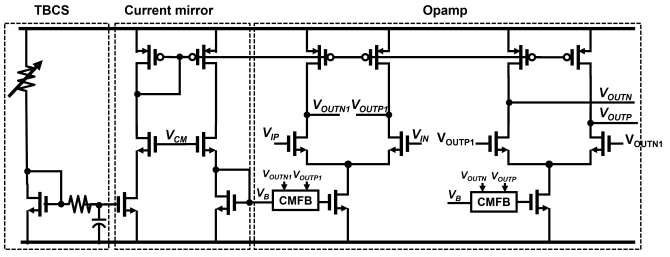


Fig. 17 Full schematic showing the TBCS and opamp integration.

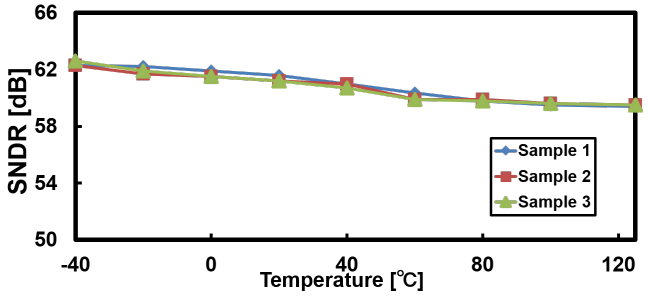


Fig. 18 SNDR measurement results of TBCS integrated ADC.

locking feature.

We report the opamp GBW simulation in Fig.13, where the opamp was biased with BGR, ideal, and TBCS current sources at different PVT variations, respectively. Identical to the simulation in Fig.4, we simulate via a simple two-stage differential opamp implemented inside an SC circuit. As discussed, since the BGR ref reduces its current in the SS condition, the GBW is also significantly reduced. In the worst corner, the opamp GBW degrades by almost 30%, significantly increasing the opamp design margin. On the other hand, TBCS can track PVT with delay-locking, and the obtained worst-case opamp GBW is almost the same as that of the ideal current source. Moreover, even in the worst corner, the GBW degradation is only 18%, which is only half of BGR ref. Thus, TBCS significantly relaxes the opamp design margin and contributes to reducing the system power consumption. The GBW variance of TBCS in Fig.13 is larger than Fig.4 because the supply voltage fluctuation of ±100mV is also included in Fig.13. Since the transistors of TBCS and opamps operate in different regions, the effects of supply voltage change cannot be fully absorbed. In addition, we report the opamp phase margins under similar simulation conditions. The opamp is designed with a phase margin of 55°@Typ. for high-speed operations, and its function is guaranteed up to 50°. While the BGR-biased opamp falls short in some corners, TBCS, helds a constant phase margin over 40° due to its current compensation under severe corner conditions.

Next, we will discuss the opamp power reduction effect with TBCS, based on the results in Fig.13. Here, we assume that the opamp is to be designed to achieve 0.82 GBW in all corners. On the other hand, since BGR biased opamps can only achieve 0.7 GBW in the worst case, we must increase the opamp current to lift the GBW. The relationship between opamp GBW and g_m is described as:

$$GBW = \frac{g_m}{2\pi C_L} \tag{4}$$

Let's assume a constant current density opamp where doubling the g_m also doubles the opamp power. Thus, for BGRs, the opamp power must be increased by 20% to lift the GBW of the worst corner to match our design criteria. Therefore, we can summarized that the use of TBCS will reduce the opamp power by 20%, compared to BGR biasing methods.

Fig.15 shows the results of the TBCS Monte Carlo analysis. The overall delay variation is about σ = 30ps in this design, which is small enough compared to the TDC LSB step of 600ps. As can be seen from the results of Fig.15(b), the effect of mismatch on I_{ref} is also tiny compared to the current resolution of 1.3uA.

The schematic of the SC circuit and the TBCS+opamp integration is shown in Fig.16 and Fig.17, respectively. Moreover, Fig.18 shows the ADC measurement results, which uses the TBCS as a current source. The SC circuit employs two-stage amplification: the opamp biased by TBCS performing coarse amplification and the successive approximation circuit performs fine amplification. The ADC achieves a high SNDR (60dB) at a range of -40 to 125°C; this results shows that TBCS is functioning in silicon, with wide-range environment changes.

Lastly, we compare TBCS against published current sources with uA order outputs in Table 2. While most aim to generate a temperature-insensitive current with PTAT/CTAT, the current generated by these works depends mainly on the absolute resistor value. To cancel out resistor variations, high-cost resistance calibration must be done as in ref. [8]. Although the basic idea under the proposed TBCS is simple, a calibration-free temperature and resistor insensitive current source is realized by exploiting PVT-insensitive frequency information as a reference. In addition, to create accurate PTAT currents, large transistors are required to reduce channel modulation effects and transistor mismatch, which is a drawback in scaled CMOS designs (e.g., ref. [12] is a BGR fabricated in 16nm CMOS but with an area 10 times larger than TBCS). On the other hand, TBCS does not rely on transistor characteristics and is mostly digital, a good feature for scaled CMOS designs.

6. Conclusions

We proposed a Time-Based Current Source (TBCS), which is a resistor-variation tolerant reference current source circuit suitable for scaled CMOS. TBCS utilizes the input clock time information and delay-locking, where the load capacitors determine the delay. This decouples the generated current from resistor values, enabling a robust reference current source. Simulation results showed that the TBCS can halve the current variation compared to a bandgap current source under wide PVT variations. When utilized as the opamp's bias, TBCS achieves the same opamp GBW as an ideal current source through PVT variations. In addition, TBCS is realized mainly with digital circuits and consumes a very small area of 1200um^2 when fabricated with 28nm CMOS.

References

[1] Benjamin Jann, Greg Chance, Ankur Guha Roy, Aishwarya Balakrishnan, Niranjan Karandikar, Thomas Brown, Xi Li, Brandon Davis, Jose Luis Ceballos, Nebil Tanzi, et al., "A 5G sub-6GHz zero-IF and mm-Wave IF transceiver with MIMO and carrier aggregation," in *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE, 2019, pp. 352–354.

[2] David J McLaurin, Kevin G Gard, Richard P Schubert, Manish J Manglani, Haiyang Zhu, David Alldred, Zhao Li, Steven R Bal, Jianxun Fan, Oliver E Gysel, et al., "A highly reconfigurable 65nm CMOS RF-to-bits transceiver for full-band multicarrier TDD/FDD 2G/3G/4G/5G macro basestations," in *2018 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE, 2018, pp. 162–164.

[3] Ahmed MA Ali, Huseyin Dinc, Paritosh Bhoraskar, Chris Dillon, Scott Puckett, Bryce Gray, Carroll Speir, Jonathan Lanford, Janet Brunsilius, Peter R Derounian, et al., "A 14 bit 1 GS/s RF sampling pipelined ADC with background calibration," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2857–2867, 2014.

[4] Ahmed MA Ali, Huseyin Dinc, Paritosh Bhoraskar, Scott Bardsley, Chris Dillon, Matthew McShea, Joel Prabhakar Periathambi, and Scott Puckett, "A 12-b 18-GS/s RF Sampling ADC With an Inte-

Table 2 Performance comparison between published current source designs.

	Lee 2012 [11]	Wu 2015 [17]	Osipov 2016 [8]	Osipov 2019 [9]	Wadhwa 2017 [12]	Our work
Technology [nm]	180	180	350	350	16	28
Approach	PTAT/CTAT	BGR	β-Multiplier	PTAT/CTAT	BGR	Time-based
Temp. range [C]	0~100	-40~80	0~110	-45~125	-40~125	-40~80
Supply range [V]	1	2.4	1.9-3.6	2.2-3.6	1.8	0.5-0.9
I_{ref} [uA]	7.8	10	16	24	20	30
Tolerate resistor variation?	No	No	Yes	No	No	Yes
Calibration?	No	No	Yes	No	No	No
Area [mm^2]	0.12	0.05	0.065	0.027	0.011	0.0012

grated Wideband Track-and-Hold Amplifier and Background Calibration," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 12, pp. 3210–3224, 2020.

[5] Jorge Lagos, Benjamin Hershberg, Ewout Martens, Piet Wambacq, and Jan Craninckx, "A single-channel, 600-MS/s, 12-b, ringamp-based pipelined ADC in 28-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 2, pp. 403–416, 2018.

[6] Tsung Chih Hung, Jia Ching Wang, and Tai Haur Kuo, "A Calibration-Free 71.7 dB SNDR 100MS/s 0.7 mW Weighted-Averaging Correlated Level Shifting Pipelined SAR ADC with Speed-Enhancement Scheme," in *2020 IEEE International Solid-State Circuits Conference, ISSCC 2020*. 2020, pp. 256–258, IEEE.

[7] Cristina Azcona, Belén Calvo, Santiago Celma, Nicolás Medrano, and Maria Teresa Sanz, "Precision CMOS current reference with process and temperature compensation," in *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2014, pp. 910–913.

[8] Dmitry Osipov and Steffen Paul, "Temperature-Compensated β Multiplier Current Reference Circuit," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 10, pp. 1162–1166, 2016.

[9] Dmitry Osipov and Steffen Paul, "Compact extended industrial range cmos current references," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 6, pp. 1998–2006, 2019.

[10] Lidan Wang and Chenchang Zhan, "A 0.7-V 28-nW CMOS subthreshold voltage and current reference in one simple circuit," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 9, pp. 3457–3466, 2019.

[11] Junghyup Lee and SeongHwan Cho, "A 1.4-μw 24.9-ppm/° c current reference with process-insensitive temperature compensation in 0.18-μm cmos," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 10, pp. 2527–2533, 2012.

[12] Sanjay Kumar Wadhwa and Nidhi Chaudhry, "High accuracy, multi-output bandgap reference circuit in 16nm finfet," in *2017 30th International Conference on VLSI Design and 2017 16th International Conference on Embedded Systems (VLSID)*. IEEE, 2017, pp. 259–262.

[13] Hironori Banba, Hitoshi Shiga, Akira Umezawa, Takeshi Miyaba, Toru Tanzawa, Shigeru Atsumi, and Koji Sakui, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, 1999.

[14] Ken Ueno, Tetsuya Hirose, Tetsuya Asai, and Yoshihito Amemiya, "A 300 nW, 15 ppm/C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs," *IEEE Journal of solid-state circuits*, vol. 44, no. 7, pp. 2047–2054, 2009.

[15] Ken Ueno, Tetsuya Hirose, Tetsuya Asai, and Yoshihito Amemiya, "A 1uW 600ppm/C Current Reference Circuit Consisting of Subthreshold CMOS Circuits," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 9, pp. 681–685, 2010.

[16] Wenbin Huang, Lianxi Liu, and Zhangming Zhu, "A sub-200nw all-in-one bandgap voltage and current reference without amplifiers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 1, pp. 121–125, 2020.

[17] Chundong Wu, Wang Ling Goh, Chiang Liang Kok, Wanlan Yang, and Liter Siek, "A low tc, supply independent and process compensated current reference," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, 2015, pp. 1–4.

[18] Tetsuya Hirose, Yuji Osaki, Nobutaka Kuroki, and Masahiro Numa, "A nano-ampere current reference circuit and its temperature dependence control by using temperature characteristics of carrier mobilities," in *2010 Proceedings of ESSCIRC*. IEEE, 2010, pp. 114–117.

[19] Tetsuya Hirose, Ken Ueno, Nobutaka Kuroki, and Masahiro Numa, "A CMOS bandgap and sub-bandgap voltage reference circuits for nanowatt power LSIs," in *2010 IEEE Asian Solid-State Circuits Conference*. IEEE, 2010, pp. 1–4.

[20] Yuji Osaki, Tetsuya Hirose, Nobutaka Kuroki, and Masahiro Numa, "1.2-V supply, 100-nW, 1.09-V bandgap and 0.7-V supply, 52.5-nW, 0.55-V subbandgap reference circuits for nanowatt CMOS LSIs," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 6, pp. 1530–1538, 2013.

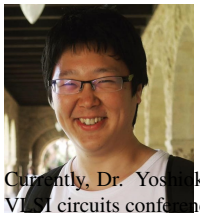
[21] Myungjoon Choi, Inhee Lee, Tae-Kwang Jang, David Blaauw, and Dennis Sylvester, "A 23pW, 780ppm/° C resistor-less current reference using subthreshold MOSFETs," in *ESSCIRC 2014-40th European Solid State Circuits Conference (ESSCIRC)*. IEEE, 2014, pp. 119–122.

[22] Kentaro Yoshioka, Tomohiko Sugimoto, Naoya Waki, Sinnyoung Kim, Daisuke Kurose, Hirotomo Ishii, Masanori Furuta, Akihide Sai, and Tetsuro Itakura, "A 0.7 V 12b 160MS/s 12.8 fJ/conv-step pipelined-SAR ADC in 28nm CMOS with digital amplifier technique," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*. IEEE, 2017, pp. 478–479.

[23] Kentaro Yoshioka, Tomohiko Sugimoto, Naoya Waki, Sinnyoung Kim, Daisuke Kurose, Hirotomo Ishii, Masanori Furuta, Akihide Sai, Hiroki Ishikuro, and Tetsuro Itakura, "Digital Amplifier: A Power-Efficient and Process-Scaling Amplifier for Switched Capacitor Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 11, pp. 2575–2586, 2019.

[24] Chuanyang Wang, "Adaptive bias current generation for switched-capacitor circuits," US Patent No. 7750837.

[25] Ron Kapsta, "Adaptive bias current generator methods and apparatus," US Patent No. 8044654.
[26] Zhu Jun, "Adaptive voltage scaling using a delay line," US Patent No. 8378738.
[27] Ron Kapusta, Junhua Shen, Steven Decker, Hongxing Li, Eitake Ibaragi, and Haiyang Zhu, "A 14b 80 Ms/s SAR ADC with 73.6 db SNDR in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3059–3066, 2013.
[28] Fredric Thompson, "Use of a DLL to optimize an ADC performance," US Patent No. 8786483.
[29] Stefanos Sidiropoulos and Mark A Horowitz, "A semidigital dual delay-locked loop," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 11, pp. 1683–1692, 1997.
[30] Thomas H Lee, Kevin S Donnelly, John TC Ho, Jared Zerbe, Mark G Johnson, and Toru Ishikawa, "A 2.5 V CMOS delay-locked loop for 18 Mbit, 500 megabyte/s DRAM," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 12, pp. 1491–1496, 1994.
[31] Behzad Razavi, "The delay-locked loop [A circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 10, no. 3, pp. 9–15, 2018.
[32] Hyunik Kim, Yongjo Kim, Taeik Kim, Hyung-Jong Ko, and Seonghwan Cho, "A 2.4-GHz 1.5-mW digital multiplying delay-locked loop using pulsewidth comparator and double injection technique," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 2934–2946, 2017.
[33] Przemysław Mroszczyk and Piotr Dudek, "Tunable CMOS delay gate with improved matching properties," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 9, pp. 2586–2595, 2014.



Kentaro Yoshioka received his BS, MS, Ph.D degrees from Keio University, Japan. Currently, he is an Assistant Professor at Keio University. He worked with Toshiba during 2014-2021, developing circuitry for WiFi and LiDAR SoCs. During 2017-2018, he was a visiting scholar at Stanford University, exploring efficient machine learning hardware and algorithms. Currently, Dr. Yoshioka serves as a technical program member of Symp. VLSI circuits conference. He was the recipient of ASP-DAC 2013 Special Feature Award, the A-SSCC 2012 Best Design Award, and 1st place winner of Kaggle 2020 Prostate Cancer Grade Assessment (PANDA) Challenge.