Main goal is to compare the performance of FPGAs and CPUs for the purpose performing tag detection in genomic data.

Uses gigabit Ethernet for all communication. The plan is to replace this with PCIe or FSB at a later point. Because of this intention, we did not fully implement the Ethernet communication. for instance, the returned header is hardcoded and there is no way to reset the board (other than reprogramming the device).

We started with MP1 as the basis for our communication layer but ultimately removed the scanner and address swap layers. Working directly with the link layer FIFOs gives us the control we need.

|  |  |  |
| --- | --- | --- |
| Number of compare units | Occupied slices | Percentage of chip |
| 2 | 800 | 7.14% |
| 4 | 851 | 7.60% |
| 8 | 1504 | 13.43% |
| 16 | 2595 | 23.17% |
| 32 | 3418 | 30.52% |
| 64 | 5969 | 53.29% |
| 96 | 9623 | 85.92% |

Limitations:

No way to restart other than reprogramming.

Very finicky with initial programming and packets, can easily get into an unreliable state.

Uses a fixed amount of return bandwidth, alternatively could report matching IDs.

Requires software to find the actual IDs.

Return UDP header is hardcoded.