CENTER OF NANOELECTRONICS & DEVICES

CND 211: Advanced Digital Design

Midterm Exam #: lab 8

Section #:

Submitted by:

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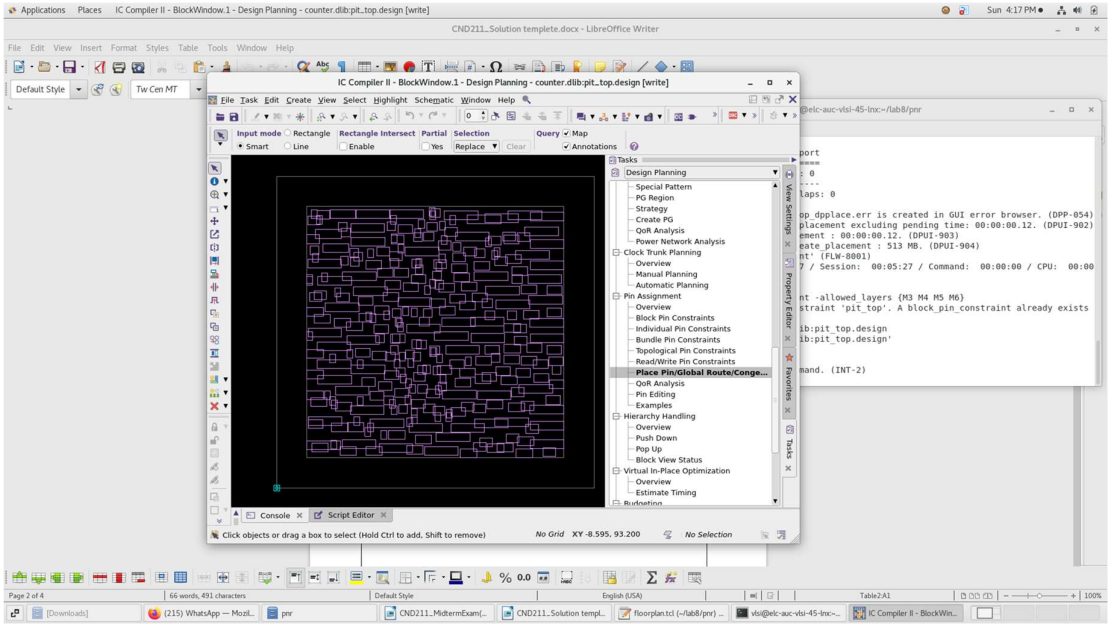
Answers

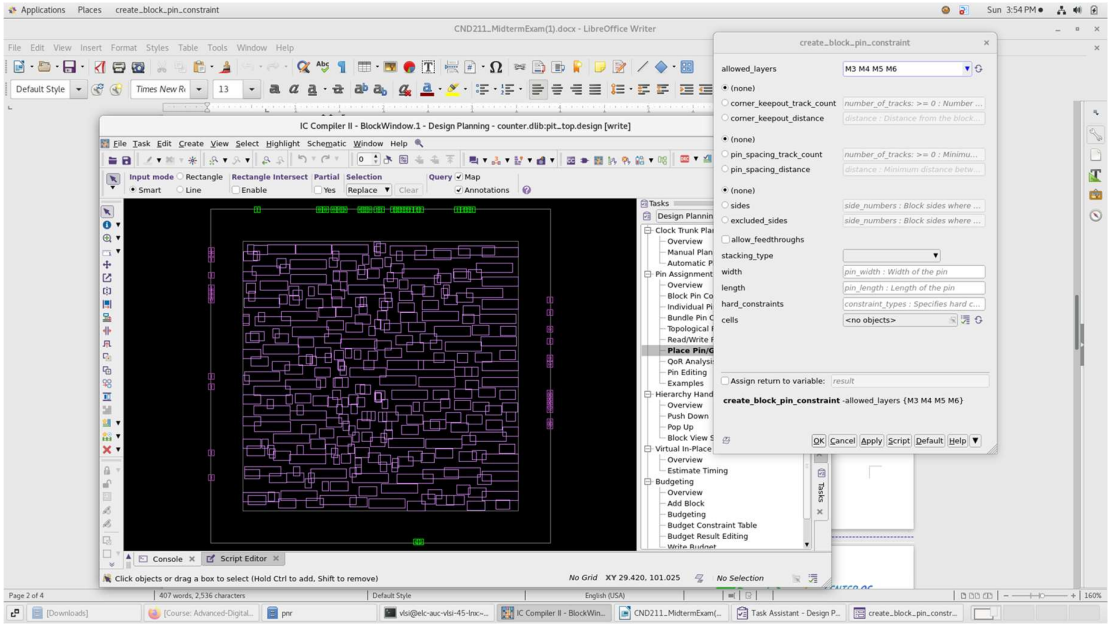
Q.1

```
.... put your script for floor planning


open_block /home/vlsi/lab8/pnr/counter.dlib:pit_top.design

link_block

set_parasitic_parameters -late_spec maxTLU   -early_spec minTLU

initialize_floorplan -core_utilization 0.6 -side_ratio {1 1} -
core_offset {10}

set_app_options -name place.coarse.fix_hard_macros -value
false

set_app_options -name plan.place.auto_create_blockages -value
auto

create_placement -floorplan

create_block_pin_constraint -allowed_layers {M3 M4 M5 M6}

save_block   counter.dlib:pit_top.design
```

Screenshot before place pins



Screenshot of final block



Q.2

Task 1

1- Type:From Reg(fliflop) To Output Port
2- propagation: 3.899 ns
3- Tc2q = 0.117 n **slack =** + 2.066 (+ve slack → No Setup Violation)
4- max frequency = 94.55 GHz

Task 2

1- Type: From Input Port to Reg(Fliflip)
2- Slack = (+0.95 slack) -> No Violation