CENTER OF NANOELECTRONICS & DEVICES

CND 212: Digital Testing and Verification

Assignment #: 03

Section #: 21

Submitted by:

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// Code your design here


assert property (valid&&ready);

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property p;
@ (posedge clk)
disable iff (rst) a |=> b |=> c;
endproperty

assert property (p);

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property data_greater_than_zero;
    @(posedge clk) disable iff (!rst_n) (data > 0);
endproperty

assert_property (
    data_greater_than_zero,
    @(posedge clk)
) else $error("data_greater_than_zero assertion failed");----------------------------
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property p;
@ (posedge clk)
a|=>a |=> b |=> c ;
endproperty

assert property (p);

--------------------------
sequence s1;
int temp_data=data_in;
 ##7 data_out== data_temp;
endsequence

property p;
@ (posedge data_valid)
s1 ;
endproperty

assert property (p);

--------------------------
sequence s1;

( S1 ##2 S2[=1:2] ##1 S3 ##1 S4[->1:3] ##1 S5);

endsequence

property p;
@ (posedge clk)
s1 ;
endproperty

assert property (p);

-----------------------------
// Code your testbench here
// or browse Examples

module seq();
    bit clk,S1,S2,S3,S4,S5;
  always #5 clk= ~clk;

sequence se1;

```

```
(S1 ##2 S2[=1:2] ##1 S3 ##1 S4[->1:3] ##1 S5);

endsequence


  initial begin


      S1=1;
    repeat(1) @(posedge clk);
    @(posedge clk)S2=1;
   // @(posedge clk);

    @(posedge clk)S3=1 ;
  //  @(posedge clk);

    @(posedge clk)S4=1;
    @(posedge clk)S5=1;

    $dumpfile("v.vcd");
    $dumpvars;
    #100 $finish;



    end

property p;
@ (posedge clk)
se1 ;
endproperty

assert property (p);

  endmodule
```