

**Assignment #: 04**

**Section #: 21**

**Submitted by:**

| Student Name           | ID        |
|------------------------|-----------|
| Serbenas seif el-eslam | V23010565 |
| Ahmed mokhtar masoud   | V23010307 |
| Eslam asaad mahmoud    | V23010461 |
|                        |           |

**Submitted to TA: mariam taher**

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## 1- Test\_bench:

```

D:/New folder/fsm_tb.sv - Default *
Ln#
1  module fsm_tb();
2  reg in,clk,reset;
3  wire [2:0] out;
4
5
6  typedef enum { S0, S1, S2, S3} S;
7
8  FSM a(.);
9
10 covergroup cb;
11
12 cp: coverpoint a.current_state
13 {
14     bins p0=(S0 =>S0);
15     bins p1=(S0 =>S1);
16     bins p2=(S1 =>S2);
17     bins p3=(S2 =>S3);
18     bins p4=(S3 =>S0);
19 }
20 endgroup
21
22 //clock generation
23 initial begin
24     clk=1;
25     forever
26     #1 clk=~clk;
27 end

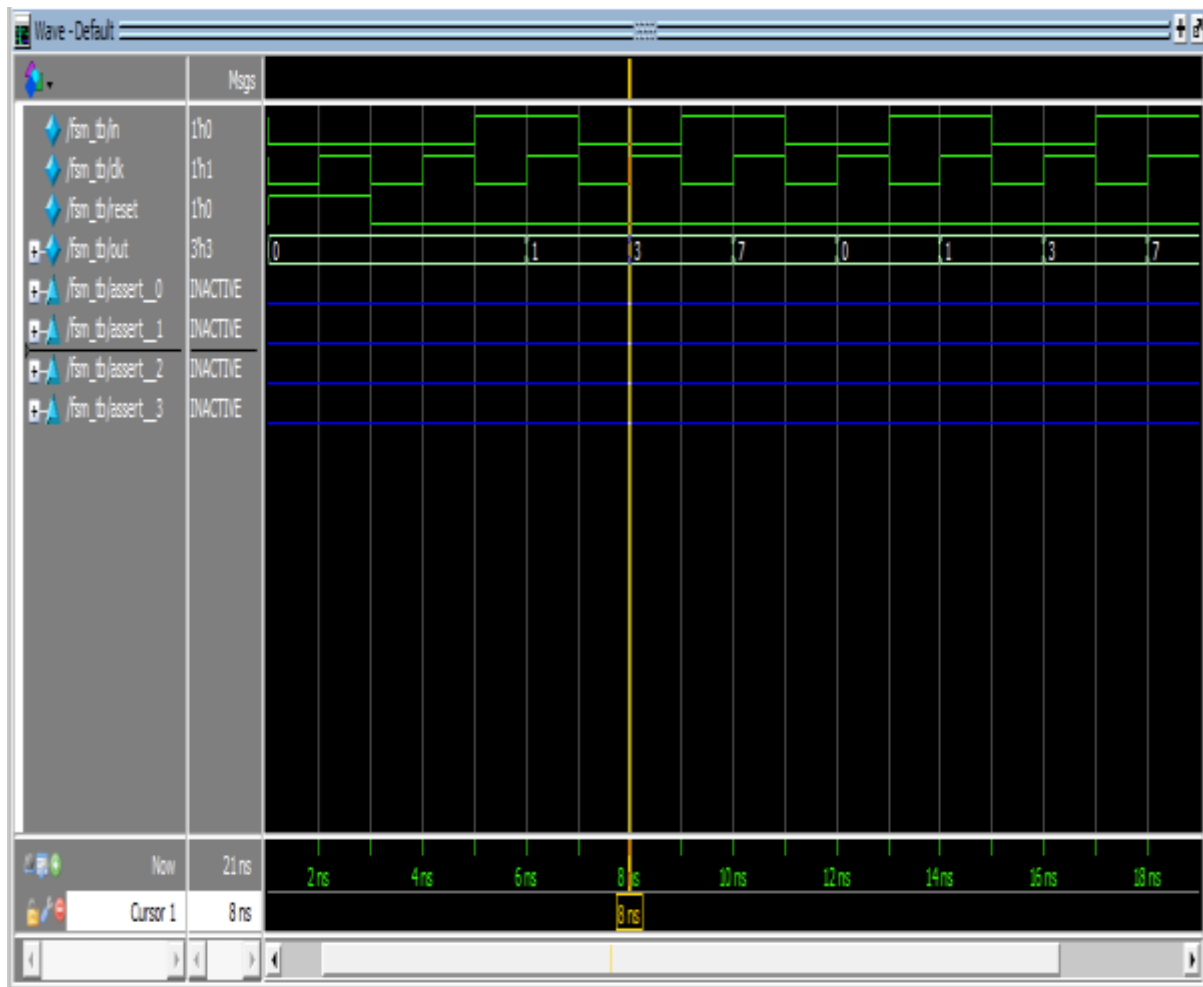
```

```

D:/New folder/fsm_tb.sv - Default *
Ln#
28
29 initial begin
30
31     cb cov;
32     cov=new();
33     reset=0; in=1;
34
35     @(negedge clk); reset=1; in=0; cov.sample();
36     @(negedge clk); reset=0; in=0; cov.sample();
37     @(negedge clk); reset=0; in=1; cov.sample();
38     @(negedge clk); reset=0; in=0; cov.sample();
39     @(negedge clk); reset=0; in=1; cov.sample();
40     @(negedge clk); reset=0; in=0; cov.sample();
41     @(negedge clk); reset=0; in=1; cov.sample();
42     @(negedge clk); reset=0; in=0; cov.sample();
43     @(negedge clk); reset=0; in=1; cov.sample();
44     @(negedge clk); reset=0; in=0; cov.sample();
45     @(negedge clk); reset=0; in=1; cov.sample();
46
47     $stop;
48 end
49
50 assert property(@(posedge clk) a.current_state==S0 |-> out==0);
51 assert property(@(posedge clk) a.current_state==S1 |-> out==1);
52 assert property(@(posedge clk) a.current_state==S2 |-> out==3);
53 assert property(@(posedge clk) a.current_state==S3 |-> out==7);
54 endmodule

```

## 2- wave form:



## 3- Report:

| Covergroup   | Metric  | Goal | Bins | Status  |
|--|---------|------|------|---------|
| TYPE fsm_tb/cb                                     | 100.00% | 100  | -    | Covered |
| covered/total bins:                                | 5       | 5    | -    |         |
| missing/total bins:                                | 0       | 5    | -    |         |
| % Hit:   | 100.00% | 100  | -    |         |
| Coverpoint cp                                      | 100.00% | 100  | -    | Covered |
| covered/total bins:                                | 5       | 5    | -    |         |
| missing/total bins:                                | 0       | 5    | -    |         |
| % Hit:   | 100.00% | 100  | -    |         |
| Covergroup instance \fsm_tb/#ublk#114964130#30/cov | 100.00% | 100  | -    | Covered |
| covered/total bins:                                | 5       | 5    | -    |         |
| missing/total bins:                                | 0       | 5    | -    |         |
| % Hit:   | 100.00% | 100  | -    |         |
| Coverpoint cp                                      | 100.00% | 100  | -    | Covered |
| covered/total bins:                                | 5       | 5    | -    |         |
| missing/total bins:                                | 0       | 5    | -    |         |
| % Hit:   | 100.00% | 100  | -    |         |
| bin p0   | 1       | 1    | -    | Covered |
| bin p1   | 2       | 1    | -    | Covered |
| bin p2   | 2       | 1    | -    | Covered |
| bin p3   | 2       | 1    | -    | Covered |
| bin p4   | 2       | 1    | -    | Covered |

=====Toggle Details=====

Toggle Coverage for instance /fsm\_tb/a --

| Node          | 1H->0L    | 0L->1H | "Coverage" |       |
|---------------|-----------|--------|------------|-------|
| clk           | 1         | 1      | 100.00     |       |
| current_state | ENUM type |        | Value      | Count |
|               |           |        | S0         | 1     |
|               |           |        | S1         | 2     |
|               |           |        | S2         | 1     |
|               |           |        | S3         | 1     |
| in            | 1         | 1      | 100.00     |       |
| next_state    | ENUM type |        | Value      | Count |
|               |           |        | S0         | 1     |
|               |           |        | S1         | 3     |
|               |           |        | S2         | 1     |
|               |           |        | S3         | 1     |
| out[2-0]      | 1         | 1      | 100.00     |       |
| reset         | 1         | 1      | 100.00     |       |

Total Node Count = 14

Toggled Node Count = 14

Untoggled Node Count = 0

Toggle Coverage = 100.00% (20 of 20 bins)

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=== Instance: /fsm\_tb