

CND 212: Digital Testing and Verification

Assignment #: 03

Section #: 21

Submitted by:

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```

1 // Code your design here
2
3
4 assert property (valid&&ready);
5
6 -----
7 property p;
8 @ (posedge clk)
9 disable iff (rst) a | => b | => c;
10 endproperty
11
12 assert property (p);
13
14 -----
15
16 property data_greater_than_zero;
17     @(posedge clk) disable iff (!rst_n) (data > 0);
18 endproperty
19
20 assert_property (
21     data_greater_than_zero,
22     @(posedge clk)
23 ) else $error("data_greater_than_zero assertion failed");-----
24 -----
25
26 property p;
27 @ (posedge clk)
28 a| =>a | => b | => c ;
29 endproperty
30
31 assert property (p);
32
33 -----
34 sequence s1;
35 int temp_data=data_in;
36 ##7 data_out== data_temp;
37 endsequence
38
39 property p;
40 @ (posedge data_valid)
41 s1 ;
42 endproperty
43
44 assert property (p);
45
46 -----
47 sequence s1;
48
49 ( s1 ##2 S2[=1:2] ##1 S3 ##1 S4[->1:3] ##1 S5);
50
51 endsequence
52
53 property p;
54 @ (posedge clk)
55 s1 ;
56 endproperty
57
58 assert property (p);
59
60 -----
61 // Code your testbench here
62 // or browse Examples
63
64 module seq();
65     bit clk,S1,S2,S3,S4,S5;
66     always #5 clk= ~clk;
67
68     sequence sel;
69

```

```
70 (S1 ##2 S2 [=1:2] ##1 S3 ##1 S4 [->1:3] ##1 S5);
71
72 endsequence
73
74
75 initial begin
76
77
78     S1=1;
79     repeat(1) @(posedge clk);
80     @(posedge clk) S2=1;
81     // @(posedge clk);
82
83     @(posedge clk) S3=1 ;
84     // @(posedge clk);
85
86     @(posedge clk) S4=1;
87     @(posedge clk) S5=1;
88
89     $dumpfile("v.vcd");
90     $dumpvars;
91     #100 $finish;
92
93
94
95     end
96
97 property p;
98 @ (posedge clk)
99 sel ;
100 endproperty
101
102 assert property (p);
103
104 endmodule
```