CENTER OF NANOELECTRONICS & DEVICES

CND 211: Advanced-Digital Design

Assignment #: 03

Section #: 21

Submitted by:

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```
create_clock -period 3 [get_ports clk]
set_clock_latency -source -max 0.7 [get_clocks clk]
set_clock_latency -max 0.3 [get_clocks clk]
set_clock_uncertainty -setup 0.15 [get_clocks clk]
set_clock_transition 0.12 [get_clocks clk]
set_input_delay -max  0.45 -clock clk [get_ports data*]
set_input_delay -max  0.4 -clock clk [get_ports sel]
set_output_delay -max  0.5 -clock clk [get_ports out1]
set_output_delay -max 2.04  -clock clk [get_ports out2]
set_output_delay -max  0.4 -clock clk [get_ports out3]
set_input_delay -max 0.3 -clock clk [get_ports Cin*]
set_output_delay -max 0.1 -clock clk [get_ports Cout]

-------------------------------------------------------
set_input_delay -clock clk -max 0.00 [all_inputs_except {clk Cin*}] -clock_fall
-clock_rise -add_delay_from_cell bufbdl
set_input_transition -max 120.0 [get_ports {Cin*}]
set_load -max 2 [capacitance_of I cellbufbd7] [all_outputs_except Gout]
set_load -max 25.0 [get_ports Cout]
```