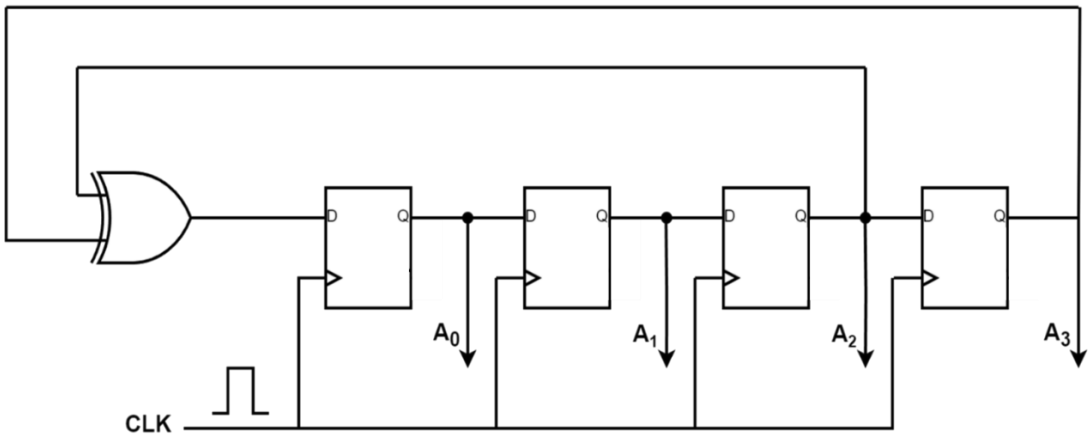
CENTER OF NANOELECTRONICS & DEVICES

# CND 221

# ADVANCED FULL CUSTOM VLSI DESIGN

## MIDTERM EXAM

Design a **4-bit Pseudo-random number generator**, to be used for test pattern generation. The random number generator uses a linear feedback shift Register approach. The block diagram of the generator is shown in the Figure below.




The goal of the project is ***ULTIMATE SPEED*** and nothing else. This means that you should minimize the clock period to the maximum extent. Area and Power are not an issue in this project. Based on the course contents. Choose a suitable CMOS implementation style for the design, including but not limited to complementary CMOS, pass-transistor logic, CPL, and dynamic logic. Suggest a good mix of the logic families in your design. All complimentary signals must be internally generated, any number of levels of logic may be used. Registers can be dynamic or static. Then select a suitable clocking strategy of your design such as: (single-phase, two-phase, ...). ***MAKE SURE, HOWEVER, THAT RACES DO NOT OCCUR***.

- Several ***CONSTRAINTS*** must be considered:
  1) A power supply of $3.3\ V$ should be used.
  2) The output signals should settle to within 10% of their final value before the next clock event can be introduced.
  3) Each output bit of the generator should have a $50\ fF$ load.
  4) You are given a primary clock signal with a rise and fall time of $200\ ps$ and a duty cycle of $50\%$. All other clock signals should be derived from this primary signal using actual logic (e.g., complementary clocks, non-overlapping clocks, clocks with a faster rise and fall time, etc.).

- ***DELIVERABLES*** must be submitted (Please, follow the attached submission template):
  1) Screenshots of the schematic diagram and TB
  2) Screenshot of the waveform viewer showing CLK, A [3:0], and XOR output
  3) Screenshot of the Layout (use Manhattan routing technique).
  4) Screenshots of DRC, LVS, and PEX reports.
  5) Screenshot of the waveform viewer for the post layout simulation