CENTER OF NANOELECTRONICS & DEVICES

CND 221: Advanced Full Custom VLSI Design

Assignment #: 01

Section #: 21

Submitted by:

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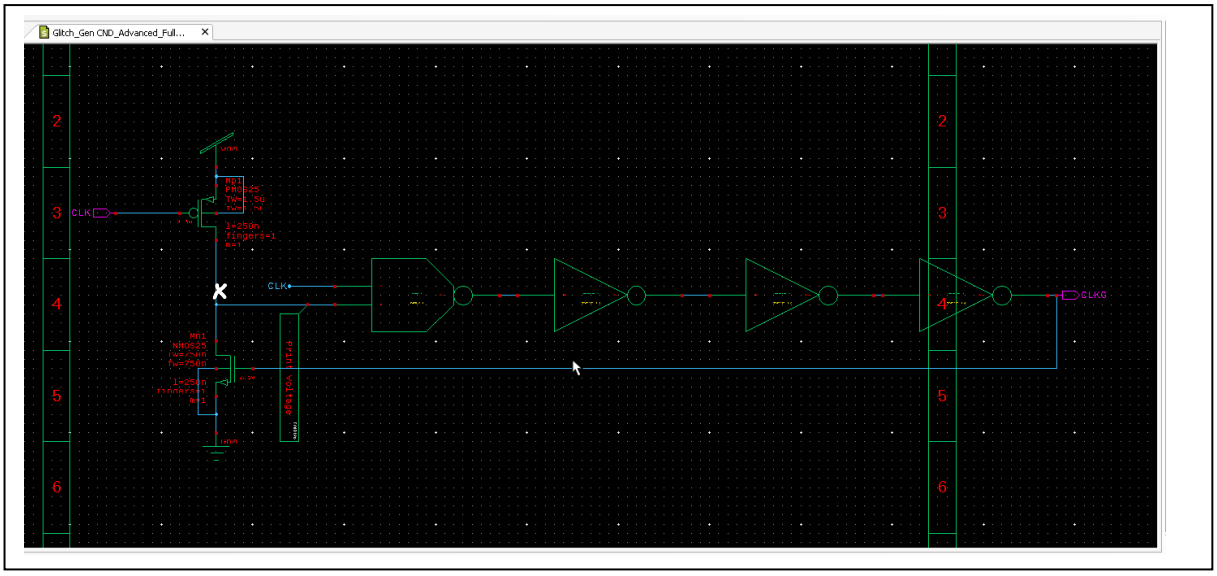
Date: ----------

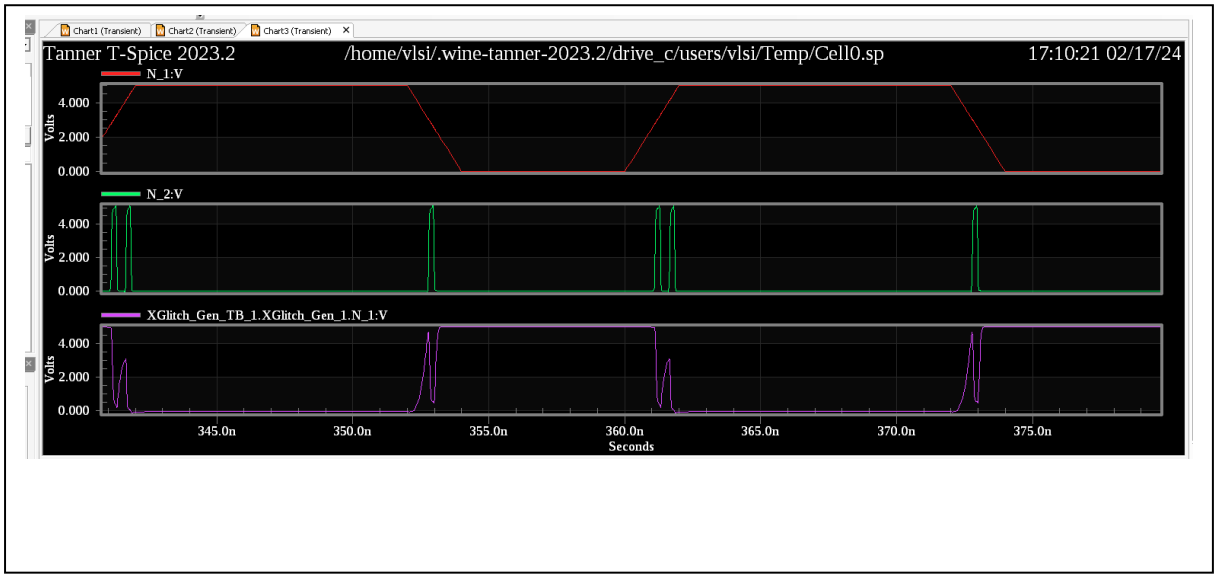
1. Glitch Circuit

- Change the period of the CLK Vpulse source in the Glitch Circuit to be = 20n.
- Change the rise and the fall time to be 20% of the pulse width (i.e. pulse width = 10n).
- Run the TB of the glitch circuit using the default transistor sizing

i. Add screenshot from your **schematic:**



ii. Add screenshot from your waveform viewer for the CLK, CLKG, D and Q. **(Note Zoom In to show how many glitches done @ one complete CLK cycle).**



iii. Decrease the setup/fall time of the Vpulse to be 10% and 5% of the pulse width then add screenshot from the waveform viewer?

iv. Analyze the previous waveforms and give your comments?

Initially CLKG is LOW

When CLK us low, node X is charged up to Vdd (Mn off when ClkG low initially)

During rising edge of CLK, for a short time both inputs of AND gate to go HIGH thereby making CLKG HIGH

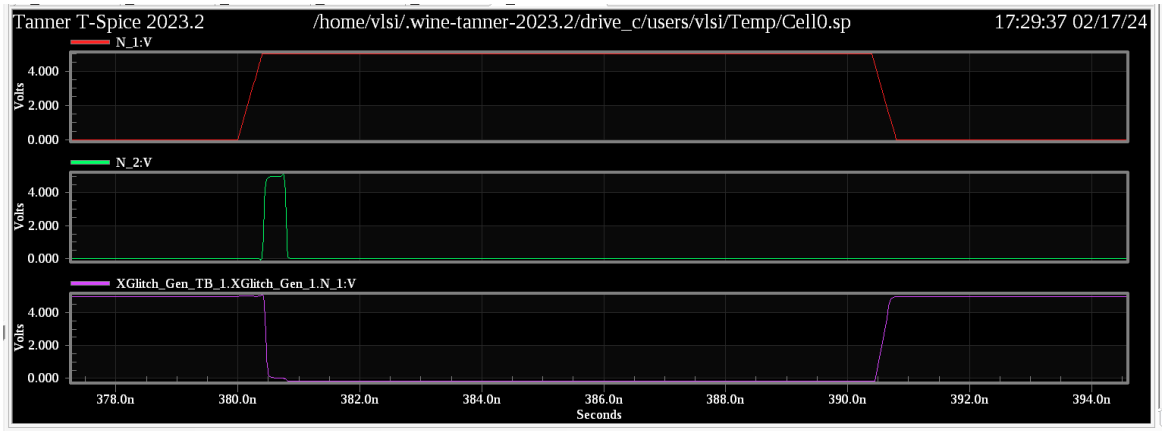
When CLKG is HIGH, Mn is ON, thereby pulling node X to GND, AND gate o/p is LOW, thereby making CLKG LOW.

The cycle repeats for next rising edge of the CLK

The CLKG pulse duration depends on the delay of the AND gate and delay of the two inverters

When decreasing the rise and fall time it decreases the time when both AND gate inputs high so it decrease the time the X node fluctuates to create the pulse

v. Add two extra buffering stages (each one contains two cascaded inverters) to the glitch circuit (with 2% setup/fall time). Compare between the new CLKG and the old one?



When adding buffering stages it increases the delay of which the Mn to be ON which increases the pulse duration as the pulse duration is the delay of the and gate and the inverters

2. BONUS

i. In the Pulse Reg TB, make a slight change to D input for a very small period (acting as a glitch). Make sure that this period$\leq 100ps$ and it is sampled with the CLKG. Take a screenshot for the Q output and compare it with the previous case with 2% setup/fall time.

Explanation? ……..