CENTER OF NANOELECTRONICS & DEVICES

CND 212: Digital Testing and Verification

Assignment #: 02

Section #: 21

Submitted by:

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```
1
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8
9   // Design
10
11  module arb (arb_int.dut intfx);
12
13    always @ (posedge intfx.clk or posedge intfx.rst )
14      begin
15        if (intfx.rst )
16          intfx.grand <= 'b0;
17        else if ( intfx.request[0] )
18         intfx.grand <= 'b01;
19        else if ( intfx.request[1] )
20           intfx.grand <= 'b10;
21        else
22           intfx.grand <= 'b0;
23
24      end
25  endmodule
```

```
1
2
3
4
5
6
7   // testbench
8
9
10  module testbench ( arb_int.tb intfy );
11    initial
12      begin
13
14         $dumpfile ("dd.vcd");
15         $dumpvars;
16         @(intfy.cb)
17        intfy.rst= 1;
18         intfy.cb.request <= 'b10;
19
20      /*   if ( !(intfy.cb.grand) )
21             $display ( "no error" );
22           else */
23         $display ( intfy.cb.grand );
24
25
26          @(intfy.cb)
27         intfy.rst= 0;
28        // intfy.cb.request<= 'b01;
29
30         /*if ( intfy.cb.grand == 'b01 )
31            $display ( "no error" );
32           else
33             $display ( "error" );*/
34           $display ( intfy.cb.grand );
35          intfy.cb.request<= 'b01;
36
37
38          @(intfy.cb)
39
40           $display ( intfy.cb.grand );
41
42          @(intfy.cb)
43
44           $display ( intfy.cb.grand );
45
46
47         /*     intfy.rst= 0;
48         intfy.cb.request<= 'b10;
49
50
51         if ( intfy.cb.grand == 'b10 )
52            $display ( "no error" );
53           else
54             $display ( "error" );             */
55
56         $finish;
57       end
58
59
60
61  endmodule
62
63  // top
64
65  module top;
66     bit clk;
67    arb_int int_top (clk);
68
69
```

```
70    always #10 clk = ~clk ;
71
72    testbench tb ( int_top ) ;
73    arb dut (int_top ) ;
74
75  endmodule
76
77
78  // interface
79
80  interface arb_int ( input clk  ) ;
81
82    logic [1:0] request;
83    logic [1:0] grand ;
84    logic rst;
85
86    clocking cb @ ( posedge clk );
87      default input #2 output #0 ;
88      output  request ;
89      input grand ;
90    endclocking
91
92    modport tb ( output rst , clocking cb);
93
94      modport dut ( input clk,input  rst , input request ,output grand );
95
96  endinterface
```

```
 the VCS_LIC_EXPIRE_WARNING environment variable to the number of days
before expiration that you want this message to start (the minimum is 0).
x
0
0
1
$finish called from file "testbench.sv", line 50.
$finish at simulation time                   70
           V C S   S i m u l a t i o n   R e p o r t
Time: 70 ns
CPU Time:      0.480 seconds;       Data structure size:   0.0Mb
Fri Mar 15 16:47:43 2024
Done
```