

CND 221: Advanced Full Custom VLSI

Design

MidTerm Exam

Section #: 21

Submitted by:

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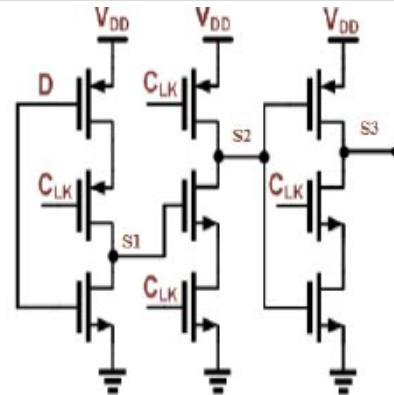
Date: -----

Pseudo-random number generator

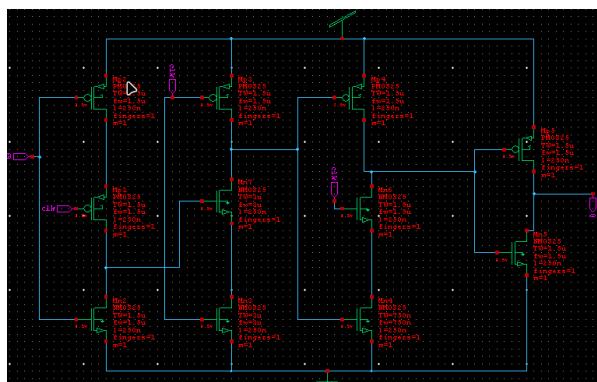
- Add 1 paragraph describes your design and elements that you used:

the D-Flip Flop is designed to be with True Single Phase Clock Technique. True Single Phase Clock has the advantages of simple and compact clock distribution, high speed and logic design flexibility . There is no clock skew problem because it uses single clock phase.

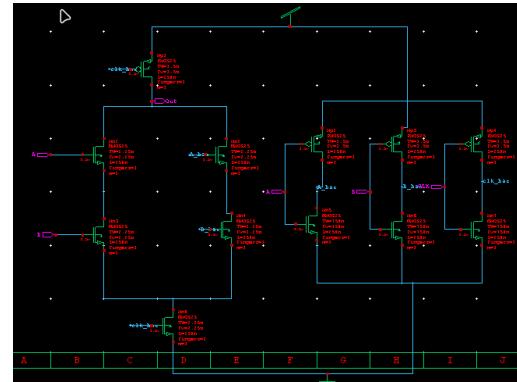
and the XOR is designed with Dynamic CMOS implementation in mind as we are targeting high speed application and disregarding the other aspects of power and area.



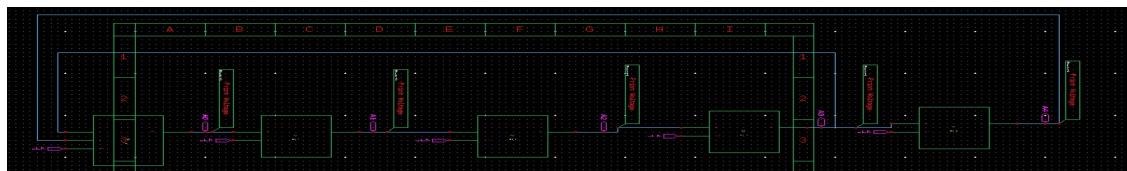
- Add a screenshot from your schematic:



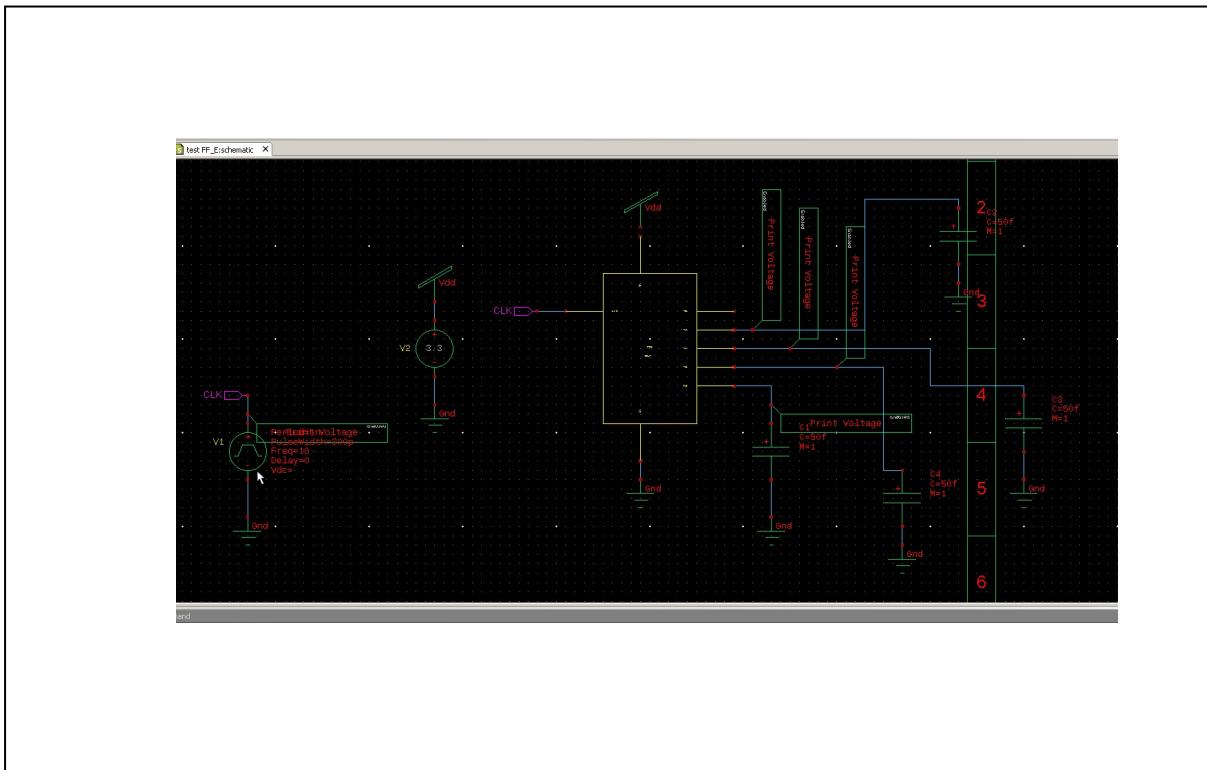
D-Flip Flop



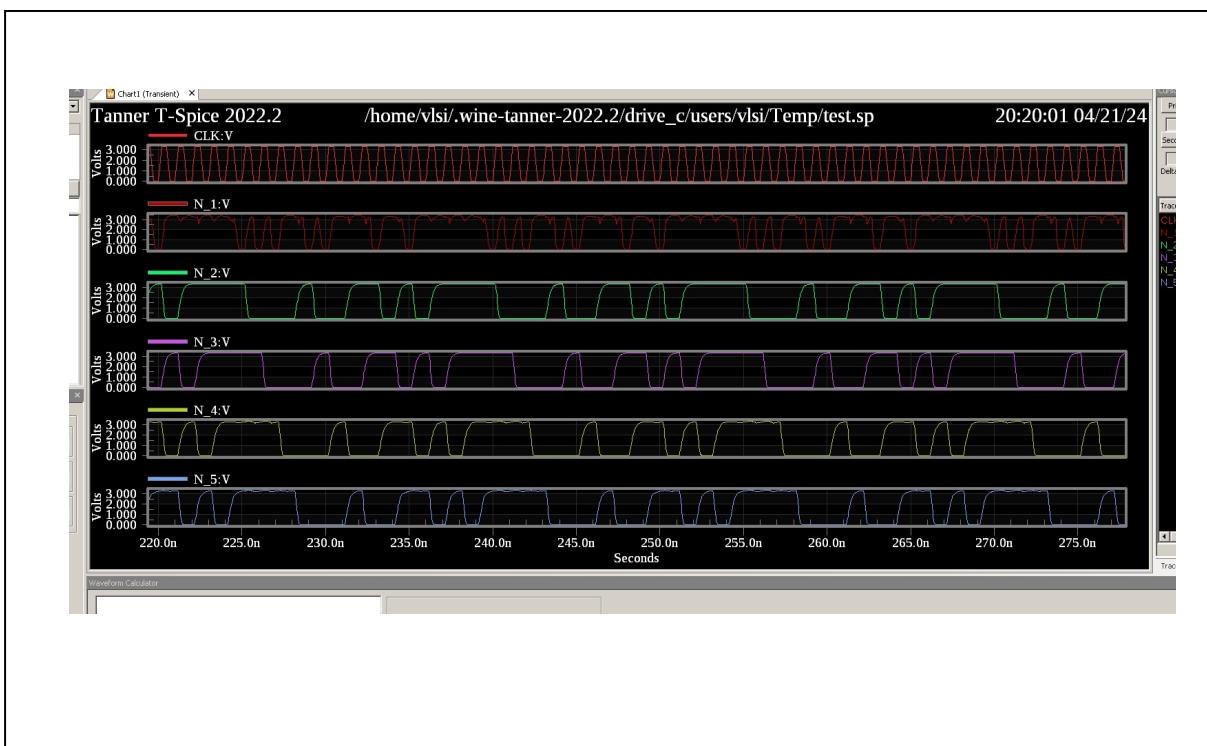
XOR



iii. Add a screenshot for your Testbench



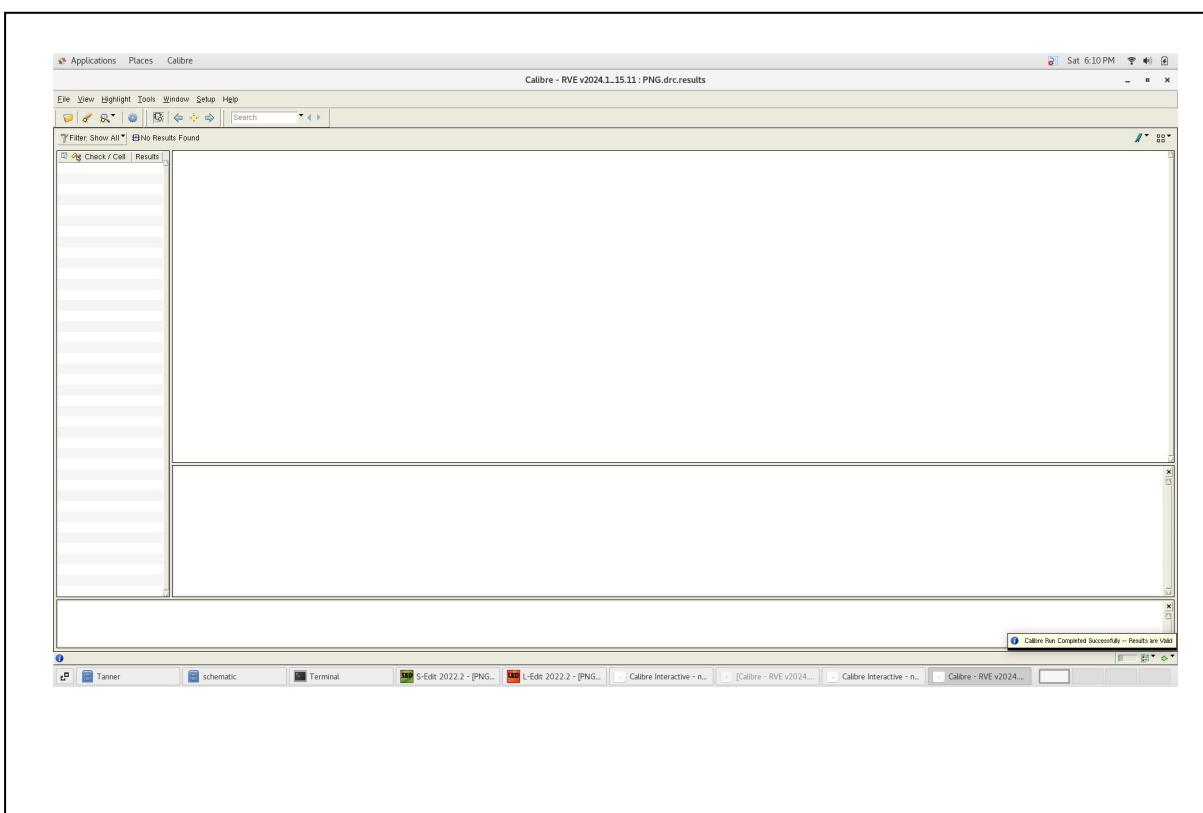
iv. Add a screenshot from your waveform viewer for the CLK, A[3:0], and Output of the XOR gate. (**Note Zoom In to show at least 6 CLK cycles**).



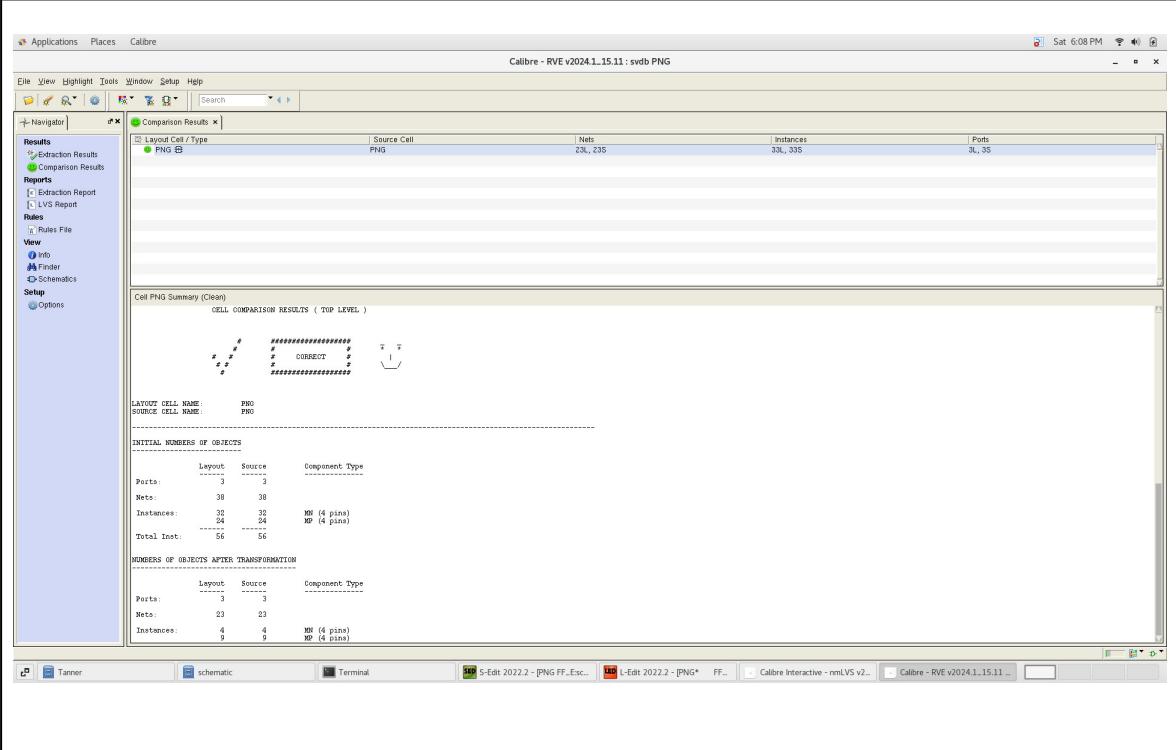
v. Add a screenshot from your Layout?



vi. Add a screenshot of the DRC report?



vii. Add a screenshot of the LVS report?



| Layout Cell / Type | Source Cell | Nets | Instances | Ports |
|--------------------|-------------|----------|-----------|--------|
| PNG | PNG | 238, 235 | 335, 335 | 30, 35 |

Cell PNG Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

LAYOUT CELL NAME: P00
SOURCE CELL NAME: P00

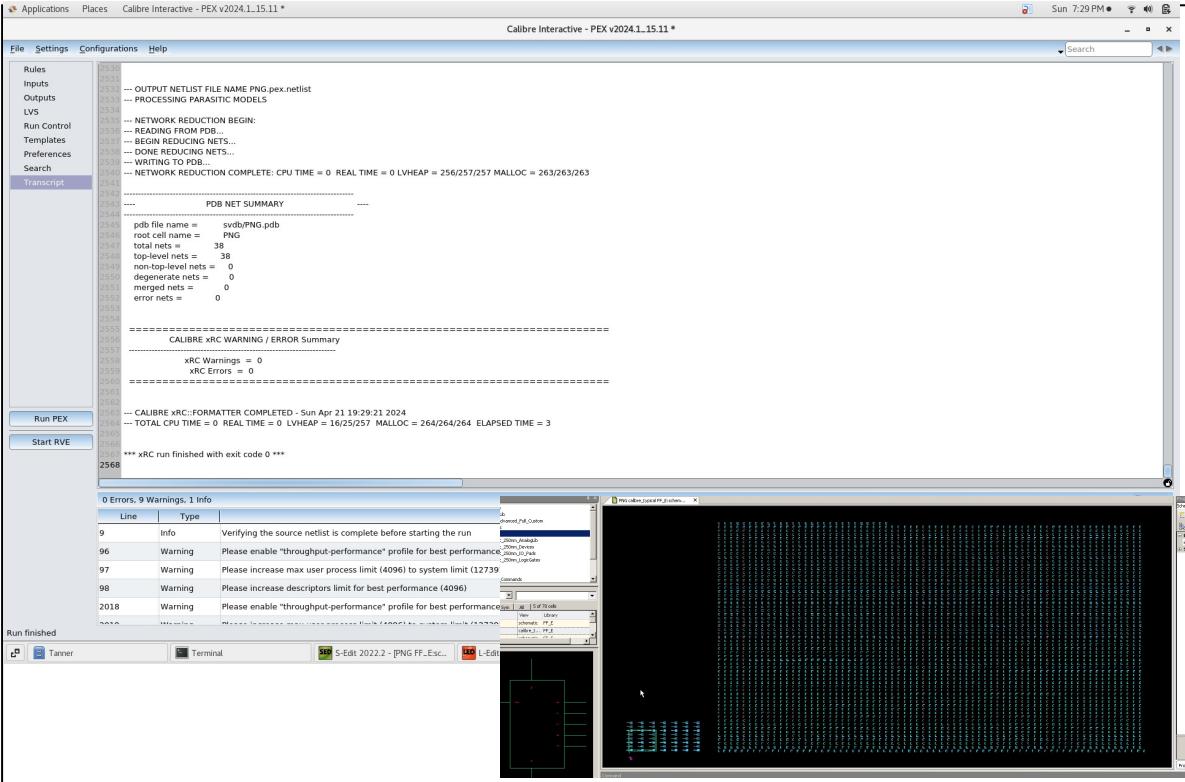
INITIAL NUMBERS OF OBJECTS

| Layout | Source | Component Type |
|-------------|--------|----------------|
| Ports: | 4 | 3 |
| Nets: | 30 | 38 |
| Instances: | 32 | 32 |
| | 24 | 24 |
| Total Inst. | 56 | 56 |

NUMBERS OF OBJECTS AFTER TRANSFORMATION

| Layout | Source | Component Type |
|-------------|--------|----------------|
| Ports: | 3 | 3 |
| Nets: | 23 | 23 |
| Instances: | 4 | 4 |
| | 9 | 9 |
| Total Inst. | 56 | 56 |

viii. Add a screenshot for PEX.



```

2530
2531 --- OUTPUT NETLIST FILE NAME PNG.pex.netlist
2532 --- PROCESSING PARASITIC MODELS
2533
2534 --- NETWORK REDUCTION BEGIN:
2535 --- READING FROM PDB...
2536 --- BEGIN REDUCING NETS...
2537 --- DONE REDUCING NETS...
2538 --- WRITING TO PDB...
2539 --- NETWORK REDUCTION COMPLETE: CPU TIME = 0 REAL TIME = 0 LVHEAP = 256/257/257 MALLOC = 263/263/263
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2544
2545 PDB NET SUMMARY
2546 pdb file name = svdb/PNG.pdb
2547 tool name = PNG
2548 total nets = 38
2549 top-level nets = 38
2549 non-top-level nets = 0
2550 degenerate nets = 0
2551 merged nets = 0
2552 error nets = 0
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2555 =====
2556 CALIBRE XRC WARNING / ERROR Summary
2557
2558 xRC_Warnings = 0
2559 xRC_Errors = 0
2560 =====
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2564 --- CALIBRE XRC:FORMATTER COMPLETED - Sun Apr 21 19:29:21 2024
2565 --- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 16/25/257 MALLOC = 264/264/264 ELAPSED TIME = 3
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2567 *** xRC run finished with exit code 0 ***
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ix. Add a screenshot to the waveform viewer for post layout simulation.

