CND: testing and verification

project

Mid-term

Section #: 21

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1. Top module:

D:/New folder (4)/top_FIFO.sv - Default

```
Ln#
 1  module top_FIFO();
 2    parameter  ADDR_WIDTH = 5;
 3    parameter  DATA_WIDTH = 32;
 4    parameter  fifo_size  =2**ADDR_WIDTH;
 5    bit clk;
 6
 7  //clock generation
 8   initial begin
 9     forever #1 clk=~clk;
10   end
11
12  //interface instance
13  intf_FIFO #( DATA_WIDTH,ADDR_WIDTH, fifo_size)
14       intf_inst (clk);
15
16
17  //FIFO INSTANCE
18  FIFO #( ADDR_WIDTH,DATA_WIDTH, fifo_size)
19        FIFO_inst(.clk          (intf_inst.clk),
20                  .data_in      (intf_inst.data_in),
21                  .data_out     (intf_inst.data_out),
22                  .Read_enable  (intf_inst.Read_enable),
23                  .Wr_enable   (intf_inst.Wr_enable),
24                  .full         (intf_inst.full),
25                  .empty        (intf_inst.empty),
26                  .reset        (intf_inst.reset));
27
28  //test_bench instance
29  tb_FIFO test_inst(intf_inst.TB);
30
31  endmodule
```

2. interface file:

D:/New folder (4)/intf_FIFO.sv - Default

```
Ln#
1  interface intf_FIFO #(parameter  DATA_WIDTH = 32,ADDR_WIDTH = 5,fifo_size =2**ADDR_WIDTH) ( input clk);
2
3
4    logic reset;
5    logic  [DATA_WIDTH-1:0] data_in ;
6    logic  [DATA_WIDTH-1:0] data_out ;
7    logic Wr_enable;
8    logic Read_enable;
9    logic full,empty;
10
11
12 // Clocking block for synchronous operations
13 clocking clk_b @(posedge clk) ;
14
15     output data_in;
16     output Wr_enable;
17     output Read_enable;
18     input data_out;
19   endclocking
20 modport TB (clocking clk_b, input full , empty ,data_out, output reset ,data_in ,Wr_enable,Read_enable);
21 endinterface
```

3. package that contain class and constraints :

D:/New folder (4)/pck.sv - Default

```
Ln#
1  package my_pck;
2
3  class randomization  #(DATA_WIDTH = 32);
4    rand  bit Wr_enable,Read_enable;
5    rand  bit  [DATA_WIDTH -1:0] data_in;
6
7
8    constraint n1 { data_in[7:0] inside {[100:230]}; }
9    constraint n2 { data_in[15:8] inside {[200:255]}; }
10   constraint n3 { data_in [23:16] dist{ [0:100]:=30,[100:200]:=60,[200:255]:=10};}
11   constraint n4 { Wr_enable dist {0:=40, 1:=60};
12                   Wr_enable==!Read_enable;
13                 }
14   constraint n5 {
15     if (data_in[7:0] > 150)
16      data_in[31:24] inside {[0:50]};
17     else
18       data_in[31:24] inside {[0:255]};
19   }
20
21
22  endclass
23 endpackage
```

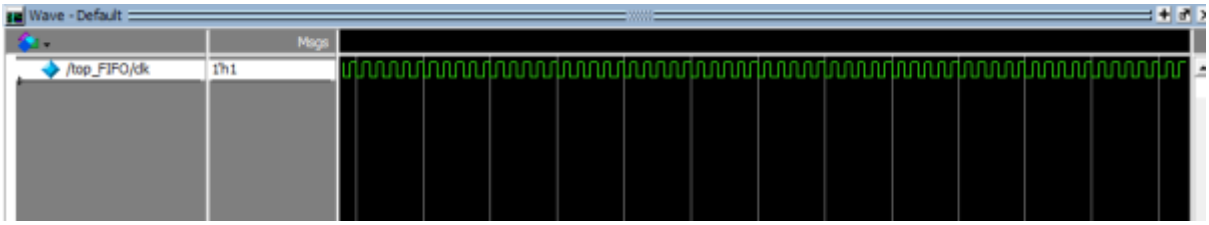
4. test_bench:

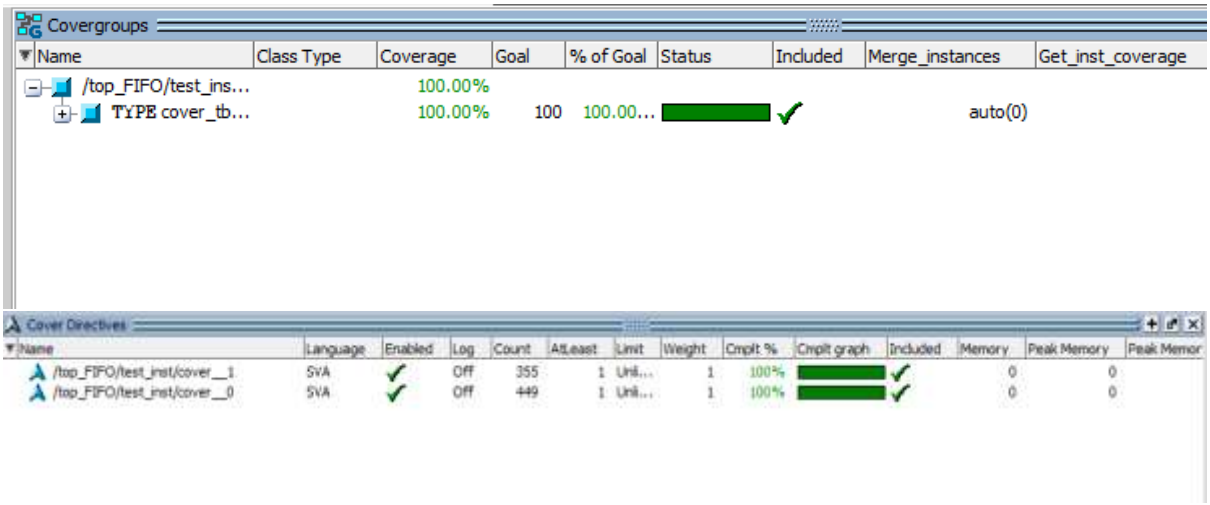
D:/New folder (4)/tb_FIFO.sv - Default

```
Ln#
 1
 2  import my_pck ::*;
 3
 4  module tb_FIFO (intf_FIFO intf_inst);
 5
 6   integer i;
 7
 8   randomization a=new();
 9
10   //coveragegroup
11   covergroup cover_tb @intf_inst.clk_b ;
12     coverpoint intf_inst.full;
13     coverpoint intf_inst.empty;
14   endgroup
15
16  cover_tb cov=new();
17
18   initial begin
19    intf_inst.reset=0; #1;
20    intf_inst.reset=1; #1;
21
22     for(i=0;i<1000;i++) begin
23
24        intf_inst.reset=0;
25        assert (a.randomize());
26        intf_inst.Wr_enable=   a.Wr_enable;
27        intf_inst.Read_enable= a.Read_enable;
28        intf_inst.data_in=     a.data_in;
29        @intf_inst.clk_b ;
30
31     end
32   $stop;
```

```
cover_tb cov=new();

 initial begin
  intf_inst.reset=0; #1;
  intf_inst.reset=1; #1;

   for(i=0;i<1000;i++) begin

      intf_inst.reset=0;
      assert (a.randomize());
      intf_inst.Wr_enable=   a.Wr_enable;
      intf_inst.Read_enable= a.Read_enable;
      intf_inst.data_in=     a.data_in;
      @intf_inst.clk_b ;

   end
  $stop;
 end


//assertions

assert property (@(intf_inst.clk_b) disable iff(intf_inst.reset)(intf_inst.Wr_enable && !intf_inst.full) |=> (FIFO_inst.write_ptr)==$past(FIFO_inst.write_ptr)+1'd1);
cover property  (@(intf_inst.clk_b) disable iff(intf_inst.reset)(intf_inst.Wr_enable && !intf_inst.full) |=> (FIFO_inst.write_ptr)==$past(FIFO_inst.write_ptr)+1'd1);

//bonus

assert property (@(intf_inst.clk_b) disable iff(intf_inst.reset)(intf_inst.data_in [7:0] > 8'd150) |-> ((intf_inst.data_in[31:24] >= 8'd0) && (intf_inst.data_in [31:24] <=8'd50)));
cover property  (@(intf_inst.clk_b)disable iff(intf_inst.reset)(intf_inst.data_in [7:0] > 8'd150) |-> ((intf_inst.data_in[31:24] >= 8'd0) && (intf_inst.data_in [31:24] <=8'd50)));

endmodule
```

5. Waveform:





6. Do file

```
vlib work
vlog FIFO.v tb_FIFO.sv   +cover
vsim -voptargs=+acc work.top_FIFO -cover
add wave *
coverage save top_FIFO.ucdb -onexit
vcover report top_FIFO.ucdb -details -all -annotate -output report.txt
run -all
```

7. Report :

```
Coverage Report by instance with details

================================================================================
=== Instance: /top_FIFO/FIFO_inst
=== Design Unit: work.FIFO
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         6         6         0   100.00%

================================Branch Details================================

Branch Coverage for instance /top_FIFO/FIFO_inst

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File FIFO.v
------------------------------------IF Branch------------------------------------
    22                                      1001     Count coming in to IF
    22              1                          1              if(reset) begin

    28              1                        449        else if( Wr_enable && ~full) begin

                                             551     All False Count
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    37                                      895     Count coming in to IF
    37              1                          1              if(reset) begin

    42              1                        386              else if( Read_enable && ~empty) begin

                                             508     All False Count
Branch totals: 3 hits of 3 branches = 100.00%
```

```
Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                       4         4         0   100.00%

================================Condition Details================================

Condition Coverage for instance /top_FIFO/FIFO_inst --

  File FIFO.v
----------------Focused Condition View-------------------
Line       28 Item    1  (Wr_enable && ~full)
Condition totals: 2 of 2 input terms covered = 100.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  -----------------------  --------------
   Wr_enable         Y
        full         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  Wr_enable_0           -
  Row   2:          1  Wr_enable_1           ~full
  Row   3:          1  full_0                Wr_enable
  Row   4:          1  full_1                Wr_enable

----------------Focused Condition View-------------------
Line       42 Item    1  (Read_enable && ~empty)
Condition totals: 2 of 2 input terms covered = 100.00%

   Input Term   Covered  Reason for no coverage   Hint
  -----------  --------  -----------------------  --------------
  Read_enable         Y
        empty         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
```

```
     Rows:       Hits  FEC Target              Non-masking condition(s)
 ---------  ---------  --------------------    -------------------------
  Row    1:          1  Read_enable_0           -
  Row    2:          1  Read_enable_1           ~empty
  Row    3:          1  empty_0                 Read_enable
  Row    4:          1  empty_1                 Read_enable

Expression Coverage:
    Enabled Coverage              Bins    Covered    Misses  Coverage
    ----------------              ----    -------    ------  --------
    Expressions                      2          2         0   100.00%

================================Expression Details================================

Expression Coverage for instance /top_FIFO/FIFO_inst --

  File FIFO.v
----------------Focused Expression View-----------------
Line       18 Item    1  (write_ptr == read_ptr)
Expression totals: 1 of 1 input term covered = 100.00%

               Input Term   Covered  Reason for no coverage   Hint
              -----------  --------  ----------------------  --------------
  (write_ptr == read_ptr)         Y

     Rows:       Hits  FEC Target                 Non-masking condition(s)
 ---------  ---------  --------------------       -------------------------
  Row    1:          1  (write_ptr == read_ptr)_0  -
  Row    2:          1  (write_ptr == read_ptr)_1  -

----------------Focused Expression View-----------------
Line       19 Item    1  (read_ptr == (write_ptr + 1))
Expression totals: 1 of 1 input term covered = 100.00%

                     Input Term   Covered  Reason for no coverage   Hint
                    -----------  --------  ----------------------  --------------
```

```
                     Input Term   Covered  Reason for no coverage   Hint
                    -----------  --------  ----------------------  --------------
  (read_ptr == (write_ptr + 1))         Y

     Rows:       Hits  FEC Target                       Non-masking condition(s)
 ---------  ---------  --------------------             -------------------------
  Row    1:          1  (read_ptr == (write_ptr + 1))_0  -
  Row    2:          1  (read_ptr == (write_ptr + 1))_1  -


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      14        14         0   100.00%

================================Statement Details================================

Statement Coverage for instance /top_FIFO/FIFO_inst --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File FIFO.v
    1                                                module FIFO #(parameter

    2                                                    ADDR_WIDTH           = 5,

    3                                                    DATA_WIDTH           = 32,

    4                                                    fifo_size            =2**ADDR_WIDTH

    5                                                  )(

    6                                                  input clk,

    7                                                    input reset,
```

```
7                                       input reset,
8                                       input Wr_enable,
9                                      input reg [DATA_WIDTH-1:0] data_in,
10                                      input Read_enable,
11                                      output full,
12                                      output empty,
13                                     output reg [DATA_WIDTH-1:0] data_out
14                                     );
15                                      reg  [DATA_WIDTH-1:0] FIFO  [fifo_size-1:0] ;
16                                      reg [ADDR_WIDTH-1:0] write_ptr,read_ptr;
17
18          1           837             assign empty   = ( write_ptr == read_ptr ) ? 1'b1 : 1'b0;
19          1           837             assign full    = ( read_ptr == (write_ptr+1) ) ? 1'b1 : 1'b0;
20                                    integer i;
21          1          1001             always @ (posedge clk , posedge reset) begin
22                                          if(reset) begin
23          1             1              for(i=0;i<fifo_size;i=i+1) begin
23          2            32
24          1            32                 FIFO[i]<=0;

24          1            32                 FIFO[i]<=0;
25                                         end
26          1             1               write_ptr <=0;
27                                        end
28                                     else if( Wr_enable && ~full) begin
29          1           449                 FIFO[write_ptr] <= data_in;
30          1           449                   write_ptr <= write_ptr + 1;
31                                        end
32
33                                    end
34
35          1           895             always @ (posedge clk, posedge reset) begin
36
37                                        if(reset) begin
38          1             1               data_out <= 0;
39          1             1               read_ptr <= 0;
40                                        end
41
42                                        else if( Read_enable && ~empty) begin
```

```
    41
    42                                                  else if( Read_enable && ~empty) begin
    43              1                       386                 data_out <= FIFO[read_ptr];
    44              1                       386                 read_ptr <= read_ptr + 1;

Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                        224       154        70    68.75%

================================Toggle Details================================

Toggle Coverage for instance /top_FIFO/FIFO_inst --

                                          Node      1H->0L      0L->1H  "Coverage"
                                          ----------------------------------------
                                    Read_enable           1           1      100.00
                                      Wr_enable           1           1      100.00
                                             clk          1           1      100.00
                                   data_in[0-13]          1           1      100.00
                                  data_in[14-15]          0           0        0.00
                                  data_in[16-31]          1           1      100.00
                                 data_out[31-16]          1           1      100.00
                                 data_out[15-14]          0           1       50.00
                                  data_out[13-0]          1           1      100.00
                                           empty          1           1      100.00
                                            full          1           1      100.00
                                          i[31-0]          0           0        0.00
                                   read_ptr[4-0]          1           1      100.00
                                           reset          1           1      100.00
                                  write_ptr[4-0]          1           1      100.00

Total Node Count     =        112
```

```
Total Node Count     =        112
Toggled Node Count   =         76
Untoggled Node Count =         36

Toggle Coverage      =      68.75% (154 of 224 bins)

================================================================================
=== Instance: /top_FIFO/test_inst
=== Design Unit: work.tb_FIFO
================================================================================

Assertion Coverage:
    Assertions                       3         3         0   100.00%
--------------------------------------------------------------------
Name                 File(Line)                   Failure      Pass
                                                  Count        Count
--------------------------------------------------------------------
/top_FIFO/test_inst/assert__1
                     tb_FIFO.sv(43)                     0          1
/top_FIFO/test_inst/assert__0
                     tb_FIFO.sv(38)                     0          1
/top_FIFO/test_inst/#ublk#176401887#22/immed__25
                     tb_FIFO.sv(25)                     0          1

Covergroup Coverage:
    Covergroups                      1        na        na   100.00%
        Coverpoints/Crosses          2        na        na        na
            Covergroup Bins          4         4         0   100.00%
----------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status

----------------------------------------------------------------------------------------------------
 TYPE /top_FIFO/test_inst/cover_tb                 100.00%        100          -    Covered
    covered/total bins:                                  4          4          -
    missing/total bins:                                  0          4          -
    % Hit:                                         100.00%        100          -
```

```
----------------------------------------------------------------------------------------------------
 TYPE /top_FIFO/test_inst/cover_tb                100.00%        100         -    Covered
    covered/total bins:                             4          4         -
    missing/total bins:                             0          4         -
    % Hit:                                       100.00%       100         -
    Coverpoint #coverpoint__0#                   100.00%       100         -    Covered
        covered/total bins:                         2          2         -
        missing/total bins:                         0          2         -
        % Hit:                                   100.00%       100         -
    Coverpoint #coverpoint__1#                   100.00%       100         -    Covered
        covered/total bins:                         2          2         -
        missing/total bins:                         0          2         -
        % Hit:                                   100.00%       100         -
 Covergroup instance \/top_FIFO/test_inst/cov    100.00%       100         -    Covered
    covered/total bins:                             4          4         -
    missing/total bins:                             0          4         -
    % Hit:                                       100.00%       100         -
    Coverpoint #coverpoint__0#                   100.00%       100         -    Covered
        covered/total bins:                         2          2         -
        missing/total bins:                         0          2         -
        % Hit:                                   100.00%       100         -
        bin auto[0]                               750          1         -    Covered
        bin auto[1]                               251          1         -    Covered
    Coverpoint #coverpoint__1#                   100.00%       100         -    Covered
        covered/total bins:                         2          2         -
        missing/total bins:                         0          2         -
        % Hit:                                   100.00%       100         -
        bin auto[0]                               991          1         -    Covered
        bin auto[1]                                10          1         -    Covered

Directive Coverage:
    Directives                      2         2         0   100.00%

DIRECTIVE COVERAGE:
```

bin auto[1] 10 1 - Covered

Directive Coverage:
Directives 2 2 0 100.00%

DIRECTIVE COVERAGE:

```
----------------------------------------------------------------------------------------------
Name                                    Design Design   Lang File(Line)      Hits Status
                                        Unit   UnitType
----------------------------------------------------------------------------------------------
/top_FIFO/test_inst/cover__1            tb_FIFO Verilog  SVA  tb_FIFO.sv(44)   355 Covered
/top_FIFO/test_inst/cover__0            tb_FIFO Verilog  SVA  tb_FIFO.sv(39)   449 Covered
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      14        14         0   100.00%
```

```
----------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status
----------------------------------------------------------------------------------------------------
 TYPE /top_FIFO/test_inst/cover_tb                 100.00%        100          -    Covered
    covered/total bins:                                  4          4          -
    missing/total bins:                                  0          4          -
    % Hit:                                         100.00%        100          -
    Coverpoint #coverpoint__0#                     100.00%        100          -    Covered
        covered/total bins:                              2          2          -
        missing/total bins:                              0          2          -
        % Hit:                                     100.00%        100          -
    Coverpoint #coverpoint__1#                     100.00%        100          -    Covered
        covered/total bins:                              2          2          -
        missing/total bins:                              0          2          -
        % Hit:                                     100.00%        100          -
 Covergroup instance \/top_FIFO/test_inst/cov      100.00%        100          -    Covered
    covered/total bins:                                  4          4          -
    missing/total bins:                                  0          4          -
    % Hit:                                         100.00%        100          -
    Coverpoint #coverpoint__0#                     100.00%        100          -    Covered
        covered/total bins:                              2          2          -
        missing/total bins:                              0          2          -
        % Hit:                                     100.00%        100          -
        bin auto[0]                                    750          1          -    Covered
        bin auto[1]                                    251          1          -    Covered
    Coverpoint #coverpoint__1#                     100.00%        100          -    Covered
        covered/total bins:                              2          2          -
        missing/total bins:                              0          2          -
        % Hit:                                     100.00%        100          -
        bin auto[0]                                    991          1          -    Covered
        bin auto[1]                                     10          1          -    Covered

TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 1

DIRECTIVE COVERAGE:



        % Hit:                                     100.00%        100          -
        bin auto[0]                                    750          1          -    Covered
        bin auto[1]                                    251          1          -    Covered
    Coverpoint #coverpoint__1#                     100.00%        100          -    Covered
        covered/total bins:                              2          2          -
        missing/total bins:                              0          2          -
        % Hit:                                     100.00%        100          -
        bin auto[0]                                    991          1          -    Covered
        bin auto[1]                                     10          1          -    Covered

TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 1

DIRECTIVE COVERAGE:
----------------------------------------------------------------------------------------------------
Name                                    Design Design   Lang File(Line)      Hits Status
                                        Unit   UnitType
----------------------------------------------------------------------------------------------------
/top_FIFO/test_inst/cover__1            tb_FIFO Verilog  SVA  tb_FIFO.sv(44)   355 Covered
/top_FIFO/test_inst/cover__0            tb_FIFO Verilog  SVA  tb_FIFO.sv(39)   449 Covered

TOTAL DIRECTIVE COVERAGE: 100.00%  COVERS: 2

ASSERTION RESULTS:
--------------------------------------------------------------------
Name                File(Line)                   Failure      Pass
                                                 Count        Count
--------------------------------------------------------------------
/top_FIFO/test_inst/assert__1
                    tb_FIFO.sv(43)                     0          1
/top_FIFO/test_inst/assert__0
                    tb_FIFO.sv(38)                     0          1
/top_FIFO/test_inst/#ublk#176401887#22/immed__25
                    tb_FIFO.sv(25)                     0          1

Total Coverage By Instance (filtered view): 95.00%
```