

## 2023 Digital IC Design Homework 1

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<b>Functional Simulation Result</b>							
Stage 1	Pass/Fail	Stage 2	Pass/Fail	Stage 3	Pass/Fail	Stage 4	Pass/Fail
<b>Stage 1</b>							
<pre> # -----Stage 1 : Maximum selection with 4-input MMS----- # # -----Stage 1 :                Pass!                ----- # </pre>							
<b>Stage 2</b>							
<pre> # -----Stage 2 : Minimum selection with 4-input MMS----- # # -----Stage 2 :                Pass!                ----- # </pre>							
<b>Stage 3</b>							
<pre> # -----Stage 3 : Maximum selection with 8-input MMS----- # # -----Stage 3 :                Pass!                ----- # </pre>							
<b>Stage 4</b>							
<pre> # -----Stage 4 : Minimum selection with 8-input MMS----- # # -----Stage 4 :                Pass!                ----- # </pre>							
<b>Description of your design</b>							

```

MMS_4num.v X
MMS_4num.v
1 module MMS_4num(result, select, number0, number1, number2, number3);
2
3 input      select;
4 input [7:0] number0;
5 input [7:0] number1;
6 input [7:0] number2;
7 input [7:0] number3;
8 output [7:0] result;
9
10 /*
11 |   Write Your Design Here ~
12 */
13 wire [7:0] temp1, temp2;
14 assign temp1 = ((number0 < number1) ^ select) ? number1 : number0;
15 assign temp2 = ((number2 < number3) ^ select) ? number3 : number2;
16 assign result = ((temp1 < temp2) ^ select) ? temp2 : temp1;
17
18
19 endmodule

```

Verilog code of **MMS\_4num**.

```

MMS_4num.v MMS_8num.v X
MMS_8num.v
1 `include "MMS_4num.v"
2 module MMS_8num(result, select, number0, number1, number2, number3, number4,
3 | number5, number6, number7);
4
5 input      select;
6 input [7:0] number0;
7 input [7:0] number1;
8 input [7:0] number2;
9 input [7:0] number3;
10 input [7:0] number4;
11 input [7:0] number5;
12 input [7:0] number6;
13 input [7:0] number7;
14 output [7:0] result;
15
16 /*
17 |   Write Your Design Here ~
18 */
19 wire [7:0] out1, out2;
20 MMS_4num m1(out1, select, number0, number1, number2, number3);
21 MMS_4num m2(out2, select, number4, number5, number6, number7);
22 assign result = ((out1 < out2) ^ select) ? out2 : out1;
23
24 endmodule

```

Verilog code of **MMS\_8num**.

/MMS_tb/MMS_4num/select	1	
/MMS_tb/MMS_4num/number0	115	115
/MMS_tb/MMS_4num/number1	13	13
/MMS_tb/MMS_4num/number2	53	53
/MMS_tb/MMS_4num/number3	107	107
/MMS_tb/MMS_4num/result	13	13
/MMS_tb/MMS_4num/temp1	13	13
/MMS_tb/MMS_4num/temp2	53	53

Segment wave of result of **MMS\_4num**, select == 1 represented for selecting minimum, so the result will be 13.

	Msgs	
/MMS_tb/MMS_4num/select	0	
/MMS_tb/MMS_4num/number0	10	10
/MMS_tb/MMS_4num/number1	112	112
/MMS_tb/MMS_4num/number2	90	90
/MMS_tb/MMS_4num/number3	207	207
/MMS_tb/MMS_4num/result	207	207
/MMS_tb/MMS_4num/temp1	112	112
/MMS_tb/MMS_4num/temp2	207	207

Segment wave of result of **MMS\_4num**, select == 0 represented for selecting maximum, so the result will be 207.

	Msgs	
/MMS_tb/MMS_8num/select	1	
/MMS_tb/MMS_8num/number0	195	195
/MMS_tb/MMS_8num/number1	60	60
/MMS_tb/MMS_8num/number2	37	37
/MMS_tb/MMS_8num/number3	12	12
/MMS_tb/MMS_8num/number4	240	240
/MMS_tb/MMS_8num/number5	251	251
/MMS_tb/MMS_8num/number6	186	186
/MMS_tb/MMS_8num/number7	110	110
/MMS_tb/MMS_8num/result	12	12
/MMS_tb/MMS_8num/out1	12	12
/MMS_tb/MMS_8num/out2	110	110

Segment wave of result of **MMS\_8num**, select == 1 represented for selecting minimum, so the result will be 12.

