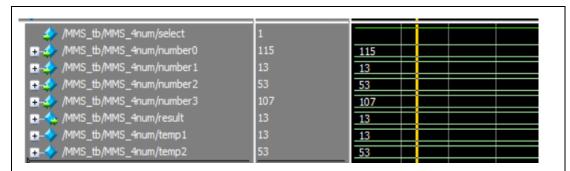
## 2023 Digital IC Design Homework 1

NAME	NAME							
Student II	Student ID N26112128							
Functional Simulation Result								
Stage 1	Pass/Fai	Stage	Pass/Fail	Stage	Pass/Fail	Stage	Pass/Fail	
2				3		4		
Stage 1								
#Stage 1 : Maximum selection with 4-input MMS #Stage 1 : Pass!								
Stage 2								
#Stage 2 : Minimum selection with 4-input MMS #Stage 2 : Pass!								
Stage 3								
#Stage 3 : Maximum selection with 8-input MMS #Stage 3 : Pass!								
Stage 4								
# # #	S1		finimum sel	ection w Pass!	ith 8-inpu	t MMS		
Description of your design								

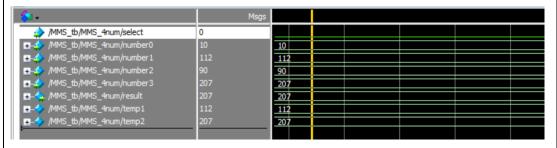
Verilog code of MMS 4num.

```
≣ MMS_8num.v X
 1 `include "MMS_4num.v"
    module MMS_8num(result, select, number0, number1, number2, number3, number4,
 3 number5, number6, number7);
                 select;
6 input [7:0] number0;
 7 input [7:0] number1;
8 input [7:0] number2;
9 input [7:0] number3;
10 input [7:0] number4;
11 input [7:0] number5;
12 input [7:0] number6;
13 input [7:0] number7;
14 output [7:0] result;
19 wire [7:0] out1, out2;
20 MMS_4num m1(out1, select, number0, number1, number2, number3);
21 MMS_4num m2(out2, select, number4, number5, number6, number7);
22 assign result = ((out1 < out2) ^ select) ? out2 : out1;</pre>
24 endmodule
```

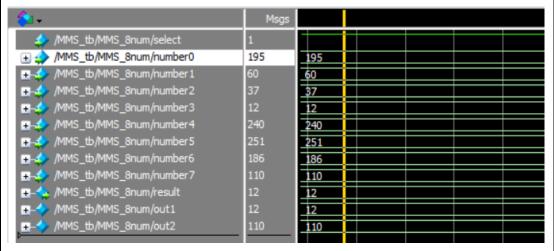
Verilog code of MMS 8num.



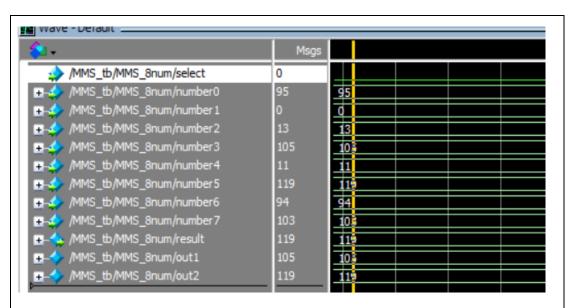
Segment wave of result of MMS\_4num, select ==1 represented for selecting minimum, so the result will be 13.



Segment wave of result of MMS\_4num, select == 0 represented for selecting maximum, so the result will be 207.



Segment wave of result of MMS\_8num, select == 1 represented for selecting minimum, so the result will be 12.



Segment wave of result of MMS\_8num, select == 0 represented for selecting minimum, so the result will be 119.