2023 Digital IC Design Homework 4

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Simulation Result

Functional simulation	PASS	Gate-level simulation	PASS

```
---------- S U M M A R Y ----------

Congratulations! Layer 0 data have been generated successfully! The result is PASS!!

Congratulations! Layer 1 data have been generated successfully! The result is PASS!!

terminate at      60423 cycle
-----------------------------------------------------

** Note: $finish    : C:/Graduate School/IC_DESIGN/HW4/testfixture.v(178)
   Time: 3021150 ns  Iteration: 0  Instance: /testfixture
1
Break in Module testfixture at C:/Graduate School/IC_DESIGN/HW4/testfixture.v line 178
```

```
#
# ---------- S U M M A R Y ----------
#
# Congratulations! Layer 0 data have been generated successfully! The result is PASS!!
#
# Congratulations! Layer 1 data have been generated successfully! The result is PASS!!
#
# terminate at      60423 cycle
# -----------------------------------------------------
#
# ** Note: $finish    : C:/Graduate School/IC_DESIGN/HW4/testfixture.v(178)
#    Time: 3021157862 ps  Iteration: 0  Instance: /testfixture
# 1
# Break in Module testfixture at C:/Graduate School/IC_DESIGN/HW4/testfixture.v line 1
```

Synthesis Result

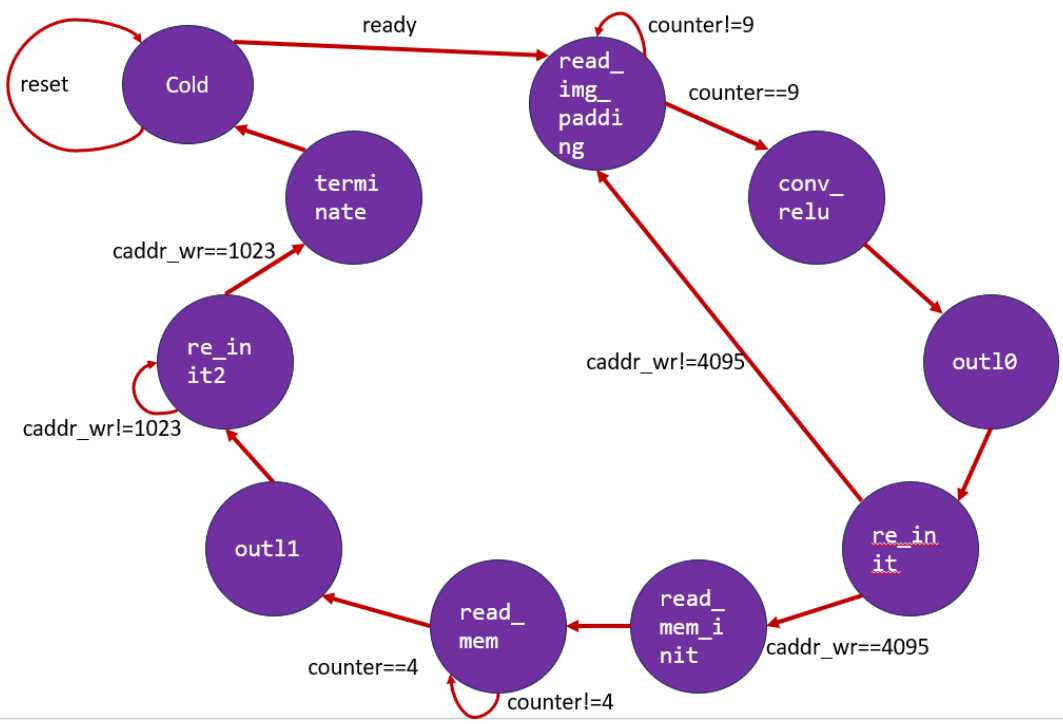
Total logic elements	545
Total memory bits	0
Embedded multiplier 9-bit elements	0
Total cycle used	60423

Flow Status	Successful - Wed May 17 15:31:01 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	ATCONV
Top-level Entity Name	ATCONV
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	545 / 55,856 (< 1 %)
Total registers	195
Total pins	82 / 325 (25 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	0 / 308 (0 %)
Total PLLs	0 / 4 (0 %)

Score = (545+0+0) * 60423 = 32930535

Description of your design

FSM



1. Read_img_padding: load partial image into buffer and implement replicate padding.
2. Conv_relu: Implement Atrous Convolution and ReLu operation.
3. Outlo: output partial result image into layer0 memory.
4. Re_init: initialize control variable like data_buffer0 or cwr.
5. Read_mem_init: initialize control variable like csel, crd, etc.
6. Read_mem: read partial image from layer0 mem and implement pooling.
7. Outl1: output partial image to layer1 mem.
8. Re_init2: initialize control variable like cwr, data_buffer0.
9. Terminate: assign busy signal.

Score = (545+0+0) * 60423 = 32930535

*Scoring = (Total logic elements + Total memory bits + 9*Embedded multipliers 9-bit elements) X Total cycle used*

*** Total logic elements must not exceed 1000.**