2023 Digital IC Design Homework 1

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| NAME | | 吳紀寬 | | | | | | |
| Student ID | | N26112128 | | | | | | |
| **Functional Simulation Result** | | | | | | | | |
| Stage 1 | Pass/Fail | | Stage 2 | Pass/Fail | Stage 3 | Pass/Fail | Stage 4 | Pass/Fail |
| **Stage 1** | | | | | | | | |
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| **Stage 2** | | | | | | | | |
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| **Stage 3** | | | | | | | | |
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| **Stage 4** | | | | | | | | |
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| **Description of your design** | | | | | | | | |
| Verilog code of MMS\_4num.    Verilog code of MMS\_8num.    Segment wave of result of MMS\_4num, select ==1 represented for selecting minimum, so the result will be 13.    Segment wave of result of MMS\_4num, select == 0 represented for selecting maximum, so the result will be 207.    Segment wave of result of MMS\_8num, select == 1 represented for selecting minimum, so the result will be 12.    Segment wave of result of MMS\_8num, select == 0 represented for selecting minimum, so the result will be 119. | | | | | | | | |