2023 Digital IC Design Homework 4

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| **Simulation Result** | | | | | |
| Functional simulation | | PASS | | Gate-level simulation | PASS |
|  | | | |  | |
| **Synthesis Result** | | | | | |
| Total logic elements | | | 545 | | |
| Total memory bits | | | 0 | | |
| Embedded multiplier 9-bit elements | | | 0 | | |
| Total cycle used | | | 60423 | | |
| ***Score = (545+0+0) \* 60423 =* *32930535*** | | | | | |
| **Description of your design** | | | | | |
| **FSM**     1. Read\_img\_padding: load partial image into buffer and implement replicate padding. 2. Conv\_relu: Implement Atrous Convolution and ReLu operation. 3. Outlo: output partial result image into layer0 memory. 4. Re\_init: initialize control variable like data\_buffer0 or cwr. 5. Read\_mem\_init: initialize control variable like csel, crd, etc. 6. Read\_mem: read partial image from layer0 mem and implement pooling. 7. Outl1: output partial image to layer1 mem. 8. Re\_init2: initialize control variable like cwr, data\_buffer0. 9. Terminate: assign busy signal. | | | | | |

***Score = (545+0+0) \* 60423 =* *32930535***

*Scoring = (Total logic elements + Total memory bits + 9\*Embedded multipliers 9-bit elements) X Total cycle used*

**\* Total logic elements must not exceed 1000.**