20.2.0 DIGITAL ELECTRONICS

20.2.01 Introduction

This unit deals with study of circuits of signals that take only two different levels. It is intended to provide the trainee with the relevant knowledge skills and attitudes necessary to make the learner competent in design, installation and maintenance of digital equipment and devices. The trainers may use phased design projects (suitable for the level) to enhance skills and competence acquisition.

20.2.02 General Objectives

At the end of the module unit, the trainee should be able to:

a) Understand number systems and perform binary arithmetic
b) Design combination logic networks
c) Design flip-flop circuits
d) Design Register and Counter Circuits
e) Understand the operation of data handling logic circuits
f) Apply arithmetic circuits in electronic circuits
g) Appreciate digital electronics as a foundation for industrial controls

20.2.03 Module Unit Summary and Time Allocation

Digital Electronics

Code	Sub Module Unit	Content	Time Hours
20.2.1	Number systems	• Number systems • Binary systems • Conversion of numbers to binary and vice versa • 'Ones' and `twos' complement s • Arithmetic • Numbers in octal • Conversion of octal numbers into other numbers and vice versa • Conversion of hexadecimal numbers to other number systems • Application of number systems	4
20.2.2	Binary codes	• Importance of Binary codes • BCD arithmetic • BCD arithmetic • Binary numbers in grey code	6

		• Alphanumeric codes • Application of alphanumeric codes. • Error detection	
20.2.3	Logic gates and Boolean algebra	• Operation of basic logic gates • Operation of hybrid (derived) logic gates • The Boolean algebra • Reduction of logic expression • Implementation of logic circuits	6
20.2.4	Combinational logic design	• Definition of Combinational logic network operation • Derivations from Boolean • Designing combinational logic using Boolean algebra • Designing combinational circuits using tabular methods • Logic circuits for industrial interlock systems including time delay	6
20.2.5	Logic families	• Transistor as a switch • Classifications of Logic Families • Operation of various logic families • Handling requirements of various logic Families • Interconnection of different logic families	4
20.2.6	Flip flops	• Latches • Types of flip-flops • Edge triggered • Master/slave flip-flop • Manufacturers data sheets and catalogues	8
20.2.7	Combinational logic circuits	• Definition of data handling logic circuits • Operation of data handling logic circuits • Applications • Similarities between decoder and demultiplexers	6
20.2.8	Sequential logic circuits	• Shift register operation • Serial register operation	8

		• Parallel register operation • Shift register modes • Use of manufacturers data sheets and catalogues to identify registers • Operation of ripple counters • Operation of synchronous counters • Comparison between ripple and synchronous • Feedback register • Application of counters • Use of manufacturers' data book and catalogue to identify counters	
20.2.9	Arithmetic Circuits	• Serial Adders • Parallel adder • Serial and parallel adder • Arithmetic circuits	6
20.2.10	Converters	• Operational amplifiers as Comparator • Terminologies • Operation of DAC • Operation of ADC • Application	6
20.2.11	Memories	• Classification of memory devices • Terminologies • Operation of semiconductor RAM and ROM memory devices • Organization of ROM memory devices • Operation and organization of secondary storage memories • Mapping • Memory organization	6
Total Time			**66**

20.2.1 NUMBER SYSTEMS

Theory

20.2.1T0 *Specific objectives*

By the end of the sub-module unit, the trainee should be able to:

a) represent numbers in decimal
b) represent numbers in binary
c) convert binary numbers into other number systems and vice versa
d) represent binary numbers into one's and two's complement
e) perform binary arithmetic
f) represent numbers in octal
g) convert octal numbers into other number systems and vice versa
h) represent numbers in hexadecimal
i) convert hexadecimal numbers to other number systems and vice versa
j) state the areas of application of number systems

Content

20.2.1T1 Number systems
20.2.1T2 Binary systems
20.2.1T3 Conversion of numbers to binary and vice versa
20.2.1T4 'Ones' and 'twos' complement s
20.2.1T5 Arithmetic
20.2.1T6 Numbers in octal
20.2.1T7 Conversion of octal numbers into other numbers and vice versa
20.2.1T8 Conversion of hexadecimal numbers to other number systems
20.2.1T9 Application of number systems

20.2.1C Competence

The trainee should have the ability to: number systems in programming

20.2.2 BINARY CODES

Theory

20.2.2T0 *Specific objectives*

By the end of the sub-module unit, the trainee should be able to:

a) explain the importance of various binary codes
b) represent decimal numbers in binary coded decimal (BCD)
c) perform BCD arithmetic
d) represent binary numbers in gray code
e) represent characters in various alphanumeric codes.
f) Identify the use of various alphanumeric codes in digital systems
g) explain various methods of error detection and correction

Content

20.2.2T1 Importance of Binary codes
20.2.2T2 Representation of decimal numbers in Binary Coded Decimal (BCD)
20.2.2T3 BCD arithmetic
20.2.2T4 Representation of binary numbers in gray code
20.2.2T5 Representation of characters in various alphanumeric codes
20.2.2T6 Use of alphanumeric codes in digital systems
20.2.2T7 Methods of error detection

20.2.3 LOGIC GATES AND BOOLEAN ALGEBRA

Theory

20.2.3T0 *Specific objectives*

By the end of the sub module unit, the trainee should be able to:

a) explain the operation of the basic logic gate
b) explain the operation of hybrid (derived) logic gates
c) understand the concepts of Boolean algebra
d) minimize logic expressions using universal gates
e) implement logic circuits using universal gates

Content

20.2.3T1 Basic Logic gates AND, OR , INVERTER
20.2.3T2 Hybrid Gates NAND, NOR, Exclusive gates
20.2.3T3 Boolean algebra
- Identities and Rules, De Morgans Theorems

20.2.3T4 Minimize logic expressions using:
i) Boolean algebra
ii) K-Map upto 4 variables

20.2.3T5 Implement logic circuits using
i) NAND gates only
ii) NOR gates only.

Practice

20.2.3P0 *Specific Objectives*

By the end of the sub-module unit the trainee should be able to:

a) identify pin configuration of logic gate ICs
b) mount the logic gate IC on a breadboard
c) verify the operation of logic gates

Content

20.2.3P1 Identifying pin configuration
20.2.3P2 Mounting logic gate IC on a breadboard
20.2.3P3 Demonstrate operation of logic gates

20.2.3C **Competence**

The trainee should have the ability to: construct and test various logic gates

Suggested teaching/Learning Activities

- Illustration
- Demonstration
- Note taking
- Practical exercise

Suggested Teaching and Learning Resources

- Digital trainer kit
- Assorted logic gate ICS
- Connecting wires
- Clock generator
- Breadboard
- DC power supply
- LED display

Suggested Evaluation Methods

- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project

20.2.4 COMBINATIONAL LOGIC DESIGN

Theory

20.2.4T0 *Specific objectives*

By the end of the sub-module unit, the trainee should be able to :

a) define combinational logic networks
b) design combinational logic circuits using Boolean algebra
c) design combinational logic circuits up to 4 input variables using Karnaugh map
d) design combinational logic circuits up to 4-input variables using tabular method.
e) design combinational logic circuits for industrial interlock systems including time delay.

Content

20.2.4T1 Combination logic & Network design

20.2.4T2 Combinational logic circuits using Boolean algebra

20.2.4T3 Combinational logic circuits up to 4 input variables using Karnaugh map

20.2.4T4 Combinational logic circuits up to 4-input variables using tabular method

20.2.4T5 Combinational logic circuits for industrial interlock systems including time delay

Practice

20.2.4P0 *Specific objectives*

By the end of the sub-module unit, the trainee should be able to:

a) use manufacturers' data sheets and catalogues to identify characteristics and pin connections of ICs.
b) interconnected different logic families

Content

20.2.4P1 Use of manufacturer's data book

20.2.4P2 Interconnection of different logic families

20.2.4C Competences

The trainee should have the ability to: use different logics gates in electronic circuit design

Suggested teaching/Learning Resources

- Logic gates
- Electronic tool kit
- Electrical measuring instruments
- Bread board

Suggested teaching/Learning Activities

- Illustration
- Demonstration
- Note taking
- Observation
- Practical exercise
- Project work

Suggested Evaluation Methods

- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project

20.2.5 LOGIC FAMILIES

Theory

20.2.5T0 *Specific objectives*

By the end of the sub-module unit, the trainee should be able to:

a) explain the use of a transistor as a switch
b) state classifications of logic families
c) explain the general operation and characteristics of various logic families
d) state the handling requirements for various logic families

Content

20.2.5T1 Transistor as a switch
- i) BJT
- ii) MOSFET
- iii) Synchronous sequential logic

20.2.5T2 Classifications of Logic Families
- i) BJT logic families
- ii) MOSFET logic families
- iii) SSI
- iv) MSI
- v) LSI
- vi) VLSI

20.2.5T3 Operation of various logic families

20.2.5T4 Ccharacteristics of various logic families in terms of
- i) Loading rules
- ii) Wired AND operation
- iii) Unused inputs
- iv) Protection
- v) Interfacing between logic families
- vi) Tri-state TTLs
- Use of manufacturers Datasheets

20.2.5T5 How to connect different logic families
- i) TTL-CMOS
- ii) MOS-TTL

Practice

20.2.5P0 *Specific Objectives*

By the end of the sub-module unit, the trainee should be able to:

a) select a particular logic gate IC using data sheets or catalogs
b) demonstrate the operation of logic gates ICs

c) interface different logic gates
d) interconnect various logic families

Content

20.2.5P1 Selecting a particular logic gate IC from a catalogue
20.2.5P2 Demonstrating the operation of logic gate ICS
20.2.5P3 Interfacing different logic gates

20.2.5C Competence

The trainee should have the ability to: construct and test logic circuits from different logic families

Suggested teaching/Learning Activities

- Illustration
- Demonstration
- Note taking
- Observation
- Practical exercise
- Project work

Suggested Evaluation Methods

- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project

20.2.6 FLIP-FLOPS

Theory

20.2.6T0 *Specific objectives*

By the end of the sub module unit, the trainee should be able to:

a) explain the operation of latches
b) explain the operation of various flip-flop circuits.
c) explain the operation of edge triggered flip-flops
d) explain characteristics of master/slave flip-flops
e) use manufacturers' data sheets and catalogues to select flip-flops.

Content

20.2.6T1 Explanation of operation of latches
i) Transistor latch
ii) NAND latch
iii) NOR latch
iv) 20.2.6T2Flip-flops
v) S-R
vi) J-K
vii) D Type
viii) T-type
20.2.6T3 Explanation operation of the following using transition tables and
i) wave forms:
ii) Edge triggered
iii) Master/slave flip-flop
20.2.6T4 Characteristics of master/slave flip flops
20.2.6T5 Use manufacturers data sheets and catalogues to identify:
i) Pin connection
ii) Characteristics of IC flip-flops

Practice

20.2.6P0 *Specific Objectives*

By the end of the sub-module unit, the trainee should be able to:

a) select a particular flip flop IC using data sheets or catalogs

b) demonstrate the operation of various flip flops

Content

20.2.6P1 Selecting a particular flip flop IC for using data sheets or catalogues

20.2.6P2 Demonstrating the operation of various flip flops

20.2.6C Competence

The trainee should have the ability to: construct and test logic circuits from different flip flops.

Suggested teaching/Learning Activities

- Illustration
- Demonstration
- Note taking
- Observation
- Practical exercise

Suggested teaching/Learning Resources

- Logic circuits
- Flip flops
- Electrical measuring instruments

Suggested Evaluation Methods

- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project

20.2.7 COMBINATION LOGIC DESIGN

Theory

20.2.7T0 *Specific objectives*

By the end of the sub-module unit, the trainee should be able to:

a) define data handling combinational logic circuits
b) explain the operation of combinational logic circuits
c) describe applications combinational logic circuits
d) state similarities between decoder and demultiplexers

Content

20.2.7T1 Definition of combinational logic circuits
- i) Decoders
- ii) Encoders
- iii) Multiplexers
- iv) Demultiplexers

20.2.7T2 Explanation of the operation of combinational logic circuits
- i) Decoders
- ii) Encoders
- iii) Multiplexers
- iv) Demultiplexers

20.2.7T3 Application of
- i) Decoders
- ii) Encoders

20.2.7T4 Similarities of Multiplexers and Demultiplexers

Practice

20.2.7P0 *Specific Objectives*

By the end of the sub - module unit, the trainee should be able to:

a) construct various combinational logic circuits
b) demonstrate the operation of various combinational logic circuits

Content

20.2.7P1 Constructing various combinational logic circuits

20.2.7P2 Demonstrating operation of various combinational logic circuits

20.2.7C Competence

The trainee should have the ability to: construct and test various combinational logic circuits.

Suggested teaching/Learning Activities

- Discussion
- Question and answer
- Demonstration
- Note taking
- Observation
- Practical exercise

Suggested teaching/Learning Resources

i) Electrical measuring instruments
ii) Electronic tool kit
iii) Dc Power supply
iv) Ac power supply
v) Logic gates
vi) Electronic components

Suggested Evaluation Methods

- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project

20.2.8 SEQUENTIAL LOGIC CIRCUITS

Theory

20.2.8T0 *Specific objectives*

By the end of the sub-module unit, the trainee should be able to :

a) explain the basic operation of a shift register
b) describe serial shift register operation
c) describe parallel shift register operation
d) explain the practical IC shift modes of operation
e) use manufacturers data sheets and catalogues to identify ICs
f) describe the operation of asynchronous (ripple through) counters
g) describe the operation of synchronous counters
h) compare synchronous with asynchronous counters
i) describe operation of feedback register
j) describe the applications of counters
k) use manufacturer's data sheets and catalogues to identify and select counters.

Content

20.2.8T1 Operation of a shift register using
- i) Transition tables
- ii) Waveforms

20.2.8T2 Describe serial shift register operation
- i) Shift right
- ii) Shift left
- iii) Shift around

20.2.8T3 Describe parallel shift operation

20.2.8T4 Explain the practical IC shift register modes
- i) SISO
- ii) SIPO
- iii) PIPO
- iv) PISO

20.2.8T5 Use manufacturers data sheets and catalogues to identify
- i) Pin connection
- ii) Characteristics of IC flip-flop

20.2.8T6 Describe the operation of the Ripple counter
- i) Modulus number
- ii) Stage and state numbers
- iii) Shortened mod
- iv) Decoding outputs
- v) Waveforms
- vi) Limitations

20.2.8T7 Describe the operation of synchronous counters

20.2.8T8 Compare asynchronous and synchronous counter

20.2.8T9 Describe the operation of the feedback register
- i) Ring counter
- ii) Twisted ring counter
- iii) Random sequence generator

20.2.8T10 Describe applications of counters

20.2.8T11 Use manufacturer's data sheets and catalogues to identify:
- i) Pin connection
- ii) IC characteristics

Practice

20.2.8P0 *Specific Objectives*

By the end of the sub-module unit the trainee should be able to:
- a) construct various sequential logic circuits
- b) operate various sequential logic circuits

Content

20.2.8P1 Constructing various sequential logic circuits

20.2.8P2 Operation of various sequential logic circuits

20.2.8C Competence

The trainee should have the ability to: construct and test various sequential logic circuits

Suggested teaching/Learning Activities
- Discussion
- Question and answer
- Demonstration
- Note taking
- Observation
- Practical exercise
- Project work

Suggested teaching/Learning Resources
- Electrical measuring instruments
- Electronic tool kit
- Dc Power supply
- Sequential logic circuits

- Electronic components
- Assorted cables and other electrical materials

Suggested Evaluation Methods
- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project

20.2.9 ARITHMETIC CIRCUITS

20.2.9T0 *Specific Objectives*
By the end of the sub-module unit, the trainee should be able to :
a) describe the operation of a serial adder
b) describe the operation of a parallel adder
c) compare serial and parallel adders
d) describe the application of arithmetic circuits

Content
20.2.9T1 Description of operation of serial adders
i) Operation
ii) Modification to perform subtraction
iii) Limitation
20.2.9T2 Description of parallel adder
i) Operation
ii) Use and operation of a look-ahead carry
20.2.9T3 Explanation of comparison of serial and parallel adders
i) Operation
ii) Complexity
20.2.9T4 Description of arithmetic circuits
- Applications of adders e.g. ALU

Practice

20.2.9P0 *Specific Objectives*
By the end of the sub module unit the trainee should be able to:
a) construct various arithmetic circuits
b) demonstrate the operation of various arithmetic circuits

Content
20.2.9P1 Constructing various arithmetic circuits
20.2.9P2 Demonstrating operation of various arithmetic circuits

20.2.9C Competence
The trainee should have the ability to: construct and test various arithmetic circuits.

Suggested teaching/Learning Activities
- Discussion
- Question and answer
- Illustration
- Demonstration
- Note taking
- Observation
- Practical exercise
- Project work

Suggested teaching/Learning Resources
- Electrical measuring instruments
- Electronic tool kit
- Electrical tool kit

- Dc Power supply
- Ac power supply
- Three phase power supply
- Arithmetic circuits
- Electronic components
- Assorted cables and other electrical materials

Suggested Evaluation Methods
- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project
- Project Report writing and presentation

20.2.10 CONVERTERS

Theory

20.2.10T0 *Specific Objectives*
By the end of the sub-module unit, the trainee should be able to :
a) describe Operational Amplifier as comparator
b) define the terminologies used in converter circuits
c) describe the operation of DAC
d) describe the operation of ADC
e) explain the applications of converter circuits

Content
20.2.10T1 Operational Amplifier as Comparator
20.2.10T2 Definition of DAC's and ADC's terminologies
20.2.10T3 Digital to Analogue Converter
i) Types
ii) Analysis
iii) Application
20.2.10T4 Analogue to Digital Converter
i) Types
ii) Analysis
20.2.10T5 Applications

Practice

20.2.10P0 *Specific Objectives*
By the end of the sub-module unit the trainee should be able to:
a) construct various converter circuits
b) demonstrate operation of various converter circuits

Content
20.2.10P1 Constructing various converter circuits
20.2.10P2 Operation of various converter circuits

20.2.10C **Competence**
The trainee should have the ability to: construct and test various converter circuits.

Suggested teaching/Learning Activities
- Demonstration
- Note taking
- Observation
- Practical exercise
- Project work

Suggested teaching/Learning Resources
i) Electrical measuring instruments
ii) Electronic tool kit
iii) Dc Power supply
iv) Signal generators
v) Electronic devices
vi) Electronic components

vii) Assorted cables and other electrical materials

Suggested Evaluation Methods

- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project

20.2.11 MEMORIES

Theory

20.2.11T0 *Specific Objectives*

By the end of the sub module unit, the trainee should be able to:

a) classify memories into various categories
b) define memory terminologies
c) describe the operations of semiconductor RAM and ROM memories
d) describe the organization of semiconductor ram and ROM
e) describe the operation and organization of secondary storage memories
f) explain memory map
g) describe memory organization

Content

20.2.11T1 Classification of Memories into various categories in a computer system

20.2.11T2 Stating the meaning of various memory terminologies

20.2.11T3 Description of operation of Semiconductor RAM and ROM

i) Memory cell
ii) Dynamic & Static memories
iii) Erasable and non-erasable memories
iv) Access timing of memories
v) Memory capacity

20.2.11T4 Description of organization of Semiconductor RAM and ROM

i) Register representation in memories
ii) Memory timing
iii) Memory expansion
iv) Memory address decoding
v) Memory pages
vi) Cache memories
vii) Storage capacity

20.2.11T5 Description of organization and operation of Secondary storage devices

i) Need for secondary storage
ii) Magnetic bubble memories
iii) Floppy & hard disks
iv) Recording surfaces
v) Accessing & timing
vi) Formats
vii) Disk drives
viii) Storage capacity
ix) Hard disk
x) CD ROM
xi) CCD
xii) Data stick/Flash Disc

20.2.11T6 Description of memory mapping

i) Address decoders
ii) Address allocation
iii) System ROM, RAM, I/O, Expansion
iv) Expansion slots
v) Timing
vi) Pages

20.2.11T7 Description of memory organization
i) Hierarchy
ii) Timing
iii) Formats
iv) Capacity
v) Functions

20.2.11C Competence
Ability to manage computer memories